Sizing Current Transformers for Line Protection Applications

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Sizing Current Transformers for Line Protection Applications

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***Abstract*—This paper discusses the factors to consider for sizing current transformers (CTs) for line protection applications. We first cover CT basics, with emphasis on errors and ac and dc saturation. We also discuss the criteria to avoid CT saturation. Then we analyze the effect of CT saturation on overcurrent, distance, directional, and differential elements. Further, we present the advances in protection element design to improve security and speed under CT saturation conditions. Finally, we discuss the tools available to the protection engineer for CT sizing and provide some guidelines.**

I. Introduction

The transient response of current transformers (CTs) has a significant impact on the performance of line protection. CT saturation during external faults can seriously affect the security of the protection scheme, especially for dual-breaker line terminals where a large portion of the fault current can enter and leave the line protection zone without flowing through the protected line.

Selecting higher-ratio CTs to prevent saturation and match the breaker load ratings may result in CTs that have considerably higher nominal current than the line loading. Sensitivity may have to be sacrificed as a result. The degree to which the various line protection elements are impacted can also vary. In the past, general rules were developed to allow the protection engineer to size the CT for a particular application. These rules were used to determine the fault current magnitude (including ac and dc components) beyond which saturation occurs and to determine the CT time to saturation for a given fault. These rules take into account the CT knee point, connected burden, and system X/R ratios. Other potentially important aspects, such as remanent flux, were typically not considered or left to the discretion of the protection engineer. These rules also did not consider CT saturation countermeasures available by design in modern relays, which reduce the impact of saturation. For a transmission line, a typical CT sizing rule called for ratings that would ensure no saturation for the end-of-line fault. This rule works well in single-breaker applications or with line CTs but clearly has limitations in dual-breaker applications with breaker CTs.

The advent of microprocessor-based relaying has allowed relay designers to incorporate novel methods for dealing with CT saturation. These methods improve relay performance in the face of saturation and can allow CT sizing requirements to be relaxed as a result. Hence, the CT can no longer be evaluated without consideration for the particular relay to which it will be connected.

II. CT Basics

A. CT Steady-State Operation

1) Ideal CT Behavior

Ideally, the secondary current of a CT is perfectly proportional to the primary current. The ideal CT has no losses or leakage flux and requires no magnetizing current. For a CT having n_P primary turns and n_S secondary turns, the ideal relationship between primary (I_P) and secondary (I_S) currents is the following:

$$I_P n_P = I_S n_S \tag{1}$$

$$I_S = \frac{n_P}{n_S} I_P = \frac{I_P}{n_S / n_P} = \frac{I_P}{n} \tag{2}$$

where:

n is the CT turns ratio, $n = n_S/n_P$.

Equation (2) can be expressed in per-unit (pu) values as:

$$I_S\,(\text{pu}) = I_P\,(\text{pu}) \tag{3}$$

2) Real CT Behavior

Real CTs have copper losses, core losses, and leakage flux and require a certain current to magnetize the core. As a result, the secondary current of a CT is not perfectly proportional to the primary current. For most operating conditions, CTs reproduce the primary currents well. However, under certain conditions, the CT core saturates and the CT fails to correctly reproduce the primary current.

Fig. 1 depicts the equivalent circuit of a CT, referred to the transformer secondary side. The CT primary current I_P is dictated by the power system because the CT primary winding is connected in series with the protected element. The current source I_P/n represents the power system in Fig. 1. CT leakage impedances are $R'_P + jX'_P$ for the primary winding (referred to secondary) and $R_S + jX_S$ for the secondary winding. As a result of the current source, the primary leakage impedance has no practical effect on the CT behavior and can be disregarded. The nonlinear excitation impedance Z_E represents CT magnetization. The excitation current I_E flowing through the excitation impedance has two components. One component is the magnetizing current (flowing through the inductive component of Z_E), which is needed to generate the flux in the CT core. The other component of I_E is the loss current (flowing through the resistive component of Z_E), which mainly results from the core hysteresis and eddy losses. The secondary excitation voltage E_S is the voltage induced in the secondary winding. Impedance Z_B represents the total load

connected to the CT secondary winding. This impedance is referred to as the CT burden. The CT secondary terminal voltage V_S appears across the CT burden.

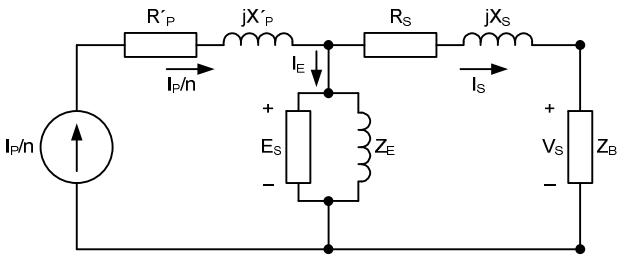

Fig. 1. CT equivalent circuit referred to the secondary side.

When the secondary voltage V_S is low, the excitation current I_E is low and the CT behaves almost linearly, with no saturation in the magnetic core. As V_S increases because of the current or the burden impedance increasing, the excitation current increases and the magnetic flux in the core also increases. At a given flux magnitude, the core saturates, the excitation current increases disproportionally, and the secondary current is no longer an accurate replica of the primary current.

Based on Fig. 1, the phasor values of the secondary current and the CT terminal voltage are, respectively:

$$I_S = \frac{I_P}{n} - I_E \tag{4}$$

$$V_S = I_S Z_B = E_S - I_S\left(R_S + jX_S\right) \tag{5}$$

Fig. 2 depicts the typical CT magnetization curve (B-H curve) showing the hysteresis loop for a CT exposed to a high-current fault, which produces core saturation in both half cycles of the magnetic flux waveform. The residual flux density is the flux at which the magnetizing force H is zero when the core material is in a symmetrically, cyclically magnetized condition. Fault clearance reduces the primary current to zero, but some magnetic flux remains trapped in the CT core [1] [2]. Remanence is the magnetic flux that remains in the magnetic circuit after the removal of the primary current. Remanence is approximately equal to the residual flux density in a nongapped-core CT. An advantage of gapped-core CTs is that their remanence is lower than the residual flux.

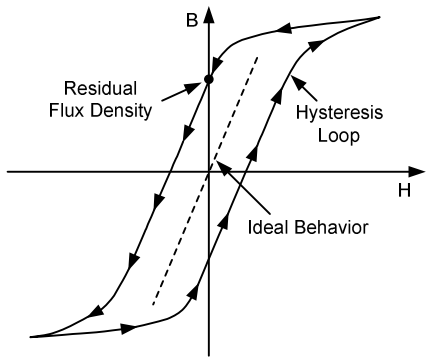

Fig. 2. CT magnetization curve showing the hysteresis loop.

Remanence may either impair or improve the CT response for the next fault, depending on the half cycle during which the next fault occurs. In the particular case shown in Fig. 2, the remanence is positive; hence, the CT is closer to saturation for future positive flux excursions. If the next fault occurs in the positive half cycle (starting with a positive flux excursion), the CT will saturate for a smaller fault current than that required for saturation when there is no remanence. On the other hand, if the next fault occurs in the negative half cycle, the CT will withstand higher current values without saturation. It is not possible to predict the effect of remanence for a particular fault. In general, however, some allowance for remanence is necessary when selecting relaying CTs.

Another effect of fault current interruption is the transient subsidence current that continues to flow in the CT secondary circuit for a short time after the primary current is interrupted. This unipolar decaying current results from energy trapped in the CT magnetic circuit. Subsidence current circulation dissipates the trapped energy into the resistive elements of the CT secondary circuit. The subsidence current can delay the resetting of overcurrent elements; overcurrent elements can remain picked up for some time after primary current stops flowing. This delayed reset postpones operation of breaker failure protection schemes. Some modern relays include algorithms to detect the subsidence current condition and reset instantaneous overcurrent elements in less than 1 cycle.

3) Secondary Excitation Characteristic

The CT secondary excitation characteristic is an alternate representation of the B-H curve. The CT secondary excitation characteristic (see Fig. 3) is a plot of the root-mean-square (rms) value of the secondary excitation voltage E_S as a function of the rms value of the excitation current I_E. The B-H curve and the secondary excitation characteristic have similar shapes because the flux density B is proportional to E_S and the magnetic field intensity H is proportional to I_E. Power engineers normally use CT secondary excitation characteristics, which are provided by manufacturers and are also easy to obtain in a laboratory or field test.

For nongapped Class C CTs (see Section II, Subsection C), the knee-point voltage (V_{KNEE} in Fig. 3) is the voltage at the point where the tangent to the curve (on log-log axes) is at 45 degrees to the abscissa [3] [4]. The saturation voltage (V_{SAT}) is graphically found by locating the intersection of the straight portions of the excitation curve on log-log axes [3].

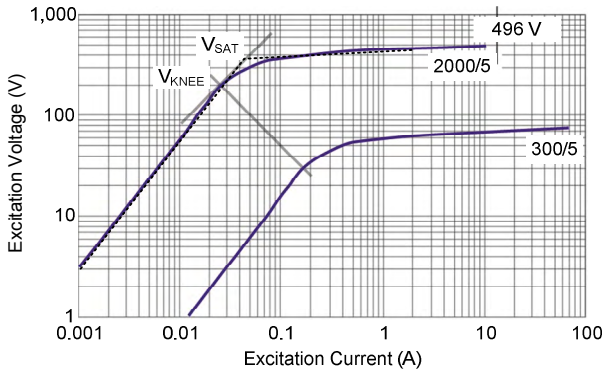

Fig. 3. Typical secondary excitation characteristic for a multiratio CT.

For a multiratio CT, manufacturers provide all the curves in the same plot. Fig. 3 shows the two extreme curves (maximum and minimum taps) of a multiratio CT.

B. CT Errors

According to (4), the CT excitation current I_E creates a difference between the secondary current I_S and the primary current referred to secondary I_P/n, also referred to as the ratio current. This difference is the CT error, which includes a difference in the current magnitudes (ratio error) and a current phase shift (phase error).

There are two ways of expressing CT ratio errors. One of them is to define a ratio correction factor (RCF). The other is to directly define an error. ANSI/IEEE uses the RCF primarily for metering CTs and a ratio error for relaying CTs [3] [4]. ANSI/IEEE defines the ratio error as the following:

$$\text{Ratio error (\%)} = \frac{I_E}{I_S} \bullet 100 \tag{6}$$

CT errors depend on the operating condition. Both ratio and phase errors vary with the CT burden and the primary current magnitude and also with current frequency and waveform [5]. An increase in the burden produces a higher excitation voltage E_S and a higher excitation current I_E. For a given primary current value, a higher value of I_E means greater values of the ratio and phase errors.

A primary current increase should produce a proportional increase of the excitation and secondary currents, and the CT relative error should remain almost unchanged. However, the excitation current I_E is not a linear function of the excitation voltage E_S and the primary current I_P. This nonlinearity is the reason for the effect the primary current magnitude has on CT errors.

Fig. 4 illustrates the effect of CT saturation on the secondary current magnitude. The real I_S versus I_P/n curve is not a straight line. In a well-designed CT with the proper burden, the behavior is very close to linear for a significant range of currents. For large primary currents, the CT experiences saturation, and the difference between the ideal secondary current (or ratio current I_P/n) and the real secondary current becomes larger.

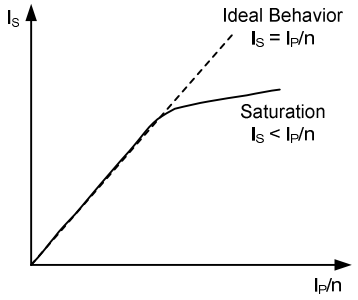

Fig. 4. CT saturation introduces an error in the secondary current.

C. CT Accuracy Classes

CTs are grouped into standardized classes based on their levels of accuracy. Each accuracy class has specified limits of allowable CT errors under prescribed conditions of use.

For relaying CTs, ANSI/IEEE defines a limit of 10 percent for the ratio error for a steady-state, symmetrical (no dc offset) secondary current equal to 20 times rated secondary current at the standard burden [4].

ANSI/IEEE designates relaying CT accuracy classes by a letter designation and a secondary terminal voltage rating (for example, C100) [3] [4]. The letter designation (*C*, *K*, or *T*) specifies the type of relaying CT.

The letter *C* designates a relaying CT that has negligible leakage flux. Hence, it is possible to use the excitation characteristic for determining the CT performance (*C* stands for calculation). The calculation procedure assumes the CT to have only one primary turn passing through the core window and the CT secondary winding to be uniformly distributed around the core [3]. These assumptions are generally true for bushing-type, bar-type, and window-type CTs. These are typically multiratio CTs, and their secondary excitation characteristic is a family of curves. The excitation characteristic depicted in Fig. 3 belongs to a Class C multiratio CT.

The letter *K* designates a CT that is the same as a Class C but that additionally has a knee-point voltage of at least 70 percent of the secondary terminal voltage rating. Almost all CTs used for relaying applications in North America are either Class C or Class K.

Given the previous assumptions, the equivalent circuit of a Class C or Class K CT can be simplified as shown in Fig. 5.

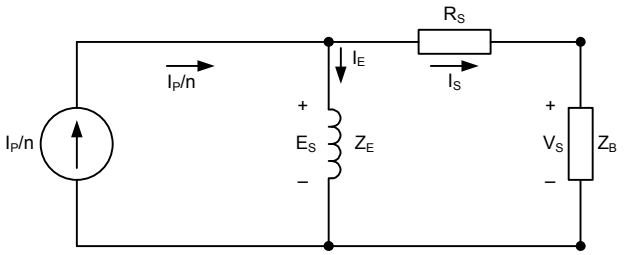

Fig. 5. Simplified equivalent circuit for Class C or Class K CTs.

The letter *T* designates a CT in which the leakage flux has a significant effect on the ratio. The ratio error must be determined by a test (*T* stands for test). Rather than secondary excitation characteristics for Class T CTs, manufacturers provide curves like the type in Fig. 4, obtained from tests. These curves (called overcurrent ratio curves) are plots of the secondary CT current as a function of the primary current. Each current is in pu of the corresponding CT rated current. Manufacturers typically provide a family of overcurrent ratio curves, one per standard burden. Wound-type CTs, which have one or more primary turns mechanically encircling the core, are typically Class T CTs.

The secondary terminal voltage rating is the voltage that the CT delivers to a standard burden at 20 times rated secondary current, without exceeding a 10 percent ratio error.

$$V_{STD} = 20\ I_{S\ RATED}\ Z_{B\ STD} \tag{7}$$

where:

V_{STD} is the secondary terminal voltage rating.

$I_{S\ RATED}$ is the rated secondary current.

$Z_{B\ STD}$ is the standard burden.

ANSI/IEEE standard burdens for relaying CTs are 1, 2, 4, and 8 Ω. For 5 A CTs, the secondary terminal voltage ratings are 100, 200, 400, and 800 V. For example, C400 accuracy class on a 5 A CT means that the performance can be determined from the excitation characteristic and that the ratio error will not exceed 10 percent at any current from 1 to 20 times the rated current (5 to 100 A) and for any burden not exceeding the 4 Ω standard burden. According to (7), the voltage rating is 20 • 5 A • 4 Ω = 400 V. For CTs rated other than 5 A, the secondary terminal voltage rating can be calculated by multiplying the voltage rating at 5 A by $5/I_{S\ RATED}$.

In multiratio CTs, the voltage rating only applies to the full winding. The voltage rating of a CT tap is directly proportional to the ratio between the CT ratio corresponding to the tap and the full CT ratio, provided the windows are fully distributed around the core. As an example, if a C400, 1200/5 CT is operated on the 600/5 tap, the voltage rating at 600/5 is 200 V.

We can use the CT secondary excitation characteristic to determine or verify the CT voltage rating and the corresponding C or K classification. Assume that a Class C, 2000/5 multiratio CT has the excitation characteristic depicted in Fig. 3. According to (6), for a secondary current of 20 times rated current (I_S = 100 A), the excitation current I_E is 10 A for a ratio error of 10 percent. From Fig. 3, the excitation voltage E_S corresponding to I_E = 10 A is 496 V. From Fig. 5, the secondary voltage V_S is the following:

$$V_S = I_S Z_B = E_S - I_S R_S \tag{8}$$

where:

I_S is the secondary current.

Z_B is the CT burden impedance.

E_S is the excitation voltage.

R_S is the CT secondary resistance.

As a first approximation, we can apply (8), assuming all the quantities to be in phase. This is a worst-case scenario. Assuming the CT secondary resistance to be 0.7 Ω for the full secondary winding (2000/5 ratio), the CT secondary voltage for this example is V_S = 496 – (100 • 0.7) = 426 V.

Because the next lowest voltage rating is 400 V, this CT has a C400 classification. If the previous calculation gives a V_S value that is just above a standard value, it is necessary to make a more exact check by calculating V_S using (8) in phasor form [4].

For Class C or Class K CTs, the ratio error will not exceed 10 percent if the secondary terminal voltage V_S is not greater than the secondary terminal voltage rating V_{STD}:

$$V_S \le V_{STD} \tag{9}$$

Incorporating (7) and (8) into (9) and replacing I_S with I_F (the symmetrical fault current referred to secondary) lead to the following:

$$\frac{I_F}{I_{S\ RATED}} \bullet \frac{Z_B}{Z_{B\ STD}} \le 20 \tag{10}$$

We can rewrite (10) as the following:

$$I_f\ Z_b \le 20 \tag{11}$$

where:

Z_b is the CT burden in pu of the rated burden ($Z_b = Z_B/Z_{B\ STD}$).

I_f is the fault current in pu of the CT secondary rated current ($I_f = I_F/I_{S\ RATED}$).

I_F is the symmetrical fault current referred to secondary.

Equation (11) represents the criterion for avoiding relaying CT saturation (ratio error not greater than 10 percent) for symmetrical fault currents. We can use (11) to determine either the maximum allowable symmetrical fault current for a given burden or the maximum allowable burden for a given fault current.

Saturation for symmetrical currents, referred to as ac saturation, can occur in a fraction of a cycle.

D. CT Transient Operation

Section II, Subsection A through Subsection C discuss CT performance in response to symmetrical currents, or steady-state CT operation. However, fault currents frequently contain an exponentially decaying component (dc offset), which produces significant CT saturation. In general, the fault current in an inductive network takes the following form:

$$i(t) = \sqrt{2} I \left[\cos\theta\ e^{-\frac{R}{L}t} - \cos\left(\omega t + \theta\right) \right] \tag{12}$$

where:

θ is the fault incidence angle, measured from the zero crossing of the voltage.

R and *L* are, respectively, the resistance and inductance of the primary faulted system Thévenin equivalent circuit.

Saturation that occurs primarily as a result of the dc offset component is sometimes referred to as dc saturation.

Selecting relaying CTs based only on symmetrical fault currents involves the risk of having heavy CT saturation during the transient process when the fault current has dc offset.

Fig. 6 depicts computer simulation plots showing the effect of dc offset current on CT behavior. The plots include CT currents and magnetic flux density. As can be seen, the CT reaches saturation after approximately one-fourth of a cycle.

Once the current waveform becomes negative, the CT comes out of saturation and begins following the ratio current (I_{RATIO}) until the next positive half cycle when it becomes saturated again. This transient saturation is the result of the high magnetic flux values produced by the dc offset current component. As the dc offset disappears, the magnetic flux returns to normal values and the secondary current again reproduces the primary current well. In this particular simulation, the symmetrical fault current causes no saturation. This is basically the case of a CT that was selected considering only the symmetrical current. There is almost no error for symmetrical fault currents, but offset fault currents heavily saturate the CT. Fig. 6 shows the extreme error caused by transient CT saturation.

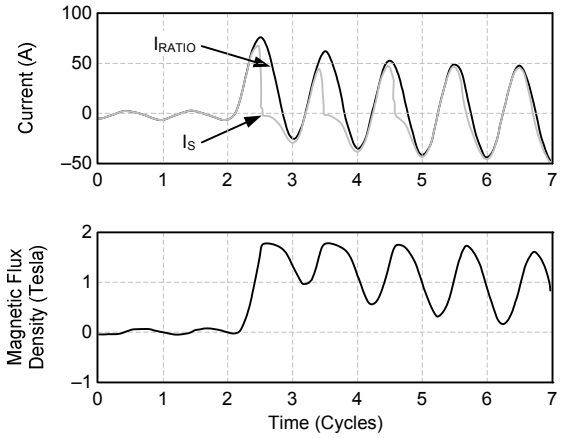

Fig. 6. Secondary current (top plot) and magnetic flux density (bottom plot) of a CT saturated by the fault current dc offset component.

Fig. 6 shows that the CT does not saturate suddenly but reproduces the primary current well for a certain time after each current zero crossing. This is the CT time to saturation [4]. It is important to consider CT time to saturation in relay design. Some relays are fast enough to operate before the CT saturation inception. Time to saturation may be on the order of 1 or more cycles, but in some cases, it can be in the range of half a cycle. The time-to-saturation value depends on many factors, such as the degree of fault current offset, the fault current magnitude, the CT core remanence level, the CT secondary circuit impedance, and the CT saturation voltage and turns ratio [4].

1) The Volt-Time Area

The CT saturation caused by the exponentially decaying fault current component is readily understood and quantified by means of the volt-time area concept [6] [7] [8]. Equation (13) expresses the instantaneous value of the secondary voltage v_S as a function of the magnetic flux φ and the secondary turns n_S, assuming the secondary excitation voltage to be equal to the secondary voltage ($e_S = v_S$) and not considering the minus sign.

$$v_S = n_S \frac{d\varphi}{dt} \tag{13}$$

Integrating (13) with respect to time, we obtain:

$$n_S \varphi = n_S B A = \int_0^t v_S dt \tag{14}$$

where:

B is the flux density.

A is the core cross-sectional area.

Equation (14) indicates that the core flux density is proportional to the area under the secondary voltage waveform. This is the volt-time area concept. When the fault current is fully offset ($\cos\theta = 1$ in (12)), the CT secondary voltage is the following:

$$v_S = \sqrt{2} I_S Z_B \left(e^{-\frac{R}{L}t} - \cos\omega t \right) \tag{15}$$

where:

R and *L* are, respectively, the resistance and inductance of the primary faulted system Thévenin equivalent circuit.

Fig. 7 shows the volt-time area (shaded) produced by an asymmetrical fault current. The effect of the dc offset component is to increase the volt-time area of the positive half cycles as compared with a symmetrical fault current. This means that an offset current produces higher flux densities than those produced by the fundamental component of the same fault current. If the CT is selected only on the basis of avoiding saturation for the maximum symmetrical fault current, the dc offset will saturate the CT. To avoid saturation for asymmetrical currents, we need a CT with a higher rating. Hence, it is important to consider the increased volt-time area caused by the asymmetrical fault current when selecting a CT.

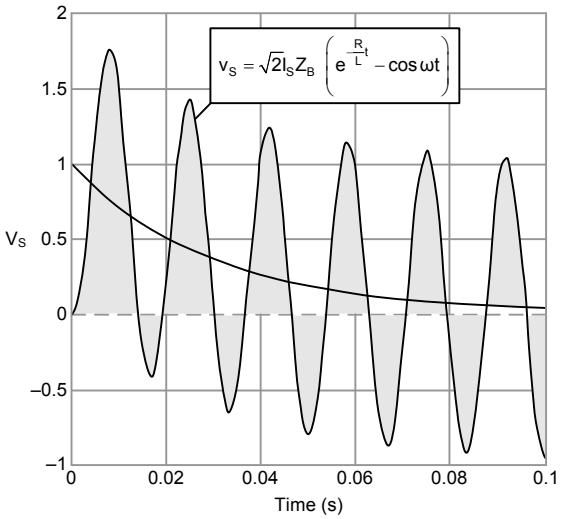

Fig. 7. Secondary voltage for an asymmetrical fault current.

Substituting (15) into (14) and integrating, we obtain:

$$n_S BA = I_S Z_B \left[\frac{L}{R} \left(1 - e^{-\frac{R}{L}t} \right) - \frac{\sin \omega t}{\omega} \right] \quad (16)$$

Using the maximum value of the expression in square brackets, considering the following classical rms voltage equation:

$$E_S = \frac{2\pi \text{ f } n_S A B_{max}}{\sqrt{2}} = 4.44 \text{ f } n_S A B_{max} \quad (17)$$

and assuming the secondary excitation voltage to be equal to the secondary voltage ($e_S = v_S$), we can write the following from (16):

$$V_S = n_S BA\omega = I_S Z_B \left(\frac{X}{R} + 1 \right) \quad (18)$$

where:

X equals ωL and is the primary faulted system equivalent reactance.

Equation (18) expresses the CT secondary voltage in terms of the physical parameters of the CT, namely the flux density B, the secondary turns n_S, the core cross-sectional area A, and the system angular frequency ω. Moreover, it gives V_S in terms of the system X/R ratio, the symmetrical secondary current I_S, and the CT burden Z_B.

2) Criterion to Avoid Saturation

As we know, when the fault current is less than 20 times the CT rated current and the burden is less than the rated standard burden, practically no saturation occurs for a symmetrical fault current. However, we also need a criterion to avoid saturation for asymmetrical fault currents. It is important to recognize the significance of the ANSI/IEEE voltage rating because the area under the voltage sine wave corresponding to the voltage rating represents the CT saturated flux density. This volt-time area signifies the threshold of saturation and marks the boundary of CT operation under a 10 percent ratio error. Substituting (7) and (18) into (9) and replacing I_S with I_F, we obtain:

$$\frac{I_F}{I_{S\,RATED}} \bullet \frac{Z_B}{Z_{B\,STD}} \left(\frac{X}{R} + 1 \right) \le 20 \quad (19)$$

We can rewrite (19) as the following:

$$I_f \; Z_b \left(\frac{X}{R} + 1 \right) \le 20 \quad (20)$$

Note that (20) is a generalization of (11) and represents the criterion to avoid relaying CT saturation (ratio error not greater than 10 percent) for asymmetrical fault currents [6] [7] [8]. We can use (20) to determine either the maximum allowable fault current for a given burden or the maximum allowable burden for a given fault current.

3) Effect of Magnetic Core Remanence on Transient Response

In Section II, Subsection A, we introduced the concept of remanence, which is a relatively frequent CT problem. For example, a survey reported in [4] showed that for 60 percent of 141 CTs on a 230 kV system, the remanent flux ranged from 20 to 80 percent of the flux at the threshold of saturation. The protection engineer has no way to predict the value of remanence that may exist at a given instant in time. In addition, the only way to remove remanence is to apply a pure ac voltage source to the CT secondary terminals and to ramp the source up to the knee point and then gradually back to zero. There is no appropriate time to carry out such an operation other than during protection maintenance.

As mentioned previously, remanence can either impair or improve the CT behavior for a given fault. The worst case is when the fault produces a flux excursion of the same sign as the remanent flux. In this case, the flux change (resulting from the fault) required to saturate the CT equals the difference between the core saturation flux and the remanent flux. Consequently, a given percentage value of remanent flux reduces the CT voltage rating by that percentage. The new voltage rating results from multiplying the voltage rating by 1 – remanence (pu), where remanence (pu) is the percentage of remanent flux divided by 100. For example, a C400 CT with 30 percent of remanent flux has effectively a C280 rating. The corresponding new standard burden for this CT is 2.8 Ω. This analysis makes it clear that (20) should be modified as follows to accommodate CT remanence [4] [9]:

$$\frac{I_f \; Z_b \left(\frac{X}{R} + 1 \right)}{1 - \text{remanence (pu)}} \le 20 \quad (21)$$

4) Practical Considerations for Applying the Criterion to Avoid Saturation

Fault current asymmetry occurs more frequently for multiphase faults than for single-phase-to-ground faults. An insulation breakdown or a flashover is more likely to occur at a voltage peak where the reactive current is at a natural zero. Consequently, single-phase-to-ground faults are more likely to be symmetrical faults. However, in three-phase faults, all currents cannot be at zero simultaneously in each phase and dc offset is inevitable in one or more phases. In addition, the phase displacement causes unequal dc offset to occur in each phase.

In transmission line CT applications, large load currents result in the use of high-ratio CTs and fault currents are typically limited to no more than 10 times rated current. This facilitates the application of the criterion to avoid saturation using the X/R + 1 factor in transmission line CTs.

It is not possible to avoid saturation for asymmetrical fault currents in some applications. Therefore, we must assess the effect of saturation for offset fault currents. Digital simulation helps us analyze CT performance in these cases.

Near generators, for example, high fault currents and high X/R ratio values are frequent. Therefore, it becomes impractical to size the CTs to avoid saturation for asymmetrical fault currents. Instead, we must abandon the criterion and select the largest practical CT rating and match the terminal- and neutral-side CTs. A problem is that the highest ANSI/IEEE accuracy class is C800, and any CT with

an excitation voltage at I_E = 10 A exceeding 800 V is classified as C800, no matter how high the voltage. For example, one 6000/5 CT may have an excitation voltage of 1,500 V at 10 A of excitation current and be classified as C800. A second 6000/5 CT of a different manufacturer may have 978 V at 10 A of excitation current and also be classified as C800. The generator CTs must have the same excitation curve with matching knee-point voltage and the same excitation voltage at 10 A excitation current [7].

In transformer differential protection schemes, the high-voltage-side CTs tend to be mounted on the transformer bushings and require long lead runs to the relay. The lower CT ratio required on the high-voltage side of the transformer and the long leads combine to cause saturation for offset currents, while the low-voltage-side CTs have a higher ratio and remain linear. The difference in saturation levels of both sets of CTs can cause differential relay misoperation for external faults [7]. However, well-designed differential relays remain secure for external faults with CT saturation. Consequently, in many cases, the ANSI/IEEE voltage rating can be selected to accept some degree of saturation, rather than applying the X/R + 1 factor in transformer CT applications.

CTs installed in power plant auxiliary equipment and industrial plants can experience fault currents as high as 40 kA, where X/R exceeds 20. Furthermore, the low-capacity equipment requires CT ratios as low as 100/5. Fault current values of 200 or more times rated current are possible [6] [10] [11] [12] [13]. The extreme CT saturation produces very distorted secondary currents and impairs the performance of instantaneous overcurrent relays. It is not possible to apply the criterion to avoid saturation in these extreme cases. The solution is to apply a special CT selection criterion [10] and/or to use relays having instantaneous overcurrent elements that respond to the peak (rather than to the fundamental) current values [6] [10] [11] [12] (see Section IV, Subsection B).

III. Effect of CT Saturation on Protection Elements

We can illustrate the impact of CT saturation on line protection elements through the use of an example. For this example, we model the system shown in Fig. 8. The system voltage is 345 kV. Fault levels at the *L* and *R* buses are 4,000 MVA and 1,000 MVA. The X/R of each source is 45. The CTs at each bus are C800, 1200/5 with one-way lead resistances of 1 Ω. The transmission line is 10 kilometers in length, with Z_1 = 0.68∠86.9 Ω per kilometer and Z_0 = 1.47∠79 Ω per kilometer.

Referring to (12), we note that the fault current is fully offset when θ = 0. This results in the maximum volt-time area, which is the worst case for CT saturation. In general, it is more likely for an insulation breakdown to occur at the voltage peak. A fully offset current for a single-phase-to-ground fault is therefore improbable. In contrast, at least two currents will contain an offset during a three-phase fault. However, for the purpose of illustration, faults are applied for the worst-case incidence angle of zero degrees in the following example.

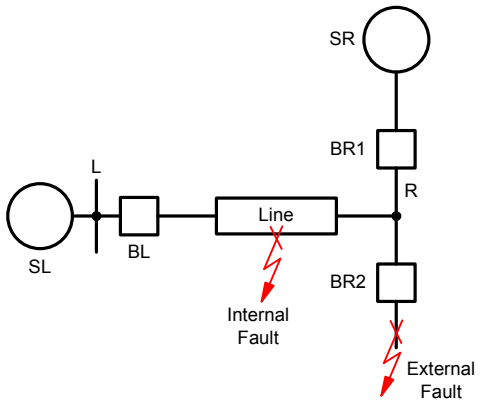

Fig. 8. Example power system.

We evaluate the protection elements by estimating phasor quantities using a standard full-cycle cosine filter and plotting the results on a characteristic operating diagram or by applying the results to the following characteristic equations.

The phase distance element equation follows:

$$m_{PP} = \frac{\mathrm{Re}\left(V_{PP} \bullet V_{POLPP}\right)}{\mathrm{Re}\left(e^{j\alpha 1} \bullet I_{PP} \bullet V_{POLPP}\right)} \tag{22}$$

The ground distance element equation is:

$$m_{PG} = \frac{\mathrm{Re}\left(V_{PG} \bullet V_{POLLG}\right)}{\mathrm{Re}\left(e^{j\alpha 1} \bullet \left(I_{PG} + 3 \bullet k_0 \bullet I_0\right) \bullet V_{POLPG}\right)} \tag{23}$$

The ground directional element equation is the following:

$$z_0 = \frac{\mathrm{Re}\left(3 \bullet V_0 \bullet 3I_0 \bullet e^{j\alpha 0}\right)}{\left|3I_0\right|^2} \tag{24}$$

The negative-sequence directional element equation is:

$$z_2 = \frac{\mathrm{Re}\left(V_2 \bullet I_2 \bullet e^{j\alpha 1}\right)}{\left|I_2\right|^2} \tag{25}$$

where:

V_{PP} and I_{PP} are the phase-to-phase voltage and current for a particular phase fault loop.

V_{PG} and I_{PG} are the phase-to-ground voltage and current for a particular ground fault loop.

V_{POLPP} and V_{POLPG} are the memorized polarizing quantities.

$\alpha 1$ and $\alpha 0$ are the positive- and zero-sequence line impedance angles.

$k_0 = (Z_{1L} - Z_{0L})/3 \bullet Z_{1L}$ is the zero-sequence compensation factor.

Z_{1L} and Z_{0L} are the positive- and zero-sequence line impedances.

V_0 and I_0 are the zero-sequence voltage and current.

V_2 and I_2 are the negative-sequence voltage and current.

A. Overcurrent Elements

Fig. 9 shows the contribution from Terminal L for an internal single-phase-to-ground fault on the example power system of Fig. 8. The fault starts at approximately 50 milliseconds, and CT saturation occurs at approximately 105 milliseconds, 55 milliseconds after fault inception. For this fault, an instantaneous overcurrent element set to 30 A would probably have time to operate and initiate breaker tripping before resetting because of CT saturation. However, for a heavier CT saturation condition, the CT time to saturation could be shorter than the element operating time. This condition would delay element operation to until the dc offset component dies out and the CT recovers. Furthermore, a poor CT selection could lead to saturation for the symmetrical fault current. In this case, the CT does not fully recover after the dc offset dies out and the instantaneous overcurrent element may fail to operate.

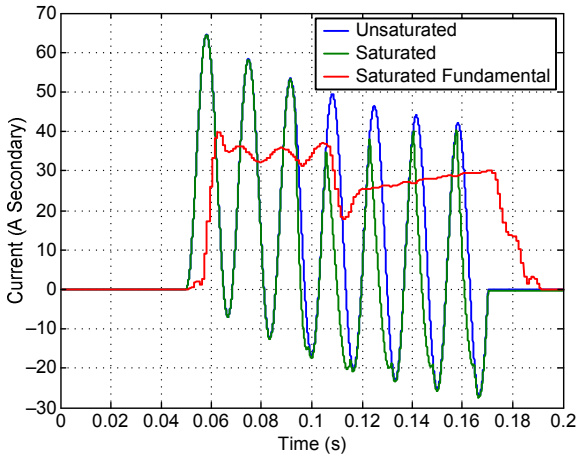

Fig. 9. Internal fault as seen from Terminal L in Fig. 8.

B. Distance Elements

Fig. 10 shows the calculation of m_{PG} using (23) for the internal single-phase-to-ground fault of Fig. 9. The distance element operates when m_{PG} is less than the element reach setting. In this example, the fault is in the center of the line and the resulting value of m_{PG} should be (0.68/2) • (1200/5) • (120/345000) = 0.28 Ω secondary. Fig. 10 shows that CT saturation causes the distance element to measure a higher m_{PG} value (because of the lower measured I_{PG} value). As a result, the element underreaches. Clearly, saturation is more likely for close-in faults because I_{PG} in (23) is larger. However, there is also a larger margin between the measured impedance and the reach setting.

For an underreaching Zone 1 element, saturation for faults close to the reach point creates the possibility of a delayed operation. The element needs to wait for the dc offset to die out and the CT to recover. However, saturation must occur before the element has a chance to pick up. The situation can be made worse if the reach is reduced because of a high source impedance ratio (SIR); however, getting CT saturation with a high SIR is unlikely. In addition, if a poorly selected CT saturates for the symmetrical fault current, it does not fully recover after the dc offset dies out, and the Zone 1 element may fail to operate.

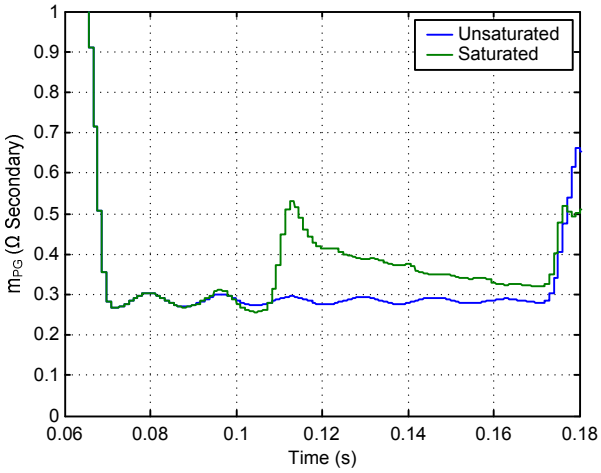

Fig. 10. A distance element underreaches for the internal fault of Fig. 9.

The backup Zone 2 could also be delayed for a fault just beyond the remote terminal. The Zone 2 instantaneous element picks up to start the timer only after the dc offset dies out and the CT recovers. The situation can be managed by increasing the reach setting.

C. Directional Elements

Directional elements are used in pilot schemes to provide sensitive ground fault protection. They are also used to supervise distance elements. Negative-sequence and zero-sequence impedance-based directional elements use the characteristic equations (24) and (25). These elements measure the impedance behind the relay for a forward fault and the impedance in front of the relay for a reverse fault. The operating characteristic for the impedance-based directional elements is shown in Fig. 11.

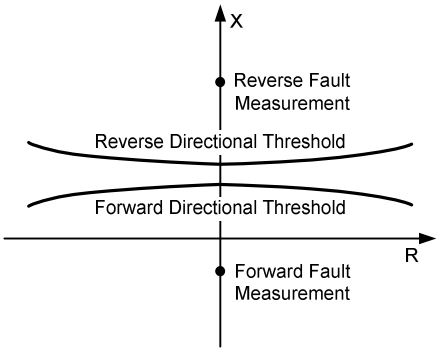

Fig. 11. Impedance-based directional element operating characteristic.

Fig. 12 shows the directional element calculations of z_0 using (24) and z_2 using (25) for the internal fault of Fig. 9. Note that the effect of saturation is to push the sequence impedance measurement farther into the negative region. Therefore, the dependability of the directional element is not a concern.

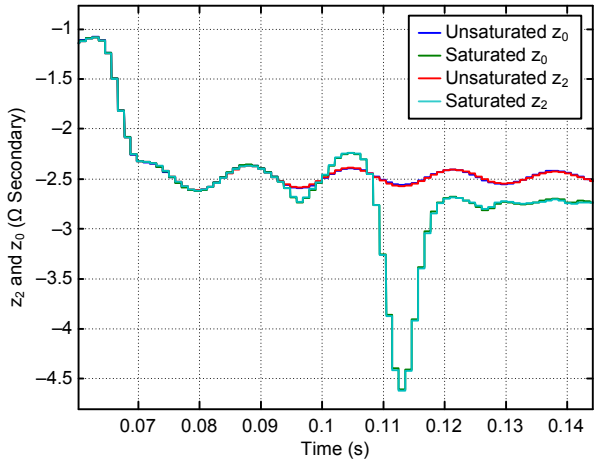

Fig. 12. Directional element response for the internal fault of Fig. 9.

We can gain some insight into the security of directional elements by looking at the case of an external fault at Terminal R on the example power system of Fig. 8. Fig. 13 shows the current at Breaker BR2, and Fig. 14 shows the directional element calculations using (24) and (25).

The relay at Breaker BR1 sees only the contribution from the source SR. However, the relay at Breaker BR2 sees the entire fault contribution. As a result, the CT at BR2 saturates in less than 2 cycles.

The measured z_2 and z_0 initially increase but then decrease as a result of saturation. This decrease creates a risk of the declaration of a forward fault and jeopardizes security. An appropriate selection of the forward direction setting mitigates this risk. For instance, if the forward directional threshold is set at half the line impedance, or 0.28 Ω secondary in our example, Fig. 14 shows that there is significant margin between the measured z_2 or z_0 and the threshold for this event.

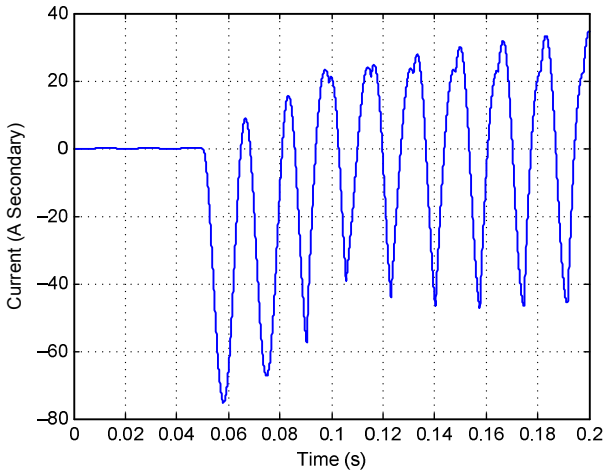

Fig. 13. Current at Breaker BR2 for an external fault at Terminal R.

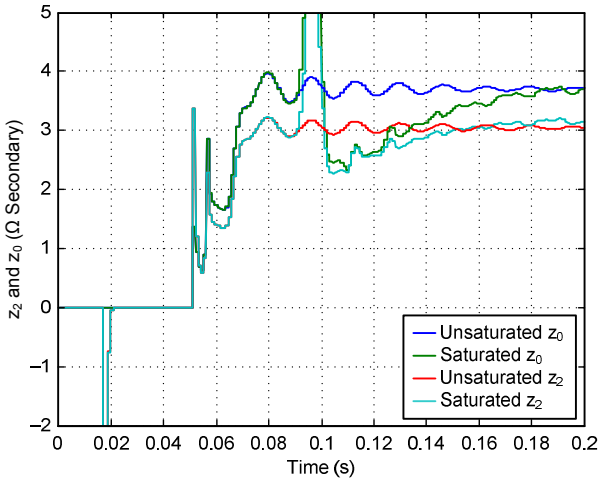

Fig. 14. Directional element response for the external fault of Fig. 13.

D. Line Current Differential Elements

Line current differential elements offer great sensitivity through the measurement of currents at each terminal. However, they can suffer from security problems during CT saturation.

Traditional line current differential schemes use percentage differential elements, which compare differential current I_{DIF} with restraining current I_{RST}. The element generates a tripping signal if I_{DIF} is greater than a percentage of I_{RST} and is also greater than a minimum pickup current. The element operating characteristic is typically a plot of I_{DIF} as a function of I_{RST}.

The current-ratio complex plane, or Alpha Plane, provides a way to analyze the operation of a two-restraint differential element [14]. In line current differential protection, the Alpha Plane is a plot of the ratio of the remote current I_R to the local current I_L, given by (26).

$$k = \frac{I_R}{I_L} \tag{26}$$

The line current differential elements that operate based on the Alpha Plane principle continuously calculate the ratio in (26) and compare this ratio with an operating characteristic defined on the Alpha Plane (see Fig. 15).

Fig. 15 shows the A-phase Alpha Plane loci for an external fault on the example power system of Fig. 8. The plot shows the responses for the cases of external summation of both CT currents at Terminal R (by paralleling the CT secondaries) and for independent measurement of both CT currents at Terminal R (using a relay with two sets of current inputs). In this example, the loci remain in the restraining region of the characteristic and the relay remains secure. Independent measurement of the currents provides a smaller excursion from the ideal blocking point (–1,0), which increases security.

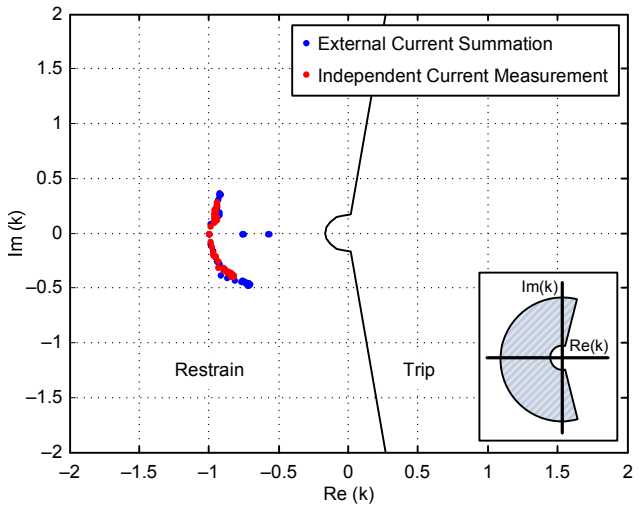

Fig. 15. An Alpha Plane phase plot for an external single-phase-to-ground fault on the Fig. 8 system.

Fig. 16 shows a percentage differential plot generated using the same currents as in Fig. 15. The beneficial effect of independent CT current measurement is evident in the boosted restraining signal.

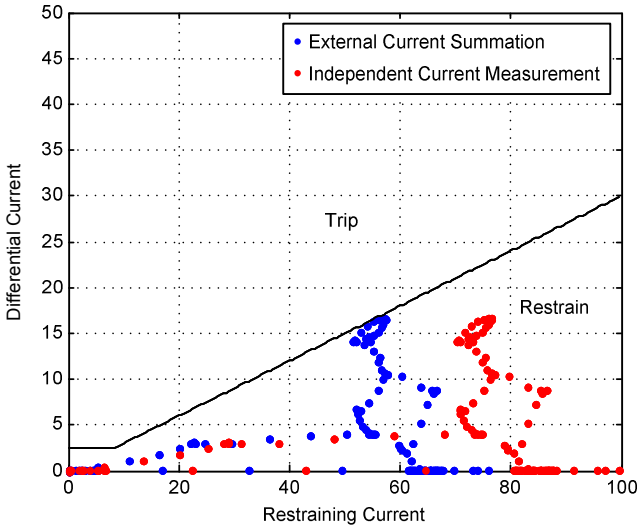

Fig. 16. A phase percentage differential plot for an external single-phase-to-ground fault on the Fig. 8 system.

Fig. 17 and Fig. 18 illustrate the response of zero-sequence differential elements to a three-phase external fault with heavy and uneven CT saturation on the example power system of Fig. 8. Because there will normally be no zero- or negative-sequence components for this fault type, any CT saturation has a serious impact on security. Independent measurement of currents is of virtually no benefit in this example. In both the Alpha Plane and percentage differential plots of Fig. 17 and Fig. 18, the locus moves solidly into the operating region of the characteristic during the fault.

Fig. 18 shows that as soon as saturation begins at any CT, the locus moves up toward the 45-degree line, which is characteristic of a single infeed fault. Saturation of the other end CT reduces the differential current; however, CTs cannot be relied upon to saturate at the same time or to the same degree—especially on multiterminal lines or on lines with dual-breaker terminals.

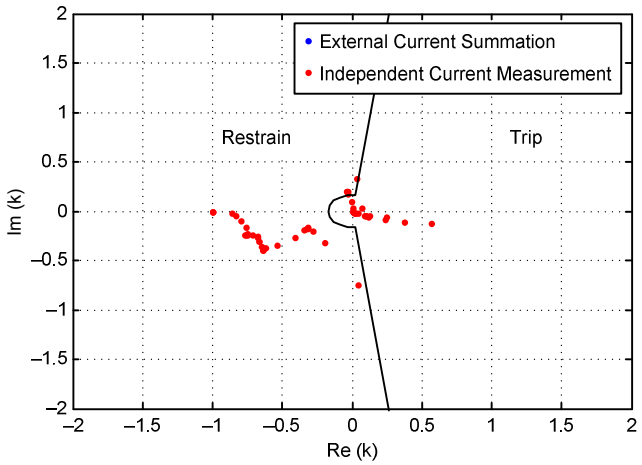

Fig. 17. A zero-sequence Alpha Plane plot for an external three-phase fault on the Fig. 8 system.

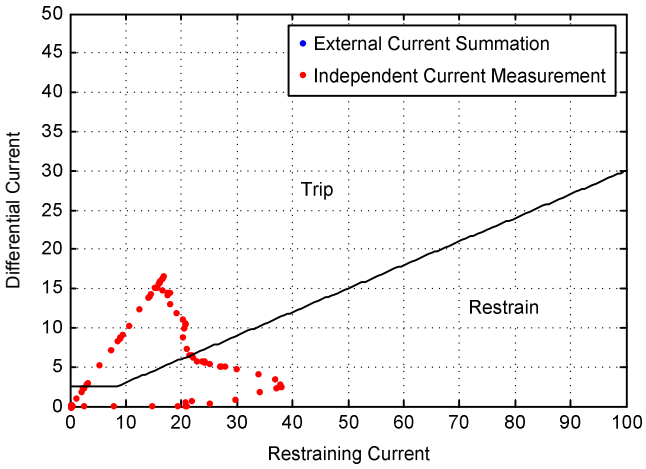

Fig. 18. A zero-sequence percentage differential plot for an external three-phase fault on the Fig. 8 system.

Due to the nature of their operating and restraining quantities, negative-sequence differential elements are at risk for three-phase external faults, while zero-sequence differential elements are at risk for phase-to-phase and three-phase faults.

IV. Advances in Modern Protection Designs

In many situations, CT saturation is unavoidable and compromises the protection element operation either by slowing down the trip or by causing a misoperation. Digital technology allows for the implementation of algorithms that mitigate the effect of CT saturation and increase the reliability of protection elements in the presence of saturation. Examples of such algorithms are provided in the next subsections.

A. High-Speed Distance Elements

Conventional distance elements based on full-cycle filters provide operating times on the order of 1 to 1.5 cycles, depending on the circumstances of the fault. Saturation

occurring within this time reduces the magnitude of the current phasor estimate, producing element underreach. Various advancements, such as the use of short window filters and incremental quantities, have pushed the operating speed of distance elements into the subcycle range [15]. Improved operating times have beneficial impacts on performance during CT saturation. For example, consider an 11 kA fault on a power system with an X/R of 12. Assume also a C400, 1200/5 CT with an R_S of 0.5 Ω, an R_B of 1 Ω, and a V_{SAT} of 350 V. We can calculate the CT time to saturation T_{SAT} as the following [4]:

$$T_{SAT} = -\frac{X/R}{\omega} \ln\left(1 - \frac{\frac{V_{SAT}}{I_F\left(R_S + R_B\right)} - 1}{X/R}\right) = 13.3 \text{ ms} \quad (27)$$

A subcycle distance element is likely to pick up before saturation occurs. The element may subsequently drop out once saturation begins, but breaker tripping will have already been initiated. We cannot make the same conclusion for the traditional 1-cycle distance element. Even in the case where saturation occurs, studies show that high-speed elements are impacted less severely [16].

B. Cosine-Peak Adaptive Filter for Instantaneous Overcurrent Elements

As mentioned previously, in power plant auxiliaries, fault current can go as high as 40 kA with an X/R ratio in excess of 20. Furthermore, low-ratio CTs can be used with instantaneous overcurrent elements set as high as 80 A. Even in the case where fault levels are not excessive, the *C* rating is sometimes limited by the available physical space for the CT. This issue has become more common recently in industrial applications.

The resulting high level of CT saturation can cause a very long delay before the fault current value measured by the digital filter of the instantaneous overcurrent element reaches the pickup setting and causes a trip. In the extreme case, the filtered current may not have sufficient magnitude to produce a trip.

To solve this problem, a cosine-peak adaptive filter (the basic principle is shown in Fig. 19) has been included at the front end of instantaneous overcurrent elements [10] [11]. The adaptive filter consists of supplementing the conventional cosine filter with a peak detector. In a situation of saturated current, the peak detector measures a higher current magnitude than the cosine filter and therefore speeds up the operation of the instantaneous overcurrent element. Transition to the peak detector to measure the current magnitude occurs when a current distortion index reaches above a threshold. The current distortion index is the ratio of the fundamental plus the second and third harmonics to the fundamental. During saturation, the distortion index reaches well above the threshold and switches the current magnitude filter to the peak detector.

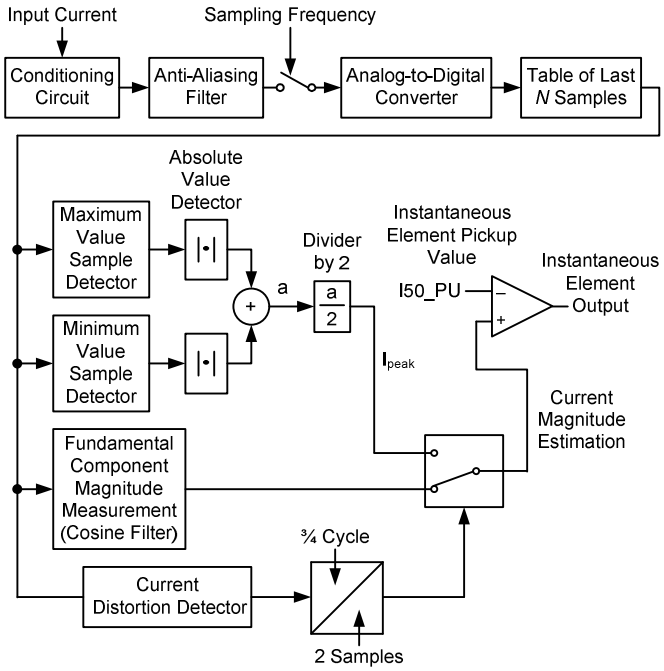

Fig. 19. Cosine-peak adaptive filter.

The performance of the adaptive filter can be demonstrated with a real case study. An instantaneous overcurrent phase element with a pickup of 67.5 A is protecting a motor. The CT has a C25 rating and a 200/5 ratio. The fault current is 35 kA with an X/R of 21. The burden is 0.189 Ω.

Fig. 20 shows the performance of the cosine-peak adaptive filter. Whereas the cosine filter picks up in about 2 cycles, the adaptive filter asserts in less than 1 cycle, allowing a gain of 1 cycle in speed. Cases with a greater speed gain can easily be found [10] [11].

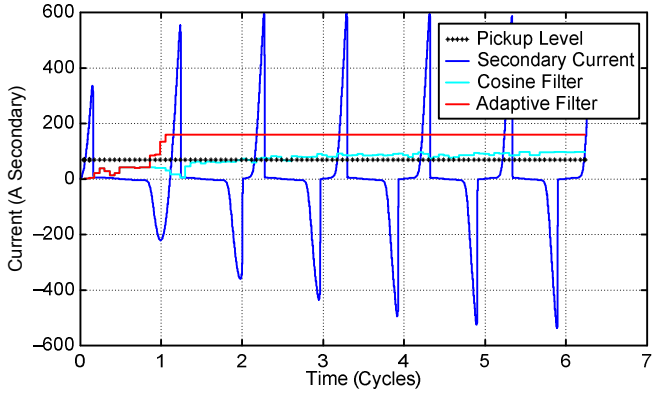

Fig. 20. Adaptive filter performance.

C. External Fault Detection Enhances Security of Differential Protection

External fault detectors (EFDs) have been used to improve security in several transformer and bus differential relay implementations with great success. The external fault detection principle has been extended for use in a line current differential relay [17]. Separate detectors are implemented to detect ac and dc saturation.

Fig. 21 shows the simplified logic diagram of the ac external fault detection logic. Input signals to this logic are the instantaneous samples of the differential current (i_{DIF}) and the restraining current (i_{RST}). During a heavy external fault, the CTs are initially expected to provide at least one-fourth of a cycle of saturation-free operation (defined by the timer pickup setting DPU_{AC}). The ac logic therefore looks for a step increase in the restraining current i_{RST} that is not accompanied by the corresponding increase in the differential current i_{DIF}. The increase must be significant—greater than the factory constant *P* and i_{DIF} times a factory constant 1/q.

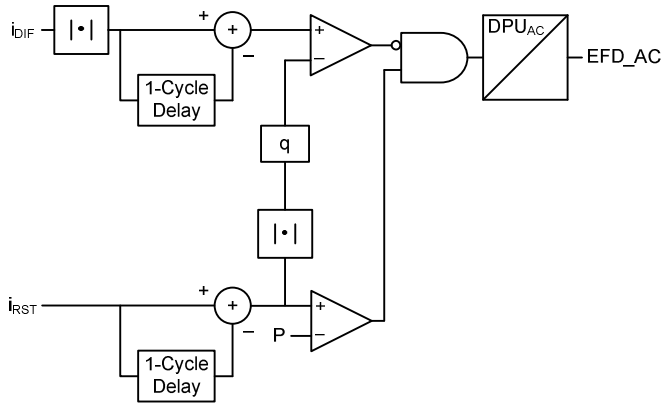

Fig. 21. AC external fault detector.

In the line current differential implementation, the relays exchange samples in order to develop instantaneous values of the differential and restraining signals. This ensures that the detector is fast enough to supervise the element without the need to slow down the differential element operation.

For detecting low-magnitude external faults that have a long decaying dc offset component, the dc logic (see Fig. 22) compares the fundamental frequency current magnitude I_{AC_MAG} with the dc component current magnitude I_{DC_MAG}. A significant dc component is declared if the dc component is greater than a fixed portion P_{DC} of the ac component at the time. An external fault is declared if the current contains a significant dc component and the differential current i_{DIF} is less than the restraining current i_{RST} times the factory constant K_{DC} and if this situation persists for several cycles (defined by the timer setting DPU_{DC}).

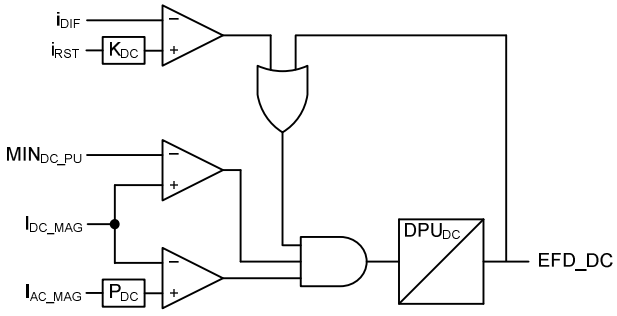

Fig. 22. DC external fault detector.

The outputs from the ac and dc external fault detectors are connected together by an OR gate.

When an external fault is detected, several steps are taken to secure the differential elements [17]. In the phase elements, a portion of the harmonic content of the differential signal is used to boost the restraining signal. In the sequence elements, a portion of the phase restraining signal is used to boost the sequence restraining signals. In both the phase and sequence elements, a delay is inserted in the tripping path. Finally, the restraining region of the operating characteristic is expanded by dynamically applying alternate settings.

D. Restraining or Blocking Sequence Elements in Line Current Differential Protection

Sequence elements (87L2 and 87LG) in line current differential protection can lose their security during external faults with CT saturation. Section III, Subsection D and [18] show that a very small amount of CT saturation can cause these elements to misoperate. The purpose of sequence elements in line current differential schemes is to detect resistive faults for which CT saturation would be very unlikely because of the low level of the fault current.

Two techniques have been used to restore the sequence differential element security. When an external fault detector is available, as described in the previous subsection, and when it asserts, a portion of the highest phase restraining current is added to the sequence element restraining signal [17]. Reference [18] describes an alternative to the external fault detector in the form of a saturation detector. The saturation detector generates an error signal composed of the highest dc and second-harmonic components of all phase currents. When the differential negative- or zero-sequence current becomes greater than the error signal, the sequence element (87L2 or 87LG) is allowed to operate. Otherwise, it is blocked. Both techniques have been implemented in relays and have been proven to ensure sequence element security in adverse CT saturation conditions.

V. Tools for CT Sizing

A. ANSI/IEEE Guidelines

In Section II, we presented equations that describe unsaturated CT operation of relaying CTs with ANSI/IEEE accuracy classes. We can apply these equations as a first step to determine CT suitability for a particular application. If unsaturated operation can be guaranteed, then no further analysis is warranted. We illustrate this concept with the following examples.

1) Symmetrical Fault Current

A C400, 2000/5 CT has a burden of 8 Ω. The standard burden of a C400 CT is $Z_{B\ STD} = 4$ Ω. Then, based on (11), the maximum pu symmetrical fault current without exceeding a 10 percent ratio error is $I_f = 20/Z_b = 20/(8/4) = 10$ pu.

The maximum primary fault current is 10 pu • 2,000 A = 20,000 A. If the CT has a burden below 4 Ω, the maximum current calculated by the previous procedure is more than 20 times rated current. The ANSI/IEEE standard does not specify what the CT behavior will be for currents above 20 times rated current. Hence, the maximum allowable current

is 20 times rated current in this case. For example, for a 2 Ω burden, the maximum current is 40 pu, or 80,000 A. However, the maximum allowable current is really 20 pu • 2,000 A = 40,000 A.

For the same CT, the maximum pu allowable burden without exceeding a 10 percent ratio error with a fault current of 30,000 A is $Z_b = 20/I_f = 20/(30{,}000/2{,}000) = 1.33$ pu.

Therefore, the allowable burden is $Z_B = 1.33$ pu • 4 Ω = 5.33 Ω.

If the CT were operating in the 1500/5 tap, the pu burden would be $Z_b = 20/I_f = 20/(30{,}000/1{,}500) = 1$ pu. For this 1500/5 tap, the standard burden is (1,500/2,000) • 4 Ω = 3 Ω.

Thus the allowable burden would be $Z_B = 1$ pu • 3 Ω = 3 Ω.

2) Asymmetrical Fault Current

Now, consider the C400, 2000/5 CT with a 1 Ω burden ($Z_b = 1/4 = 0.25$ pu). If the system X/R ratio is 12 (X/R + 1 = 13), we can use (20) to find the maximum pu fault current without exceeding a 10 percent ratio error: $I_f = 20/((0.25)\,(13)) = 6.15$ pu.

The maximum primary fault current is 6.15 pu • 2,000 A = 12,307.7 A.

In the previous example, we concluded that a C400, 2000/5 CT with a 1 Ω burden allows a pu fault current of 6.15 pu for an X/R of 12. Now, assume that this CT has 30 percent of remanent flux. Using (21), it follows that the allowable fault current is 6.15 (1 – 0.3) = 4.305 pu, or 8,610 A.

For the same CT, the maximum pu allowable burden without exceeding a 10 percent ratio error for a fault current of 10,000 A ($I_f = 10{,}000/2{,}000 = 5$ pu) is $Z_b = 20/((5)\,(13)) = 0.3077$ pu.

Hence, the allowable burden is $Z_B = 0.3077$ pu • 4 Ω = 1.23 Ω.

The example can be repeated considering remanence using (21).

B. IEC Guidelines

IEC 44-6 presents the requirements for CT transient performance in the form of a minimum saturation voltage as the following [19]:

$$E_{al} = K_{ssc} K_{td} \left(R_{ct} + R_b\right) I_{sn} \tag{28}$$

where:

E_{al} is the CT secondary excitation voltage, which corresponds to a magnetizing current that produces the maximum permissible error.

K_{ssc} is the ratio of fault current to nominal current.

K_{td} is the transient dimensioning factor.

R_{ct} is the CT secondary resistance.

R_b is the CT burden.

I_{sn} is the nominal secondary current.

K_{td} is derived from the transient factor K_{tf}, given as the following:

$$K_{tf} = \frac{\omega T_P T_S}{T_P - T_S}\left(e^{-t/T_P} - e^{-t/T_S}\right) - \sin \omega t \tag{29}$$

where:

T_P is the time constant of the primary circuit.

T_S is the time constant of the secondary circuit.

K_{tf} is essentially the factor required for saturation-free operation for a fully offset waveform at a given instant of time. The use of this factor recognizes that protection elements may operate before the CT enters saturation.

Local maxima occur whenever sin ωt = –1. The transient dimensioning factor is therefore given as the following:

$$K_{td} = \frac{\omega T_P T_S}{T_P - T_S}\left(e^{-t/T_P} - e^{-t/T_S}\right) + 1 \tag{30}$$

For the typical case where $T_P >> T_S$, K_{td} reduces to the following:

$$K_{td} = \omega T_P \left(1 - e^{-t/T_P}\right) + 1 = \frac{X}{R}\left(1 - e^{-t/T_P}\right) + 1 \tag{31}$$

Fig. 23 shows the plot of (31) for an arbitrary system with an X/R of 19. Noting that K_{td} in (31) converges to X/R + 1, we can now see a similarity between (20) and (28).

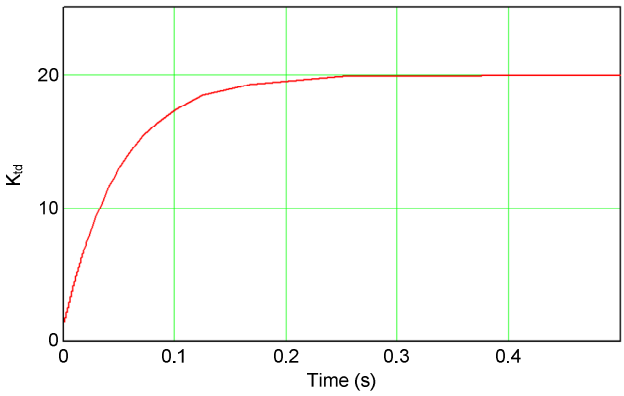

Fig. 23. Plot of K_{td} for an X/R of 19.

In general, if the operating time is longer, then a larger K_{td} is required and a better CT is needed. If the relay operating time and time constants are known, the protection engineer can determine K_{td} from (31).

C. Manufacturer Guidelines

Ideally, the CTs should be sized based on equations, such as (20) and (28), that avoid saturation. However, CT sizing restrictions make CT saturation possible in some applications. The relay design techniques described in Section IV improve protection element response to CT saturation and allow for a more relaxed CT selection.

Some manufacturers provide guidance on CT selection considering some tolerance to saturation. For example, [16] proposes adding a CT dimensioning factor to (20) to account for CT saturation, which results in (32). This equation, valid for relaying CTs with ANSI/IEEE accuracy classes, allows the calculation of the maximum burden for which CT saturation will not affect the performance of a particular relay.

$$Z_B \le \frac{kV_{STD}}{I_F\left(\frac{X}{R}+1\right)} \tag{32}$$

where:

Z_B is the CT burden.

k is a dimensioning factor.

V_{STD} is the secondary terminal voltage rating.

I_F is the fault current referred to secondary.

Extensive real-time digital simulator tests allow the determination of the k values for different relays. For example, for a particular distance relay, $k = 6$ is recommended [17], and for a line differential relay, $k = 7.5$ is recommended.

Similarly, the manufacturer can recommend a value for K_{td} for the IEC equation (28). The manufacturer may carry out simulator testing over a range of system parameters and conditions in order to determine the optimum value of K_{td}. This testing accounts for the operating time of the relay and any advanced algorithms for dealing with CT saturation. Use of the manufacturer recommendations can therefore result in a relaxed requirement for the CTs.

D. Simulation Software

As mentioned previously, CT saturation is unavoidable in many applications. However, relays provide methods to address saturation. These methods may take the form of the advanced algorithms described in Section IV or simply traditional secure settings, such as a pickup or slope setting. We can evaluate the combined performance of the CT and the relay through time-domain computer simulation. These tools have become increasingly accessible to protection engineers. Available software packages include Electromagnetic Transients Program/Alternative Transients Program (EMTP/ATP), PSCAD®, and MATLAB® Simulink. In general, these tools allow the user to model the power system, including the transmission line, terminal sources, breakers, and the CTs and their secondary burdens. A complex scenario, such as a permanent fault with autoreclosing, can be modeled. The output of the simulation is a data set representing the instantaneous values of the CT secondary currents throughout the fault. These data provide useful information regarding the time to saturation and the degree of saturation of the CTs. Fig. 9 and Fig. 13 are examples of computer simulation results.

The CT secondary current data can be further processed to gain a better understanding of relay response. Some simulation packages allow this processing to be carried out directly. Another option is to pass the data to a second software tool. Available tools include Mathcad®, MATLAB, and Microsoft® Excel®.

With these tools, the user can model the relay processes of low-pass filtering, sampling, and phasor estimation. Next, the phasor data can be further processed using a characteristic equation, which represents the particular protection element. Fig. 10, Fig. 12, and Fig. 14 through Fig. 18 are examples of this processing.

While this approach can provide the most accurate and insightful assessment of combined CT and relay performance, computer simulation is not widely applied today for several reasons. The first reason is the cost of the various software packages. However, these costs are coming down, and some available tools are in the public domain. The second reason is the nontrivial effort required to develop the power system model and simulate relay processing. In particular, modeling relay behavior requires a good understanding of digital signal processing. References [20] and [21] provide detailed guidance on the process. Finally, some manufacturers may not provide all the relevant details required to model relay behavior. The user can resort to the use of generic filters and characteristic equations. Still, some doubt will remain concerning the accuracy of the model.

E. CT Modeling Tools

A simplification of the method described in Section V, Subsection D focuses on the CT transient response. One method is described in [7] and implemented in Mathcad.

The CT behavior is modeled using Frolich's equation inserted into a differential equation that is solved numerically to produce the saturated CT secondary current [7].

The result is passed through a low-pass analog filter and a full-cycle cosine filter to produce the calculated current magnitude shown in Fig. 24.

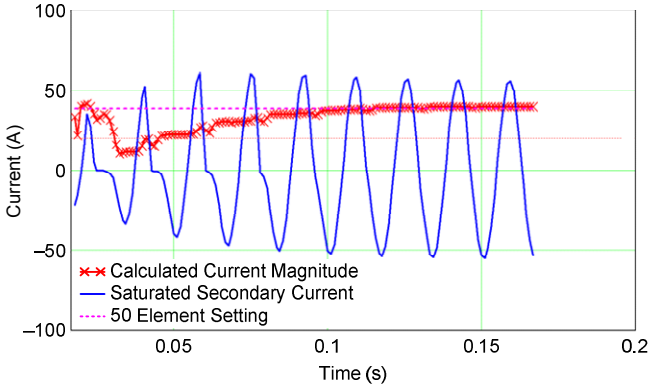

Fig. 24. Mathcad model of a CT and relay response.

A second CT modeling approach makes use of the IEEE CT saturation calculator. This is an Excel spreadsheet available for download on the IEEE Power System Relaying Committee (PSRC) website [22]. The primary current is defined similarly to the previous Mathcad example. The spreadsheet then undertakes a numerical solution to a differential equation to arrive at the saturated CT secondary current. The spreadsheet also generates phasor values using a full-cycle Fourier filter.

The output from this tool can be linked dynamically to a second spreadsheet in order to model the relay characteristic.

Fig. 25 shows an example of this approach, where an Alpha Plane characteristic is implemented in an Excel spreadsheet, which is linked to the PSRC spreadsheet.

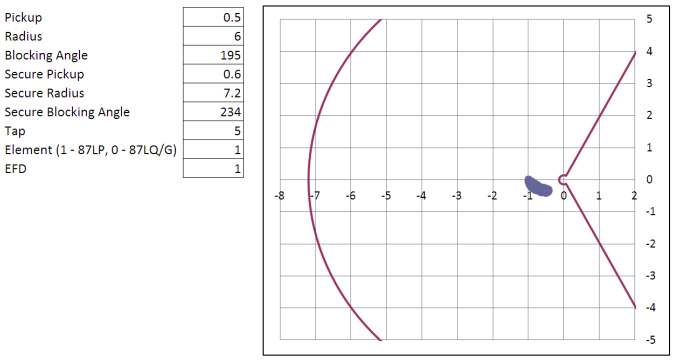

Fig. 25. Alpha Plane plot in Excel.

VI. Conclusion

Ideally, we would like to select CTs that always operate in their linear regions during system faults. However, CT saturation is sometimes unavoidable. Some line protection elements are more adversely impacted. For instance, differential elements that respond to sequence quantities must be designed with enhanced security for external faults with CT saturation.

Algorithms have been developed to secure protection elements for CT saturation. These new algorithms allow relaxing the CT requirements. However, they also present a challenge for the protection engineer, who now must consider relay behavior in addition to CT behavior.

Manufacturers provide guidelines and dimensioning factors that greatly simplify the task of CT selection. The adequacy of these guidelines has been confirmed by the manufacturer—often through rigorous testing of the particular relay over a range of system parameters.

Modeling tools are also available and are increasingly more accessible to protection engineers. More effort is required to apply these tools. Often, however, they provide more insight into the transient behavior of the protection system as a whole (CT and relay). These tools can also be useful for examining how relay settings can be optimized to deal with CT saturation in an existing system.

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VIII. BIOGRAPHIES

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