Beyond Protection and Control Schematic and Logic Diagrams

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Presented at the
42nd Annual Western Protective Relay Conference
Spokane, Washington
October 20–22, 2015

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***Abstract*—This paper explains why new design possibilities provided by modern intelligent electronic devices (IEDs) make it very difficult to describe protection and control (P&C) system functionality using traditional schematic diagrams. It also shows that diagrams representing logic programmed in P&C devices do not fully depict the application. The paper describes the experience of a specific utility as they worked to modernize their logic and documentation while also supporting a very mature P&C documentation and standards environment. Specifically, the paper explains new guidelines for logic diagram creation (LDC) developed by Comisión Federal de Electricidad (CFE), Mexico's national electric utility. These LDC guidelines have been used to document functional interactions between IEDs and switchgear in P&C systems. The paper also explains how the LDC guidelines make allowances for developing models, how they can be extended for use in specialized applications, and how this technique allows new applications to be developed as required. The paper describes models for switchgear and protection functions and explains how they could be applied by other electric utilities to document P&C systems. Finally, the paper provides an analysis of the current status of CFE LDC guidelines and describes the way they have been adopted and further developed by equipment manufacturers and system integrators.**

I. Introduction

The design documentation package of a protection and control (P&C) system should provide detailed information for physical construction of the system. It should also document the functions of the system so the designer can verify design accuracy and so operations and maintenance personnel can operate, test, commission, and troubleshoot the system [1] [2].

In traditional designs where the P&C system logic is hardwired into the panel, electrical diagrams (elementary/schematic and wiring diagrams) provide all the information required by operations personnel. In microprocessor-based P&C systems, part of the logic is programmed in the relays and other intelligent electronic devices (IEDs). In these systems, logic diagrams supplement electrical diagrams to show the functions programmed in each IED. In addition, in a digital substation automation system (DSAS), many communications-assisted P&C functions require digital messaging. A communications diagram showing digital message configuration for data flow engineering, the cable routing, and the communications network device data flow configuration (including tables and files) may also be part of the design documentation package.

Often, logic diagrams for a utility's P&C systems are created by external engineering companies using various programming tools. As a result, the final user has to deal with many different types of logic diagrams, which complicates commissioning and troubleshooting tasks and increases the likelihood of human error. Based on the experience of Comisión Federal de Electricidad (CFE), in some cases the initial logic diagrams and the final program lines of code or their graphical representation are radically different.

In addition, depending on substation requirements, CFE uses either copper wires or optical fiber—using IEC 61850 Generic Object-Oriented Substation Event (GOOSE) messages—for the circuit breaker tripping signals. There are two options for sending tripping signals over optical fiber: point-to-point communication using remote input/output (RIO) modules with logic programming ability (called CuFO by CFE); or point-to-multipoint communication using remote processing modules (RPMs) with logic programming and IEC 61850 manufacturing message specification (MMS) server ability (called MESs by CFE). For switchgear control, CFE uses programmable logic, hardwiring, and/or GOOSE messaging. The resulting level of P&C system complexity makes it difficult to fully describe these systems in traditional electrical and logic diagrams.

Considering all of these problems, CFE started developing rules to create graphics logic diagrams for DSASs in November 2012. The resulting guidelines for logic diagram creation (LDC) have been used to document functional interactions between IEDs and switchgear in CFE P&C systems [3] [4] [5] [6].

CFE has a set of DSAS specifications called Substation Automation System (SAS), which addresses network topology, functionality, device requirements, and data models [7]. These specifications describe IEC 61850-based systems [8], and consist of 21 documents (for an example, see [7]). These specifications include requirements resulting from CFE's best design practices that are not addressed by IEC 61850. Today, CFE has more than 100 substations in operation based on these specifications [9] [10] and nine years of experience in designing, commissioning, and documenting DSASs [8]. CFE also has a set of guidelines for creating DSAS design documentation (for an example, see [1]), which covers systems based or not based on the IEC 61850 standard. The CFE LDC guidelines described in this paper are part of the design documentation guidelines.

This paper provides a brief description of the CFE LDC guidelines, explains the concept of models, shows how the

guidelines can be extended for use in specialized applications such as specific bus arrangements, and discusses how this technique makes allowances for developing new applications when required. The paper describes models for switchgear and protection functions and explains how they could be applied by other electric utilities to document P&C systems using any hardwiring, programmable logic, and communications channels. Finally, the paper provides an analysis of the current status of the CFE LDC guidelines and describes the way they have been adopted and further developed by equipment manufacturers and system integrators.

II. Function Modeling

A. Basic Definitions

Part 1 of the CFE LDC guidelines covers basic definitions and general requirements, such as actions, signals, functions, and models [3].

A function is a task to be performed by one or more devices to protect or control elements in a substation. The devices process the received signals to execute actions in order to perform their function. The number of devices to be used depends on the utility's approach to ensuring P&C system dependability and security. When a set of devices performs a function, each device may perform subfunctions or small tasks. Functions can be classified in different ways and take different names.

A model is the graphical representation of a function. It describes the signals used, the way they are processed, and the actions executed. Models can be implemented in different ways using different technologies. Models define functions and subfunctions, provide function names, and standardize function behavior descriptions. Models show the input and output signals required to perform the function, but they do not show the way these signals are obtained from their sources or how they are sent to the receivers to perform an action. For example, a model does not specify if an input is a switchgear status dry contact signal or if it is a GOOSE message from an IED installed in the substation switchyard. Similarly, a model does not show if a task, such as energizing a circuit breaker close coil, is performed by closing a bay controller contact or by sending a GOOSE message to an IED installed in the switchyard.

The model represents a function performed in exactly the same way by different IEDs or describes the behavior of the substation switchgear equipment. For this reason, the CFE LDC guidelines define a model only one time in only one place; other parts of the documentation refer to that definition in order to avoid errors or unexpected performance. When engineers detect a system misoperation caused by logic (programmed or hardwired) implemented using a model, they fix it by updating the model definition in the CFE LDC guidelines. Some parts of the documentation referencing that model may require updating to reflect the model changes; some other parts may not require updating. After the updates, it is necessary to update device configurations or hardwiring to reflect the change in the model.

CFE basic guidelines for logic diagrams are covered in Part 1 and Part 2 of the CFE LDC guidelines [3] [4]. As with many other standards, the CFE LDC guidelines apply the "don't repeat yourself" concept as the basis for all logic diagram definitions. This phrase refers to defining the model once and then using and referencing that model multiple times instead of repeatedly creating similar models.

B. Model Definition

1) Model Representation

A model is represented in a logic diagram as a "black box" with inputs and outputs, as shown in Fig. 1. The model representation may include the logic required to perform the function (Fig. 15 shows an example of this type of representation).

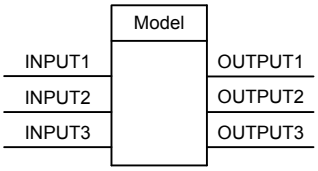


Fig. 1. Example of model representation used in logic diagrams.

Once a model is defined, such as the model for a protection function or switchgear, it is reused in logic diagrams and adapted to specific applications to create specialized models. Fig. 2 shows the use of models in a logic diagram. This figure depicts a breaker-failure (50BF) function logic. It processes the primary relay tripping signals (breaker-failure initiate signals), attempts to retrip the breaker after some time, and trips the backup breaker(s) when the breaker-failure timer expires.

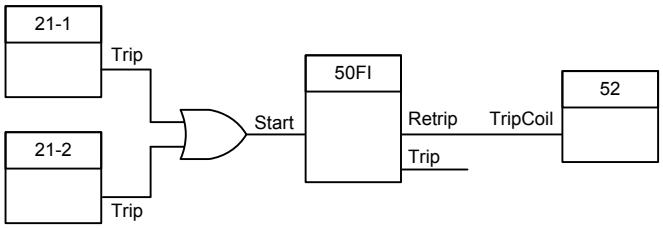


Fig. 2. Using models in the logic diagram of a breaker-failure protection scheme.

2) Signal Naming

Signal naming is a key aspect of the CFE LDC guidelines. Part 1 covers naming definition conventions, and Part 2 addresses basic naming for signals and model definitions [3] [4]. The switchgear and protection functions in Part 3-1-1 and Part 3-2-1 define standard naming to avoid unclear or incomplete signal naming [5] [6].

The naming definition conventions given in Part 1 are based on Part 7-3 and Part 7-4 of IEC 61850 [11] [12]. They take the same semantics and names from IEC 61850 and add new ones as required, following IEC 61850 rules.

Mexico's National Energy Control Center (CENACE) defined the rules for creating numbers to identify circuit breakers and disconnect switches. These numbers implicitly reflect the location and function of switchgear equipment in the substation.

The CFE LDC naming definition convention uniquely names data and meets both the IEC 61850 conventions and the CENACE nomenclature. For example, the CFE LDC guidelines use the generic name 00XCBR.Pos.stVal.on for a model requiring circuit breaker "close" status in a bay; the CFE LDC guidelines use the name 01XSWI.Pos.stVal.on for the model of a disconnect switch in a Number 1 bus. To use the circuit breaker model in the switchgear logic for a given installation, the model name is made more specific by applying the CENACE nomenclature: 93100XCBR.Pos.stVal.on (93100 is the CENACE name for a circuit breaker). This naming methodology has general value because utilities typically have naming conventions for applications such as supervisory control and data acquisition (SCADA) and need a method to map them to newer IEC 61850 configurations.

3) Modeling Language Used in the CFE LDC Guidelines

The CFE LDC guidelines use the Unified Modeling Language™ (UML®), a visual modeling language for modeling business and similar processes and for the analysis, design, and implementation of software-based systems. UML is intentionally process independent.

UML was adopted in 1997 by the Object Management Group® (OMG®), an international, open membership, not-for-profit technology standards consortium, founded in 1989. OMG manages and updates the UML specification. The latest version is UML 2.5 [13].

A UML model is a specialized package that describes a system from a certain point of view. A model hides or masks details, bringing out the big picture, or focuses on different aspects of the system. Models allow working at a high level of abstraction. Models are used to draw diagrams.

A UML diagram is a partial graphical representation of a model of a system under design or being implemented, or already in existence. UML diagrams contain graphical elements (symbols or UML nodes) connected with paths. These graphical elements represent elements in the UML model of the designed system.

The primary graphical symbols shown on a UML diagram define its kind. For example, a diagram where the primary symbols are classes is a class diagram. A diagram which shows use cases and actors is a use case diagram. A sequence diagram shows the sequence of message exchanges. UML specification allows different kinds of diagrams to be mixed.

The CFE LDC guidelines use UML class symbols to represent models. They use UML class diagrams in the model definition to describe when a model is an extension of an existing model.

In the CFE LDC guidelines, the UML path interconnections of graphical elements represent the signal interchange between model inputs and outputs. The guidelines add standard symbols and naming conventions to represent signal types and sources.

4) Components of the Model Definition

The model definition procedure established in Part 2 is comprehensive, defining class tables, UML hierarchy models, logic diagrams, and truth tables, as follows [4]:

- Class tables define name semantics for input and output signals and state if some of them should be "hidden" when a model is inherited and instantiated. Class tables are a key concept in the CFE LDC guidelines because they provide standard input and output signal naming and semantics in order to avoid misunderstandings about how the tables should be used and to aid in logic diagram interpretation.
- UML hierarchy defines class inheritance. The base class defines the basic inputs, outputs, and signal processing logic. To create specialized (derived) classes, CFE adds inputs, outputs, and processing logic to the base class. Specialized classes inherit signals and processing from the predecessor classes. UML hierarchy is a powerful method used to extend or adapt models to specialized applications while keeping them small and clear.
- Logic diagrams define how inputs should be processed to provide model outputs. Logic diagrams process inputs with logic gates, timers, and standard techniques to provide the output responses and behavior expected by the designer. They can use any standard symbols but should also use CFE model symbols to represent the inputs and outputs of other models. CFE uses IEC standard symbols [14]. However, ANSI/IEEE symbols can be used instead [15].
- Truth tables represent all model input combinations and the corresponding output responses. CFE uses truth tables to write algebraic Boolean equations when designing logic diagrams. Truth tables are particularly useful when using simulation software to analyze logic diagram functionality.

In the process of model definition, the designer analyzes all required predecessor classes in order to understand their inputs and the way they are processed to produce the outputs. Then, the designer defines the additional inputs, outputs, and processing required for the new specialized model to provide the expected behavior in the specific application and then assigns names for new inputs when required. This method allows the designer to concentrate on specific applications and avoid changing any previously defined behavior.

C. Abstract and Instantiable Models

1) Abstract Models

An abstract model provides basic functionality for other models to inherit when they reference the model. Abstract models cannot be used directly in a concrete application because they do not provide all the required functionality or because using them makes no sense for a given application. However, abstract models provide a mechanism to standardize and document the basic functionality of a model, allowing it to be referenced and reused.

Part 3-1-1 and Part 3-2-1 of the CFE LDC guidelines define abstract models for switchgear and protection functions, respectively [5] [6]. Part 3-1-1 defines an XSWC abstract model as a base class for circuit breakers and disconnect switches (X), which provides basic functionality, such as close and open commands and interlocks for local and remote operations (SWC). Part 3-2-1 defines an RPRT abstract model as the base class for all protection related functions (R); this class provides test mode and block mode functionalities (PRT).

CFE is still working to define the most common applications and to extend or add new abstract models to provide the expected P&C system dependability and security. These models should be applicable to any technological platform.

2) Instantiable Models

Models can also be created that refer to specific IEDs or signal interchange techniques (hardwiring or GOOSE messages, for example). The resulting logic diagrams show the terminals and GOOSE messages used in a specific application installation. This process is called instantiation. This allows CFE LDC guidelines to represent the processing logic (internal and external to the IED) required to perform functions. For example, concrete (specific or instantiable) models can be created by combining model graphical symbols (see Fig. 1) with logic gates (see Fig. 2).

Once a model is defined for a concrete application, such as a circuit breaker model for a breaker-and-a-half bus arrangement, it becomes a concrete or instantiable model. Instantiable models are extensions of abstract models or of other instantiable models. They include all additional inputs, outputs, and processing required to get the expected functionality or to fit a different application. For example, they can provide secure open and close commands by adding signals for interlocking. Fig. 14 shows an instantiable model example.

Instantiable models must be applied in all the utility substations as part of the company's engineering process. This practice formalizes the utility's P&C philosophy (which is not tied to a specific technology), simplifies the engineering process, and improves reliability by avoiding different behavior for the same functionality. In the previous example, the model for the circuit breaker in a breaker-and-a-half bus arrangement must be applied to all the circuit breakers in all the substations with this type of bus arrangement. As a result, the utility can have one type of engineering for each applied technology, always based on the same philosophy. In addition, the utility can be prepared to apply new technologies without changes in the system's expected behavior.

D. How Many Models to Use?

According to [1], defining models is the first step in the design of a P&C system. The number of models to define depends on the utility's P&C philosophy and the technology to be used. Abstract models express the philosophy. Engineers instantiate them according to the particular P&C technology to be used. The CFE approach for using these models in concrete applications is to create an instantiable model for each function and to program this function in the IEDs or use it in contact arrangements (as described in Section III, Subsection C of this paper). In other words, CFE defines one instantiable model per function, not per IED. For example, when circuit breaker IEDs perform the function to provide GOOSE message publication for status and GOOSE message subscription for tripping, CFE defines one instantiable model for this function and applies it to all circuit breaker IEDs that perform this function.

A more conservative approach is for the utility to define instantiable models that describe the engineering in use, in order to document the P&C philosophy for future generations of engineers. For example, the utility defines a model for exchanging signals among functions that meet the utility P&C philosophy regardless of the signal exchange technology used. Later, the utility can define instantiable models for concrete applications using hardwiring, proprietary relay-to-relay communications protocols, GOOSE messaging, or any technology available in the future.

III. Model Instantiation

A. Rules for Model Instantiation

Part 2 defines the rules for model instantiation, which is the process of defining sources and actions for signals in an instantiable model [4]. The sources are digital inputs that are processed on programmed logic. The actions are outputs, such as an output contact closing to energize a circuit breaker trip coil.

Part 2 defines how to represent actions and which symbols to use depending on the different alternatives for action manifestation defined in Part 1. The term "action manifestation" is used to describe the possible concrete results of an action, such as closing or opening a contact, assigning a Boolean value to a digital variable, changing the status of a GOOSE message published by the IED, or issuing a light alarm signal.

As mentioned before, all concrete applications of the same type requiring the same signals must use the same instantiable model. For an application requiring more signals, engineers can create a new model, maybe as an extension of the most widely used model in the substation. Part 2 uses the CENACE numbering system in the model instantiation process and for generic naming conventions. These data naming practices were developed to meet both the IEC 61850 conventions and the CFE corporate data naming practices.

B. IED Programmable Logic

Programmable logic is a powerful feature of microprocessor-based IEDs that reduces hardwiring and practically eliminates auxiliary relays in P&C systems.

For protection schemes with only one relay, CFE recommends using programmable logic to exchange signals between functions, monitor switchgear statuses, and perform any other task not requiring a different IED.

For protection schemes with more than one relay, such as line protection schemes, CFE recommends programming each

relay to perform the tasks that it must execute independently. Common tasks, such as signal exchange and interdevice logic (interlocks, for example), can be performed by one of the relays by using programmable logic or a contact arrangement including all the IEDs required to perform the task.

The instantiable model of programmed logic is a set of instantiable models that exchange signals, which is represented as a logic diagram inside a dashed rectangle (see Fig. 14). The name that identifies the IED in the system must be displayed above the top left corner of the dashed rectangle. The external signal exchange is represented by lines that connect the instantiable model outputs or logic results of outputs, with other instantiable models in other programmed logic or contact arrangements. The diagram also represents output binary contacts, showing the number of terminals—separated by a comma—within a set of parentheses. The diagram represents GOOSE message subscription and publication signals in square brackets with the GOOSE identification and reference to the data received or transmitted.

C. Contact Arrangements

Contact arrangements consist of IED binary outputs and auxiliary relay contacts combined to perform a task, such as interlocking for closing or tripping commands. In the CFE LDC guidelines, contact arrangements are included in instantiable models because they represent a specific technology for performing P&C tasks.

The instantiable model of a contact arrangement is a set of instantiable models that exchange signals, which is represented as a logic diagram inside a dot-dash rectangle (see Fig. 14). Logic gates process the signals. The model inputs could be outputs of other instantiable models, and the model outputs could act on terminals or other instantiable models, such as a circuit breaker trip contact arrangement.

Most logic diagrams include programmed logic and contact arrangements. The combination of both allows for the execution of all tasks, while ensuring high P&C reliability.

D. GOOSE Messages

As previously mentioned, the documentation package of P&C systems with microprocessor-based IEDs must include logic diagrams in addition to schematic and wiring diagrams. However, logic diagrams do not provide a way of representing GOOSE message signal sources or publishing. Even if a logic diagram can specify a signal as the contents of a GOOSE message, this information may not be enough to create a GOOSE configuration.

Part 2 of the CFE LDC guidelines defines documentation of the GOOSE Control Block and the Data Reference in the Data Set for both GOOSE publishing and subscribing. This requirement defines the type and number of GOOSE messages to configure in the IEC 61850 system, the contents of these messages, and the IEDs that should subscribe to the messages, while preserving the semantics about why a message is triggered and how a signal is used by other IEDs.

IV. Switchgear Models

Part 3-1-1 defines switchgear abstract models [5]. The XSWC abstract model shown in Fig. 3 is the base class for switchgear equipment. There are four derived model classes: disconnect switches (XSWI), circuit breakers (XCBR), switchgear with three-pole operation (XSWT), and switchgear with single-pole operation (XSWM). The XSWC model does not define the way to determine switchgear position because the sources required to determine this position (represented by Pos.stVal.on) depend on the type of operation (three-pole or single-pole). The XSWT and XSWM models provide this information.

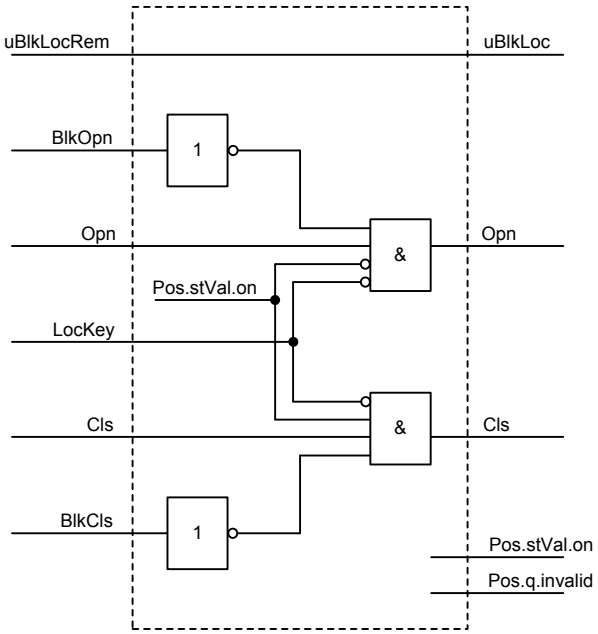


Fig. 3. XSWC abstract model for switchgear equipment.

Fig. 4 shows the UML heritage diagram for the models of circuit breakers (XCBT) and disconnect switches with three-pole operation (SWIT). In this diagram, the rectangles represent classes, and the arrows show the inheritance by pointing from one class to the higher-level class from which it inherits.

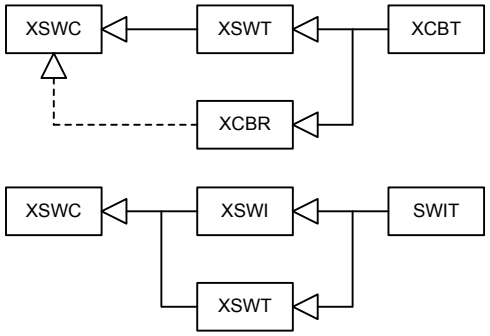


Fig. 4. XSWC UML heritage diagram for XCBT and SWIT.

The disconnect switch XSWI model is an extension of the XSWC class that is obtained by hiding block open (BlkOpn) and block close (BlkCls) input signals and using only the

uBlkOp input signal. A logical zero value of uBlkOp blocks disconnect switch open and close operations.

The circuit breaker XCBR model is also an extension of the XSWC class, obtained by hiding the BlkOpn input signal because CFE does not use open or trip interlocks. This is the base class for all circuit breakers and must be combined with one of the XSWM or XSWC classes. Part 3-1-1 defines the circuit breaker trip logic as a contact arrangement to reflect the electrical nature of the interconnections.

Switchgear models represent their basic functionality in different applications. Engineers extend them to create instantiable models in the design stage. These instantiable models reflect the P&C philosophy and the particular bus arrangement in the substation. In a second stage, CFE will create new abstract models to define switchgear control for the bus arrangements used in CFE substations.

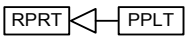
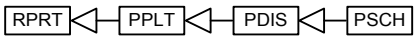
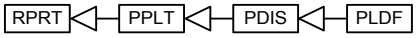
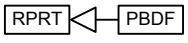
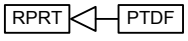
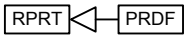
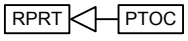
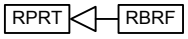
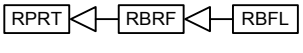
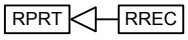
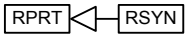
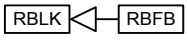
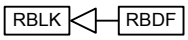
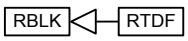
V. Protection Models

A. Protection Function Abstract Models

Part 3-2-1 defines the abstract models of relay protection functions [6]. The model names come from IEC 61850-7-4 [12]. The RPRT protective relay abstract model is the base class for all protection functions. The RPRT model has two input signals: Mod.test (test mode) and Blk (block mode). In the test mode, the model inputs, protection functions, and outputs are enabled, and the model tripping contact outputs are blocked. GOOSE messages are published, but they must include a test bit enable. Part 3-2-1 also defines the trip and lockout function as an auxiliary function (see RBLK in Table I).

Table I lists the protection models and the auxiliary functions, and it provides their description, ANSI numbers, and UML heritage diagrams. A heritage diagram shows the process for defining a new model from a base (father) model. An arrow points from each new model to its father model. To create a new specialized protection model, CFE adds input and output signals to the base RPRT model and/or other specialized models and describe the processing of these signals. Signals inherited from the predecessor models may need to be hidden. The UML heritage diagrams show the model's relationship with the predecessor models of its class. Each model inherits the inputs, outputs, and processing logic of its predecessor model(s). Similarly, all the auxiliary trip and lockout functions are based on the RBLK model. For example, Section V, Subsection B of this paper describes the PTDF model.

TABLE I
PROTECTION MODELS AND AUXILIARY FUNCTIONS

Model	Description (ANSI Number)	UML Heritage Diagram
RPRT	Protective relay model	 (Base class)
PPLT	Line primary protection	
PDIS	Distance protection (21)	
PSCH	Directional comparison protection (85L)	
PLDF	Line differential protection (87L)	
PDOC	Directional overcurrent protection (67)	
PBDF	Bus differential protection (87B)	
PTDF	Transformer differential protection (87T)	
PRDF	Reactor differential protection	
PTOC	Overcurrent protection	
RBRF	Breaker-failure protection (50BF)	
RBFL	Line breaker-failure protection	
RREC	Automatic reclosing (79)	
RSYN	Synchronism check (25)	
RBLK	Auxiliary trip and lockout function (86)	 (Auxiliary function)
RBFB	Multiple breaker-failure trip and lockout (86BU)	
RBFR	Individual breaker-failure trip and lockout (86BF)	
RBDF	Bus differential trip and lockout (86B)	
RTDF	Transformer differential trip and lockout (86T)	

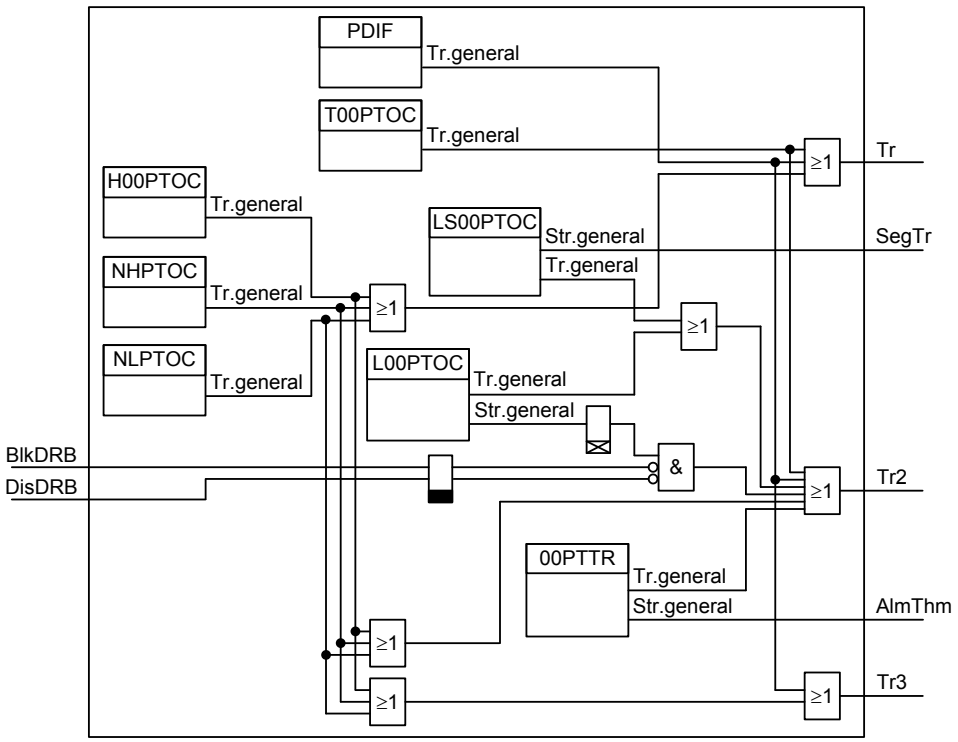


Fig. 5. Transformer differential protection model PTDF.

B. Transformer Differential Protection Model PTDF

The PTDF model is a specialized class of the RPRT base class. In addition, the PTDF model has the following input signals:

- Phase and neutral currents of the primary, secondary, and tertiary (if any) transformer windings.
- Logic signals used to block fast tripping of the low-side circuit breaker in the fast-bus-tripping logic when a feeder instantaneous overcurrent (50) element picks up.
- A logic signal to disable the fast-bus-tripping logic.

The PTDF model has the following additional output signals:

- Tripping commands of high-side, low-side, and tertiary (if any) circuit breakers.
- A tripping command for transformer overload conditions.

The PTDF model includes all of the transformer protection functions defined in CFE Specification VG000062 [16], and it describes the model signal processing (see Fig. 5). These functions include PDIF (87T), H00PTOC (51H), NHPTOC (51NT-H), L00PTOC (51L), NLPTOC (51NT-L), T00PTOC (51T), and LS00PTOC (51LS), all defined in Part 3-2-1 of the CFE LDC guidelines [6].

VI. Control Models

A. Bay Controller Model

A bay controller collects all significant data from the substation switchyard for a particular bay, such as a transmission line, power transformer, or capacitor bank bay, and it forwards these data to the SCADA gateway. The bay controller also performs local/remote switchgear control, interlocking, and circuit breaker supervision. Presently, the CFE LDC guidelines do not cover bay controllers so equipment manufacturers have to develop their own models. This subsection describes the bay controller model developed by a particular manufacturer.

The bay controller model includes the models of the bay switchgear equipment and also the control and interlocking models, which depend on the substation bus arrangement and the P&C schemes. The goal is to design a general and robust bay controller model with enough flexibility to fit into any bus arrangement.

For any bus arrangement, this bay controller model includes the following models:

- Circuit breaker model.
- Disconnect switch model (one per device).
- Control logic model (one per device).
- Interlocking logic model (one per device).

The control and interlocking models are based on the control switch logic (CSWI) and control interlocking logic (CILO) IEC 61850 logic nodes:

- CSWI: This model provides basic logic for control functions, such as local and remote control selection and avoidance of overlapping open and close commands. The CSWI model also provides contact unlatching and contact failure alarming. Each bus arrangement requires a CSWI model.
- CILO: This model allows enabling switchgear operation locally or remotely. It receives all blocking/enabling signals from other IEDs and executes user-defined logic. Each bus arrangement requires a CILO model.

As an example, Fig. 6 depicts a screen capture of the human-machine interface (HMI) of a CFE SAS. The figure shows the bay of a 230 kV line (Line 93720 OCN) connected to a main and transfer bus single-breaker arrangement. This line has a single-pole tripping protection scheme.

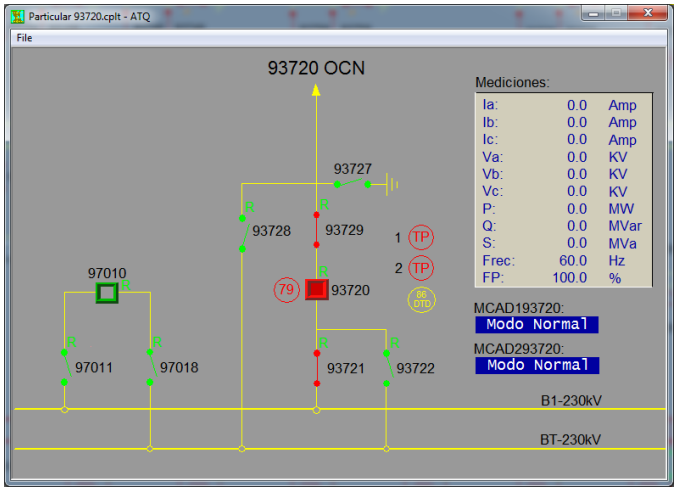


Fig. 6. HMI screen capture of a CFE SAS showing a 230 kV line bay connected to a main and transfer bus single-breaker arrangement.

A bay controller UML heritage diagram that is valid for all CFE bus arrangements was developed along with a library of CSWI and CILO models for these bus arrangements. To adapt the heritage diagram to a particular bus arrangement, designers start from the CSWI and CILO models for this bus arrangement and create the corresponding specialized models.

Fig. 7 depicts the UML heritage diagram of the bay controller model for the Fig. 6 line bay (called the 00PAMCA model). The CSWI and CILO abstract models for this particular bus arrangement serve as base models for this bay controller model. Specialized models were created that describe the specific control and interlocking functions of this bus arrangement. For example, designers created the line circuit breaker control model in Fig. 7 by converting CSWI to 00CSWI. The 00CSWI model has the information to manage trip and close commands of the line circuit breaker in a main and transfer bus single-breaker arrangement. Similarly, designers created the line circuit breaker interlocking model 00CILO by adapting CILO to enable/block circuit breaker open and close operations in this particular bay and bus arrangement.

Fig. 7 shows that, for any bus arrangement, the specialized *xx*CILO functions inherit their properties only from the CILO base function. However, the specialized *xx*CSWI functions inherit their properties from the CSWI base function and the corresponding specialized *xx*CILO functions.

In summary, the 00PAMCA bay controller model for this line includes the following specialized models:

- 00CILO interlocking model for line Circuit Breaker 93720.
- 00CSWI control model for line Circuit Breaker 93720.
- PA01CILO interlocking model for main bus-side Disconnect Switch 93721.
- PA01CSWI control model for main bus-side Disconnect Switch 93721.
- PA02CILO interlocking model for auxiliary bus-side Disconnect Switch 93722.
- PA02CSWI control model for auxiliary bus-side Disconnect Switch 93722.
- PA08CILO interlocking model for bypass Disconnect Switch 93728.
- PA08CSWI control model for bypass Disconnect Switch 93728.
- PA09CILO interlocking model for line-side Disconnect Switch 93729.
- PA09CSWI control model for line-side Disconnect Switch 93729.

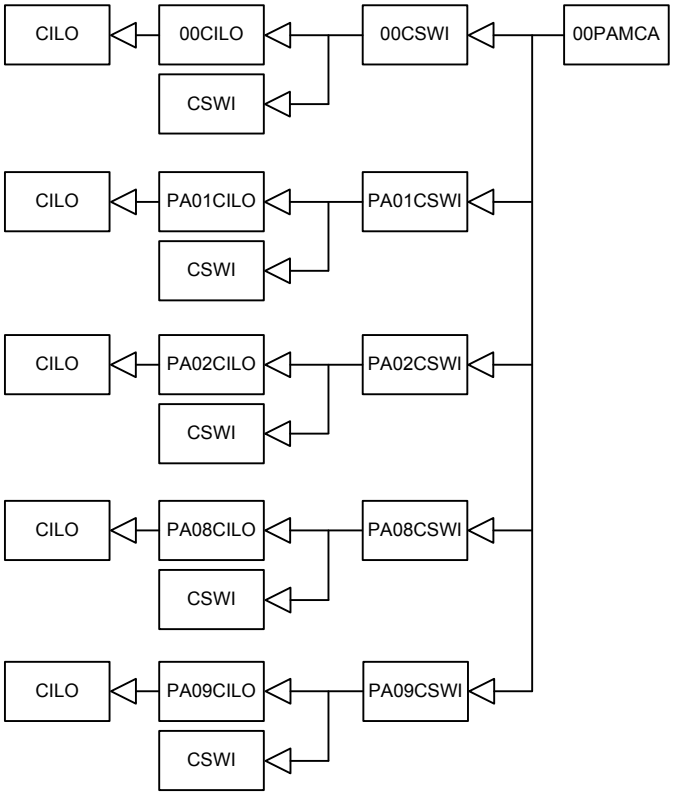


Fig. 7. UML heritage diagram of the 00PAMCA bay controller model for the Fig. 6 line bay.

Bay controller modeling is a complex task: it requires knowledge of the P&C scheme, the IEC 61850 standard, and programmable logic controller (PLC) programming. The CFE LDC guidelines only describe part of the necessary models, so supplier companies need to develop the bay controller models on a per-project basis. As a result, CFE may receive slightly different models from different suppliers for the same bay and bus arrangements. CFE continues to work on developing guidelines for bay controller modeling.

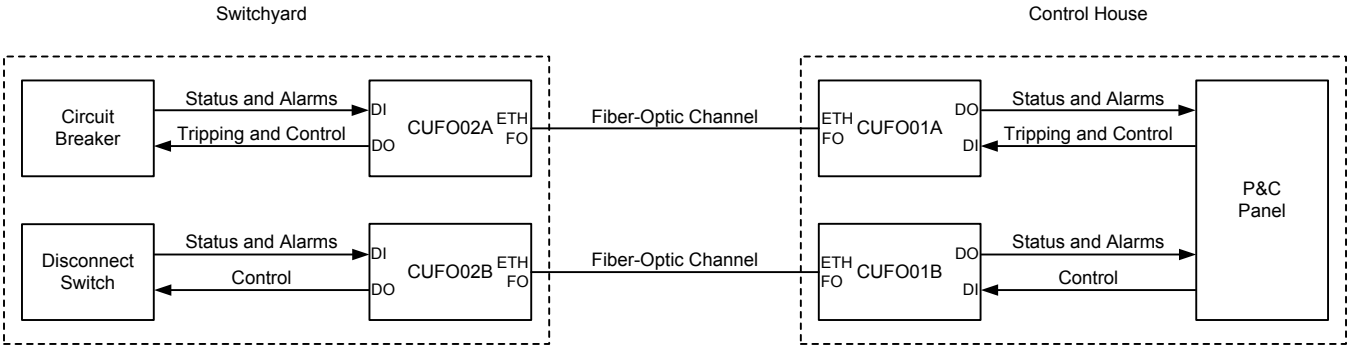


Fig. 8. RIO (CuFO)-based system for a circuit breaker and a disconnect switch.

B. RIO (CuFO) Module Model

A RIO (CuFO)-based system consists of a pair of IEDs converting digital input signals to published GOOSE messages and converting received signals into output signals through a subscription. The GOOSE messages are exchanged through a directly connected optical fiber. This system significantly reduces copper wiring and provides a medium for exchanging all signals at the same time. RIO (CuFO) modules communicate tripping, control, status, and alarm signals between control house P&C panels and switchyard equipment, such as power transformers, circuit breakers, and disconnect switches.

Fig. 8 shows a RIO (CuFO)-based system composed of four IEDs. The RIO modules installed in the control house are named CUFO01*x*, and the RIO modules at the switchyard are named CUFO02*x*. The output contacts from the P&C panel IEDs at the control house are connected to the CUFO01*x* module digital inputs. The CUFO01*x* modules digitize the received tripping and control signals and convert them to a unique GOOSE message. At the other end of the fiber, the CUFO02*x* modules receive the GOOSE messages and convert each one of them to a digital output signal useful for tripping or control purposes. Similarly, the CUFO02*x* modules collect status and alarm signals from switchyard equipment, convert them into GOOSE messages, and send them to the CUFO01*x* modules.

Fig. 9 depicts the abstract model of a remote module (RM), which is applicable to RIO (CuFO) modules and to RPMs (MESs) (as shown in Section VI, Subsection C). The RM model processes digital input signals to provide output GOOSE messages, and it also processes input GOOSE messages to provide digital output signals.

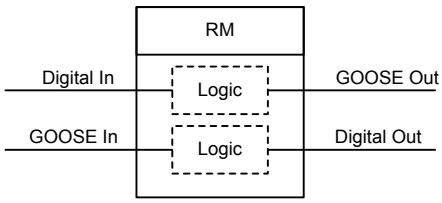


Fig. 9. RM abstract model for RIO (CuFO) modules and RPMs (MESs).

Some complex applications require the RIO (CuFO) modules to perform some signal logic processing. The logic depends on user and application requirements, which makes it impossible to have a unique RM model for RIO (CuFO) modules. RM models are designed and chosen according to the particular application.

A common requirement in CFE substations is to use RIO (CuFO) modules for tripping and controlling circuit breakers. Consider, for example, a line bay in a main and transfer bus single-breaker arrangement, similar to that shown in Fig. 6. The RM model for the RIO (CuFO) modules of a line protection scheme with three-pole tripping includes at least the following signals:

- Trip.
- Trip and lockout (86BF/86DTT/86BU/86B).
- Close blocking (25/27, 86BF/86DTT/86BU/86B).
- Close/reclose command.
- Remote open command.
- Circuit breaker position.
- Transfer circuit breaker position.
- Disconnect switch position.

Fig. 10 shows part of the control house RM model for this application. The model includes the tripping, closing, and reclosing signals from the P&C IEDs, and also the status and alarm signals from the switchyard equipment. The model takes advantage of the logic processing ability available on the RIO (CuFO) module IEDs to simplify the output GOOSE messages. This method reduces the communications burden and simplifies GOOSE messaging administration. As a result, the model issues only the following trip and control signals:

- One circuit breaker tripping message.
- One circuit breaker opening message.
- One circuit breaker closing/reclosing message.
- One circuit breaker blocking message.

Similarly, the control house RIO (CuFO) module receives circuit breaker and disconnect switch status signals from the switchyard RIO (CuFO) modules and processes these signals.

Fig. 10 shows the auxiliary symbols for inputs and outputs to help supplier company engineers read diagrams. CFE will remove these symbols when the familiarization stage finishes, which will reduce the size of diagrams and facilitate printing.

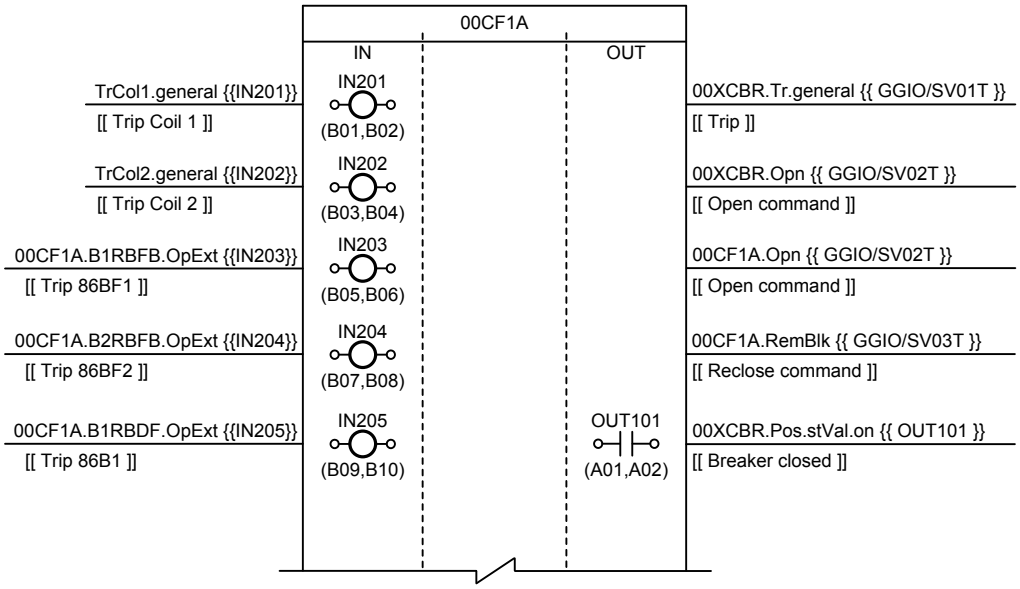


Fig. 10. Part of the RM model for a RIO (CuFO) module of a line bay in a main and transfer bus single-breaker arrangement.

C. RPM (MES) Model

CFE released a specification that covers RIO (CuFO) modules and RPMs (MESs) [17]. The RPMs (MESs) are located at the switchyard and connected to the substation network to perform point-to-multipoint communication. The RPMs (MESs) have analog and digital inputs and logic programming ability. They collect digital signals from the switchyard equipment, process them, convert the resulting signals into GOOSE messages, and publish these messages in the network. At the control house, P&C IEDs subscribe to the signals designated for them. The RPMs (MESs) can provide IEC 61850 server functions through the MMS protocol to send alarm signals and analog measurements, such as oil temperature in transformers.

Developing models for the RPMs (MESs) is a work in progress. The RM model shown in Fig. 9 is valid for the RPMs (MESs).

VII. Application Example

This section provides an example to help understand the application of the CFE LDC guidelines. The example consists of creating the logic diagram to send a close command to the circuit breaker shown in Fig. 11 through a bay controller. This application uses IEC 61850 GOOSE messaging to get the following interlock signals:

- Position of Disconnect Switches 89-1 and 89-2 published by an RPM (MES) located at the substation switchyard.
- Status of Lockout Relay 86B1 of the bus differential protection scheme (87B).
- Status of Lockout Relay 86BF of the breaker failure protection scheme (50BF).

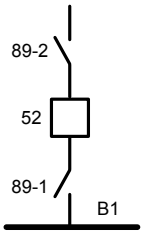


Fig. 11. Single-line diagram showing the circuit breaker used in the example application.

A. Circuit Breaker Close Schematic Diagram

Fig. 12 shows a simple circuit breaker close schematic diagram. The dashed box represents the circuit breaker control circuit. The diagram shows two output contacts of the bay controller. The normally closed contact OUT1/BCU provides voltage to the local control circuit at the circuit breaker cabinet. The normally open contact OUT2/BCU is connected to the circuit breaker close coil. AA/27 is the coil of an undervoltage relay that monitors the dc control voltage. This schematic diagram shows how the circuit breaker close coil is operated via hardwiring from a cabinet located at the control room and how the local control voltage circuit of the circuit breaker is controlled by the bay controller, depending on the interlocks. However, the schematic diagram does not provide information on the logic programmed in the bay controller and the signals used for interlocking.

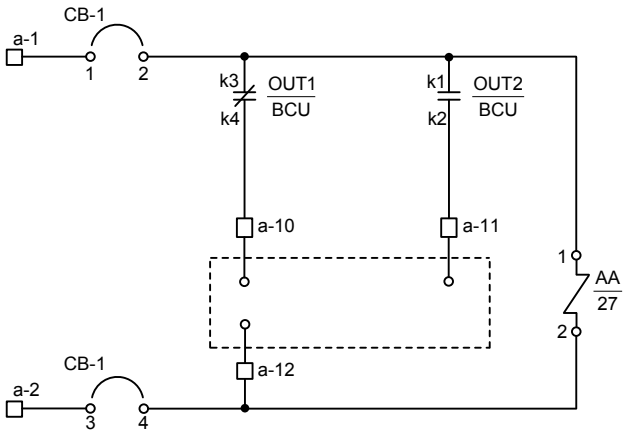


Fig. 12. Simple circuit breaker close schematic diagram.

B. Circuit Breaker Close Logic Diagram

Fig. 13 shows the interlocking logic programmed in the bay controller. The OUT2 bit asserts when no lockout relay has operated (i.e. 86B1 and 86BF inputs have logical zero values) and both disconnect switches in Fig. 11 are closed (i.e. 89-1 and 89-2 inputs have logical one values).

This logic diagram does not answer the following questions:

- How is OUT2 used to cause the output contact OUT2/BCU of the bay controller to close and energize the circuit breaker close coil, as shown in Fig. 12?
- Are there some external interlocks to check before performing a close command?

In addition, the logic diagram does not provide information on the nature of the input signals.

The signals required for interlocking are programmed as bay controller subscriptions to GOOSE messages from the RPM (MES) and the 87B and 50BF relays. The logic diagram shown in Fig. 13 does not provide this information.

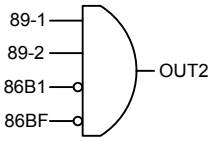


Fig. 13. Simple circuit breaker close logic diagram.

C. Circuit Breaker Close Logic Diagram Based on the CFE LDC Guidelines

Fig. 14 shows the logic diagram that follows the CFE LDC guidelines. The figure shows the instantiation of different models that interchange signals using GOOSE messaging to energize the circuit breaker close coil by energizing a cabinet terminal through Terminals k1 and k2 (OUT2) of the bay controller.

The diagram in Fig. 14 provides a complete picture of the interchanged signals and the binary inputs and outputs of all devices required to perform the function (a circuit breaker close command, in this example).

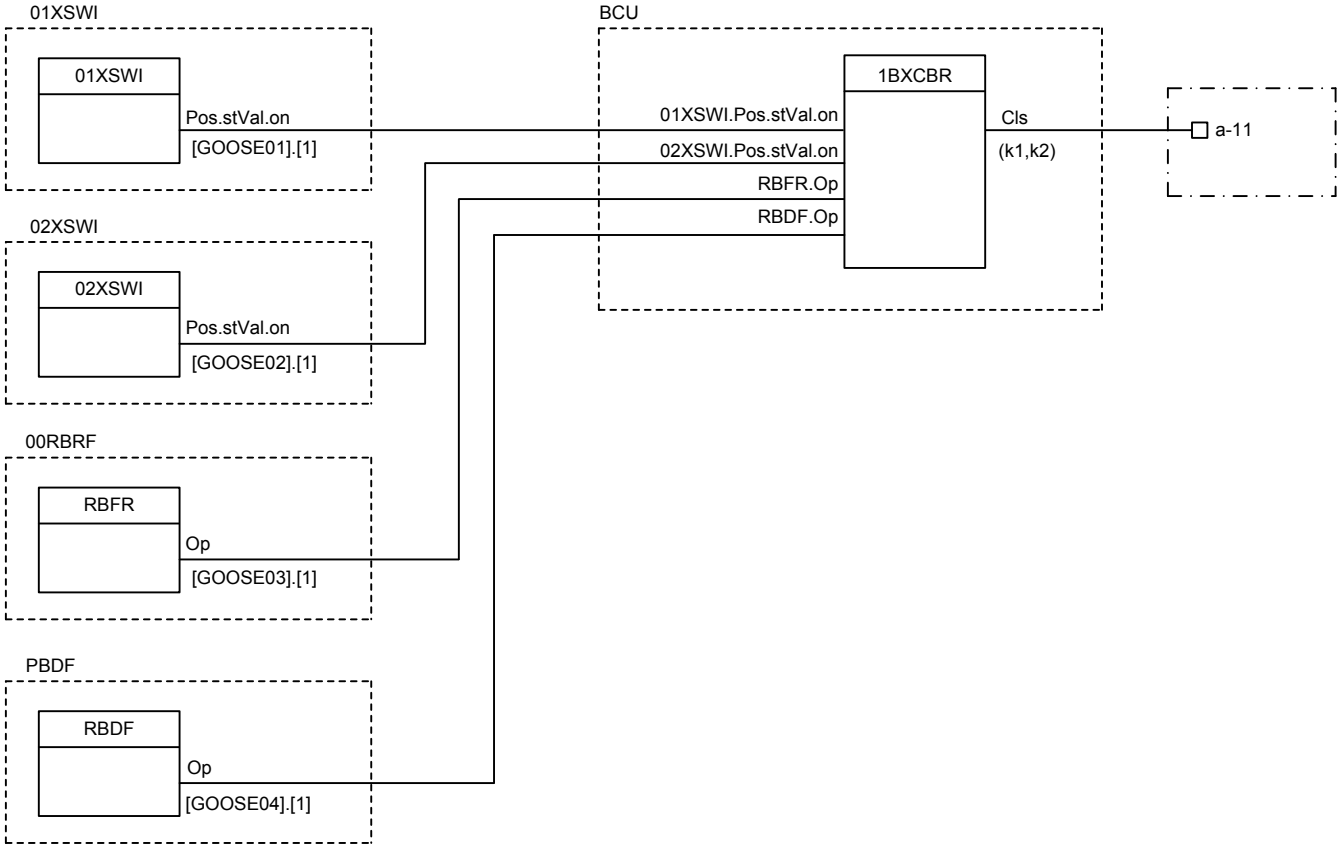


Fig. 14. Circuit breaker close logic diagram based on the CFE LDC guidelines.

The dashed rectangles in Fig. 14 represent the instantiable models of logic programmed in the IEDs. Their names are located over the top left side of the rectangles. The dot-dash rectangle represents the instantiable model of a contact arrangement.

The IEDs involved in performing the circuit breaker close function are the following:

- 01XSWI and 02XSWI: IEDs located at disconnect switch centralized cabinets, providing information on disconnect switch closed position (Pos.stVal.on).
- 00RBRF and PBDF: 50BF and 87B relays, respectively, providing information on the operation of 86BF and 86B lockout relays.
- BCU: bay controller, providing the close signal to the circuit breaker close coil.

The bay controller subscribes to the first elements of the GOOSE messages sent by 01XSWI, 02XSWI, 00RBRF and PBDF, identified by GOOSE01, GOOSE02, GOOSE03 and GOOSE04 (GoID). These signals are used by the 1BXCBR model instantiated by the bay controller as interlocks for the circuit breaker close command.

The subscribed signals are processed by the 1BXCBR model logic to provide a close command (Cls) through a closing digital output on Terminals k1 and k2, which energizes Terminal a-11.

Fig. 15 shows the 1BXCBR model definition instantiated by the bay controller in Fig. 14. It extends an XCBR model by adding interlock signals acting on its BlkCls input. The Cls output of the XCBR model is used as the close command of 1BXCBR. The XCBR model definition is part of the documentation. Fig. 15 uses IEC logic gate standard symbols, where ≥1 is equivalent to an OR gate, and & is equivalent to an AND gate.

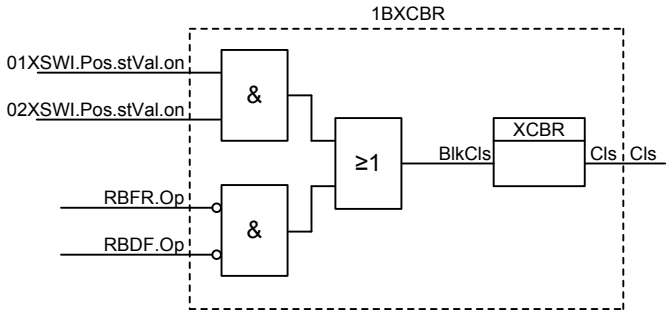


Fig. 15. Circuit breaker close 1BXCBR model definition instantiated in the bay controller.

VIII. Adopting the CFE LDC Guidelines

Individual members of CFE's staff have reacted to the LDC guidelines described in this paper in different ways. Some engineers were initially opposed to their application, mainly because there was poor knowledge about UML, GOOSE messages, and model definitions. Other engineers have become familiar with the LDC guidelines through engineering process supervision and review. The educational opportunities provided by the thorough documentation available in the CFE LDC guidelines include GOOSE message publication and subscription, the way these messages are processed by the IEDs, and how the models are used. This education has been a key factor for CFE engineers in the adoption of this new method of creating and documenting P&C systems, especially when engineers are interested in the way messages are interchanged and processed. Training sessions on the CFE LDC guidelines and related technologies will further foster acceptance and stimulate development of new models for current and future applications.

As part of the adoption process, CFE will provide a set of procedures for protection staff and control staff in order to facilitate flawless information exchange and work coordination, considering that modern IEDs perform P&C functions.

Most CFE suppliers are adopting the CFE LDC guidelines. Initially, these companies applied the guidelines to create and document each design separately, which limited the advantages of the methodology and increased workload. Eventually, supplier company engineers also started to standardize engineering procedures by developing their own P&C system models (like the ones described in this paper) and extending their application from system designers to personnel performing factory testing and on-site commissioning.

The CFE LDC guidelines are very useful in the operation and maintenance activities of P&C systems because they provide enough information to find the root cause of misoperations and then correct the models, add new functionalities, and improve system performance. Today, the LDC guidelines are helping engineers increase confidence in P&C systems that use GOOSE messages. They could be seen as an extra burden when documenting the system, especially when the utility uses standard schematic diagrams. However, the CFE LDC guidelines are important for documenting the utility's philosophy, and they have safely guided the transition from traditional hardwired systems to communications-assisted digital P&C systems that use programmed logic and signal interchange through GOOSE messages. These guidelines may serve as a basis for other utilities to standardize their P&C system design documentation.

IX. Conclusion

In microprocessor-based P&C systems, part of the logic is programmed in the IEDs. Schematic and wiring diagrams do not provide all the information on the system. Therefore, logic diagrams are an important part of design documentation. In addition, logic diagrams for utility P&C systems are typically created by external supplier companies. As a result, the final user has to deal with many different types of logic diagrams. The CFE LDC guidelines described in this paper address these problems by providing rules to create graphics logic diagrams for DSASs.

The CFE LDC guidelines define abstract and instantiable models, define standard symbols and naming, and provide rules for model instantiation. They describe models for switchgear equipment, protection systems, and control and monitoring systems. The CFE LDC guidelines undergo a continuous improvement process as a result of the joint efforts of CFE engineers and their suppliers.

The CFE LDC guidelines provide powerful tools for standardizing P&C system designs. They aid in creating P&C system documentation that provides utility staff with all of the information required for designing, reviewing, commissioning, operating, maintaining, and troubleshooting microprocessor-based P&C systems.

The CFE LDC guidelines allow different technologies to be combined, such as hardwiring, programmable logic, and various communications channels. CFE and supplier company engineers can fully describe their own P&C philosophy and show how they use the different technologies to perform the required P&C functions, from the critical protection functions that use hardwiring and/or GOOSE messages, to less critical control functions that use communications channels.

The CFE LDC guidelines serve as a proven example for other utilities to standardize their P&C system design documentation. They are backed by the experience of more than 45 projects since the first version was released at the end of 2012. These projects have provided valuable information and have been very useful in assessing the way suppliers implement the requested P&C system functionality under the CFE philosophy.

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XI. Biographies

Daniel Espinosa received his B.S.E.E. degree from the Instituto Politécnico Nacional, Mexico City in 1998. He joined Comisión Federal de Electricidad (CFE) in 1998, where he is currently head of the supervisory control discipline at the protection, control, and communications department of the Transmission and Transformation Project Coordination (CPTT). Mr. Espinosa has been a member of the CFE Permanent Protection Engineers Committee since 1999 and is involved in standardization and normalization activities of CFE protection and automation systems. Since 1999, he has been responsible for preparing bid specifications for distribution substation integrated systems and for 13.8 kV to 400 kV power lines in the CPTT. Mr. Espinosa has significantly contributed to CFE's adoption and implementation of the IEC 61850 standard. Mr. Espinosa is a non-member observer of the CIGRE SC B5 committee.

Santos López received his B.S.E.E. degree from Tuxtla Gutiérrez Technological Institute in 1991. He attended the graduate courses taught jointly by the University of Guanajuato, Mexico and the General Electric Company in 1997. Mr. López joined Comisión Federal de Electricidad (CFE) in 1991, where he is currently head of the protection, control, and metering department of the Southeastern Transmission Region. During this time, he has performed relay setting calculations and protection scheme commissioning, including single-pole tripping schemes, in many transmission and subtransmission substations. He commissioned the substations of the Mexico-Guatemala interconnection. Mr. López has been a leader in the introduction of digital technology and fiber-optic channels in CFE substations. He is currently involved in substation integration projects based on the IEC 61850 standard. Mr. López has been a member of the CFE Permanent Protection Engineers Committee since 2008.

Humberto Calderón received his B.S.E.E. from the Laguna Technological Institute in 1991. He attended the graduate courses taught jointly by the University of Guanajuato, Mexico and the General Electric Company in 1997. He joined Comisión Federal de Electricidad (CFE) in 1991 to serve as a regional training supervisor. Mr. Calderón is currently head of the protection department of the CFE Northern Transmission Region. He is also the president of the CFE Permanent Protection Engineers Committee. Mr. Calderón has significantly contributed to developing procedures for functional and dynamic acceptance testing of relays from different manufacturers at the CFE Mexican Laboratory for Electrical Testing (LAPEM). He has presented technical papers at the Summer Power Meeting of the IEEE Mexico Section (RVP-IEEE).

Carlos Meléndez received his B.S.E.E. degree from the Instituto Politécnico Nacional, Mexico City in 1994 and took M.Sc. courses at the National Autonomous University of Mexico in 1997. He joined Comisión Federal de Electricidad (CFE) in 1994, where he is currently head of the power system protection discipline of the CFE Transmission Vice-Direction.

Maycol Flores received his B.S.E.E. degree in automatic control engineering from the Instituto Politécnico Nacional, Mexico City in 2001. He joined Comisión Federal de Electricidad (CFE) in 2001, where he initially worked on automation projects for medium- and high-voltage substations. In 2008, he was promoted to be responsible for electrical substation automation projects. Mr. Flores is currently responsible for protection, control, and communications in CFE substations. Mr. Flores has presented technical papers at the Summer Power Meeting of the IEEE Mexico Section (RVP-IEEE) and the Fall Communications Meeting of the IEEE Mexico Section (ROCC-IEEE). He is a member of the National Association for Normalization and Certification of the Electric Sector (ANCE) of Mexico, where he works on revisions and proposals for IEC 61850 standard-based projects.

Angel Reza received his B.S.E.E. degree from the Laguna Technological Institute in 1999. From 1999 until 2011, he worked for SENSA Digital Control in Torreon, Mexico. From 1999 until 2007, he worked as a SCADA service engineer responsible for commissioning and troubleshooting SCADA systems, mainly for Comisión Federal de Electricidad. From 2007 until 2011, he was a research and development engineer in charge of supporting, testing and performing conceptual design of new SCADA systems and protective relays. In February 2011, Mr. Reza joined Schweitzer Engineering Laboratories, Inc. (SEL), where he is currently a protection engineering leader in San Luis Potosí, Mexico. His activities include protection and control system design. His expertise includes SCADA devices and communications protocols, programmable logic controller programming, and protection system design.

Eliseo Alcázar received his B.S.E.E. degree from the Oaxaca Technological Institute in 1998 and his M.Sc. degree from the Autonomous University of San Luis Potosí in 2015. From 1999 until 2001, he was the head of the protection, control, and metering department in the Southeastern Distribution Division (SDD) of Comisión Federal de Electricidad (CFE) in Tehuantepec, Mexico. From 2001 until 2004, he was head of the protection office of the CFE SDD. During this time, he was engaged in supervision, maintenance, improvement, and commissioning of protection, control, and metering systems. In April 2004, Mr. Alcázar joined Schweitzer Engineering Laboratories, Inc. (SEL), where he is currently a protection engineering supervisor in San Luis Potosí, Mexico. His activities include protection, control, and metering system design and commissioning, as well as technical support and training on SEL products for engineers from utilities and industrial plants. His expertise includes fault analysis, short-circuit studies, protection coordination, and protection system design.

Héctor J. Altuve received his B.S.E.E. degree in 1969 from the Central University of Las Villas in Santa Clara, Cuba, and his Ph.D. degree in 1981 from Kiev Polytechnic Institute in Kiev, Ukraine. From 1969 until 1993, Dr. Altuve served on the faculty of the Electrical Engineering School at the Central University of Las Villas. From 1993 to 2000, he served as a professor of the Graduate Doctoral Program in the Mechanical and Electrical Engineering School at the Autonomous University of Nuevo León in Monterrey, Mexico. From 1999 through 2000, he was the Schweitzer Visiting Professor in the Department of Electrical and Computer Engineering at Washington State University. Dr. Altuve joined Schweitzer Engineering Laboratories, Inc. (SEL) in January 2001, where he is currently a distinguished engineer and dean of SEL University. He has authored and coauthored more than 100 technical papers and several books and holds four patents. His main research interests are in power system protection, control, and monitoring. Dr. Altuve is an IEEE fellow.