Innovative Data Acquisition and Redundancy Methods Enable Previously Impractical High-Speed, Wide-Area Control

D. Dolezilek, F. Calero, A. Kalra, and B. Waldron
Schweitzer Engineering Laboratories, Inc.

J. M. Herrera, M. S. Mingarro, and S. L. Barba
Red Eléctrica de España

Presented at the
13th International Conference on Developments in Power System Protection
Edinburgh, United Kingdom
March 7–10, 2016

Innovative data acquisition and redundancy methods enable previously impractical high-speed, wide-area control

D. Dolezilek*, F. Calero*, A. Kalra*, B. Waldron*, J. M. Herrera†, M. S. Mingarro†, S. L. Barba†

**Schweitzer Engineering Laboratories, Inc., 2350 NE Hopkins Court, Pullman, WA 99163 USA, dave_dolezilek@selinc.com*

†Red Eléctrica de España, Paseo del Conde de los Gaitanes, 177 28109, Alcobendas, Madrid, Spain

Keywords: IEC 61850, high-speed algorithms, analog GOOSE, IEC 61131, HVDC.

Abstract

This paper describes the new high-speed data acquisition and precise synchronization strategies (in addition to the special considerations and engineering best practices) used to design a communications network for a high-voltage dc (HVDC) link between France and Spain. Because of the mission-critical nature of the system, various contingency scenarios to optimize the availability and dependability of the system are discussed. Additionally, the paper discusses several new hardware and software redundancy methods within the system that improve the overall control system dependability and security.

1 Introduction

The new high-voltage dc (HVDC) voltage source converter (VSC) interconnection between Spain and France is embedded within an ac network. Operation of the interconnection requires frequent calculation of the power flow across four parallel ac lines and the status of the bus configuration at the associated substations. High-speed analog data acquisition and data redundancy are necessary to satisfy the design requirements of this system. These were previously not available.

Several control modes of operation are implemented in the HVDC VSC link between Spain and France. The power flow mode is based on the knowledge of the total power exchanged and changes in power flow across the existing ac lines. The simulation mode models the dc link as a simulated ac line by monitoring the angular difference between the ac buses.

The power flow mode requires that the sum of the active power flows through all of the ac interconnection lines be sent to the HVDC controller. Power flow information must be collected from four substations and sent to the HVDC controller. The distance between the HVDC controller and the four remote substations ranges from 80 to 600 km. Different technologies (including typical, event-driven IEC 61850 Generic Object-Oriented Substation Event [GOOSE] and IEEE and IEC synchrophasor protocols) were investigated and compared. However, none of these protocols could satisfy the stringent design requirement for detection and notification of a change in power flow within 35 ms.

This paper explains a novel data acquisition method that supports accurate, synchronized, wide-area power flow summation at fixed intervals. This method uses the power calculated within the protective relays at each substation. The calculated power in each relay is published as analog data within IEC 61850 GOOSE messages. The system requires constant supervision of the communications status and the synchronization of the distributed time. A failure alarm for either of these supervised processes causes the data to be sent from the relays to the system's redundant central processing units (CPUs). This is done with standardized IEC 61850 communications protocols and IEC 61131 logic algorithms.

A set of redundant centralized controllers executing algorithms with an IEC 61131 logic engine validates the incoming repetitive IEC 61850 GOOSE messages. Power calculations are triggered and published at the same instant in the protective devices at all four substations. The power in each relay is calculated at a fixed rate, typically 2.5 ms. To preserve bandwidth and reduce computation at the HVDC controller, the calculated power from each of the protective relays is transmitted to the HVDC instead of the individual voltage and current signals. The calculated active power values are uniquely labeled and published as the contents of IEC 61850 GOOSE messages as soon as they are available. The centralized controller validates the communications status, relay time synchronization status, and message delivery latency due to network congestion. This innovative data acquisition method using IEC 61131 logic synchronizes the IEC 61850 GOOSE contents to compensate for the nondeterministic behavior of Ethernet-based message exchange.

Due to the mission-critical nature of the system, various contingency scenarios to improve the availability and dependability of the system were identified. Several new hardware and software redundancy methods within the system improved the dependability and security of the control system.

This paper describes a new high-speed data acquisition system with precise time synchronization. The paper also discusses strategies used in the design of the HVDC controller, as well as the special considerations in the design of the communications network.

2 Background

The HVDC link between France and Spain will result in reliable delivery of electric power and ensure that the increasing distributed generation in the region can be integrated into the power system without compromising the stability of the power system. Additionally, this link will be instrumental in doubling the present energy exchange capacity of 1,400 MW between the two countries.

The two converter stations for the HVDC link are situated in Baixas, France and Santa Llogaia, Spain. The Modos de Funcionamiento del Enlace (MFE) system is installed in the Santa Llogaia converter station. The MFE system feeds precise analog signals to adjust power flows and to allow correct operation of the converter based on the present real-time condition of the Spanish ac power system. The real-time power measurements are collected using various modern IEDs distributed throughout the Spanish-French border. Fig. 1 shows the geographical location of the various substations that have these IEDs installed. The IEDs send both analog and digital information using high-speed IEC 61850 GOOSE messages to two redundant CPUs located in the Santa Llogaia converter station. The station architecture consists of two identical systems operating independently.

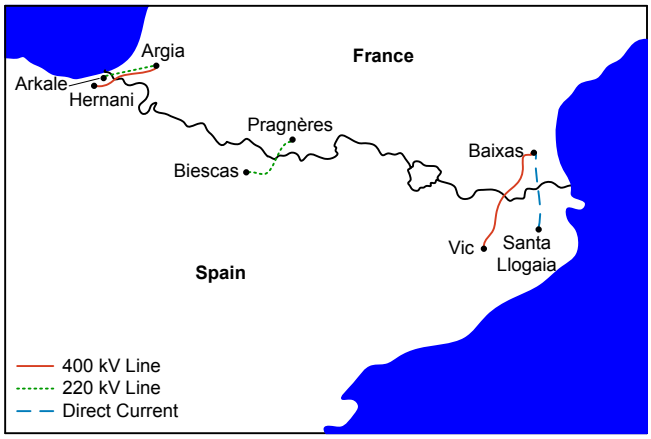

Fig. 1. Geographical location of the interconnections between Spain and France.

The following signals are sent over the wide-area network (WAN) to the CPUs:

- Locally calculated power flow (active power only) in different Spain-to-France interconnections.
- Statuses of the lines (in or out of service) in the nearest area of influence.
- Frequency.
- Supervision status of system health parameters.

3 System requirements

3.1 Hardware requirements

Because of the mission-critical nature of the application, the devices used in the field have very strict requirements. All of the field devices and CPUs must have a low failure rate, as indicated by their mean time between failures (MTBF) and the ability to withstand a temperature range from –40 to +85°C. Because data validation, computation, and decision-making are performed in redundant CPUs, these devices had the following stringent requirements:

- High-speed communications. The system must support standardized communications to provide high-speed, low-latency, deterministic, and reliable communications links between the CPUs and the I/O modules. EtherCAT® was chosen because it is an Ethernet-based fieldbus protocol designed exclusively for deterministic high-speed data acquisition and to serve control applications on a dedicated Ethernet network. EtherCAT messages combine data from multiple EtherCAT nodes into a single message as large as 4 GB. EtherCAT directly transfers data between modules without encoding or decoding messages, thereby providing a high-speed data exchange. This process is initiated by an EtherCAT master executing an application that starts the EtherCAT messages on a fixed interval and evaluates them on return. EtherCAT messages are designed to optimize the frame size for speed and determinism [1] [2] [3].
- Event recording and retrieval capabilities. The CPUs must be able to record sequential events records for all of the associated I/O distributed throughout the field.
- An IEC 61131 logic engine. The CPUs must support IEC 61131-3 programming languages and provide the flexibility to write custom function blocks.
- High-speed processing. The CPUs must have high-speed processing capabilities to synchronously process the time-aligned data acquired via various I/O modules.
- Hardware modularity. The CPUs must have expandability to allow for use at multiple sites with different numbers and variations of combined analog and I/O modules.
- Multiple communications ports. The CPUs must be able to support multiple communications ports to communicate data to multiple centralized servers both in-band on the Ethernet network and out-of-band.
- A built-in human-machine interface (HMI). The CPUs must have a built–in, web-based HMI for viewing the health and status of field devices [3].

3.2 Software requirements

The system required very robust software designed to avoid a single point of failure in either the hardware or software. Simultaneous executions of multiple applications with different performance requirements were carried out. The ability to segregate the software into multiple threads with unique processing rates was a requirement. In addition to reducing the probability of error, this modular processing structure also provides future expandability. Various specific function blocks needed to be built.

3.3 Performance requirements

One of the biggest challenges of the MFE system was to create an analog output command signal for the HVDC controller within 50 ms of any change in the power flow at any one of the four monitored substations. This 50 ms includes the unavoidable latency of the Ethernet messages traveling hundreds of kilometers through two local-area networks (LANs) and the WAN multiplexer system as well as a safety check that requires any change to be confirmed by two consecutive calculations. After predicting the worst-case latency and sufficient margin for WAN communications to be 15 ms, the engineering team accepted 35 ms as the maximum processing time of the application. Therefore, a maximum delay of 35 ms from the time that the ac power changed at any one of the substations until an analog output was sent from the CPU to drive the HVDC controller could be guaranteed.

4 Feasibility study

Various technologies, such as synchrophasors and IEC 61850 GOOSE, were considered for the project. Although other update rates exist, synchrophasor data via standard protocols are typically updated 25 or 50 times per second, based on a nominal frequency of 50 Hz. Considering other delays, such as hardware delay and latency through the network, it was not feasible to meet the system requirements using synchrophasors. New technology, however, satisfied the speed requirements using IEC 61850 GOOSE messages in a carefully designed system. However, because of the nondeterministic nature of Ethernet and GOOSE messages, as well as the large payload, a feasibility study was required to verify the performance of the technology. Fig. 2 shows a test setup where the synchronized logic IED (SLI1) invokes a test in the CPU and the field device (FD) records the test start and resulting control output from the CPU.

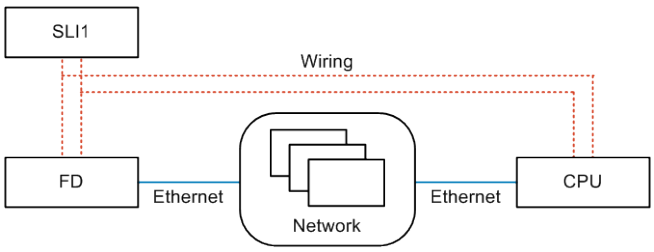

Fig. 2. Setup of test bench.

Fig. 3 shows a waveform capture of the typical test results as captured by the field device.

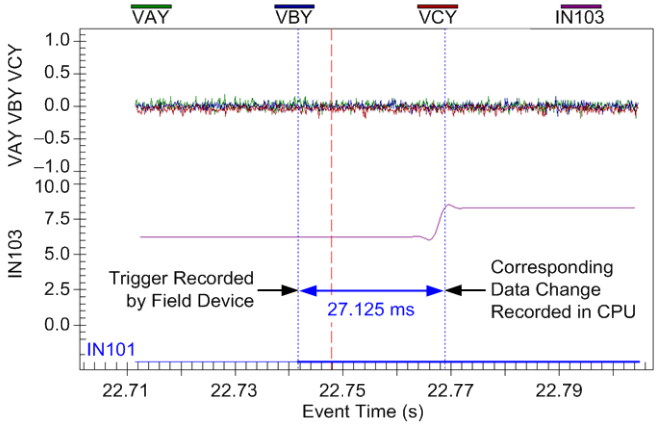

Fig. 3. Waveform showing trigger and response time.

The left vertical blue dashed line indicates the trigger recorded by IN101 on the field device. The right vertical blue dashed line represents the resulting change of the control output from the CPU recorded by IN103 on the field device. This example shows the time duration between a sudden change of power flow in a field device and the resulting analog output of the CPU to the HVDC controller to be 27 ms. All of the test results were well under the 35 ms design maximum and verified the performance of the design.

5 System description

The control system requires that the sum of the active power flows through all of the ac interconnection lines be sent to the HVDC controller. The system must satisfy the stringent design requirement for detection and notification of a change in power flow within 35 ms. Fig. 4 shows a simplified diagram of the substations involved in the project. These substations send analog and binary GOOSE messages to Santa Llogaia, the HVDC controller substation.

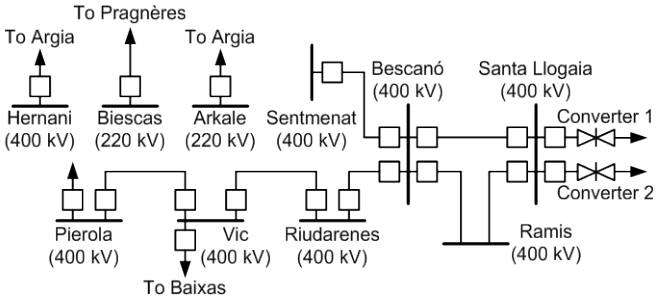

Fig. 4. Simplified substation layout.

5.1 Communications architecture

Fig. 5 shows a simplified diagram of the communications architecture of the system.

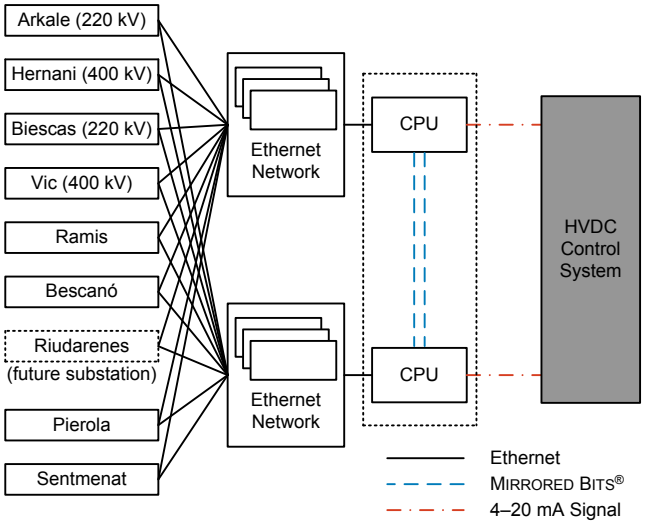

Fig. 5. Communications architecture.

The centralized station receives Ethernet traffic from each of the substations via a WAN. The WAN is built using multiplexers at each substation and is connected to an Ethernet LAN in each substation. Each LAN includes a field IED communicating Ethernet messages (including GOOSE) through the LAN and into the WAN via the multiplexer. The WAN distances for the stations vary from 80 to 600 km. Calculations based on the time to transfer data through fiber plus an appropriate safety margin reveal that direct GOOSE transfer takes approximately 4 ms. The WAN team predicted that the additional latency caused by entering the source multiplexer hardware, passing through interim multiplexers, and exiting the multiplexer at the HVDC station would be approximately 6 ms. Therefore, the WAN team accepted a 10 ms time budget for power flow data transfer, leaving a 40 ms margin for the remaining CPU decision logic at the centralized station.

5.2 Centralized station

The centralized station consists of redundant CPUs that subscribe to IEC 61850 GOOSE messages from field devices. The CPUs run innovative IEC 61131 logic algorithms to ensure data validity, verify synchronization, and output analog information in the form of 4–20 mA signals. These signals are then fed to the HVDC controller.

6 CPU logic algorithm

IEC 61131 Structured Text (ST) and Continuous Function Chart (CFC) languages were used to write innovative data processing and system redundancy logic. Fig. 6 shows various logic processing steps inside the CPU. Software redundancy provides resilience to the system against multiple hardware and software failure scenarios.

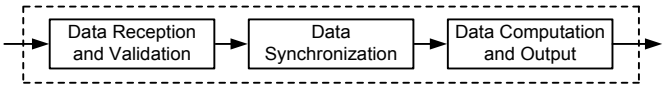

Fig. 6. Stages of data acquisition logic.

7 Conclusion

By using modern data acquisition field devices, following proven network engineering best practices, and using rugged and modular centralized controllers, it is possible to achieve high-speed, wide-area control that uses real-time analog measurements and interconnects multiple substations spanning hundreds of kilometers.

References

[1] D. Dolezilek, N. Fischer, and R. Schloss, "Improvements in Synchronous Wide-Area Data Acquisition Design and Deployment for Telecontrol and Teleprotection," proceedings of the 14th Annual Western Power Delivery Automation Conference, Spokane, WA, March 2012.

[2] M. Vaughan, R. Schloss, S. Manson, S. Raghupathula, and T. Maier, "Idaho Power RAS: A Dynamic Remedial Action Case Study," proceedings of the 64th Annual Georgia Tech Protective Relaying Conference, Atlanta, GA, May 2010.

[3] D. Kirby, N. Fischer, A. Kalra, and D. Haes, "Case Study: Centralized Ground Fault Detection System for LADWP Ungrounded Distribution System," proceedings of the 41st Annual Western Protective Relay Conference, Spokane, WA, October 2014.