Considerations for Using High-Impedance or Low-Impedance Relays for Bus Differential Protection

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Considerations for Using High-Impedance or Low-Impedance Relays for Bus Differential Protection

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***Abstract*—Two drastically different types of differential relays, one with a single set of very high-impedance inputs and another with multiple sets of low-impedance inputs, are available for bus differential protection. Protection engineers often question which type to choose for their bus protection applications. This paper discusses for each type of relay the concepts used, the pros and cons, and the importance that current transformer selection plays in applications.**

***Index Terms*—Bus differential, CT saturation, high impedance, low impedance, protection, relay**

I. Introduction

Kirchoff's current law states that the vectorial sum of all currents at a node or bus is equal to zero. This principle is applied to bus protection in power system networks. Current transformers (CTs) are installed to monitor all currents entering and leaving a bus through the normal circuits connected to the bus.

A bus differential protection scheme, regardless of the type of relay used, simply compares the current entering the bus with the current leaving the bus. Any difference in the current entering and leaving the bus, above some predetermined threshold, is an indication of a bus fault that must be isolated quickly. Bus differential relays perform this function by detecting the differential current and tripping all breakers directly associated with the bus to isolate the fault.

Unlike transformer differential relay schemes, the bus differential relay does not need to provide magnitude or phase angle compensation because of transformer winding ratios and connections. Likewise, bus differential schemes do not have to contend with magnetizing inrush currents that require transformer bus differential relay schemes to employ harmonic blocking, restraint, or other waveform recognition techniques. On the surface, bus differential schemes should be very simple to apply.

A simple bus differential scheme can be implemented by paralleling CTs from all circuit breakers on the bus, in which case the sum of the current on each phase for all normal through-load and external through-fault conditions is zero, as shown in Fig. 1. The first complication arises because all paralleled CTs must have the same ratio to ensure that all secondary currents are compared on the same base as the primary currents.

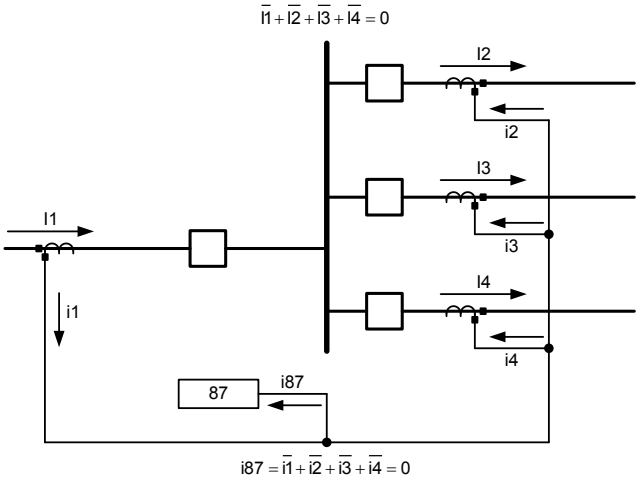

Fig. 1. Simple current differential scheme with paralleled CTs

The relay in this simple bus differential scheme could use a simple, instantaneous overcurrent element set with a very sensitive pickup, because ideally no current flows to the relay under normal through-load and through-fault conditions. This, of course, assumes that all paralleled CTs not only have the same ratio but that they also perform identically under all conditions, including external faults with heavy through current and asymmetrically offset waveforms caused by high source X/R ratios.

The reality is that all conventional iron-core current transformers, regardless of ratio and accuracy class, are susceptible to saturation, during which time their secondary output current fails to accurately represent the primary current flowing in the bus [1][2][3][4]. This causes a difference current that the differential relay may interpret as an internal fault. Bus differential relays, regardless of the design, must differentiate between true internal bus faults and false differential currents caused by CT saturation for a fault outside the bus differential zone of protection.

One technique applied to simple overcurrent differential schemes is to use sufficient time delay to ride through the period of CT saturation. Delayed tripping is generally unwanted, so other, more sophisticated techniques are available to provide secure operation for external faults with CT saturation and still provide fast operation for internal bus faults. This paper discusses the two most common techniques: low-impedance and high-impedance bus differential.

II. Low-Impedance Bus Differential

Low-impedance bus differential relays are so named because the differential relay current inputs have a low impedance to the flow of CT secondary current. This means that the low-impedance bus differential relays can share the CTs with other relays, meters, transducers, etc. The low-impedance bus differential scheme typically has one set of current inputs for each phase from every set of CTs in the scheme. Fig. 2 shows a single-phase representation of a low-impedance bus differential relay installation. A single low-impedance bus differential relay can provide protection for a single phase, two phases, or all three phases, depending on the number of relay current inputs.

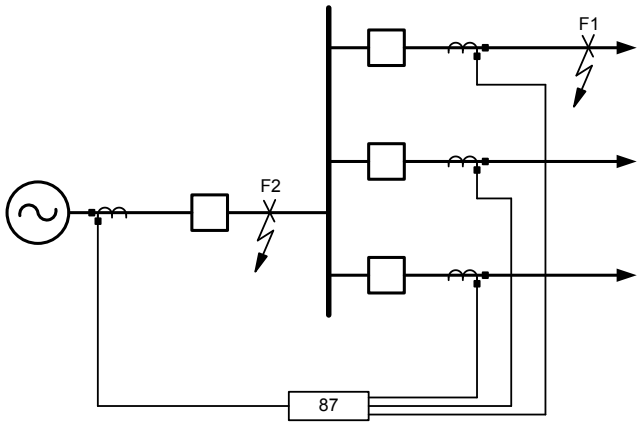

Fig. 2. Low-impedance bus differential scheme showing an external fault, F1, and an internal fault, F2

Having individual current inputs also allows the circuits comprising the differential zone to have different CT ratios, an important attribute where the CTs are shared with other protection and monitoring functions. The relay compensates for the difference in secondary current magnitudes from different CT ratios by using tap settings on each input to normalize the currents to a common base. Individual CT current measurements from each breaker position also make it possible for the differential relay to perform breaker failure protection and end-zone fault detection.

In some applications, the shared CT polarities may not all be oriented the same with respect to the bus. Having the same polarity is critical to proper current summation unless the relay can internally switch the sign of each respective current measurement to account for the CT polarity. Modern microprocessor-based low-impedance bus differential relays generally provide a means to change the CT polarity sensing in the relay settings without rewiring the CT input on the relay or changing the CT polarity connection. One disadvantage of the low-impedance bus differential relay is that it needs CT current inputs for all breaker positions on the bus. This can limit future bus expansion or prevent low-impedance bus differential relay application on buses with more breakers than the relay has current inputs. Some exceptions are possible where two or more sets of CTs can be paralleled. However, paralleling CTs carries the following specific restrictions:

- Paralleled CTs must have the same ratio.
- Only CTs on load circuits can be paralleled without risk. Paralleling CTs on circuits with external sources of fault current increases the risk of unwanted relay operation for through-fault conditions.
- The combined maximum load current from the paralleled CTs must not exceed the continuous rating of the relay current inputs.

A. *Low-Impedance Bus Differential Relay Operation*

The low-impedance bus differential relay vectorially sums the normalized currents from all CT inputs to detect the difference current resulting from an internal fault (i.e., internal to the protection zone defined by the location of all CTs connected to the relay). To account for small differences in CT performance, the relay also arithmetically sums the current magnitudes to create a restraint current, I_{RT}. The difference current from the vectorial current summation, referred to as the operate current, I_{OP}, is compared with I_{RT}. The relay operates when I_{OP} exceeds a minimum threshold and a percentage of I_{RT}, defined by a slope setting. Fig. 3 shows this "percentage current differential characteristic" graphically.

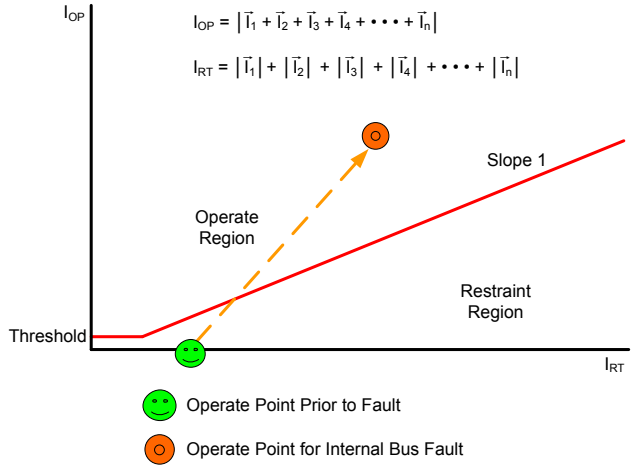

Fig. 3. Percentage current differential characteristic of a low-impedance bus differential relay with and without an internal bus fault

1) Normal Load Conditions

Fig. 3 shows that under normal load conditions prior to a fault the operate current is virtually zero and the restraint current is a finite value proportional to the load current through the bus.

2) Internal Fault Conditions

Fig. 3 also shows that an internal bus fault produces an increase in both operate and restraint current proportional to the fault magnitude, moving the I_{OP}/I_{RT} operating point from the restraint region into the operate region. This change causes the differential element to operate and the relay to trip. Fig. 4 shows the oscillographic representation of two currents in a low-impedance bus differential scheme. The internal fault produces current flow into the bus from all sources, so the currents seen by the bus differential relay are in phase with each other.

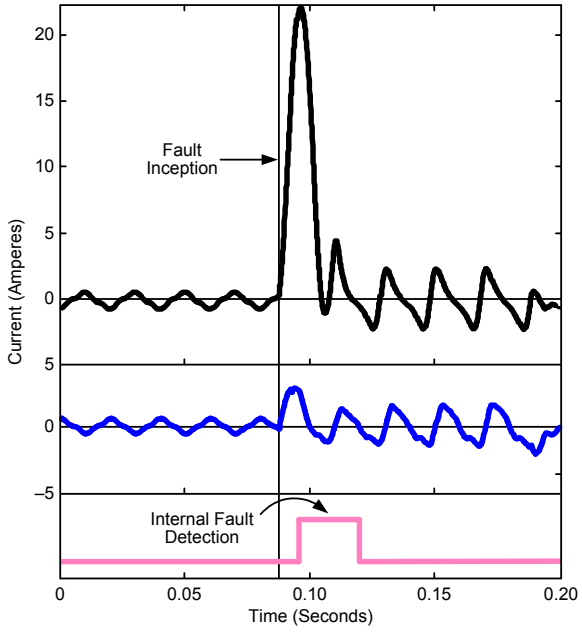

Fig. 4. Subcycle relay operation for an internal bus fault

3) External Fault Conditions

Conversely, the relay must be secure against tripping for external faults, switching transients, bus-mounted surge arrester operation, and normal through-current load flow changes caused by motor starting, transformer energization, etc. Modern low-impedance bus differential relays employ a variety of techniques to distinguish between internal and external faults and other nonfault transients to secure the relay against tripping. External faults with CT saturation are particularly troublesome because of the large operate current, shown as I_{diff} in Fig. 5, that can occur after the faulted circuit CT saturates.

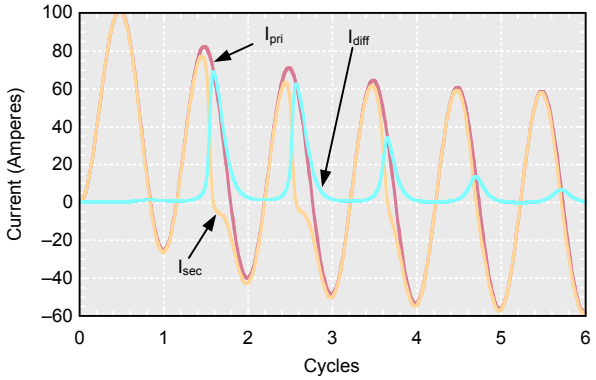

Fig. 5. Saturated CT secondary current and resulting difference current, I_{diff}

Fig. 6 shows currents from two CTs for a through-fault condition where the CT producing current I_1 goes into saturation shortly after fault inception, while the CT producing current I_2 does not.

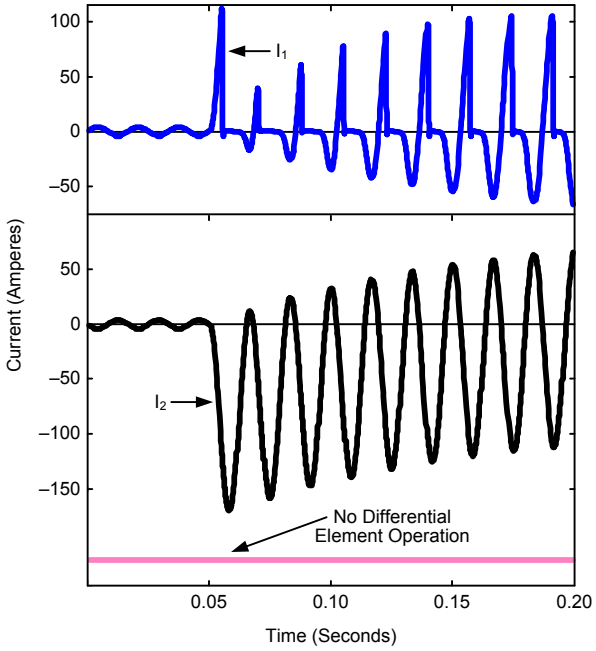

Fig. 6. The relay securely avoids tripping even with severe CT saturation

To distinguish between internal and external faults, one low-impedance bus differential technique uses the first few milliseconds of rising current in each half cycle before CT saturation occurs. If the relay detects an increase in restraint current without a proportional change in operate current, then the fault is external, and the relay switches to a more secure slope setting to avoid tripping for this condition, as shown in Fig. 7. Note that the security mode simply changes the slope setting to avoid tripping for an external fault. The differential relay element is still enabled and ready to trip if the fault evolves into an internal fault.

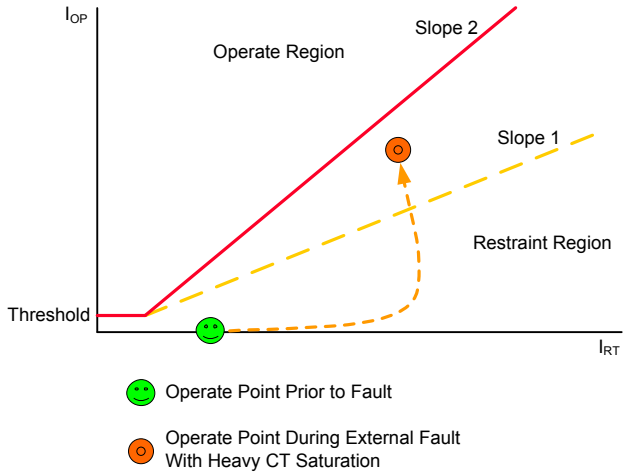

Fig. 7. High-security bus differential relay characteristic

If the operate current and restraint current increase at the same time, the fault is internal, and the relay trips as soon as the operate current exceeds the restraint characteristic and minimum operate current threshold, as in Fig. 3.

4) Other Conditions

Bus differential zones can include other equipment, such as surge arresters, auxiliary power transformers, and voltage transformers (VTs) that either momentarily or continuously provide a "leakage current" path in the protection zone. Surge arresters conduct current to ground when they operate. Modern metal oxide varistor (MOV) surge arresters have little or no power follow current, so the conduction time is very brief. Low-impedance differential relays need to apply a small delay, typically one-half cycle, to prevent tripping on MOV surge arrester operation. Older gapped surge arresters typically have a power follow current that can last up to one-half cycle, so we suggest adding an additional one-half cycle delay where these older style arresters are present.

Auxiliary power transformers and VTs continuously conduct current and also conduct magnetizing inrush current when energized. VTs are typically high-impedance and have very small burdens, so their leakage current can generally be disregarded. Secondary faults on VTs also produce very little primary current, so they generally can also be ignored.

For auxiliary power transformers, on the other hand, check to make sure that the magnetizing inrush and primary current that a secondary fault produces do not cause the bus differential relay to operate. Magnetizing inrush can reach levels of 6 to 10 times full load current. Secondary faults can produce primary currents greater than 20 times full load current, depending on the transformer impedance. On larger auxiliary transformers, motor starting can cause sufficient primary current to be a potential source of unwanted relay operation. It may be possible to raise the relay minimum current tripping threshold to avoid nuisance trips. If not, then add a time delay to ride through these transient conditions. If delayed tripping is not desired, then apply CTs to the transformer, with the secondary circuits paralleled with the existing bus differential CTs or connected to spare restraint current inputs to exclude the transformer from the bus differential protection zone. Then apply primary protection, such as fuses, to protect the transformer.

Stray bus capacitance is another source of leakage current that can produce differential relay operate current. But the stray capacitance associated with typical substation buses is usually negligible, so this source of leakage current generally can be ignored.

B. Supplemental Protection Functions

The low-impedance bus differential relay lends itself to additional monitoring and logic to perform supplemental protection functions, such as end-zone fault detection, breaker failure detection, and open or shorted CT detection.

1) End-Zone Fault Detection

End-zone faults occur between the circuit breaker and the CT associated with the breaker, shown as F3 in Fig. 8.

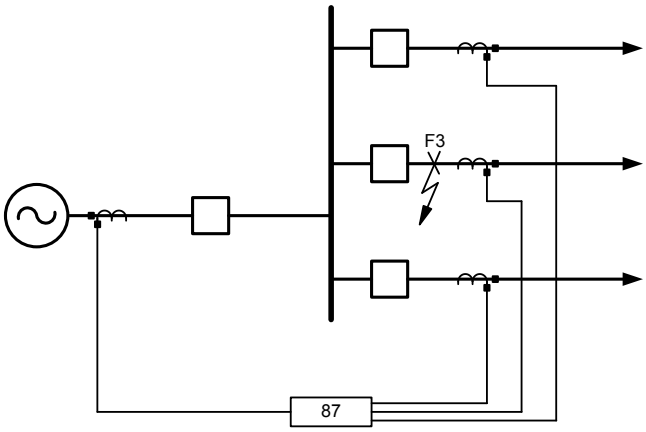

Fig. 8. Low-impedance bus differential scheme showing an end-zone fault, F3, between the breaker and CT

The bus differential scheme detects the end-zone fault as an internal fault, but, if a source on the remote end of the faulted circuit exists, the fault current may not be interrupted by opening all of the breakers associated with the bus differential scheme. The relay's end-zone protection logic determines that the breaker is open, but the current the CT measures has not gone to zero. The logic sends a transfer trip to the breaker at the remote source to interrupt the final source of current to the fault.

2) Breaker Failure Detection

Breakers called upon to trip can fail to interrupt current for a variety of reasons. The operating mechanism can fail to mechanically open the breaker for electrical or mechanical reasons. Or, if the breaker operates to mechanically open the current-interrupting contacts, there may be insufficient

dielectric strength across the open contacts to interrupt the arc.

In either case, implement breaker failure protection by starting a timer when the breaker trip is applied and detecting if the breaker interrupts current by the end of the fixed time delay. Establish the time delay according to the rated breaker interrupting time plus some small margin. The margin time depends, in part, on how fast the relay recognizes that the current is interrupted.

CT secondary current includes a dc component known as subsidence current that can delay zero-current detection by longer than one cycle, sometimes by as long as several cycles. Unless accounted for, breaker failure time-delay settings must include sufficient margin to accommodate this subsidence current.

Subsidence current detection logic ensures zero-current detection in less than three-fourths cycle, thereby minimizing the required time-delay margin and speeding up breaker failure fault detection to improve the total clearing time.

When a breaker fails to interrupt current, backup tripping must open all other sources of current to the failed breaker. The modern microprocessor-based bus differential relay has built-in breaker failure detection logic with timers and current detection thresholds. It can trip all breakers on the bus, either individually if trip outputs are wired to each breaker or as a group through a bus lockout auxiliary relay.

3) Open and Shorted CT Detection

An open or shorted CT in a low-impedance differential relay scheme produces a difference (operate) current proportional to the load current on the circuit with the faulty CT circuit. For example, a shorted CT on a circuit that is carrying one-fourth of the load current on the bus will cause the restraint current to drop to three-fourths of its prior value and the operate current to increase by the same amount that the restraint current decreased. The absolute value of operate current will depend on tap settings, CT ratios, and the total bus loading at the time.

With modern microprocessor-based low-impedance bus differential relays, the tap settings can eliminate virtually any difference current under normal load conditions, so an operate current threshold can be set quite sensitively to detect open or shorted CTs. Use this threshold to alarm, trip the bus, or disable the bus differential scheme, depending on security and operating requirements. This threshold is extremely important, considering that open CTs are hazardous and that shorted CTs can compromise the bus differential relay security for external bus fault conditions. Both conditions must be investigated and resolved quickly.

A more sophisticated approach detects the change in operate and restraint current when the output of a CT is lost because of a short or open. The loss of a CT output current on a circuit carrying load results in an increase in operate current and a decrease in restraint current. The magnitude of the change depends on the circuit and bus loading at the time, as described previously. However, the delta operate/restraint thresholds should be set quite sensitively to detect CT problems.

If the CT circuit is shorted or opened when no load is on the circuit or when the circuit breaker is open, such as during maintenance, neither the simple sensitive operate current threshold method nor the delta operate/restraint technique will detect a problem. As the circuit and bus loading increases, the operate current and restraint current will both increase, so the only technique that will detect the problem is the simple but sensitive operate current threshold detector. It is therefore advisable to use both techniques to ensure detection of this abnormal condition as quickly as possible.

Grounding jumpers or chains are usually connected to the isolated terminals on both sides of a breaker during breaker maintenance, effectively shorting the primary side of the CT. This has no effect on a low-impedance bus differential scheme because there should be no current flow in the breaker during maintenance.

Conversely, if an external ground fault occurs during breaker maintenance, sufficient ground current may flow through the breaker grounds to cause the low-impedance bus differential relay to operate. If possible, the grounding jumpers on both sides of the breaker should be connected to the same point on the ground mat to avoid this problem. Leaving the breaker contacts open during maintenance also eliminates this potential problem.

C. CT Performance Requirements

Individual CT inputs on low-impedance bus differential relays include magnitude compensation (tap settings) necessary to normalize currents from different CT ratios. Relays typically limit the magnitude compensation (tap setting) range, which results in a limit on the range of CT ratios that the relay can accommodate. Bus differential CTs should be connected with their maximum ratio for best performance during fault conditions.

While avoiding CT saturation for bus differential applications is preferred, the reality is that completely avoiding CT saturation is virtually impossible. Low-impedance bus differential relays must therefore tolerate some degree of CT saturation. Low-impedance bus differential relays employ various techniques to mitigate the effects of CT saturation during external faults that otherwise would result in unwanted tripping.

CT saturation presents itself as a nonsinusoidal secondary current waveform with a reduced peak magnitude, reduced output energy (area under the curve), and an advanced (more leading) current phase angle, as shown in Fig. 9.

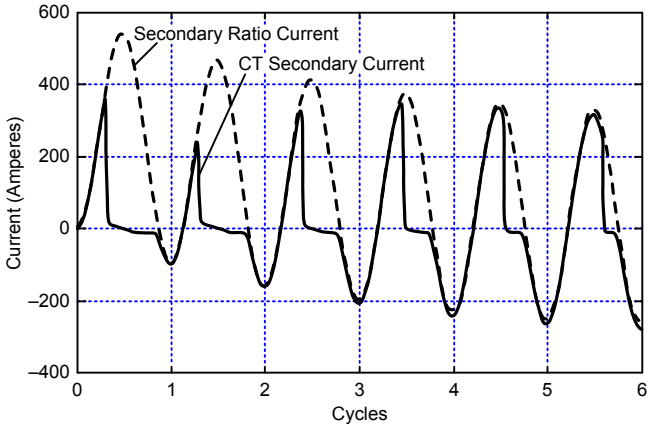

Fig. 9. Current waveforms of a C100, 1200:5 CT with burden of 0.5 ohms, 50 kA, and X/R equal to 17

Protective relay schemes generally rely on the faithful reproduction of primary current, scaled to secondary quantities that the protective relay measures to detect power system faults. By standard, relaying accuracy CTs produce a secondary current value that is within 10 percent of the primary current divided by the CT ratio for currents as great as 20 times the CT current rating. The ratio error results primarily from the excitation current conducted by the magnetizing branch of the CT, thereby reducing the current available to the CT secondary circuit and the relay(s). With a typical 5 A secondary CT, the primary to secondary ratio current is within 10 percent when the excitation current is less than 10 percent of the secondary current. At 100 A secondary, the excitation current must be less than 10 A.

CT excitation curves are available from the CT manufacturer, or can be created by test, showing the relationship between applied voltage and excitation current. Fig. 10 shows an example CT excitation curve.

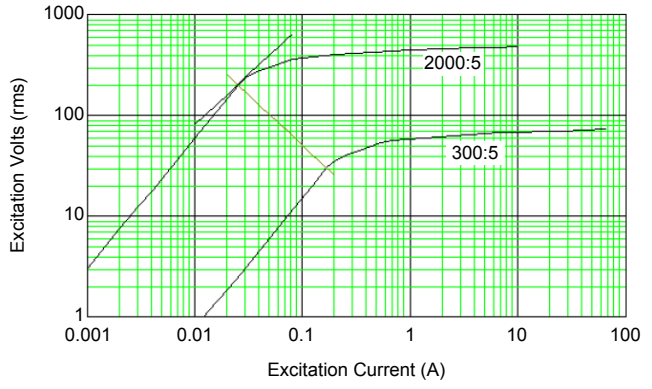

Fig. 10. 2000:5 CT excitation curve and its 300:5 tap, both with knee-point tangents and normal lines

As shown in this example CT excitation curve, the excitation voltage must be well above the CT knee-point voltage to produce a significant excitation current. IEEE standards define the knee point of the curve as the point at which a 45-degree line touches the excitation curve. The saturation voltage, V_S, is typically defined as the voltage that produces 10 A of excitation current in a 5 A secondary CT or 2 A of exciting current in a 1 A CT. The saturating voltage is roughly twice the IEEE knee-point voltage. The example curve also shows that lowering the connected tap on multiratio CTs proportionately reduces the excitation voltage necessary to produce significant excitation current.

The excitation voltage applied to a CT is a function of the voltage drop produced by the CT secondary current as it passes through the secondary circuit consisting of CT leads, relays, meters, and transducers. By IEEE standard, the relay accuracy classification (C rating) of the CT is based on the ability to produce a secondary output current that is within 10 percent of the primary current, reflected to secondary by the CT turns ratio, at 20 times the CT secondary current rating with standard burden. For a 5 A secondary rated CT, this is 100 A secondary. For a C200 class CT, this means that the voltage across the CT secondary terminals will not produce more than 10 A of exciting current when connected to a standard 2-ohm burden. The voltage necessary to produce 10 percent or more excitation current is sometimes referred to as the CT saturation voltage.

Unfortunately, CT saturation is an unwanted reality in many applications and is quite common in industrial applications that use switchgear. Very often, switchgear contains relatively low-ratio and low-accuracy CTs because of their lighter weight, smaller size, and lower cost than higher accuracy and higher ratio CTs. Small ratio CTs are also commonly applied to improve relaying sensitivity and metering resolution on circuits that supply small loads. The combination of low-accuracy rating and low ratio increases the likelihood of CT saturation as fault current levels and source X/R ratios increase. High X/R ratios are most commonly found on the load side of generators and power transformers because of their predominately inductive impedance.

A percentage current differential characteristic, as in Fig. 3, is common in low-impedance bus differential relays. Relays with a dual-slope characteristic may be used to further mitigate the effects of CT saturation at higher fault currents. Empirical methods are available to determine characteristic slope settings adequate for preventing inadvertent operation during external faults with CT saturation on the faulted circuit CT [5][6].

More sophisticated techniques to overcome the effects of CT saturation during external faults are available in modern microprocessor-based bus differential relays. As discussed under “Open and Shorted CT Detection” in Section II, one technique requires that each CT only needs to supply replica secondary current for a very short time at the beginning of each half cycle. For example, a minimum of 2 milliseconds of good CT secondary current at the beginning of each half

cycle is sufficient for some modern bus differential relays to distinguish internal and external faults [7]. Therefore, CT performance analysis must be conducted to ensure sufficient CT output, using CT excitation characteristics, CT secondary circuit parameters, and maximum fault [8][9].

D. Real-Time Operating Data

The microprocessor-based low-impedance bus differential relay measures currents on each of the circuit breakers associated with the bus. Bus differential relays that also include voltage inputs can combine voltage and current measurements to calculate directional watt and VAR measurements. The low-impedance bus differential relay is therefore a good source of real-time operating data for utility SCADA (supervisory control and data acquisition) and industrial distributed control systems.

III. HIGH-IMPEDANCE BUS DIFFERENTIAL RELAYS

High-impedance bus differential relays are applied to the paralleled output of all CTs from each phase connected to a common bus, as shown in Fig. 11. As the name implies, the high-impedance bus differential relay presents a very high impedance to the flow of current. The paralleled CTs must have the same ratio and proper polarity connection to ensure that the secondary current outputs from the paralleled CTs vectorially add up to zero in the same way the primary currents in the bus do under normal through-load conditions. Any current difference is forced through the high impedance of the bus differential relay causing a voltage drop across the relay. The high-impedance relay, which is calibrated and set to trip based on the voltage across the relay, is extremely sensitive to CT difference current. For this reason, not only must the CT ratios match, but the CT accuracy ratings must also match to minimize the CT performance differences that could create CT difference current.

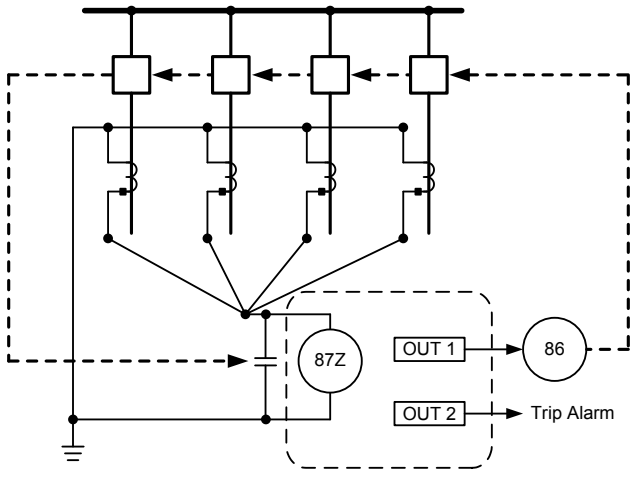

Fig. 11. Paralleled CTs connected to a high-impedance bus differential relay

A. High-Impedance Bus Differential Relay Operation

The high-impedance input is created by an internal impedance, typically resistive, of 2000 ohms or higher. A sensitive current element in series with the high-impedance element is calibrated in volts based on the voltage drop across the internal impedance.

Fig. 12 shows the basic elements of a high-impedance bus differential relay. The 87Z element is a sensitive, low-impedance, adjustable, pickup current element scaled in voltage. An MOV is connected across the high-impedance circuit to prevent high voltage from damaging the relay and CT circuitry. The energy absorption capability of the MOV must be sufficient to tolerate the energy the paralleled CTs deliver for a period of several cycles. Under worst-case scenarios with a breaker that fails to interrupt fault current, the current can continue to flow for as long as 20 to 30 cycles. Some high-impedance bus differential relays offer MOVs with sufficient size to tolerate the energy absorption over this extended period. Others reduce the MOV energy absorption requirements by connecting a lockout relay (86) contact across the high-impedance branch of the relay. This diverts current away from the high-impedance relay path after the relay trips the lockout relay for an internal bus fault.

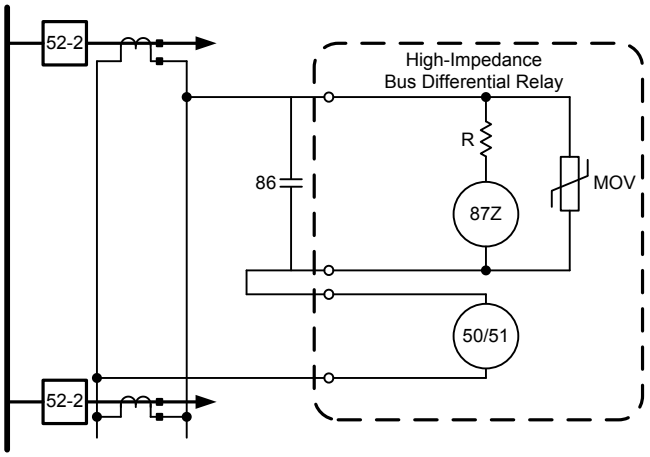

Fig. 12. High-impedance bus differential relay internal elements

Modern microprocessor-based high-impedance bus differential relays often include at least two levels of voltage elements: one level set higher for fast and secure tripping and one level set lower for triggering event reports and/or providing a more sensitive trip function with time delay added for security.

A separate set of overcurrent elements connected in series with the parallel combination of high-impedance element and MOV provides backup protection for MOV failure and a separate current measurement after the lockout relay contact closes. This circuit bypasses the high-impedance voltage element.

1) Normal Through-Load Conditions

Under normal conditions with through-load current and equal performance from all CTs, the secondary CT current circulates around the paralleled CT circuit as in the equivalent two-CT drawing in Fig. 13.

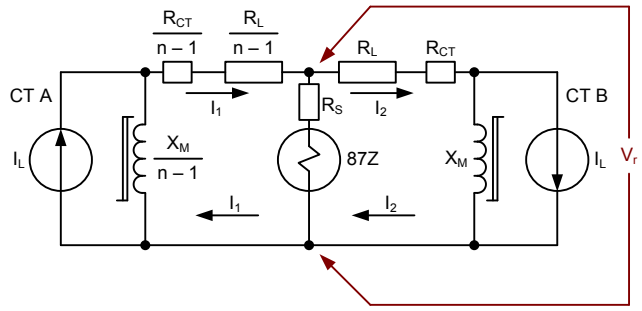

Fig. 13. Equivalent two-CT circuit showing balanced current in parallel CTs

Fig. 13 shows a constant current source for CT A, which is the sum of all CT secondary currents except one. The constant current source labeled CT B represents the current flowing through the remaining single CT. Under balanced load conditions or during an external fault condition, if the CTs do not saturate and all CTs have the same ratio, the current from CT A will be equal to the current from CT B. As a result, the current will circulate among the CTs, and no current will flow through the high-impedance relay path (R_S and 87Z), regardless of the internal impedance of the relay.

For an external fault condition, CT A is the parallel combination of the CTs that are providing current to the bus, and CT B is the CT that is on the faulted circuit. Because CT A is a parallel combination, the exciting branch reactance and the series resistance is divided by $n - 1$, where n is the total number of CTs in the scheme. This assumes that all CTs have the same or very similar magnetizing branch impedances, internal resistance, and CT lead resistance.

With no CT saturation and equal performance from matched CTs, there is very little or no difference current to create a voltage across the high-impedance relay element, as shown in Fig. 13 and Fig. 14.

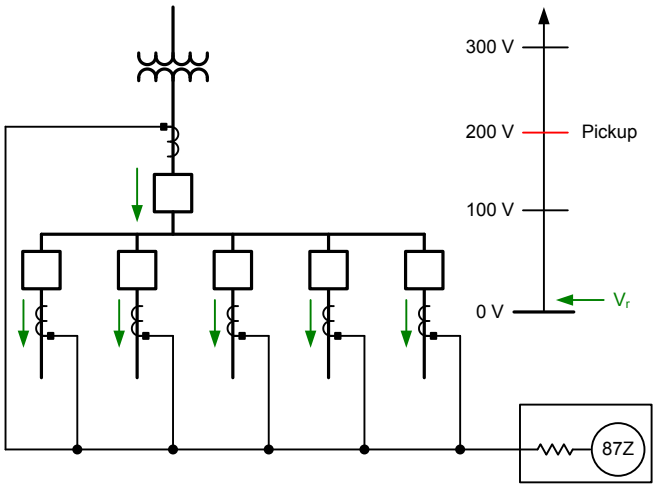

Fig. 14. Balanced current flow in CTs for through-load condition

2) Through-Fault Conditions

Under through-fault conditions, the faulted circuit CT carries the most current, making it the most likely to saturate. The high-impedance bus differential relay tripping voltage threshold must be set above the voltage that could develop across the relay with a completely saturated CT. A completely saturated CT produces no current output. The saturated CT circuit becomes a simple current path represented by the internal CT resistance, R_{CT}. Because the CT lead and internal resistance are small with respect to the internal resistance of the high-impedance relay path, the worst-case voltage, V_r, across the relay is the voltage drop across the CT lead and internal resistance under maximum external fault conditions, as shown in Fig. 15.

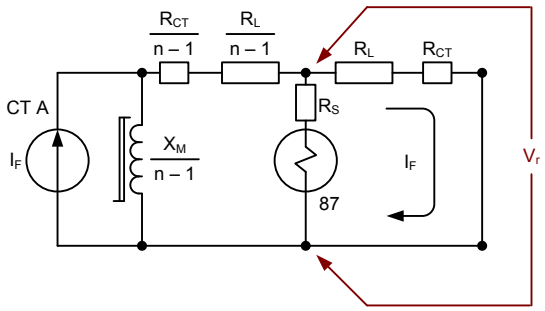

Fig. 15. Equivalent two-CT circuit showing effects of complete saturation on the fault circuit

Fig. 16 shows the current flow in the bus for an external fault and the relay voltage, V_r, developed because of the fully saturated CT. The relay trip threshold voltage pickup must be set higher than the maximum voltage developed across the high-impedance relay element, usually by a factor of 1.5 or more, for the worst-case external fault.

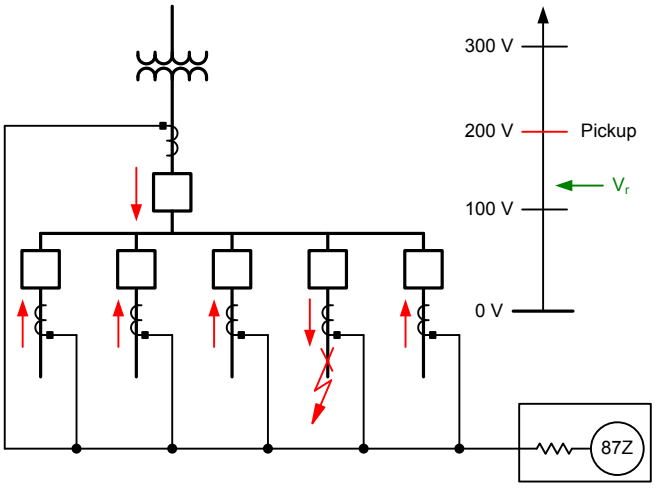

Fig. 16. Fault current flow for an external bus fault

The combination of fault current and the resulting secondary circuit voltage drop must be examined for each circuit on the bus using the maximum external fault current for each circuit position and the corresponding CT lead and internal resistance, as shown in (1). The CT lead resistance used in the calculation must take into account the fault type. For three-phase faults, the one-way lead resistance is used ($k = 1$); for single-phase-to-ground faults, the round trip lead resistance must be used ($k = 2$).

$$V_t = \frac{I_F}{N} \bullet (R_{CT} + R_{LEAD} \bullet k) \quad (1)$$

where:

I_F is the maximum external fault current.

N is the CT ratio (at a particular tap).

R_{CT} is the CT secondary winding and lead resistance up to the CT terminals.

R_{LEAD} is the one-way resistance of lead from junction points to the most distant CT.

k is equal to 1 for three-phase faults and 2 for single-phase-to-ground faults.

The pickup setting for the relay element should be set at:

$$V_S = K \bullet V_r \quad (2)$$

where:

K is a safety factor representing the necessary security level and CT performance.

This calculation is simple if the CT leads are routed individually to a common junction point, as shown in Fig. 11. The calculation is more complex if the CTs are "daisy-chained" as implied by the one-line representations in Fig. 14 and Fig. 16. High-impedance bus differential relay manufacturers typically recommend that CT leads be routed to a common junction to simplify the setting calculations and post-fault performance analysis for this type of relay.

The safety factor used to determine the relay setting is normally 1.5 or even higher. The safety factor allows for future fault current increases because of power system expansion and capacity increases. To be even more conservative, the maximum breaker interrupting duty may be used to calculate V_r, thereby taking into account future increases in available fault current up to the breaker interrupting limit.

CT internal resistance may not be readily available for older CTs. In general, for 5 A secondary CTs with fully distributed windings, the internal CT resistance can be estimated using 0.0025 ohms per turn.

3) Internal Bus Faults

During an internal bus fault, all the primary current sources contribute to the total bus fault current. Likewise, the CT secondary currents try to force the equivalent total secondary current into the high-impedance bus differential relay. Fig. 17 shows the equivalent circuit of n number of CTs driving current into the high internal impedance of the high-impedance relay. Analyzing the result is quite complex. Essentially, the high internal impedance of the relay presents an open circuit to the parallel CTs. This would normally produce extremely high voltages that could be damaging and hazardous. In this case, the MOV safely clamps the voltage spikes every half cycle to prevent any damage to the relay or wiring.

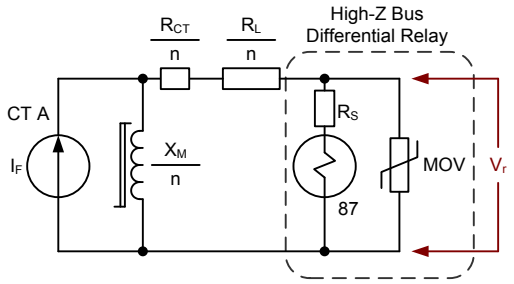

Fig. 17. Equivalent circuit of n CTs driving current into the high-impedance bus differential relay during an internal bus fault

Fig. 18 shows the primary current flow for an internal bus fault. It also shows that the voltage developed across the relay exceeds the pickup setting on the relay to produce a trip.

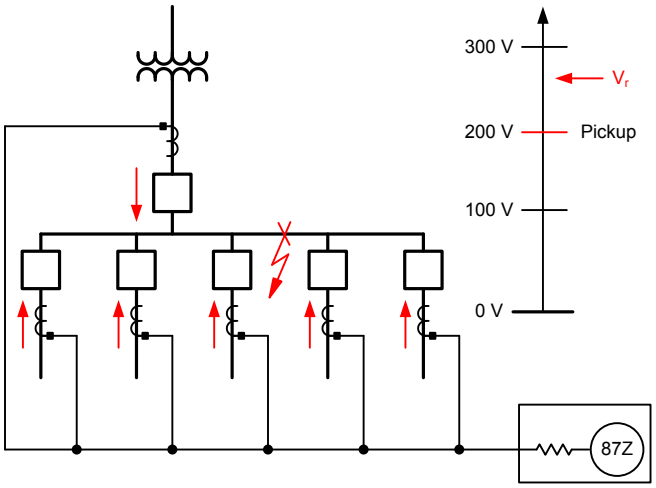

Fig. 18. Fault current flow for an internal bus fault

What voltage the relay measures, however, is very much dependent on the relay design. As stated earlier, severe CT saturation creates voltage spikes, and the MOV acts to clamp the voltage across the relay voltage element, clipping the voltage spikes. As a result, the voltage developed across the relay is extremely nonsinusoidal, as shown in Fig. 19, for a 60 kA symmetrical internal fault in a system with four C200, 1200/5 CTs.

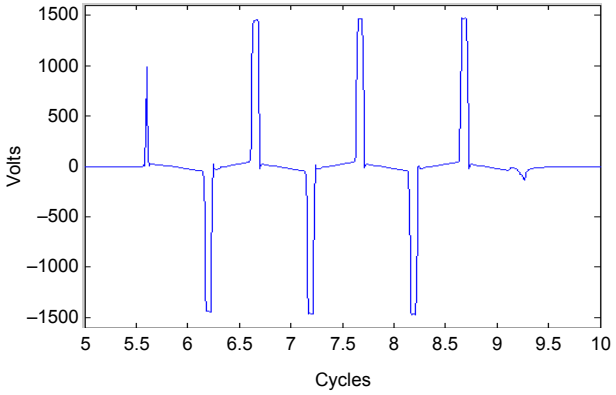

Fig. 19. Voltage waveform for a 60 kA primary current through a 1200/5, C200 class CT connected to a high-impedance bus differential relay with a 1400 V MOV

Modeling the dynamics of CTs and MOVs in this circuit is extremely complex, so primary current tests were used to confirm the performance of the relay under these conditions.

Modern microprocessor-based relays employ sampling and filtering techniques to measure the fundamental component of a waveform. Fig. 20 shows the results of measuring the waveform in Fig. 19 with a one-half-cycle cosine digital filter.

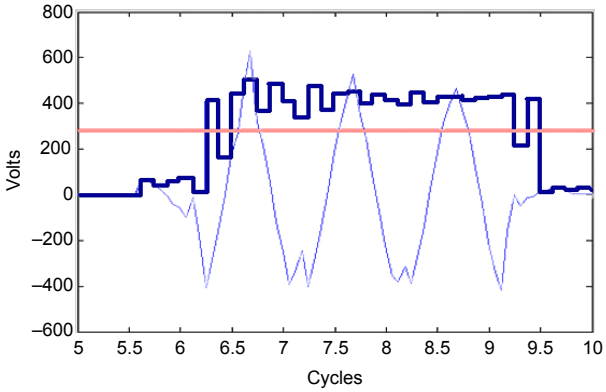

Fig. 20. One-half-cycle cosine filtered output (thin blue line), the magnitude of the output (thick blue line), and the relay 200 V trip threshold (peak of setting shown with red line)

The magnitude of the filter output exceeds the 200 V pickup threshold, but not by as much as one might expect for a 60 kA internal bus fault. In fact, the filtered output voltage does not change appreciably with fault current or even CT ratio. The nearly constant MOV clamping voltage and the fast rise-time voltage across the CTs create a nearly identical voltage waveform regardless of fault current or CT ratio for the same CT accuracy class. The magnitude of the voltage waveform in Fig. 19 is limited by the MOV, and the pulse width is limited to the volt-time area of the C200 CT. Increasing the CT accuracy class to C400 doubles the volt-time area of the pulse and increases the filtered output, as shown in Fig. 21.

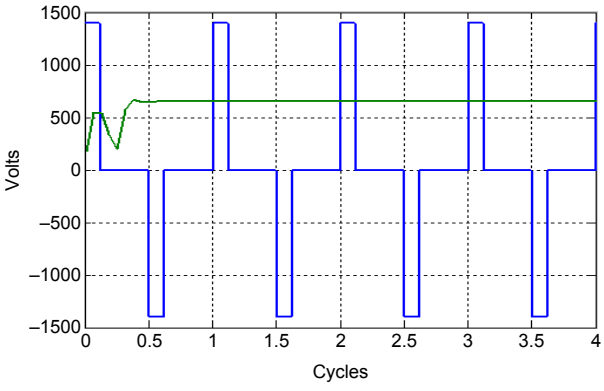

Fig. 21. Voltage waveform and filtered output magnitude for a 60 kA primary current through a 1200/5, C400 class CT connected to a high-impedance bus differential relay with a 1400 V MOV

4) Other Conditions

As discussed under “Other Conditions” in Section II, for low-impedance relays, high-impedance bus differential relay protection is similarly affected by shunt connected equipment, such as surge arresters, auxiliary power transformers, and VTs that either momentarily or continuously provide a leakage current path in the protection zone.

High-impedance differential relays may need to apply a small delay, typically 1 cycle, to prevent tripping on MOV surge arrester operation. Older gapped surge arresters typically have a power follow current that can last up to one-half cycle, so we suggest adding an additional one-half-cycle delay where these older style arresters are present.

We also need to account for the possible adverse effects caused by auxiliary power transformers and their loads. Raising the relay tripping threshold voltage to avoid nuisance trips caused by auxiliary transformer magnetizing inrush, secondary faults, or motor starting may be necessary. If that is not possible, then a time delay may be added to ride through these transient conditions. If a time delay is undesirable, then matching CTs need to be applied to the transformer, with the secondary circuits paralleled with the existing bus differential CTs to exclude the transformer from the bus differential protection zone. Primary protection, such as fuses, needs to be applied to protect the transformer.

As with low-impedance bus differential schemes, stray bus capacitance is usually ignored when applying high-impedance bus differential relays because of the negligible capacitive leakage current associated with typical substation buses.

5) Minimum Current Sensitivity

Once the relay pickup threshold is established, the minimum primary current sensitivity can be determined using (3).

$$I_{min} = \left(n \bullet I_e + I_r + I_m\right) \bullet N \tag{3}$$

where:

I_{min} is the minimum current.

n is the number of current transformers in parallel with the relay, per single phase.

I_e is the CT exciting current at relay setting voltage, V_r.

I_r is the current through the relay at relay setting voltage, V_r.

I_m is the current through the MOV at relay setting voltage, V_r.

N is the number of turns for the CT ratio.

This calculation requires information about the excitation characteristics for all the CTs used in the scheme. High-impedance bus differential applications generally require the same accuracy class CTs for all circuit positions, so it is customary to use one CT excitation characteristic curve to determine the exciting current for all CTs in the circuit.

Experience indicates that CT excitation characteristics can vary considerably within the same accuracy class. Published excitation curves from the CT manufacturer may also be generic for the particular CT class. CT excitation tests may be required to accurately determine the values used to determine minimum current sensitivity.

As an example, minimum current sensitivity was calculated for 1200/5, C200 class CTs using measured and published excitation curve data shown in Fig. 22. For a relay pickup setting of 100 V, the measured excitation current is 0.0349 A, and the excitation current from the published curve is 0.0379 A.

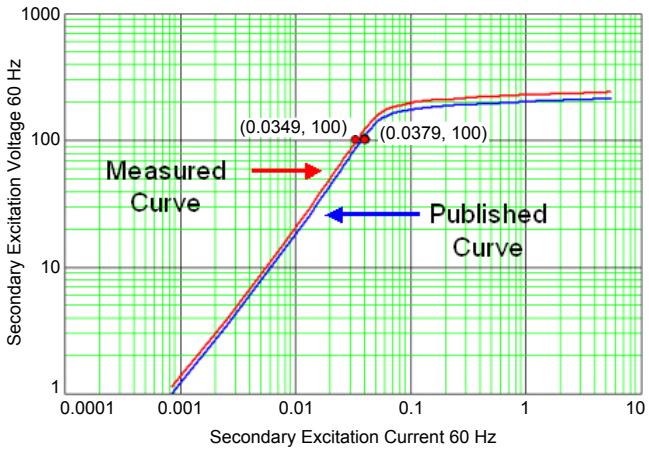

Fig. 22. Measured and published excitation current characteristics for a 1200/5, C200 class CT with a relay pickup voltage threshold of 100 V

The calculated results for a four-CT bus differential circuit are within five percent as shown in (4) and (5).

From published curve data:

$$\begin{aligned} I_{min} &= \left(n \bullet I_e + I_r + I_m\right) \bullet N \\ &= \left[4\left(0.0379\right) + 0.052 + 0\right] \bullet 240 \\ &= 48.9\,\text{A} \end{aligned} \tag{4}$$

From measured curve data:

$$\begin{aligned} I_{min} &= \left(n \bullet I_e + I_r + I_m\right) \bullet N \\ &= \left[4\left(0.0349\right) + 0.052 + 0\right] \bullet 240 \\ &= 45.98\,\text{A} \end{aligned} \tag{5}$$

Tests performed on the circuit confirmed a pickup current of about 47 A, validating the calculated values.

For the same four-CT differential circuit, the minimum current sensitivity was calculated and measured for a relay pickup voltage threshold of 200 V, as shown in Fig. 23. For this case, the measured excitation current is 0.1 A, and the excitation current from the published curve is 0.4 A, a considerable difference.

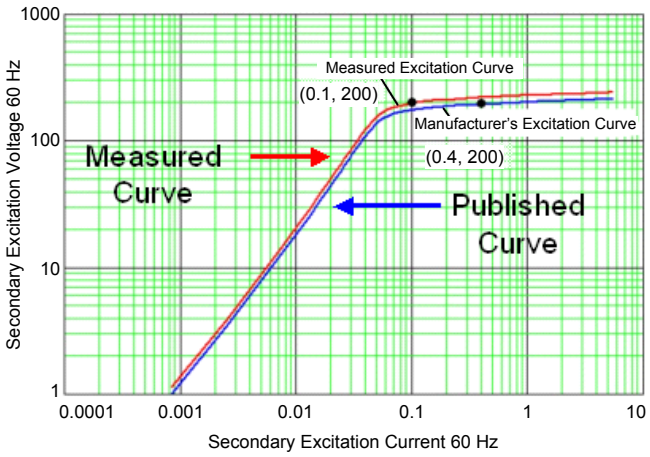

Fig. 23. Measured and published excitation current characteristics for a 1200/5, C200 class CT with a relay pickup voltage threshold of 200 V

The calculated results for a four-CT bus differential circuit are also considerably different as shown in (6) and (7).

From published curve data:

$$\begin{aligned} I_{min} &= \left(n \bullet I_e + I_r + I_m\right) \bullet N \\ &= \left[4\left(0.4\right) + 0.1 + 0\right] \bullet 240 \\ &= 408\,A \end{aligned} \tag{6}$$

From measured curve data:

$$\begin{aligned} I_{min} &= \left(n \bullet I_e + I_r + I_m\right) \bullet N \\ &= \left[4\left(0.1\right) + 0.1 + 0\right] \bullet 240 \\ &= 120\,A \end{aligned} \tag{7}$$

Tests performed on the circuit determined the minimum pickup current to be 88 A, which is considerably lower than either calculated value. This points out an interesting issue. The excitation curves, measured or published, are derived by applying sinusoidal voltage to the CT and measuring the resulting exciting current. In the minimum current sensitivity tests with the relay pickup voltage above the knee-point voltage on the excitation curve, the applied voltage is no longer sinusoidal, as shown in Fig. 24.

With nonsinusoidal voltage applied to the CT, there is no simple way to determine the CT excitation current magnitudes for the minimum current sensitivity calculation. If the relay pickup setting voltage is above the knee point of the excitation curve, the minimum current sensitivity can only be determined accurately by test. In the case of the C200 CT excitation characteristics in Fig. 23, reading the excitation current at a 200 V setting above the knee point from either the published or measured curve produced a value that did not match test results. From the test results for this set of CTs, a more accurate estimate of excitation current at the 200 V setting was obtained by using twice the excitation current read at 100 V (a point below the knee point).

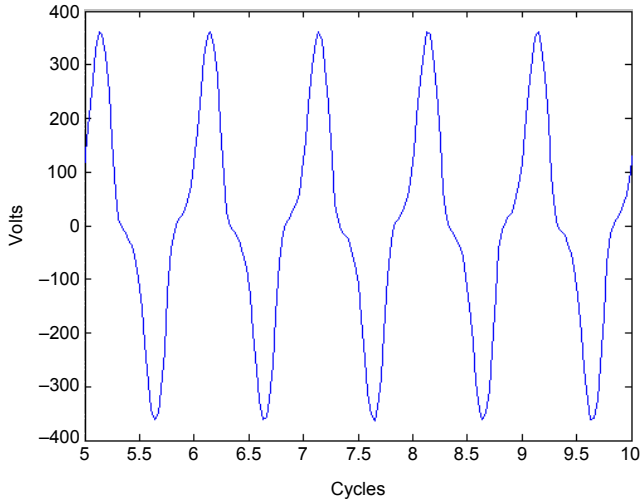

Fig. 24. Voltage waveform at the 200 V pickup point with C200 rated CTs

Using this empirical method from published curve data:

$$\begin{aligned} I_{min} &= \left(n \bullet I_e + I_r + I_m\right) \bullet N \\ &= \left[4\left(0.0379 \bullet 2\right) + \left(0.052 \bullet 2\right) + 0\right] \bullet 240 \\ &= 98\,A \end{aligned} \tag{8}$$

Using this empirical method from measured curve data:

$$\begin{aligned} I_{min} &= \left(n \bullet I_e + I_r + I_m\right) \bullet N \\ &= \left[4\left(0.0349 \bullet 2\right) + \left(0.052 \bullet 2\right) + 0\right] \bullet 240 \\ &= 92\,A \end{aligned} \tag{9}$$

Both of these results compare very well with the test results of 88 A, and both tend to err on the conservative side, which is generally considered desirable in protective relay applications.

Conventional wisdom and standards indicate that the high-impedance bus differential relay tripping voltage threshold should not be set above the lowest effective CT accuracy rating of the CTs connected in the bus differential scheme [10][11]. Doing so results in an undefined bus differential relay minimum current sensitivity. The empirical method expressed above for determining minimum current sensitivity is only applicable up to the rated accuracy class of the CTs used in the scheme (200 V for a C200 CT, 400 V for a C400 CT, and so on).

If possible, a second set of differential relay voltage elements, commonly available on modern microprocessor-based high-impedance bus differential relays, should be set below the knee point of the curve to provide better sensitivity. However, the additional element setting must never be below the maximum voltage, V_r, calculated using (1). Improved security can be obtained by applying a few cycles of time delay for the tripping output using this lower voltage setting.

B. *Supplemental Protection Functions*

High-impedance bus differential relays offer no opportunity for supplemental protection functions such as breaker failure protection or end-zone protection because the individual circuit current measurements are lost when the CTs are paralleled.

1) *Open CT Detection*

An open CT connection creates a hazardous voltage across the open-circuited CT. By virtue of the open circuit, this voltage is not applied to the high-impedance relay. However, the secondary current unbalance created by the output lost from one of the paralleled CTs creates a voltage across the relay proportional to the load current on the circuit with the open-circuited CT. The difference current will attempt to flow through the high internal impedance in the bus differential relay that will almost assuredly cause the relay to trip. Fig. 25 shows an example one-line diagram with an open CT circuit.

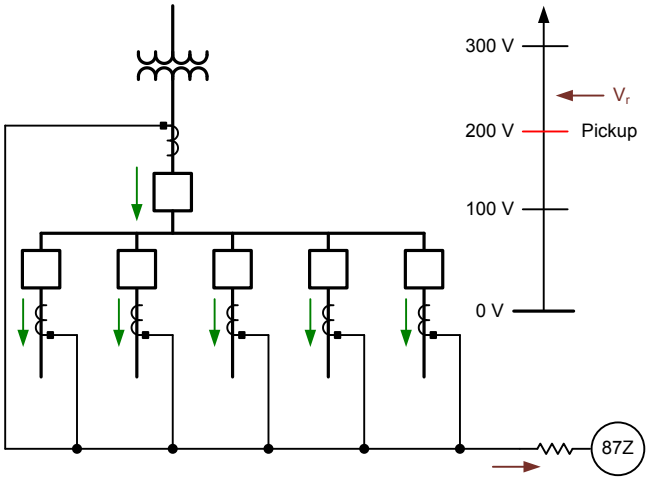

Fig. 25. Example one-line diagram with an open CT connection

Consider a 200 V trip threshold setting on the relay. It will only take 0.1 A of difference current to reach the 200 V trip threshold. For a 1200/5 CT ratio, this translates to about 24 A of primary load current on the circuit with the open CT connection. Any more than this will cause the relay to trip for the open-circuited CT condition. Considering that an open CT condition is hazardous, tripping the bus for this condition may be desirable.

Setting a second voltage element in the bus differential relay with a lower threshold to detect an open CT condition under lower loading conditions may sound beneficial. But the practical benefit from this second threshold is extremely limited because of the very small load required to reach the normal trip voltage.

2) *Shorted CT Detection*

Shorted CTs will disable the high-impedance differential relay. Of concern is that the relay cannot detect this condition because the voltage across the high-impedance bus differential relay is normally zero. The shorted CT connection keeps the voltage across the relay at zero volts even under fault conditions, as shown in Fig. 26.

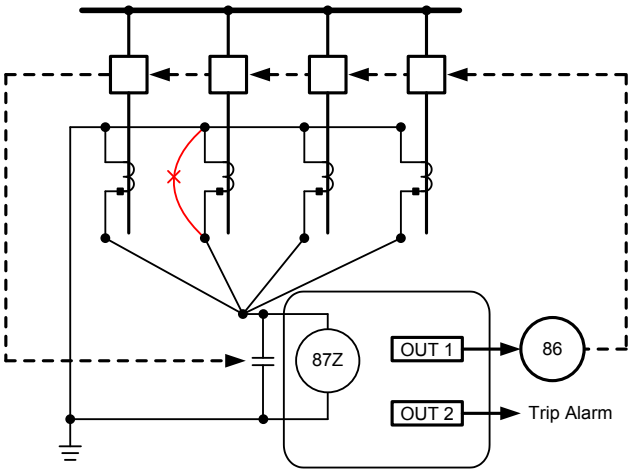

Fig. 26. Shorted CT disables high-impedance bus differential relay

One test technique that is used to detect shorted CTs in a high-impedance bus differential relay circuit is to apply a relatively low ac voltage across the relay terminals and measure the current. Only a few volts should be necessary to detect a short circuit in the parallel CT circuit. The high magnetizing branch impedance of the CTs and the high internal impedance of the bus differential relay under normal operation should prevent any appreciable current from flowing unless a short exists across one of the CTs.

Breaker maintenance may also be a concern for the high-impedance bus differential scheme. Grounding jumpers or chains are usually connected to the isolated terminals on both sides of a breaker when breaker maintenance is performed, as shown in Fig. 27. If the breaker contacts are closed, the breaker grounds provide a primary short circuit on the CTs internal to the dead-tank breaker. Generally there is enough resistance in the ground path that, when reflected to the secondary side through the CT ratio, the “short circuit” is more of a resistive bypass that can reduce the sensitivity of the high-impedance bus differential relay.

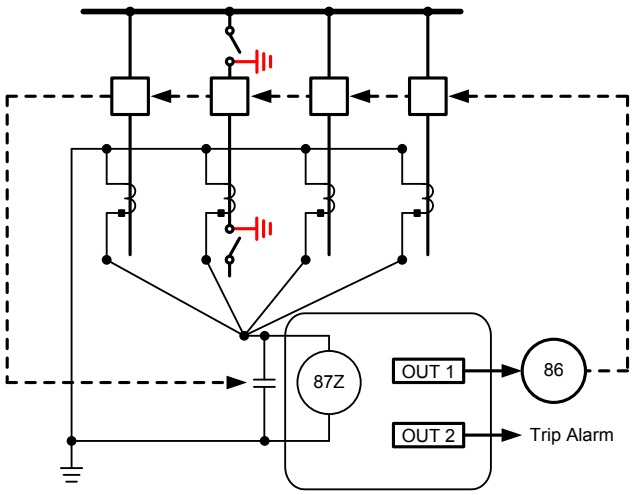

Fig. 27. Grounding chains during breaker maintenance can disable or desensitize a high-impedance bus differential relay

Conversely, if an external ground fault occurs during breaker maintenance, sufficient ground current may flow through the breaker grounds to cause the high-impedance bus differential relay to operate. It is therefore desirable to connect the grounding jumpers on both sides of the breaker to a common point on the substation ground mat.

Both of these undesirable conditions can be avoided by leaving the breaker contacts open during the maintenance period as much as possible.

C. CT Performance Requirements

High-impedance bus differential relays are designed to perform securely during external faults, even with severe CT saturation on the CT associated with the faulted circuit. Secure operation for external faults requires that the relay tripping threshold voltage is set appropriately based on (1) and (2), presented earlier. Higher CT ratios will reduce the secondary CT circuit voltage developed for an external fault. However, this is slightly offset by the higher internal CT resistance associated with a greater number of turns. Higher CT accuracy class also results in a slightly higher internal CT resistance because of the larger core area and length. However, neither of these concerns is sufficient to override the benefits of higher CT ratios and CT accuracy class in a high-impedance bus differential scheme.

Severe CT saturation will occur on internal faults, during which condition the high-impedance bus differential relay voltage measuring algorithm must be able to distinguish sufficient voltage to establish a trip output. For this reason, the relay tripping voltage threshold must not be set above the CT accuracy class rating. Conversely, there is typically a minimum CT accuracy class required to work with a specific relay design. For example, a C200 class CT rating may be required for some modern microprocessor-based relay designs.

Mixed ratio CTs are strongly discouraged because of the complexities that arise from reduced CT accuracy proportional to the CT tap used. Generally, two connection methods are available when matched CT ratios are not available. Both methods rely on the higher ratio CT having taps that match the lower ratio CTs.

Fig. 28 shows a method that simply uses the matching tap of the higher ratio CT connected in parallel with the lower ratio CTs. The higher ratio CT must have a higher accuracy class rating such that its derated accuracy class at the lower tap is equal to or greater than the accuracy class of the lower ratio CTs.

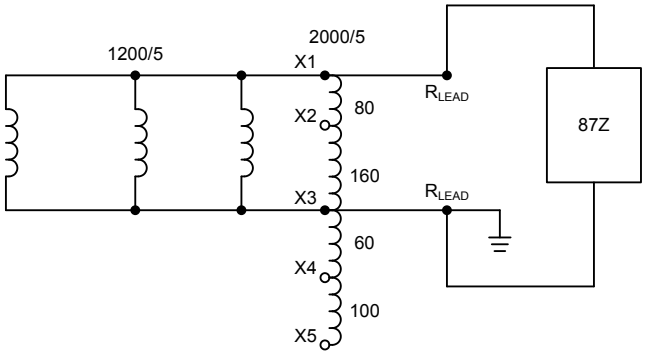

Fig. 28. Mismatched CT connection using the matching tap of the higher ratio CT

The disadvantage to using the connection shown in Fig. 28 is that the voltage developed across the relay for internal or external faults will be amplified through autotransformer action on the unconnected windings of the higher ratio CT. However, these high voltages are only present for a very short period of time, and the internal voltage suppression circuitry associated with typical high-impedance bus differential relays should keep the voltage within the insulation class of the wiring and relays. If the maximum voltage exceeds the dielectric strength of the CT windings, additional voltage suppression must be applied across the CT open windings.

Fig. 29 shows a method that connects the full winding of the highest ratio CT across the relay. The lower ratio CTs are connected to the matching tap of the highest ratio CT.

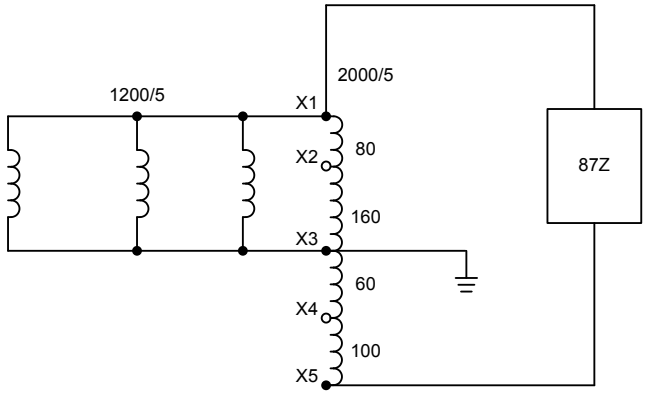

Fig. 29. Mismatched CT connection using the full ratio tap of the higher ratio CT connected to the high-impedance relay

The method shown in Fig. 29 also requires that the derated accuracy class of the tapped higher ratio CT be equal to or greater than the accuracy class of the lower ratio CTs. This method eliminates the overvoltage concerns because all the CT windings are directly protected by the voltage surge suppression in the high-impedance relay. What is not so apparent is that the thermal capacity of the CT may be jeopardized by this tap connection. For the 2000/5 CT shown in Fig. 28, if the primary current reaches the 2000 A full primary rating of the CT, the winding outside the parallel connection (in this case the 800/5 windings) will be forced to carry 2000 x 5/800, or 12.5 A secondary. That is 2.5 times the CT secondary rating. If the CT has a thermal rating factor of 1.0, it may require that the breaker current rating be derated to prevent thermal damage to the CT.

D. Real-Time Operating Data

High-impedance bus differential relays offer no opportunity for real-time operating data because the individual circuit current measurements are lost when the CTs are paralleled. The modern microprocessor-based high-impedance bus differential relay monitors and reports the voltage across its terminals, but this is normally near zero. Only transient conditions produce a measureable voltage that is of very little interest or use for real-time power system operations.

IV. Comparison and Conclusions

Table I provides a subjective comparison between high- and low-impedance bus differential relays. The check marks offer the authors' opinions regarding the superiority of one type of relay over the other for a specific consideration. Table I is provided to raise awareness of the considerations typically needed for high-impedance and low-impedance bus differential relay applications. The end user needs to evaluate the advantages and disadvantages of each relay based on the intended application and installation. For example, low-impedance relays offer the opportunity to share CTs with other applications. However, in an application where it is desirable to overlap the breaker with bus and line protection, the bus protection CTs will be installed on the line side of the line circuit breaker, and the line protection CTs will be installed on the bus side of the line circuit breaker. Dedicated CTs may very well be available for the bus protection scheme, so there is no benefit for the relay that can share CTs and no disadvantage for the relay that cannot.

TABLE I
COMPARISON TABLE FOR MICROPROCESSOR-BASED HIGH-IMPEDANCE AND LOW-IMPEDANCE BUS DIFFERENTIAL RELAYS

	High-Impedance	**Low-Impedance**
Shared CTs	No	Yes ✓
Multiple CT ratios	No	Yes ✓
Switched zone reconfiguration	No	Yes ✓
Shorted CT detection	No	Yes, alarms on unbalance ✓
Open CT detection	Yes (relay trips)	Yes, alarms on unbalance ✓
CT polarity compensation	No	Yes ✓
Speed	~1.5 cycles	< 1 cycle ✓
Sensitivity	Dependent on security setting	Settable ✓
Security	Good (better with dual-level settings)	Excellent ✓
Evolving fault logic	Not required ✓	Yes ✓
Selective breaker failure protection	No	Yes ✓
Selective end-zone fault protection	No	Yes ✓
Individual circuit metering	No	Yes ✓
Direct breaker tripping	No	Yes ✓
Scalability	Yes ✓	Limited by number of current inputs
Setting complexity	Low ✓	Moderate
Wiring complexity	Low ✓	Moderate
Panel space required	Low ✓	Moderate to high
Cost	Low ✓	Moderate to high

V. References

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VI. Further Reading

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VII. Biographies

Ken Behrendt received his B.S.E.E. from Michigan Technological University. After graduating, he served nearly 24 years at Wisconsin Electric Power Company (now We Energies), where he worked in distribution planning, substation standards development, distribution protection, and transmission planning and protection. He joined Schweitzer Engineering Laboratories, Inc. in 1994, where he is a senior field application engineer, located in New Berlin, Wisconsin. He is a senior member of IEEE, a member of the Power System Relay Main Committee, and has authored and presented several papers on power system protection topics.

David Costello graduated from Texas A&M University in 1991 with a B.S.E.E. He worked as a system protection engineer at Central Power and Light and Central and Southwest Services in Texas and Oklahoma. He has served on the System Protection Task Force for ERCOT. In 1996, David joined Schweitzer Engineering Laboratories, Inc. where he has served as a field application engineer and regional service manager. He presently holds the title of senior application engineer and works in Boerne, Texas. He is a senior member of IEEE and a member of the planning committee for the Conference for Protective Relay Engineers at Texas A&M University.

Stanley E. Zocholl has a B.S.E.E. and M.S.E.E. from Drexel University. He is an IEEE fellow and a member of the Power Engineering Society and the Industrial Applications Society of IEEE. He is a member of the Power System Relay Committee. He also participates as a member of the planning committees of the Georgia Tech and Western Protective Relay Conferences.

He joined Schweitzer Engineering Laboratories, Inc. in 1991 in the position of distinguished engineer. He was with ABB Power T&D Company-Allentown (formerly ITE, Gould, BBC, Westinghouse ABB) since 1947 where he held various engineering positions including director of protection technology.

His biography appears in Who's Who in America. He holds over a dozen patents associated with power system protection using solid-state and microprocessor technology and is the author of numerous IEEE and Protective Relay Conference papers. He received the best paper award of the 1988 Petroleum and Chemical Industry Conference. In 1991, he was recognized by Power System Relay Committee for distinguished service to the committee.

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