Analysis of Complex Power System Faults and Operating Conditions

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***Abstract*—Short-circuit calculations are extremely important in the application and settings of protective relays and in the analysis of system operations. Short-circuit programs provide the bus voltages and line currents, in the sequence and phase domain, for simple balanced and unbalanced short circuits in the network under study. Frequently, protection engineers have to analyze faults that are more complex than simple shunt faults. In many cases, they have to analyze simultaneous shunt and/or series faults, study systems with unbalanced network elements, and calculate equivalent impedances required to study the stability of a network during system faults and during open-phase conditions in single-phase tripping applications.**

This paper is a tutorial on the calculation of complex short-circuit faults, intended to help new protection engineers analyze complex system faults and system operating conditions.

I. Introduction

Protection engineers should be well versed in symmetrical component theory and analysis of faulted power systems to calculate appropriate relay settings and to analyze system operations. In this paper, we make extensive use of symmetrical components for short-circuit analysis [1].

Significant advances in short-circuit computations in the last 30 years have resulted in new short-circuit computer programs that handle different fault types and very large networks [2]–[8]. Often, standard short-circuit programs do not handle most complex faults, such as simultaneous shunt and/or series-faults. Engineers must then resort to complex hand calculations or to more advanced programs such as the Electromagnetic Transient Program (EMTP) to solve protection problems.

New protection engineers often have difficulty solving complex faults and operating conditions because the methods for studying these situations are not taught in most four-year electrical engineering curricula.

The application examples in this paper provide the protection engineer with information for calculating proper relay settings and for investigating relay operations that cannot be studied using typical short-circuit or load-flow programs. In addition, this paper demonstrates the importance of hand calculations in solving complex power system protection problems.

We discuss formulating the bus admittance and impedance matrices and calculating single and two-port Thevenin equivalents necessary for calculating simultaneous faults in different parts of the network. We also present several application examples that illustrate these methods in real system studies. These examples help explain complex fault analysis and help provide protection engineers with tools for studying similar or more advanced power system phenomena.

One example is an analysis of an unbalanced transformer bank consisting of three single-phase units with one of the phases having impedance and an MVA rating that are different from those of the other two phases. This situation occurs in power systems when a single-phase transformer fails and a system spare serves customers until the failed transformer is repaired or replaced. This example provides answers to both an operation-related question regarding permissible transformer bank loading, and a protection-related question on the level of circulating zero-sequence current in the transformer tertiary windings that may impact relay settings.

Another example explains how to calculate the appropriate impedances for studying the stability of the network during open-phase conditions in single-phase tripping applications.

II. Short-Circuit Analysis

A short-circuit analysis is a steady-state simulation in which the power system is modeled as a linear network driven by constant excitation. The network is assumed to be a balanced three-phase system with the exception of small localized changes in topology, which are referred to as faults. Short-circuit analysis provides the faulted network voltages and currents used for selecting power system equipment ratings and for setting and coordinating protective relays.

This section is a brief review of short-circuit analysis. It is not intended to show how modern short-circuit programs compute the postfault voltages and currents of large power system networks. Several IEEE Transactions papers cover the short-circuit analysis problem in greater detail [2]–[8]. In addition, Anderson has an excellent book on analyzing faulted power systems [9].

A. Classical Short-Circuit Analysis

The classical short-circuit method models the power system network using the bus impedance matrix, Z_{Bus}. The steps required to calculate the short-circuit voltages and currents are as follows:

1. Compute the sequence network bus impedance matrices.
2. Extract the sequence network single-port Thevenin equivalent impedances of the faulted bus, given by the diagonal terms, Z_{ii}, of the respective sequence network Z_{Bus} matrices, where i is the index of the faulted bus.
3. Use the sequence equivalent networks to compute the sequence fault currents at the faulted bus.
4. Use the computed sequence fault currents as compensating currents to calculate the network postfault voltages and currents.

Fig. 1 shows the single-port sequence impedance Thevenin equivalent networks used in the classic short-circuit calculation method. Elements $Z_{ii(1)}$, $Z_{ii(2)}$, and $Z_{ii(0)}$ are the positive-, negative, and zero-sequence network Thevenin equivalent impedances of Bus i or the sequence network driving point impedances of Bus i.

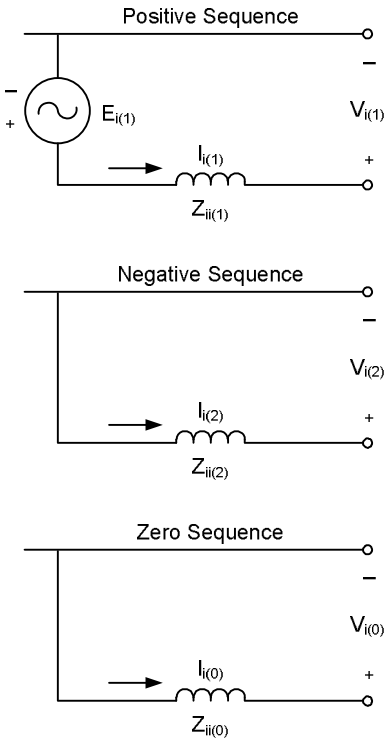

Fig. 1 Sequence network Thevenin equivalent circuits

For a single-phase-to-ground fault, we connect the positive-, negative-, and zero-sequence networks in series. For a phase-to-phase-to-ground fault, we connect the positive-, negative-, and zero-sequence networks in parallel. For a phase-to-phase fault, we connect the positive- and negative-sequence networks in parallel, and for three-phase faults, we use only the positive-sequence network.

B. Example of Classic Short-Circuit Calculations

Calculate the sequence currents for a solid A-phase-to-ground fault at Bus 2 for the system model shown in Fig. 2. All quantities are in pu.

Connect the positive-, negative-, and zero-sequence networks in series to model the A-phase-to-ground fault at Bus 2. We connect the sequence networks in series to satisfy the boundary conditions at the fault point, namely, $Va = 0$ and $Ib = Ic = 0$. Compute the sequence network fault currents.

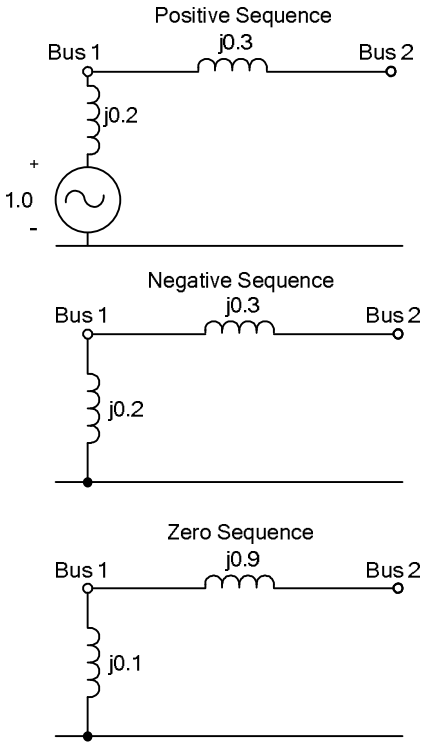

Fig. 2. Sequence network system model

Fig. 3 shows the sequence network connection for the A-phase-to-ground fault at Bus 2 and the resulting sequence network fault currents.

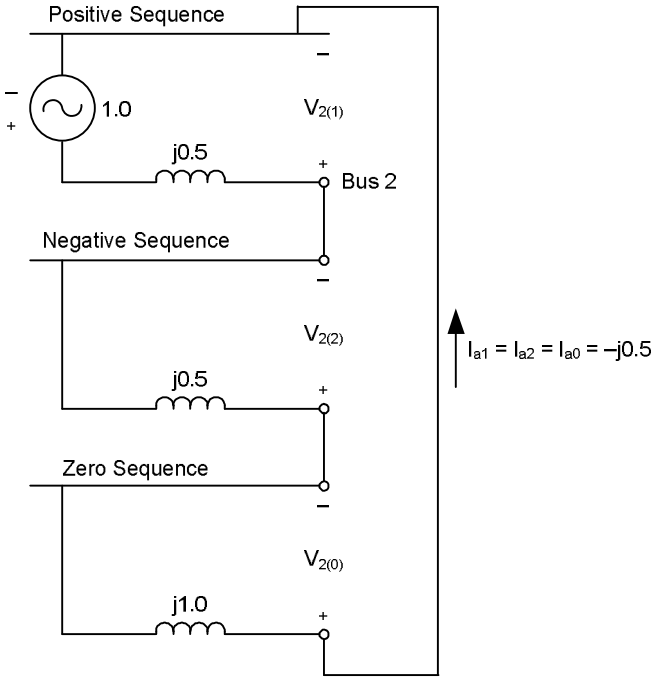

Fig. 3. A-phase-to-ground fault at Bus 2

Calculate the change in the sequence bus voltages by injecting the sequence network fault currents from Fig. 3 into the unmodified sequence networks. Network compensation is a powerful concept that allows us to model the changes in network topology by injecting appropriate compensating currents into the unmodified sequence networks.

Fig. 4 shows the sequence network compensation currents for the A-phase-to-ground fault at Bus 2.

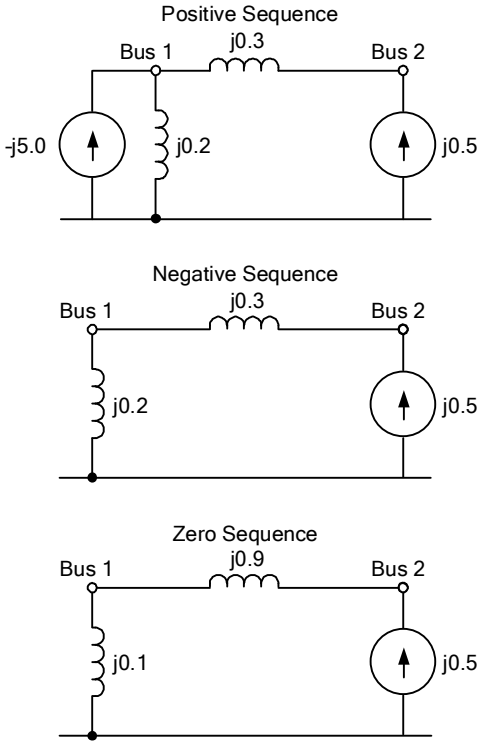

Fig. 4. Compensation currents for a single-phase-to-ground fault at Bus 2

III. Formulation of Bus Admittance and Bus Impedance Matrices

The impedance matrix is an excellent network description to use in solving faulted networks. We can calculate the total fault current at the faulted bus and the network branch currents from the bus impedance matrix elements. The bus impedance matrix contains the driving point impedances of every network bus with respect to the reference bus, which is the common bus behind the generator transient or subtransient reactances. The diagonal elements of the bus impedance matrix represent these driving point impedances.

The bus impedance matrix also contains the transfer impedances between the buses. The off-diagonal elements of the bus impedance matrix represent the transfer impedances between buses. We determine the transfer impedance from Bus *i* to Bus *j*, for example, by injecting 1 pu current at Bus *i* and computing the voltage at Bus *j*.

For us to calculate the sequence currents at the faulted bus, the bus injection currents, the bus voltage changes and the line currents we must first compute the bus impedance matrix elements of the sequence networks.

There are several methods to calculate the bus impedance matrix elements. In this paper, we calculate the bus impedance matrix by inverting the bus admittance matrix, even though this is not the method used in short-circuit programs that handle large networks. We use this approach because the network examples in the paper consist of only a few buses. We intend to illustrate the calculation of complex fault analysis methods by using the elements of the bus impedance matrix. We do not demonstrate the most efficient algorithms used in commercial short-circuit programs.

The bus admittance matrix is a square matrix of dimension *n* x *n*, where *n* is the number of network buses or nodes. The bus admittance matrix is sparse because each bus is only connected to a few nearby buses. In most cases, more than 95 percent of the matrix elements equal zero. The bus admittance matrix is a complex and symmetric matrix, but it is much simpler to build and modify than the bus impedance matrix. The zero-sequence mutual coupling is incorporated directly without any approximations. We demonstrate this with an example in Section III-C. In Section III-B, we discuss the formulation of the bus admittance matrix in networks with mutual coupling.

We will discuss two methods to calculate the bus admittance matrix. The first method consists of a few simple steps and is applicable to networks that do not have mutual coupling between lines or branches. The second method uses the primitive branch admittance matrix and the bus incidence matrix. The second method is applicable to networks that have mutual coupling between lines or brances.

A. Networks Without Mutual Coupling

We use the following steps to calculate the bus admittance matrix elements:

1. The diagonal entries of the Y_{Bus} matrix, Y_{ii}, are the sum of the primitive admittances of all lines and ties to the reference at Bus *i*.
2. The off-diagonal entries of the Y_{Bus} matrix, Y_{ij}, are the negatives of the admittances of lines between Buses *i* and *j*. If there is no line between Buses *i* and *j*, this entry is zero.

B. Networks With Mutual Coupling

We use the following steps to calculate the bus admittance matrix elements for networks with mutual coupling:

1. Form the primitive impedance matrix Z_p. This is a *b* x *b* matrix, where *b* is the number of network branches. The diagonal elements of the Z_p matrix are the primitive impedances of the network branches. The off-diagonal elements are typically zero, unless there is mutual coupling between branches.
2. Invert Z_p to obtain the primitive admittance matrix Y_p.
3. Build the bus incidence matrix A. This matrix defines the network branch connections and the direction of the branch currents. To build the bus incidence matrix A, we begin with an *n* x *b* array of zeroes, where *n* is the number of network buses and *b* is the number of network branches. We always take the positive direction of the branch current from the smaller bus number to the larger bus number. We then use the following rule to make nonzero entries for each column in rows corresponding to the two buses to which that branch is connected:

- $a_{pq} = +1$ if current in Branch q is leaving Bus p.
- $a_{pq} = -1$ if current in Branch q is entering Bus p.
- $a_{pq} = 0$ if Branch q is not connected to Bus p.
- a_{pq} are the elements of the bus incidence matrix where $p = 1 \ldots n$ and $q = 1 \ldots b$.

We use (1) to calculate the bus admittance matrix.

$$Y_{Bus} = A \bullet Y_p \bullet A^T \tag{1}$$

We then calculate the bus impedance matrix by inverting the bus admittance matrix.

$$Z_{Bus} = Y_{Bus}^{-1} \tag{2}$$

C. Example: Bus Impedance Matrix Formulation

Calculate the sequence network bus impedance matrices for the system shown in Fig. 5.

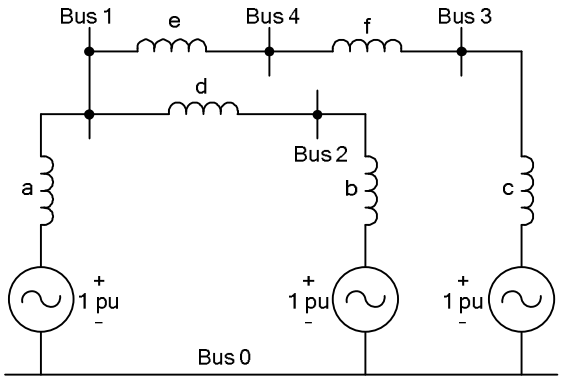

Fig. 5. Impedance diagram of a four-bus network

Table I lists the positive-sequence and the zero-sequence source, line, and mutual coupling impedance data.

TABLE I
SEQUENCE NETWORK IMPEDANCE DATA

Line	Starting Bus	Terminating Bus	Self Reactance		Mutual Coupling Reactance
			Pos. Seq.	Zero Seq.	
a	0	1	0.03	0.10	d – e = 0.10
b	0	2	0.10	0.50	d – f = 0.20
c	0	3	0.15	0.50	
d	1	2	0.12	0.40	
e	1	4	0.08	0.20	
f	3	4	0.10	0.30	

First, we use the method outlined in Section III-B to formulate the sequence network primitive impedance matrices. We assume the negative-sequence network primitive impedance matrix to be equal to the positive-sequence network primitive impedance matrix. The positive- and zero-sequence network primitive impedance matrices are as follows:

$$Z_{p(1)} = j\begin{pmatrix} 0.03 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0.1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0.15 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.12 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.08 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0.1 \end{pmatrix} \tag{3}$$

$$Z_{p(0)} = j\begin{pmatrix} 0.1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0.5 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0.5 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.4 & 0.1 & -0.2 \\ 0 & 0 & 0 & 0.1 & 0.2 & 0 \\ 0 & 0 & 0 & -0.2 & 0 & 0.3 \end{pmatrix} \tag{4}$$

Note that the primitive impedance matrices are of dimension 6 x 6 because there are six branches in the example network. In addition, the rows and columns of the primitive impedance matrices are in ascending alphabetical order of the network branches, in other words, a to f. Note also that the zero-sequence primitive impedance matrix has off-diagonal elements representing the mutual coupling of branches d-e and d-f. In the primitive zero-sequence impedance matrix the d-f mutual coupling impedance has a negative value because the positive direction of the currents in Branches d and f have opposite direction from each other.

The bus incidence matrix for the network in Fig. 5 is as follows:

$$A = \begin{pmatrix} -1 & 0 & 0 & 1 & 1 & 0 \\ 0 & -1 & 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & -1 & -1 \end{pmatrix} \tag{5}$$

We use (6) and (7) to calculate the positive-sequence bus impedance matrix:

$$Y_{Bus\_1} = A \bullet {Y_{p(1)}}^{-1} \bullet A^T \tag{6}$$

$$Z_{Bus\_1} = Z_{(1)} = Y_{Bus\_1}^{-1} \tag{7}$$

$$Z_{(1)} = j\begin{pmatrix} 0.02444 & 0.01111 & 0.01111 & 0.01852 \\ 0.01111 & 0.0596 & 0.00505 & 0.00842 \\ 0.01111 & 0.00505 & 0.08687 & 0.04478 \\ 0.01852 & 0.00842 & 0.04478 & 0.07464 \end{pmatrix} \tag{8}$$

Similarly, we use (9) and (10) to calculate the zero-sequence bus impedance matrix:

$$Y_{Bus\_0} = A \bullet {Y_{p(0)}}^{-1} \bullet A^T \tag{9}$$

$$Z_{Bus\_0} = Z_{(0)} = Y_{Bus\_0}^{-1} \tag{10}$$

$$Z_{(0)} = j\begin{pmatrix} 0.08617 & 0.03723 & 0.03191 & 0.06596 \\ 0.03723 & 0.20745 & 0.10638 & 0.05319 \\ 0.03191 & 0.10638 & 0.23404 & 0.11702 \\ 0.06596 & 0.05319 & 0.11702 & 0.20851 \end{pmatrix} \tag{11}$$

IV. Simultaneous Fault Calculations Using Two-Port Network Theory

Some of the most difficult problems in the solution of faulted networks are those that involve two or more simultaneous faults. Simultaneous faults do not occur very often in power system networks. However, when they occur, they can cause relay misoperations. Understanding relay behavior during simultaneous faults requires a good knowledge of symmetrical components and short-circuit calculations.

Before we further analyze simultaneous faults, we will briefly review the theory of two-port networks. In our brief treatment of two-port networks, we intend only to cover the parts necessary for studying complex network faults and operating conditions. References [9] and [10] are excellent resources on this subject.

A. Two-Port Networks

A two-port network has two pairs of terminals, as shown in Fig. 6. In a two-port network the current that leaves one terminal (the bottom terminal) must enter the other terminal (the top terminal). This is not a restriction on the network itself, but on the external connections made to the network. This current requirement must always be preserved no matter how complicated the connections are among a group of two-port networks. We often guarantee this by placing 1:1 isolation transformers on the ports before making any external connections.

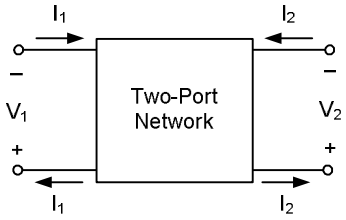

Fig. 6. A two-port network

Passive two-port networks are typically specified in terms of the network parameters showing the relationship between pairs of variables, as listed below:

- Impedance parameters *Z*:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{12}$$

- Admittance parameters *Y*:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{13}$$

- Hybrid parameters H:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \tag{14}$$

We will not discuss the remaining two-port network parameters, such as the inverse hybrid parameters, transmission parameters, and inverse transmission parameters, because we will not be using them in studying simultaneous faults.

To obtain the two-port impedance parameters of a passive network, we inject current I_1 = 1 pu at Port 1 with I_2 = 0 and measure the voltages at Ports 1 and 2. Next, we inject current I_2 = 1 pu at Port 2 with I_1 = 0 and measure the voltages at Ports 1 and 2. The impedance parameters are sometimes called the open circuit *Z* parameters. From these two tests, we obtain the two-port impedance parameters as shown below:

$$Z_{11} = (V_1/I_1)_{I_{2=0}}, Z_{21} = (V_2/I_1)_{I_{2=0}} \text{ and}$$

$$Z_{22} = (V_2/I_2)_{I_{1=0}}, Z_{12} = (V_1/I_2)_{I_{1=0}}$$

The two-port impedance parameters above are the two-port Thevenin equivalent impedances. In general, the two-port Thevenin equivalent impedance is given by (15):

$$Z^{TH} = \begin{bmatrix} U_{i-j}^{i-j} & U_{k-m}^{i-j} \\ U_{i-j}^{k-m} & U_{k-m}^{k-m} \end{bmatrix} = \begin{bmatrix} Z_{i-j}^{i-j} & Z_{k-m}^{i-j} \\ Z_{i-j}^{k-m} & Z_{k-m}^{k-m} \end{bmatrix} \tag{15}$$

where:

$$U_{i-j}^{k-m} = e_i^{k-m} - e_j^{k-m} = Z_{i-j}^{k-m} \tag{16}$$

and

$$Z_{i-j}^{k-m} = Z_{ik} - Z_{im} - Z_{jk} + Z_{jm} \tag{17}$$

The term e_i^{k-m} represents the voltage at Node *i* when 1 pu current is injected between Nodes *k* and *m*, and the term e_j^{k-m} represents the voltage at Node *j* when 1 pu current is injected between Nodes *k* and *m*. The term $U_{i-j}^{k-m} = e_i^{k-m} - e_j^{k-m}$ is the voltage difference between Nodes *i* and *j* when 1 pu current is injected between Nodes *k* and *m*. The *Z* terms in (15), (16), and (17) represent the respective bus impedance matrix elements. In general, the bus impedance matrix element Z_{ik} represents the voltage measured at Node *i* when 1 pu current is injected at Node *k*.

Note that if Nodes *j* and *m* are 0, representing the reference bus, we have the result shown in (18).

$$U_{i-0}^{k-0} = e_i^{k-0} = Z_{ik} \tag{18}$$

B. Example: Calculation of the Two-Port Z Parameters

Calculate the positive- and zero-sequence two-port Z parameters of the network in Fig. 5 for Ports S = {(1-0), (4-0)}.

The two-port positive-sequence impedance parameters are as given in (19), which uses the corresponding elements from the positive-sequence bus impedance matrix (8):

$$Z_{(1)}^{TH} = \begin{bmatrix} U_{1-0}^{1-0} & U_{4-0}^{1-0} \\ U_{1-0}^{4-0} & U_{4-0}^{4-0} \end{bmatrix} = \begin{bmatrix} Z_{11(1)} & Z_{41(1)} \\ Z_{14(1)} & Z_{44(1)} \end{bmatrix} \tag{19}$$

$$Z_{(1)}^{TH} = \mathrm{j}\begin{bmatrix} 0.02444 & 0.01852 \\ 0.01852 & 0.07464 \end{bmatrix}$$

Similarly, the zero-sequence impedance parameters are given in (20), which uses the corresponding elements from the zero-sequence bus impedance matrix (11):

$$Z_{(0)}^{TH} = \begin{bmatrix} U_{1-0}^{1-0} & U_{4-0}^{1-0} \\ U_{1-0}^{4-0} & U_{4-0}^{4-0} \end{bmatrix} = \begin{bmatrix} Z_{11(0)} & Z_{41(0)} \\ Z_{14(0)} & Z_{44(0)} \end{bmatrix} \quad (20)$$

$$Z_{(0)}^{TH} = \mathrm{j}\begin{bmatrix} 0.08617 & 0.06596 \\ 0.06596 & 0.20851 \end{bmatrix}$$

C. Two-Port Y-Equivalent Sequence Networks

The two-port Y-equivalent sequence networks are very useful for studying simultaneous faults that occur in different parts of the network. We can use the two-port Y-equivalent sequence networks to calculate the fault currents at intermediate points along a transmission line. We could also study complex series unbalances such as the one resulting from a three-phase transformer bank consisting of dissimilar single-phase units.

Fig. 7 shows the positive-sequence two-port Y-equivalent network for Ports *i* and *j*. $E_{i(1)}$ and $E_{j(1)}$ are the prefault positive-sequence voltages of ports i and j.

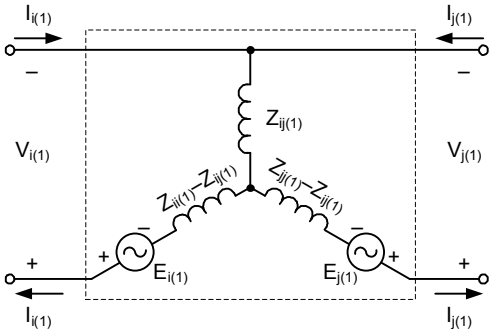

Fig. 7. Positive-sequence two-port Y-equivalent network

Remove the independent sources from the positive-sequence network to draw the two-port Y-equivalent negative-sequence network. Fig. 8 shows the negative-sequence two-port Y-equivalent network for Ports *i* and *j*.

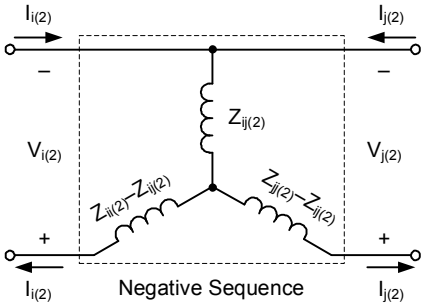

Fig. 8. Negative-sequence two-port Y-equivalent network

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The zero-sequence two-port Y-equivalent network is shown in Fig. 9.

Note that the positive-sequence network is an active two-port network because it contains independent sources, while the negative- and zero-sequence networks are passive two-port networks.

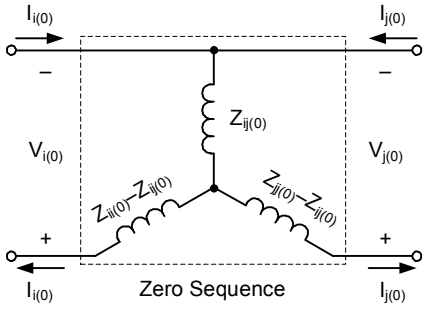

Fig. 9. Zero-sequence two-port Y-equivalent network

We derive the two-port Y-equivalent sequence networks from the two-port Z^{TH} sequence equivalents. Several methods are available for obtaining the two-port Y-equivalent sequence networks. So far, we have discussed using the elements of the bus impedance matrix to obtain the two-port parameters. There are other methods for accomplishing the same result; see the appendix in [11].

Sometimes we want to find a two-port Y-equivalent network and at the same time retain one branch, for example a transmission line, between two buses. We accomplish this by first removing the line from the network before formulating the sequence network bus impedance matrices.

V. Connecting Sequence Networks for Simultaneous Faults

Simultaneous faults are faults that occur simultaneously at one network location or at two or more different network locations. We consider both shunt and series faults in this paper. A shunt fault is an unbalance between phases or between phase(s) and ground (for example, phase-to-phase or a phase-to-ground fault). A series fault is an unbalance in the line impedances; it does not involve the ground or any interconnection between phases (for example, an open-phase condition resulting from a single-phase trip).

When two faults occur simultaneously at Ports *i* and *j*, there are three cases of interest:

1. A shunt fault at Port *i* and a shunt fault at Port *j*.
2. A shunt fault at Port *i* and a series fault at Port *j*.
3. A series fault at Port *i* and a series fault at Port *j*.

The case of a series fault at Port *i* and a shunt fault at Port *j* is identical to Case 2, so we will not discuss it further.

A. Simultaneous Fault Connection of Sequence Networks

We will discuss three different two-port sequence network connections: the series-series (Z-type faults), the parallel-parallel (Y-type faults), and the series-parallel (H-type faults) connections. The interconnections between the two-port sequence networks help us form more complicated networks that allow us to study complex network faults and operating conditions.

1) Series-Series Connection (Z-Type Faults)

We use the series-series connection of the two-port sequence networks to study the following fault types:

1. A single-phase-to-ground fault at Port *i* and a single-phase-to-ground fault at Port *j*.
2. A single-phase-to-ground fault at Port *i* and two open phases at Port *j*.

3. Two open phases at Port *i* and a single-phase-to-ground fault at Port *j*.
4. Two open phases at Port *i* and two open phases at Port *j*.

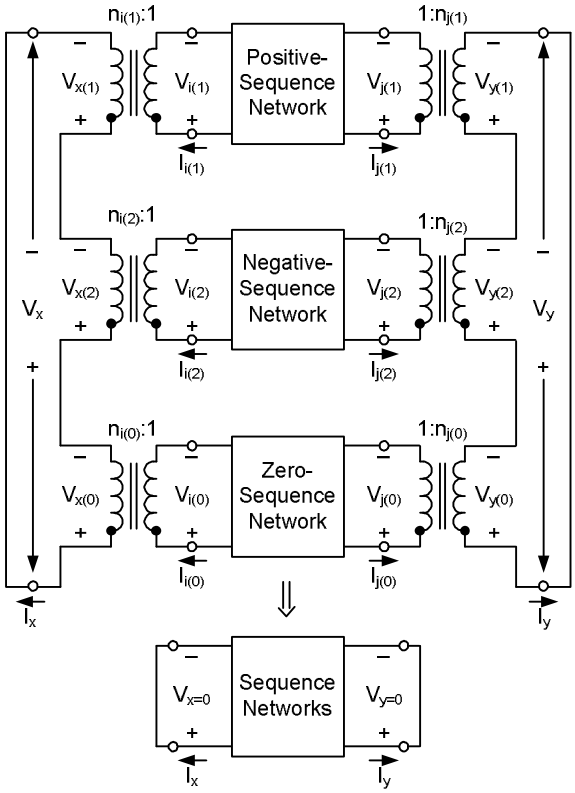

Fig. 10. Sequence network connection for simultaneous Z-type faults

Fig. 10 shows the series-series (Z-type faults) two-port sequence network interconnection.

The sequence networks in Fig. 10, indicated by square boxes, represent the two-port Y-equivalent networks (dashed squares) of Fig. 7, Fig. 8, and Fig. 9.

We use (21) to calculate Port *i* and Port *j* positive-sequence voltages (see Fig. 7):

$$\begin{bmatrix} V_{i(1)} \\ V_{j(1)} \end{bmatrix} = \begin{bmatrix} E_{i(1)} \\ E_{j(1)} \end{bmatrix} - \begin{bmatrix} Z_{ii(1)} & Z_{ij(1)} \\ Z_{ji(1)} & Z_{jj(1)} \end{bmatrix} \begin{bmatrix} I_{i(1)} \\ I_{j(1)} \end{bmatrix} \tag{21}$$

From Fig. 10, we can also write (22) and (23), where $k = 0, 1, 2$:

$$n_{i(k)} = V_{x(k)}/V_{i(k)} = I_x/I_{i(k)} \tag{22}$$

$$n_{j(k)} = V_{y(k)}/V_{j(k)} = I_y/I_{j(k)} \tag{23}$$

Premultiplying (21) by $\begin{bmatrix} n_{i(1)} & 0 \\ 0 & n_{j(1)} \end{bmatrix}$, results in (24):

$$\begin{bmatrix} V_{x(1)} \\ V_{y(1)} \end{bmatrix} = \begin{bmatrix} n_{i(1)} \bullet E_{i(1)} \\ n_{j(1)} \bullet E_{j(1)} \end{bmatrix} - \begin{bmatrix} Z_{ii(1)} & \frac{n_{i(1)} \bullet Z_{ij(1)}}{n_{j(1)}} \\ \frac{n_{j(1)} \bullet Z_{ji(1)}}{n_{i(1)}} & Z_{jj(1)} \end{bmatrix} \begin{bmatrix} I_x \\ I_y \end{bmatrix} \tag{24}$$

Similarly, we use (25) to calculate Port *i* and Port *j* negative-sequence voltages.

$$\begin{bmatrix} V_{x(2)} \\ V_{y(2)} \end{bmatrix} = - \begin{bmatrix} Z_{ii(2)} & \frac{n_{i(2)} \bullet Z_{ij(2)}}{n_{j(2)}} \\ \frac{n_{j(2)} \bullet Z_{ji(2)}}{n_{i(2)}} & Z_{jj(2)} \end{bmatrix} \begin{bmatrix} I_x \\ I_y \end{bmatrix} \tag{25}$$

Since $n_{i(0)} = n_{j(0)} = 1$, we use (26) to calculate Port *i* and Port *j* zero-sequence voltages.

$$\begin{bmatrix} V_{x(0)} \\ V_{y(0)} \end{bmatrix} = - \begin{bmatrix} Z_{ii(0)} & \frac{n_{i(0)} \bullet Z_{ij(0)}}{n_{j(0)}} \\ \frac{n_{j(0)} \bullet Z_{ji(0)}}{n_{i(0)}} & Z_{jj(0)} \end{bmatrix} \begin{bmatrix} I_x \\ I_y \end{bmatrix} \tag{26}$$

The final result is in (27).

$$\begin{bmatrix} V_{x(0)} \\ V_{y(0)} \end{bmatrix} = - \begin{bmatrix} Z_{ii(0)} & Z_{ij(0)} \\ Z_{ji(0)} & Z_{jj(0)} \end{bmatrix} \begin{bmatrix} I_x \\ I_y \end{bmatrix} \tag{27}$$

From Fig. 10, we observe that:

$$\begin{bmatrix} V_x \\ V_y \end{bmatrix} = \begin{bmatrix} V_{x(1)} \\ V_{y(1)} \end{bmatrix} + \begin{bmatrix} V_{x(2)} \\ V_{y(2)} \end{bmatrix} + \begin{bmatrix} V_{x(0)} \\ V_{y(0)} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{28}$$

Performing the addition in (28) and substituting (24), (25), and (26), we get the result in (29):

$$\begin{bmatrix} V_x \\ V_y \end{bmatrix} = \begin{bmatrix} n_{i(1)} \bullet E_{i(1)} \\ n_{j(1)} \bullet E_{j(1)} \end{bmatrix} - \begin{bmatrix} Z_{ii} & Z_{ij} \\ Z_{ji} & Z_{jj} \end{bmatrix} \begin{bmatrix} I_x \\ I_y \end{bmatrix} \tag{29}$$

where:

$$Z_{ii} = Z_{ii(1)} + Z_{ii(2)} + Z_{ii(0)} \tag{30}$$

$$Z_{ij} = (n_{i(1)}/n_{j(1)}) \bullet Z_{ij(1)} + (n_{i(2)}/n_{j(2)}) \bullet Z_{ij(2)} + Z_{ij(0)} \tag{31}$$

$$Z_{ji} = (n_{j(1)}/n_{i(1)}) \bullet Z_{ji(1)} + (n_{j(2)}/n_{i(2)}) \bullet Z_{ji(2)} + Z_{ji(0)} \tag{32}$$

$$Z_{jj} = Z_{jj(1)} + Z_{jj(2)} + Z_{jj(0)} \tag{33}$$

Note that when the two-port sequence networks are connected in series as in Fig. 10, the Z-parameter matrix of the resulting two-port network is equal to the sum of the Z-parameter matrices of the original two-port sequence networks.

We use (34) to calculate currents I_x and I_y:

$$\begin{bmatrix} I_x \\ I_y \end{bmatrix} = \begin{bmatrix} Z_{ii} & Z_{ij} \\ Z_{ji} & Z_{jj} \end{bmatrix}^{-1} \begin{bmatrix} n_{i(1)} \bullet E_{i(1)} \\ n_{j(1)} \bullet E_{j(1)} \end{bmatrix} \tag{34}$$

Note that for short-circuit calculations in an unloaded network, we have $E_{i(1)} = E_{j(1)} = 1$ pu. Knowing I_x and I_y, we can calculate the sequence network currents $I_{i(k)}$ and $I_{j(k)}$, where $k = 0, 1, 2$. We then calculate the two-port injected sequence network currents. We calculate the sequence network bus voltage changes by multiplying the sequence network bus impedance matrices with the appropriate node injected current vectors. An example later in this section (V-B) illustrates this method.

2) Parallel-Parallel Connection (Y-Type Faults)

The parallel-parallel connection of the two-port sequence networks is necessary for studying the following fault types:

1. A double-phase-to-ground fault at Port *i* and a double-phase-to-ground fault at Port *j*.
2. A double-phase-to-ground fault at Port *i* and one open phase at Port *j*.
3. One open phase at Port *i* and a double-phase-to-ground fault at Port *j*.
4. One open phase at Port *i* and one open phase at Port *j*.

Fig. 11 shows the parallel-parallel (Y-type faults) two-port sequence network interconnection.

For parallel-parallel sequence network connections, we work with the two-port admittance parameters (Y-parameters). We calculate the Y-parameters by inverting the two-port sequence network impedance parameters (Z-parameters).

We use (35) to calculate Port *i* and Port *j* positive-sequence currents:

$$\begin{bmatrix} I_{i(1)} \\ I_{j(1)} \end{bmatrix} = \begin{bmatrix} I_{si(1)} \\ I_{sj(1)} \end{bmatrix} - \begin{bmatrix} Y_{ii(1)} & Y_{ij(1)} \\ Y_{ji(1)} & Y_{jj(1)} \end{bmatrix} \begin{bmatrix} V_{i(1)} \\ V_{j(1)} \end{bmatrix} \tag{35}$$

From Fig. 11, we can also write (36) and (37), where $k = 0, 1, 2$:

$$n_{i(k)} = V_{x(k)}/V_{i(k)} = I_x/I_{i(k)} \tag{36}$$

$$n_{j(k)} = V_{y(k)}/V_{j(k)} = I_y/I_{j(k)} \tag{37}$$

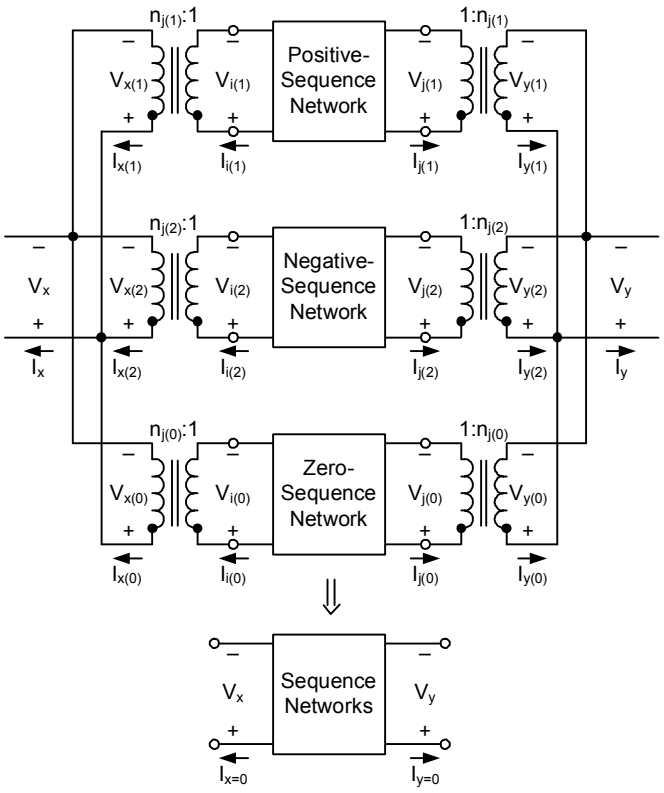

Fig. 11. Sequence network connection for simultaneous Y-type faults

Premultiplying (35) by $\begin{bmatrix} n_{i(1)} & 0 \\ 0 & n_{j(1)} \end{bmatrix}$, results in (38).

$$\begin{bmatrix} I_{x(1)} \\ I_{y(1)} \end{bmatrix} = \begin{bmatrix} n_{i(1)} \bullet I_{si(1)} \\ n_{j(1)} \bullet I_{sj(1)} \end{bmatrix} - \begin{bmatrix} Y_{ii(1)} & \frac{n_{i(1)} \bullet Y_{ij(1)}}{n_{j(1)}} \\ \frac{n_{j(1)} \bullet Y_{ji(1)}}{n_{i(1)}} & Y_{jj(1)} \end{bmatrix} \begin{bmatrix} V_x \\ V_y \end{bmatrix} \tag{38}$$

Similarly, we use (39) to calculate Port *i* and Port *j* negative-sequence currents.

$$\begin{bmatrix} I_{x(2)} \\ I_{y(2)} \end{bmatrix} = - \begin{bmatrix} Y_{ii(2)} & \frac{n_{i(2)} \bullet Y_{ij(2)}}{n_{j(2)}} \\ \frac{n_{j(2)} \bullet Y_{ji(2)}}{n_{i(2)}} & Y_{jj(2)} \end{bmatrix} \begin{bmatrix} V_x \\ V_y \end{bmatrix} \tag{39}$$

Since $n_{i(0)} = n_{j(0)} = 1$, we use (40) to calculate Port *i* and Port *j* zero-sequence currents:

$$\begin{bmatrix} I_{x(0)} \\ I_{y(0)} \end{bmatrix} = - \begin{bmatrix} Z_{ii(0)} & \frac{n_{i(0)} \bullet Z_{ij(0)}}{n_{j(0)}} \\ \frac{n_{j(0)} \bullet Z_{ji(0)}}{n_{i(0)}} & Z_{jj(0)} \end{bmatrix} \begin{bmatrix} V_x \\ V_y \end{bmatrix} = - \begin{bmatrix} Z_{ii(0)} & Z_{ij(0)} \\ Z_{ji(0)} & Z_{jj(0)} \end{bmatrix} \begin{bmatrix} V_x \\ V_y \end{bmatrix} \tag{40}$$

From Fig. 11, we observe that:

$$\begin{bmatrix} I_x \\ I_y \end{bmatrix} = \begin{bmatrix} I_{x(1)} \\ I_{y(1)} \end{bmatrix} + \begin{bmatrix} I_{x(2)} \\ I_{y(2)} \end{bmatrix} + \begin{bmatrix} I_{x(0)} \\ I_{y(0)} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{41}$$

Performing the addition indicated in (41) and substituting (38), (39), and (40), we get the result in (42):

$$\begin{bmatrix} I_x \\ I_y \end{bmatrix} = \begin{bmatrix} n_{i(1)} \bullet I_{si(1)} \\ n_{j(1)} \bullet I_{sj(1)} \end{bmatrix} - \begin{bmatrix} Y_{ii} & Y_{ij} \\ Y_{ji} & Y_{jj} \end{bmatrix} \begin{bmatrix} V_x \\ V_y \end{bmatrix} \tag{42}$$

where:

$$Y_{ii} = Y_{ii(1)} + Y_{ii(2)} + Y_{ii(0)} \tag{43}$$

$$Y_{ij} = (n_{i(1)}/n_{j(1)}) \bullet Y_{ij(1)} + (n_{i(2)}/n_{j(2)}) \bullet Y_{ij(2)} + Y_{ij(0)} \tag{44}$$

$$Y_{ji} = (n_{j(1)}/n_{i(1)}) \bullet Y_{ji(1)} + (n_{j(2)}/n_{i(2)}) \bullet Y_{ji(2)} + Y_{ji(0)} \tag{45}$$

$$Y_{jj} = Y_{jj(1)} + Y_{jj(2)} + Y_{jj(0)} \tag{46}$$

Note that when the two-port sequence networks are connected in parallel as in Fig. 11, the Y-parameter matrix of the resulting two-port network is equal to the sum of the Y-parameter matrices of the original two-port sequence networks.

We use (47) to calculate voltages V_x and V_y:

$$\begin{bmatrix} V_x \\ V_y \end{bmatrix} = \begin{bmatrix} Y_{ii} & Y_{ij} \\ Y_{ji} & Y_{jj} \end{bmatrix}^{-1} \begin{bmatrix} n_{i(1)} \bullet I_{si(1)} \\ n_{j(1)} \bullet I_{sj(1)} \end{bmatrix} \tag{47}$$

There is a relationship among the different two-port network parameters. We can calculate one set of two-port network parameters from another known set of two-port network parameters [10]. For example, to calculate the Y-parameters needed for a parallel-parallel connection, we invert the two-port Z-parameter matrix.

3) Series-Parallel Connection (H-Type Faults)

We use the series-parallel connection of the two-port sequence networks to study the following type of faults:

1. A single-phase-to-ground fault at Port *i* and a double-phase-to-ground fault at Port *j*.
2. A single-phase-to-ground fault at Port *i* and one phase open at Port *j*.
3. Two open phases at Port *i* and a double-phase-to-ground fault at Port *j*.
4. Two open phases at Port *i* and one open phases at Port *j*.

Fig. 12 shows the series-parallel connection of the two-port sequence networks.

We use the same connection also to study parallel-series faults by reversing the left and right port definitions. We use

(48) to calculate the hybrid parameter matrices (H-parameters) from the two-port Z-parameter matrices [10]:

$$[H_{(k)}] = \begin{bmatrix} \frac{\det Z_{(k)}}{Z_{jj(k)}} & \frac{Z_{ij(k)}}{Z_{jj(k)}} \\ -\frac{Z_{ji(k)}}{Z_{jj(k)}} & \frac{1}{Z_{jj(k)}} \end{bmatrix} \quad (48)$$

where:

k = 0, 1, 2 representing the zero-, positive-, and negative-sequence networks, respectively.

$\det Z_{(k)}$ = the determinant of matrix $Z_{(k)}$.

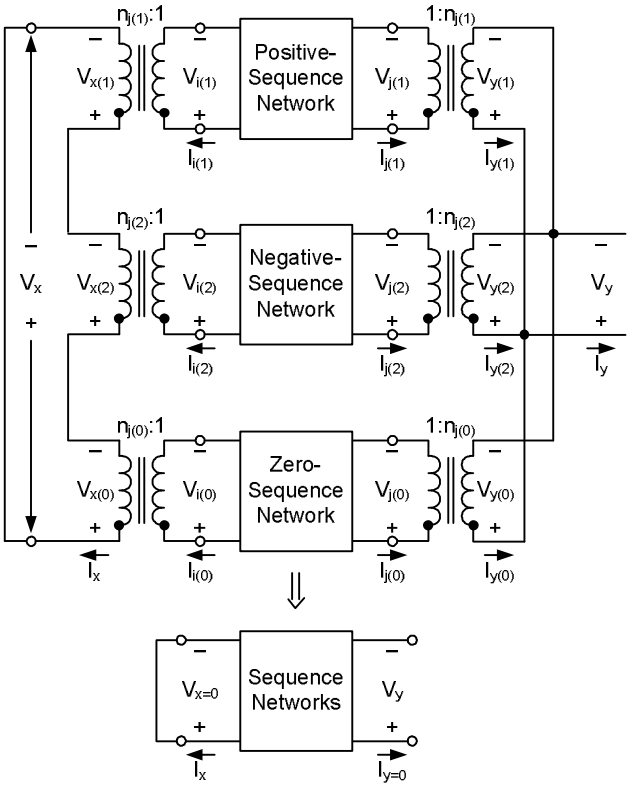

Fig. 12. Sequence network connection for simultaneous H-type faults

When the two-port sequence networks are connected in series-parallel, as shown in Fig. 12, the H-parameter matrix of the resulting two-port network is equal to the sum of the H-parameter matrices of the original two-port sequence networks. We calculate the H-parameter matrix of the resulting two-port network by following the steps we used in the series-series and parallel-parallel connections. Refer to [8] and [9] for more detailed analysis and derivation of H-parameters.

The sequence network voltages and currents in Fig. 10, Fig. 11, and Fig. 12 between the isolation transformers are all referenced to A-phase of the power system. The connections on the other side of the isolation transformers represent the boundary conditions for the series or shunt unbalance of the particular phases involved. The isolation transformer ratios are all 1:1 and may include a phase shift equal to $a = e^{j120}$ or $a^2 = e^{j240}$. Table II shows the appropriate isolation transformer ratios for different types of shunt and series faults.

TABLE II
ISOLATION TRANSFORMER RATIOS

Fault Type	Zero Seq.	Pos. Seq.	Neg. Seq.
A-Gnd	1	1	1
B-Gnd	1	a^2	a
C-Gnd	1	a	a^2
B-C-Gnd	1	1	1
C-A-Gnd	1	a^2	a
A-B-Gnd	1	a	a^2
A-Phase Open	1	1	1
B-Phase open	1	a^2	a
C-Phase Open	1	a	a^2
B&C-Phases Open	1	1	1
C&A-Phases Open	1	a^2	a
A&B-Phases Open	1	a	a^2

B. Example: Simultaneous Line-to-Ground Faults

Calculate the two-port network sequence currents and the total fault currents for the network in Fig. 5 for a B-phase-to-ground fault at Bus 2 and a C-phase-to-ground fault at Bus 4. Table III lists the source voltage magnitudes and angles.

TABLE III
SOURCE DATA

Source	Magnitude in pu	Angle in Degrees
Bus 1	1.1	30
Bus 2	1.0	0.0
Bus 3	1.0	0.0

First we calculate the two-port sequence impedance parameters following the procedure in Section IV-B. The two-port sequence impedance parameters are extracted from the sequence bus impedance matrices as shown in (49):

$$Z_{(k)} = \begin{bmatrix} Z_{22(k)} & Z_{24(k)} \\ Z_{42(k)} & Z_{44(k)} \end{bmatrix} \quad (49)$$

where k = 0, 1, 2 represent the zero-, positive-, and negative-sequence networks, respectively.

The two-port negative-sequence impedance parameters are identical to the two-port positive-sequence impedance parameters as shown in (50):

$$Z_{(1)} = Z_{(2)} = \begin{bmatrix} Z_{22(1)} & Z_{24(1)} \\ Z_{42(1)} & Z_{44(1)} \end{bmatrix} = j \begin{bmatrix} 0.05960 & 0.00842 \\ 0.00842 & 0.07464 \end{bmatrix} \quad (50)$$

We use (51) to calculate the two-port zero-sequence impedance parameters:

$$Z_{(0)} = \begin{bmatrix} Z_{22(0)} & Z_{24(0)} \\ Z_{42(0)} & Z_{44(0)} \end{bmatrix} = j \begin{bmatrix} 0.20745 & 0.05319 \\ 0.05319 & 0.20851 \end{bmatrix} \quad (51)$$

Because we are considering two shunt faults (Z-type faults), we need to use the series-series connection of the sequence networks shown in Fig. 10. The boundary conditions at Port *x* in Fig. 10 for a B-phase-to-ground fault are according to (52) and (53):

$$I_a = 0,\ I_c = 0, \text{and } V_b = 0 \quad (52)$$

$$V_x = V_b = V_{b0} + V_{b1} + V_{b2} = V_{a0} + a^2 \bullet V_{a1} + a \bullet V_{a2} \quad (53)$$

All quantities in the sequence networks between the isolation transformers in Fig. 10 are referred to A-phase. Therefore, the two-port (Port *i*, left side of Fig. 10) isolation transformer ratios are as in (54):

$$n_{2(0)} = 1,\ n_{2(1)} = a^2, \text{ and } n_{2(2)} = a \quad (54)$$

Similarly, the boundary conditions at Port *y* for a C-phase-to-ground fault are according to (55) and (56):

$$I_a = 0,\ I_b = 0, \text{and } V_c = 0 \quad (55)$$

$$V_x = V_c = V_{c0} + V_{c1} + V_{c2} = V_{a0} + a \bullet V_{a1} + a^2 \bullet V_{a2} \quad (56)$$

Therefore, the Port 4 (Port *j*, right side of Fig. 10) isolation transformer ratios are as in (57):

$$n_{4(0)} = 1,\ n_{4(1)} = a, \text{ and } n_{4(2)} = a^2 \quad (57)$$

The resulting two-port equivalent impedance parameter matrix is derived from the addition of the two-port sequence network impedance parameter matrices. Therefore, we can use (30), (31), (32) and (33) to obtain (58), (59), (60), and (61):

$$Z_{22} = Z_{22(1)} + Z_{22(2)} + Z_{22(0)} = j0.32665 \quad (58)$$

$$Z_{24} = \left(\frac{n_{2(1)}}{n_{4(1)}}\right) \bullet Z_{24(1)} + \left(\frac{n_{2(2)}}{n_{4(2)}}\right) \bullet Z_{24(2)} + Z_{24(0)}$$
$$Z_{24} = a \bullet Z_{24(1)} + a^2 \bullet Z_{24(2)} + Z_{24(0)} = j0.04477 \quad (59)$$

$$Z_{42} = \left(\frac{n_{4(1)}}{n_{2(1)}}\right) \bullet Z_{42(1)} + \left(\frac{n_{4(2)}}{n_{2(2)}}\right) \bullet Z_{42(2)} + Z_{42(0)}$$
$$Z_{42} = a^2 \bullet Z_{42(1)} + a \bullet Z_{42(2)} + Z_{42(0)} = j0.04477 \quad (60)$$

$$Z_{44} = Z_{44(1)} + Z_{44(2)} + Z_{44(0)} = j0.35779 \quad (61)$$

The network prefault bus voltages of Fig. 5 are as follows:

$$\begin{bmatrix} E_{1(1)} \\ E_{2(1)} \\ E_{3(1)} \\ E_{4(1)} \end{bmatrix} = \begin{bmatrix} 1.061 \cdot e^{j25.0} \\ 1.003 \cdot e^{j11.7} \\ 1.003 \cdot e^{j11.7} \\ 1.028 \cdot e^{j19.3} \end{bmatrix}$$

We calculate the bus prefault voltages by first converting the voltage sources into current sources and then by multiplying the positive-sequence bus impedance matrix by the current injection vector. In this example, the current injection vector is of dimension 4 x 1, and only the Bus 4 current injection is zero.

Next, we use (62) to calculate the Port *x* and Port *y* currents:

$$\begin{bmatrix} I_x \\ I_y \end{bmatrix} = \begin{bmatrix} Z_{22} & Z_{24} \\ Z_{42} & Z_{44} \end{bmatrix}^{-1} \begin{bmatrix} n_{2(1)} \bullet E_{2(1)} \\ n_{4(1)} \bullet E_{4(1)} \end{bmatrix} \quad (62)$$

The prefault voltages at Bus 2 and Bus 4 are as follows:

$$E_{2(1)} = 0.98245 + j0.20370$$

$$E_{4(1)} = 0.97076 + j0.33951$$

Therefore, the Port *x* and Port *y* currents are as follows:

$$\begin{bmatrix} I_x \\ I_y \end{bmatrix} = \begin{bmatrix} -3.229 + j0.677 \\ 2.279 + j2.094 \end{bmatrix}$$

We calculate the Port 2 and Port 4 sequence currents in (63) and (64):

$$\begin{bmatrix} I_{2(0)} \\ I_{2(1)} \\ I_{2(2)} \end{bmatrix} = I_x \bullet \begin{bmatrix} 1/n_{2(0)} \\ 1/n_{2(1)} \\ 1/n_{2(2)} \end{bmatrix} = \begin{bmatrix} -3.229 + j0.677 \\ 1.028 - j3.135 \\ 2.201 + j2.458 \end{bmatrix} \quad (63)$$

$$\begin{bmatrix} I_{4(0)} \\ I_{4(1)} \\ I_{4(2)} \end{bmatrix} = I_y \bullet \begin{bmatrix} 1/n_{4(0)} \\ 1/n_{4(1)} \\ 1/n_{4(2)} \end{bmatrix} = \begin{bmatrix} 2.279 + j2.094 \\ 0.674 - j3.021 \\ -2.953 + j0.927 \end{bmatrix} \quad (64)$$

The total fault currents at Port 2 and Port 4 are as follows:

$$\begin{bmatrix} I_{a(2)} \\ I_{b(2)} \\ I_{c(2)} \end{bmatrix} = \begin{bmatrix} 0 \\ -9.687 + j2.03 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ 9.9 \bullet e^{j168.2} \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} I_{a(4)} \\ I_{b(4)} \\ I_{c(4)} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 6.838 + j6.281 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 9.3 \bullet e^{j42.6} \end{bmatrix}$$

C. Representing an Open Phase in Stability Studies

Stability programs represent the power system by a single-phase positive-sequence impedance network [12]. To simulate any unbalanced network conditions, we connect the equivalent negative-sequence and zero-sequence impedances at the appropriate point in the positive-sequence network.

In single-phase tripping applications, we clear single-phase-to-ground faults by opening only the faulted phase. While the faulted phase is open, the two healthy phases still transmit reduced power. The power system experiences a series unbalance that causes negative- and zero-sequence currents to flow in the network. It is beneficial to study how long the system can operate with one phase open, to allow self-extinction of the secondary arc before making a reclosing attempt, and whether the system will remain stable during the open phase condition.

Such studies require complex calculations to determine the equivalent impedance that will replace the line positive-sequence impedance in stability simulations. In most cases, planning engineers request the equivalent impedance for such studies from the protection department. For the open-phase condition, the general practice is to represent the line open in one end only, even though both ends of the line are open. A common approach is to insert an impedance value equal to the parallel combination of the negative- and zero-sequence impedances as seen from the open point in series with the positive-sequence line impedance.

Representing the open phase at one end of the line only is approximate, but sufficiently accurate for short lines because the shunt capacitance is relatively small. However, this approximate representation could result in a significant error in long transmission line applications [12]. The following example illustrates how to compute the equivalent impedance that replaces the positive-sequence impedance of a transmission line with an open phase in a stability study.

D. Example: Open-Phase Representation in Stability Studies

Calculate the equivalent impedance that must be inserted in the positive-sequence network in a stability study to represent the single-phase tripping of A-phase on Line 1 of the network in Fig. 13.

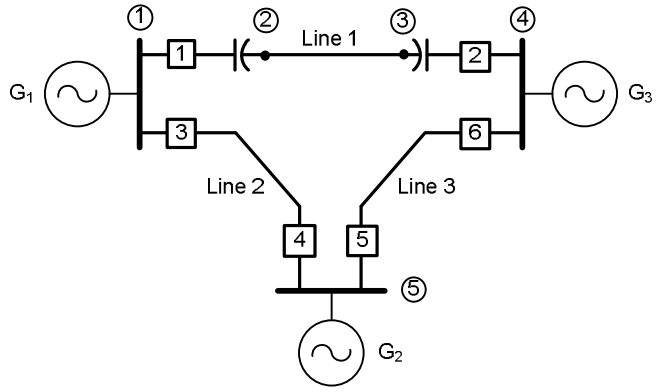

Fig. 13. Simple network to study A-phase open of Breakers 1 and 2

Fig. 14 depicts the impedance diagram of the network in Fig. 13 with A-phase of Breakers 1 and 2 open on Line 1. Table IV lists the positive- and zero-sequence impedances of each network element.

The impedance diagram in Fig. 14 consists of 10 elements (a through j) and seven nodes. The network in Fig. 13 consists of five nodes, one node for each bus and one node for each series capacitor. To model the Line 1 open-phase condition, we must create two additional nodes between Breakers 1 and 2 and the Line 1 series capacitors. In addition, in this example we model the shunt capacitance of Line 1, to demonstrate how to properly calculate the equivalent impedance as seen from Ports 1–6 and 4–7. This equivalent impedance represents the opening of A-phase of Breakers 1 and 2 during single-phase tripping. Lines 2 and 3 of the network in Fig. 13 are also series compensated, which the figure does not show; however, the series capacitance is reflected in the sequence impedances of Lines 2 and 3 in Table IV.

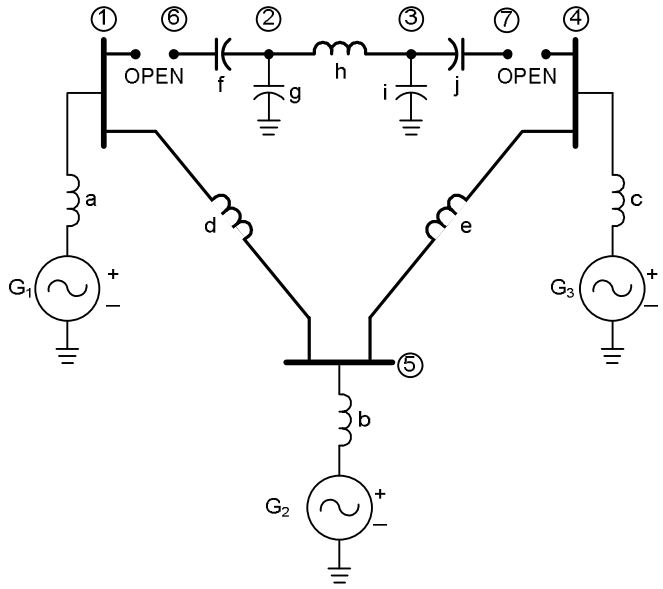

Fig. 14. Impedance diagram of the network shown in Fig. 13

TABLE IV
SEQUENCE NETWORK IMPEDANCE DATA OF FIG. 14

Element	Start Bus	End Bus	Self Reactance	
			Pos. Seq.	Zero Seq.
a	0	1	0.01095	0.01997
b	0	5	0.03229	0.28120
c	0	4	0.00523	0.00725
d	1	5	0.00606	0.04650
e	4	5	0.00323	0.03086
f	2	6	–0.01020	–0.01020
g	0	2	–0.78192	–1.10583
h	2	3	0.03087	0.09638
i	0	3	–0.78192	–1.10583
j	3	7	–0.01020	–0.01020

The positive- and zero-sequence bus impedance matrices for the impedance diagram in Fig. 14 are as follows:

$$Z_{(1)} = j\begin{pmatrix} 0.00589 & 0 & 0 & 0.00191 & 0.0031 & 0 & 0 \\ 0 & -0.38309 & -0.39883 & 0 & 0 & -0.38309 & -0.39883 \\ 0 & -0.39883 & -0.38309 & 0 & 0 & -0.39883 & -0.38309 \\ 0.00191 & 0 & 0 & 0.00383 & 0.00297 & 0 & 0 \\ 0.0031 & 0 & 0 & 0.00297 & 0.00481 & 0 & 0 \\ 0 & -0.38309 & -0.39883 & 0 & 0 & -0.39329 & -0.39883 \\ 0 & -0.39883 & -0.38309 & 0 & 0 & -0.39883 & -0.39329 \end{pmatrix}$$

$$Z_{(0)} = j\begin{pmatrix} 0.01598 & 0 & 0 & 0.00127 & 0.0067 & 0 & 0 \\ 0 & -0.52772 & -0.57811 & 0 & 0 & -0.52772 & -0.57811 \\ 0 & -0.57811 & -0.52772 & 0 & 0 & -0.57811 & -0.52772 \\ 0.00127 & 0 & 0 & 0.00668 & 0.00424 & 0 & 0 \\ 0.0067 & 0 & 0 & 0.00424 & 0.0223 & 0 & 0 \\ 0 & -0.52772 & -0.57811 & 0 & 0 & -0.53792 & -0.57811 \\ 0 & -0.57811 & -0.52772 & 0 & 0 & -0.57811 & -0.53792 \end{pmatrix}$$

The dimension of the bus incidence matrix of the impedance diagram in Fig. 14 is 7 x 10. The positive- and zero-sequence bus impedance matrices have dimension 7 x 7, and we can formulate these by using the same method we discussed earlier for the impedance diagram in Fig. 5. We assume the negative-sequence bus impedance matrix to be the same as the positive-sequence bus impedance matrix.

We use (65) and (66) to obtain the negative- and zero-sequence Thevenin equivalent impedances for Ports 1–6 and 4–7:

$$Z_{(2)}^{TH} = Z_{(1)}^{TH} = \begin{bmatrix} U_{1-6}^{1-6} & U_{4-7}^{1-6} \\ U_{1-6}^{4-7} & U_{4-7}^{4-7} \end{bmatrix} = \begin{bmatrix} Z_{11(1)} - Z_{16(1)} - Z_{61(1)} + Z_{66(1)} & Z_{41(1)} - Z_{46(1)} - Z_{71(1)} + Z_{76(1)} \\ Z_{14(1)} - Z_{17(1)} - Z_{64(1)} + Z_{67(1)} & Z_{44(1)} - Z_{47(1)} - Z_{74(1)} + Z_{77(1)} \end{bmatrix} \quad (65)$$

$$Z_{(2)}^{TH} = \mathrm{j}\begin{bmatrix} -0.387393 & -0.396919 \\ -0.396919 & -0.389453 \end{bmatrix}$$

$$Z_{(0)}^{TH} = \begin{bmatrix} U_{1-6}^{1-6} & U_{4-7}^{1-6} \\ U_{1-6}^{4-7} & U_{4-7}^{4-7} \end{bmatrix} = \begin{bmatrix} Z_{11(0)} - Z_{16(0)} - Z_{61(0)} + Z_{66(0)} & Z_{41(0)} - Z_{46(0)} - Z_{71(0)} + Z_{76(0)} \\ Z_{14(0)} - Z_{17(0)} - Z_{64(0)} + Z_{67(0)} & Z_{44(0)} - Z_{47(0)} - Z_{74(0)} + Z_{77(0)} \end{bmatrix} \quad (66)$$

$$Z_{(0)}^{TH} = \mathrm{j}\begin{bmatrix} -0.521936 & -0.576836 \\ -0.576836 & -0.531242 \end{bmatrix}$$

The sequence network connection for A-phase open at Port 1–6 and A-phase open at Port 4–7 is the connection for Y-type faults in Fig. 11. The ratio of all isolating transformers is 1:1 because we are studying an A-phase open condition in both ports. To represent the parallel connection of the negative- and zero-sequence networks, we sum the negative- and zero-sequence admittance matrices $Y_{(2)}^{TH}$ and $Y_{(0)}^{TH}$, which we obtain by taking the inverse of $Z_{(2)}^{TH}$and $Z_{(0)}^{TH}$. The result of the sum is the following:

$$Y^{TH02} = j\begin{bmatrix} -67.9353 & 69.8761 \\ 69.8761 & -67.4589 \end{bmatrix}$$

We invert Y^{TH02} to obtain the corresponding impedance matrix Z^{TH02}, which is shown below:

$$Z^{TH02} = j\begin{bmatrix} -0.224987 & -0.233049 \\ -0.233049 & -0.226576 \end{bmatrix}$$

We then combine Z^{TH02} with the positive-sequence two-port impedance parameters of Line 1 to obtain the equivalent impedance matrix. This matrix represents the equivalent line parameters that should be used in place of the positive-sequence impedance of Line 1 in stability studies.

To obtain the two-port parameters of Line 1, including the series capacitors, we use the method presented in Section III-C and the impedance diagram in Fig. 15. Note that the node numbers in Fig. 15 are not related to the node numbers in Fig. 14.

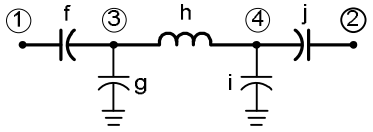

Fig. 15. Impedance diagram of Line 1 and the series capacitors

The bus incidence matrix for the impedance diagram in Fig. 15 is of dimension 4 x 5, and the corresponding bus impedance matrix is of dimension 4 x 4. The bus impedance matrix for the impedance diagram in Fig. 15 is as follows:

$$Z = j\begin{pmatrix} -0.3932871 & -0.3988329 & -3830871 & -0.3988329 \\ -0.3988329 & -0.3932871 & -0.3988329 & -0.3830871 \\ -0.3830871 & -0.3988329 & -0.3830871 & -0.3988329 \\ -0.3988329 & -0.3830871 & -0.3988329 & -0.3830871 \end{pmatrix}$$

We are interested only in the two-port (1-0 and 2-0) impedance parameters from this network that we calculate with (67):

$$Z^{TH1} = \begin{bmatrix} U_{1-0}^{1-0} & U_{2-0}^{1-0} \\ U_{1-0}^{2-0} & U_{2-0}^{2-0} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{21} \\ Z_{12} & Z_{22} \end{bmatrix} \quad (67)$$

$$= \mathrm{j}\begin{bmatrix} -0.393287 & -0.398833 \\ -0.398833 & -0.393287 \end{bmatrix}$$

Next, we sum Z^{TH02} and Z^{TH1} to obtain the two-port equivalent impedance that will represent Line 1, the series capacitors, and the opening of A-phase of Breakers 1 and 2.

$$Z^{EQ\_1} = Z^{TH1} + Z^{TH02} = \mathrm{j}\begin{bmatrix} -0.618274 & -0.631882 \\ -0.631882 & -0.619863 \end{bmatrix} \quad (68)$$

Inverting Z^{EQ_1} gives us the positive-sequence admittance matrix Y^{EQ_1}:

$$Y^{EQ\_1} = \mathrm{j}\begin{bmatrix} -38.6703 & 39.4201 \\ 39.4201 & -38.5712 \end{bmatrix}$$

We can represent the network in Fig. 15 with a pi-equivalent circuit between Nodes 1 and 2 (or between Nodes 1 and 4 in Fig. 14), as in Fig. 16.

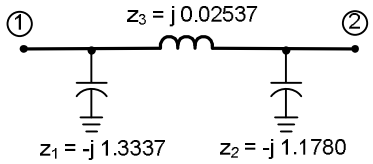

Fig. 16. Equivalent positive-sequence impedance parameters

In Fig. 16, primitive impedances z_1, z_2, and z_3 are the inverse of primitive admittance elements y_1, y_2, and y_3 that we derive from Y^{EQ_1} with (69), (70), and (71):

$$y_1 = Y_{11}^{EQ\_1} + Y_{12}^{EQ\_1} \quad (69)$$

$$y_2 = -Y_{12}^{EQ\_1} \quad (70)$$

$$y_3 = Y_{12}^{EQ\_1} + Y_{22}^{EQ\_1} \quad (71)$$

We can use a similar approach to study an A-phase open condition in each of two parallel transmission lines.

VI. Transformer Banks of Dissimilar Units

Large EHV transformer banks are typically composed of three single-phase units. If one of the single-phase transformers fails, the utility may use a spare transformer located in the same substation, or a mobile system spare to replace the failed transformer. In either case, the impedances of the spare transformer are most likely different from the impedances of the other two healthy transformer units.

When such a situation arises, should the operating department limit the transformer loading? The problem is that the tertiary winding rating is normally 30 to 35 percent of the main winding rating. A small zero-sequence current in the main windings may result in a large zero-sequence current in the tertiary windings, which could cause these windings to overheat. Protection engineers must verify that the transformer tertiary overcurrent protection will not operate improperly because of maximum allowed transformer loading. Therefore, it is imperative that we calculate the impact of the unbalance resulting from unequal transformer impedances.

The solution technique we describe is based on the symmetrical component method of circuit representation. The symmetrical component equivalent circuit of a balanced transformer bank, consisting of three identical single-phase units, is uncoupled. This means that a balanced loading condition causes current to flow only in the positive-sequence network. When the high-low, high-tertiary, and low-tertiary reactances of one of the transformer units are different from the reactances of the other two transformers, the symmetrical component networks are mutually coupled.

Fig. 17 shows the T-equivalent circuits of the three single-phase transformer banks.

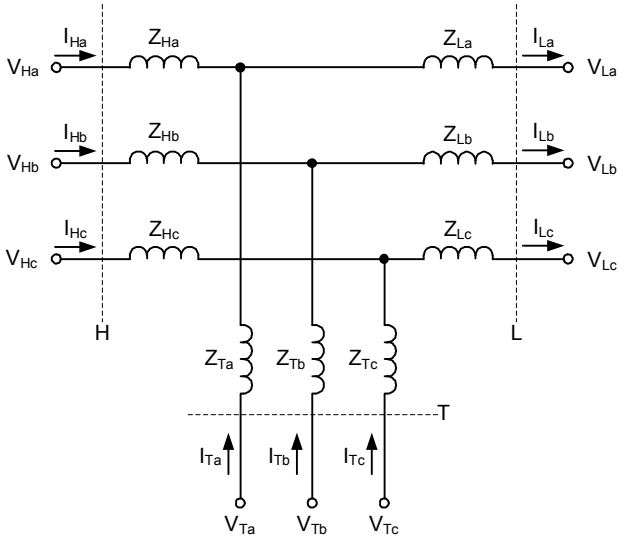

Fig. 17. T-equivalent circuit of three single-phase transformers

Let us assume that the A-phase transformer has different impedances from those of the transformers of the other two phases. We use the impedances of A-phase and B-phase transformers to redraw the T-equivalent circuits of Fig. 17, in Fig. 18.

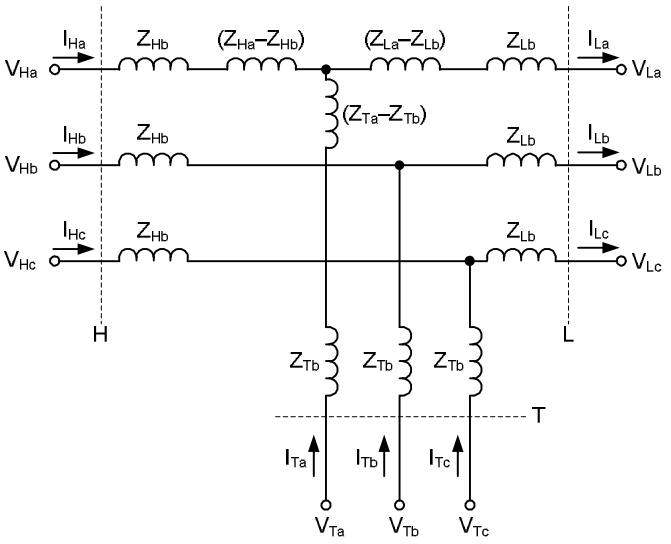

Fig. 18. T-equivalent circuits with series unbalances in the A-phase transformer

We replace the high, low, and tertiary impedances of the C-phase in Fig. 17 with those of the B-phase transformer, because those units are identical. We replace the A-phase high, low, and tertiary impedances with the B-phase impedances and the difference impedance terms $Z_{Ha}–Z_{Hb}$, $Z_{La}–Z_{Lb}$, and $Z_{Ta}–Z_{Tb}$.

The goal now is to find a symmetrical component circuit representation of the three-phase unbalanced circuit in Fig. 18. The symmetrical component transformation for the voltages and currents in the respective transformer windings are as follows:

$$\begin{bmatrix} V_{Ha0} \\ V_{Ha1} \\ V_{Ha2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_{Ha} \\ V_{Hb} \\ V_{Hc} \end{bmatrix} \quad (72)$$

$$\begin{bmatrix} V_{La0} \\ V_{La1} \\ V_{La2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_{La} \\ V_{Lb} \\ V_{Lc} \end{bmatrix} \quad (73)$$

$$\begin{bmatrix} V_{Ta0} \\ V_{Ta1} \\ V_{Ta2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_{Ta} \\ V_{Tb} \\ V_{Tc} \end{bmatrix} \quad (74)$$

$$\begin{bmatrix} I_{Ha0} \\ I_{Ha1} \\ I_{Ha2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_{Ha} \\ I_{Hb} \\ I_{Hc} \end{bmatrix} \quad (75)$$

$$\begin{bmatrix} I_{La0} \\ I_{La1} \\ I_{La2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \quad (76)$$

$$\begin{bmatrix} I_{Ta0} \\ I_{Ta1} \\ I_{Ta2} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_{Ta} \\ I_{Tb} \\ I_{Tc} \end{bmatrix} \quad (77)$$

Now, let us use voltages and currents as designated in Fig. 18 to compute the voltage drop from the high- to the low-voltage winding.

$$V_{Ha} = V_{La} + I_{Ha}Z_{Hb} + I_{Ha}(Z_{Ha} - Z_{Hb}) + I_{La}(Z_{La} - Z_{Lb}) + I_{La}Z_{Lb} \quad (78)$$

$$V_{Hb} = V_{Lb} + I_{Hb}Z_{Hb} + I_{Lb}Z_{Lb} \quad (79)$$

$$V_{Hc} = V_{Lc} + I_{Hc}Z_{Hb} + I_{Lc}Z_{Lb} \quad (80)$$

Using (72), (73), (75), (76) and (78), (79), (80), we compute the sequence network voltage difference from the high- to the low-voltage windings as in (81), (82), and (83):

$$V_{Ha0} - V_{La0} = I_{Ha0}Z_{Hb} + (I_{Ha0} + I_{Ha1} + I_{Ha2})\left(\frac{Z_{Ha} - Z_{Hb}}{3}\right) + (I_{La0} + I_{La1} + I_{La2})\left(\frac{Z_{La} - Z_{Lb}}{3}\right) + I_{La0}Z_{Lb} \quad (81)$$

$$V_{Ha1} - V_{La1} = I_{Ha1}Z_{Hb} + (I_{Ha0} + I_{Ha1} + I_{Ha2})\left(\frac{Z_{Ha} - Z_{Hb}}{3}\right) + (I_{La0} + I_{La1} + I_{La2})\left(\frac{Z_{La} - Z_{Lb}}{3}\right) + I_{La1}Z_{Lb} \quad (82)$$

$$V_{Ha2} - V_{La2} = I_{Ha2}Z_{Hb} + (I_{Ha0} + I_{Ha1} + I_{Ha2}) \bullet \left(\frac{Z_{Ha} - Z_{Hb}}{3}\right) + (I_{La0} + I_{La1} + I_{La2}) \bullet \left(\frac{Z_{La} - Z_{Lb}}{3}\right) + I_{La2}Z_{Lb} \quad (83)$$

Next, we use voltages and currents as designated in Fig. 18 to compute the voltage drop from the tertiary to the low-voltage winding.

$$V_{Ta} = V_{La} + I_{Ta}Z_{Tb} + I_{Ta}(Z_{Ta} - Z_{Tb}) + I_{La}(Z_{La} - Z_{Lb}) + I_{La}Z_{Lb} \quad (84)$$

$$V_{Tb} = V_{Lb} + I_{Tb}Z_{Tb} + I_{Lb}Z_{Lb} \quad (85)$$

$$V_{Tc} = V_{Lc} + I_{Tc}Z_{Tb} + I_{Lc}Z_{Lb} \quad (86)$$

Using (84), (85), (86) and (73), (74), (76), (77), we compute the sequence network voltage difference from the tertiary to the low-voltage windings as in (87), (88), and (89):

$$V_{Ta0} - V_{La0} = I_{Ta0}Z_{Tb} + (I_{Ta0} + I_{Ta1} + I_{Ta2}) \bullet \left(\frac{Z_{Ta} - Z_{Tb}}{3}\right) + (I_{La0} + I_{La1} + I_{La2}) \bullet \left(\frac{Z_{La} - Z_{Lb}}{3}\right) + I_{La0}Z_{Lb} \quad (87)$$

$$V_{Ta1} - V_{La1} = I_{Ta1}Z_{tb} + (I_{Ta0} + I_{Ta1} + I_{Ta2}) \bullet \left(\frac{Z_{Ta} - Z_{Tb}}{3}\right) + (I_{La0} + I_{La1} + I_{La2}) \bullet \left(\frac{Z_{La} - Z_{Lb}}{3}\right) + I_{La1}Z_{Lb} \quad (88)$$

$$V_{Ta2} - V_{La2} = I_{Ta2}Z_{tb} + (I_{Ta0} + I_{Ta1} + I_{ta2}) \bullet \left(\frac{Z_{Ta} - Z_{Tb}}{3}\right) + (I_{La0} + I_{La1} + I_{La2}) \bullet \left(\frac{Z_{La} - Z_{Lb}}{3}\right) + I_{La2}Z_{Lb} \quad (89)$$

Fig. 19 shows the symmetrical component representation of the unbalanced transformer bank, assuming that the tertiary winding is unloaded and that it is connected in delta.

The next example illustrates application of the equivalent circuit to calculate the zero-sequence current circulating in the tertiary winding because of the series unbalances resulting from the unequal impedances of the A-phase transformer bank.

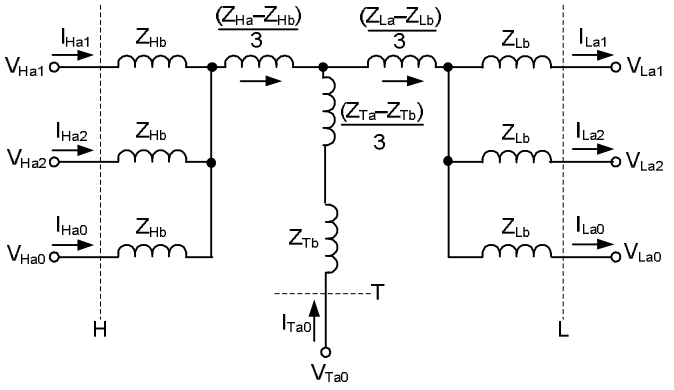

Fig. 19. Symmetrical component circuit representation for an unbalanced transformer bank

A. Example: Dissimilar Transformer Banks

Calculate the circulating current in the tertiary winding of an unbalanced three-phase transformer bank consisting of three single-phase units. We assume the 525/230/13.8 kV transformer bank to be loaded on the 230 kV side at 100 percent of the A-phase transformer. The 525 kV system and transformer impedances are as follows:

525 kV Source Impedances:

Z_{S1} = j 0.00587 p.u. at 100 MVA and 525 kV base

Z_{S0} = j 0.00472 p.u. at 100 MVA and 525 kV base

Transformer impedances:

A-Phase: 150/200/280 MVA (32.0/42.67/53.34 MVA)
$Z_{H\text{-}L}$ = 7.31 % at 150.0 MVA
$Z_{H\text{-}T}$ = 7.07 % at 33.6 MVA
$Z_{L\text{-}T}$ = 4.59 % at 33.6 MVA

B-Phase: 2000/267/334 MVA (33.6/44.8/56 MVA)
$Z_{H\text{-}L}$ = 6.64 % at 200.0 MVA
$Z_{H\text{-}T}$ = 7.62 % at 44.8 MVA
$Z_{L\text{-}T}$ = 5.36 % at 44.8 MVA

C-Phase: 2000/267/334 MVA (33.6/44.8/56 MVA)
$Z_{H\text{-}L}$ = 6.64 % at 200.0 MVA
$Z_{H\text{-}T}$ = 7.62 % at 44.8 MVA
$Z_{L\text{-}T}$ = 5.36 % at 44.8 MVA

230 kV side load: 112 ohms/phase

Fig. 20 shows the sequence network connections for the previous example data. We use a 100 MVA base in calculating all impedances.

From Fig. 20, we can calculate the zero-sequence current flowing in the tertiary winding:

I_{Ta0} = 0.00334 + j 0.02259 p.u. or 374.7 A

We confirmed the magnitude of the circulating current in the tertiary winding by modeling the same unbalanced bank in ATP.

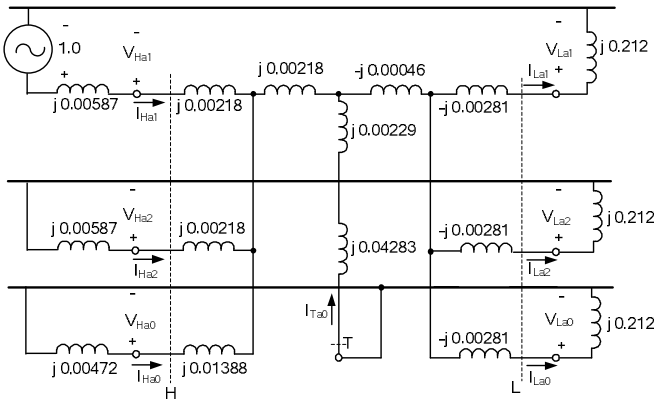

Fig. 20. Complete sequence network connection for unbalanced transformer

VII. Conclusions

1. Short-circuit calculations are extremely important in the application and settings of protective relays. Protection engineers should be well versed in the analysis of faulted power systems so that they can make appropriate relay settings and analyze complex system operations.
2. The two-port theory is very useful for the analysis of simultaneous faults and complex operating conditions in power systems.
3. To accurately represent the effect of single-phase open conditions in stability studies, the equivalent impedance parameters that replace the line under study should be calculated considering the line open at both ends instead of open at one end only.
4. We derived the symmetrical component equivalent for an unbalanced transformer bank in this paper. The magnitude of the circulating current in the tertiary winding of the unbalanced transformer bank agrees very closely with the results from a more sophisticated modeling approach that uses ATP.

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IX. Biography

Demetrios A. Tziouvaras has a B.S.E.E. and M.S.E.E. from the University of New Mexico and Santa Clara University, respectively. He is an IEEE Senior member and a member of the Power Engineering Society, the Power System Relaying Committee, and CIGRE. From 1980 until 1998 he was with Pacific Gas and Electric Co. where he held various protection engineering positions including Principal Protection Engineer responsible for relay settings, analysis of relay operations and system disturbances, protection design standards, application of new technologies, and substation automation. He joined Schweitzer Engineering Laboratories, Inc. in 1998 and currently holds the position of Senior Research Engineer. His main interests are protection of power systems, power system transients, and digital relaying. He holds four patents and has several pending in the area of power system protection. He is the author and co-author of more than 50 IEEE and Protective Relay Conference papers. Currently, he is the convener of CIGRE WG B5.15 on "Modern Distance Protection Functions and Applications" and is a member of several IEEE PSRC and CIGRE working groups.