Protection of Fuseless Capacitor Banks Using Digital Relays

Malkiat S. Dhillon
Pacific Gas and Electric Co.

Demetrios A. Tziouvaras
Schweitzer Engineering Laboratories, Inc.

Presented at the
26th Annual Western Protective Relay Conference
Spokane, Washington
October 26–28, 1999

PROTECTION OF FUSELESS CAPACITOR BANKS USING DIGITAL RELAYS

Malkiat S. Dhillon
Pacific Gas and Electric Co.
San Francisco, CA USA

Demetrios A. Tziouvaras
Schweitzer Engineering Laboratories, Inc.
Pullman, WA USA

ABSTRACT

This paper reviews existing shunt capacitor bank technologies, discusses the advantages and disadvantages of the different capacitor technologies, and details the reasons why Pacific Gas and Electric Co. (PG&E) is implementing fuseless capacitor technology on all new shunt capacitor designs in their 115 and 230 kV system.

In addition, we discuss the protection of shunt capacitors banks and present innovative techniques for fuseless shunt capacitor banks using digital relays to provide complete and economical protection. These techniques eliminate the need for high voltage transducers for voltage differential protection, provide more sensitive protection, and make the relay settings insensitive to system voltage variations, as well as to capacitance variation caused by temperature. This paper also discusses the additional benefits of applying multi-function digital relays, including ease of identification of shorted capacitor cans, reduced maintenance costs, and simpler implementation of monitoring and control.

INTRODUCTION

Many power system components in a network consume large amounts of reactive power. For example, transmission line shunt reactors, and other industrial and commercial loads need reactive power. Reactive current supports the magnetic fields in motors and transformers. Supporting both real and reactive power with the system generation requires increased generation and transmission capacity, because it increases losses in the network. Shunt-connected capacitors or synchronous condensers near the load centers are another way to generate reactive power. Shunt capacitors have the advantage of providing reactive power close to the load centers, minimizing the distance between power generation and consumption, and do not have the maintenance problems associated with synchronous condensers. Controlling capacitance in a transmission or distribution network could be the simplest and most economical way of maintaining system voltage, minimizing system losses, and maximizing system capability.

PG&E operates one of the largest transmission and distribution networks in the US, with a maximum peak demand of about 23 Gigawatts. PG&E has a large number of shunt capacitor installations in their network and plan additional installations to meet reactive power demands. Inadequate reactive support was a significant cause of the summer 1996 major disturbances in the Western Systems Coordinating Council (WSCC) area. Voltage collapse remains a great concern to PG&E and many other area utilities. Studies conducted by engineers associated with the WSCC after these disturbances mandated additional reactive support at critical load centers. In 1998, PG&E installed 425.6 MVARs of shunt capacitors in one 115 kV and two 230 kV substations. These recent shunt capacitor bank installations, and planned future installations, required a new look at the overall design of shunt capacitor banks, especially at protecting and controlling shunt capacitor banks while minimizing installation and operating costs. PG&E charged a team of substation and protection engineers, construction, operating, and maintenance personnel with evaluating shunt capacitor bank technologies and recommending a design standard for current and future shunt capacitor installation projects.

This paper discusses the different shunt capacitor bank technologies, their advantages and disadvantages, and the reasons why PG&E selected the fuseless technology on all new installations in their 115 and 230 kV system. The paper also addresses the protection of fuseless capacitor bank design, using multifunction digital relays, and the economic and operating benefits of the design. In addition, we present innovative techniques that eliminate the need for high voltage transducers for voltage differential protection, and provide more sensitive protection. We discuss how these techniques make the relay settings insensitive to system voltage variations and to capacitance variation caused by temperature.

SHUNT CAPACITOR BANK TECHNOLOGIES

Before discussing the protection of capacitor units and banks, let us first should review the design differences between capacitor units manufactured today and those manufactured thirty years ago. Earlier generation capacitor units were manufactured using very refined kraft paper with a PCB impregnant. The kraft paper had many non-uniformities or flaws. Several layers of paper were used between the foil layers to avoid weak spots in the design. With this design, the stress levels were low but the dielectric losses were higher than that of today's capacitor can designs. High dielectric losses resulted in high hot spot temperatures. High temperatures accelerate deterioration of the capacitor dielectric strength. Failure of the dielectric material resulted in continued arcing, charring, and gas generation that swelled the capacitor cans and eventually ruptured the cases.

Today's capacitor units are built with polypropylene film (instead of kraft paper), and dielectric fluids with electrical characteristics superior to those of PCB. The polypropylene film is very thin, pure, and uniform, with exceptionally few design flaws. This latest design only requires two to three layers of film. While this increases the stress levels, , it reduces the dielectric losses which results in low hot spot temperatures. As a result of these changes, today's capacitor units do not age quickly. Swelling or case rupture is now very rare. Because film layers are thin and of high quality, element failures do not cause arcing and charring. Instead, the foil welds together.

Capacitor units for power system applications are built with dielectric polypropylene film, aluminum foil, and impregnant. Thin layers of dielectric film are wound between the aluminum foils, which act as the electrode. The major difference between units is in the internal design of the capacitor, i.e., the number of elements in parallel and in series, and in whether protection is for externally-fused, internally-fused, or fuseless capacitors. Capacitor elements in a unit are connected in a matrix. The electrical requirements of the capacitor unit determine the number of elements in parallel and in series. Similarly, bank requirements determine whether capacitor units are connected in-parallel or in-series. For example, bank capacitance fluctuations must be minimized in filter applications. Thus, designers should select a capacitor unit with many elements in parallel per group and many units in series within the capacitor bank. In addition, the design should have a capacitor unit with elements that are disconnected when they fail and do not short out the remaining elements in the group.

Capacitor Unit Designs

The three types of power capacitor designs listed below may affect selection of the protection scheme:

- Externally-fused power capacitors.
- Internally-fused power capacitors.
- Fuseless power capacitors.

Externally-Fused Power Capacitors

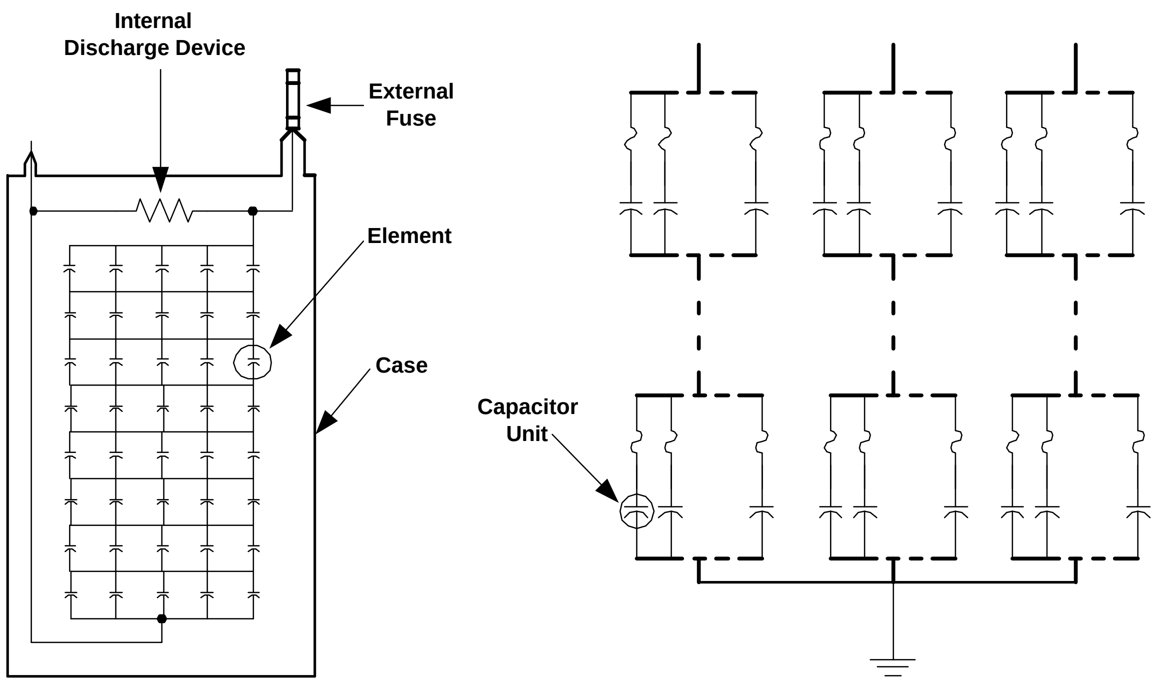
External fuses remove a failed capacitor unit to prevent case rapture and allow the rest of the capacitor bank to remain in operation. Earlier generations of capacitor units needed fuses because the PCB-soaked kraft paper made these units very vulnerable to case rupture. Although highly refined, the kraft paper had many flaws: many layers were needed between the electrodes to ensure a reasonably high level of insulation. In the event of a puncture, the cellulose of the kraft paper charred, the electrodes were kept separated, and a sustained arcing led to gassing and potential case rupture. Prompt isolation of the capacitor unit from the bank was an absolute requirement to avoid case rapture, and prevent PCB spills.

Present day capacitor units, built with polypropylene film, have fewer flaws and only two or three layers of film between the electrodes. In the event of a puncture, the film draws back and allows the electrodes to weld together instead of arcing. This design is less prone to generate gases and to cause case raptures. In addition, the external fuse does not melt with the additional current drawn by the unit. Thus, the capacitor unit stays in-service until additional failures of series elements cause fuses to operate.

Figure 1a shows the construction of an externally-fused capacitor unit. This design places many elements in series within the capacitor unit. Each series group consists of a few elements in parallel. An externally-fused capacitor bank, shown in Figure 1b, consists of many capacitor units in parallel within each series group, in order to stay within the output kVAR tolerances in the event of a unit failure under normal operating conditions.

Externally-fused capacitor banks have a perceived visual advantage since the failed unit is identified by the blown fuse. Detection of incipient faults and identification of partially failed units requires a complete capacitance measurement of all units. Intact fuses do not necessarily mean that the capacitor units are in perfect operating condition, nor does a failed fuse necessarily indicate that the capacitor unit has failed. In addition, when a fuse operates in a capacitor bank, the bank may have to be taken out-of-service to replace the fuse and prevent other capacitor units from failure caused by overvoltage and overstressing.

Pollution, corrosion, and fluctuating climatic conditions reduce the reliability of external fuses. These fuses must be checked and replaced periodically. This adds to operating costs and to bank unavailability. In addition, the bank connections are not isolated and animals climbing inside the bank can cause undesired flashovers and bank operations.



a. Externally-Fused Capacitor Unit **b. Externally-Fused Capacitor Bank**

Figure 1: Externally-Fused Power Capacitors

Internally-Fused Power Capacitors

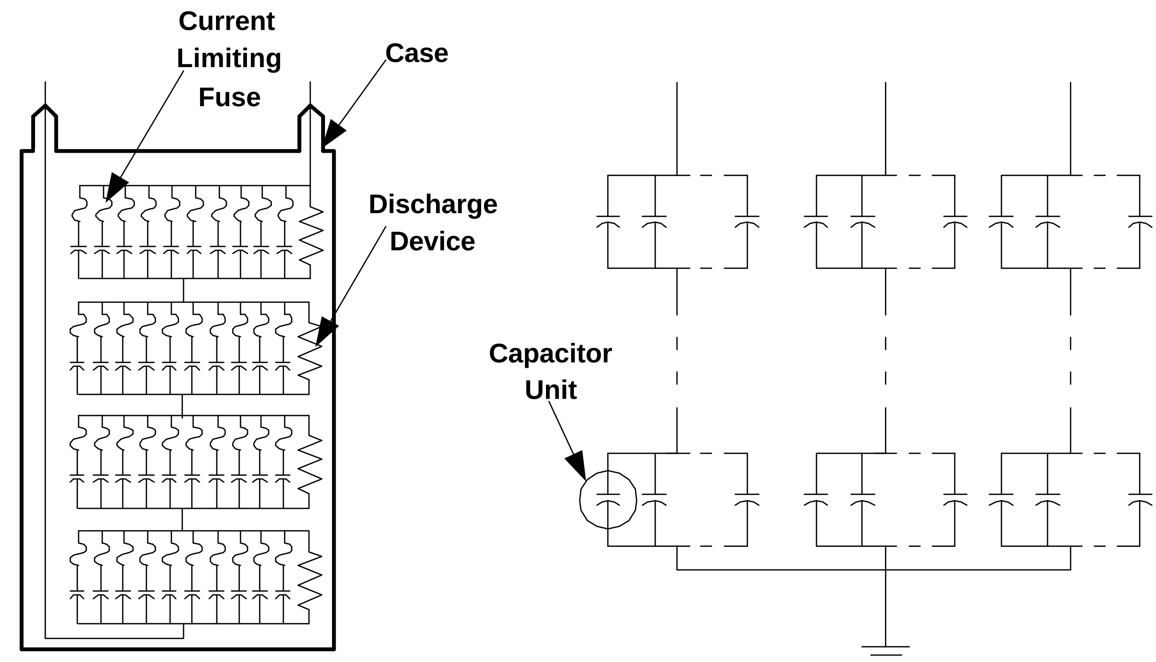
Internal fuses are current-limiting fuses intended to isolate failed capacitor unit elements in a capacitor unit and allow operation of the remaining elements within the unit. Figure 2a shows a design typical of an internally-fused capacitor unit. An element failure and subsequent isolation removes only a small part of the capacitor unit and allows the capacitor unit and bank to remain in service.

The design philosophy of internally-fused capacitor units places a large number of elements in parallel in each series group within a capacitor can. A failed element causes the fuse to melt and this, in turn, causes a small increase in the voltage across the parallel elements. Since the capacitor unit is designed to limit this voltage increase, the unit can be left in service indefinitely. Instantaneous disconnection of a failed element prevents the unit from being exposed to sustained arcing, minimizing the risk of capacitor-can rupture.

Some of the advantages of internally-fused capacitors are:

- There is no need for fuses, fuse rail assemblies, or insulators.
- Fuses operate properly without electrical clearances between units.
- The output of the capacitor unit is not limited by the type and size of external fuses, which results in a substantial reduction of the total number of cans required for a particular bank design.

- The bank design is very compact and contains very few live parts, making it very easy to cover and insulate the connections. This design reduces the exposure to faults from animals and increases the bank reliability and availability.



a. Internally-Fused Capacitor Unit **b: Internally-Fused Capacitor Bank**

Figure 2: Internally-Fused Power Capacitors

The design philosophy of internally-fused capacitor banks places many units in series within the bank, as shown in Figure 2b. This is the design of choice for filter bank applications where bank capacitance fluctuations must be minimized, because it allows the overall capacitance to remain within very small tolerances, even with several failed elements.

Fuseless Power Capacitors

Fuseless capacitor units eliminate capacitor fusing. The role played by fuses in previous generations of capacitor designs has become secondary because of the high quality insulating materials used in present day capacitors. The design philosophy of fuseless capacitor units, shown in Figure 3a, consists of a few elements in parallel and many in series. This design is similar to the one used for externally-fused capacitors. Figure 3b shows the design philosophy of a fuseless capacitor bank where the capacitor units are connected in series. Failure of an individual capacitor element leads to a very small voltage increase on the remaining series elements in that string. Because the small voltage increase is shared by all the series elements in the string, additional element failures in the string are unlikely.

The fuseless bank design has the same advantages as the internally-fused capacitor bank design. In addition, the fuseless design produces lower losses than the fused design since there are no I^2R losses associated with capacitor unit or capacitor can fuses.

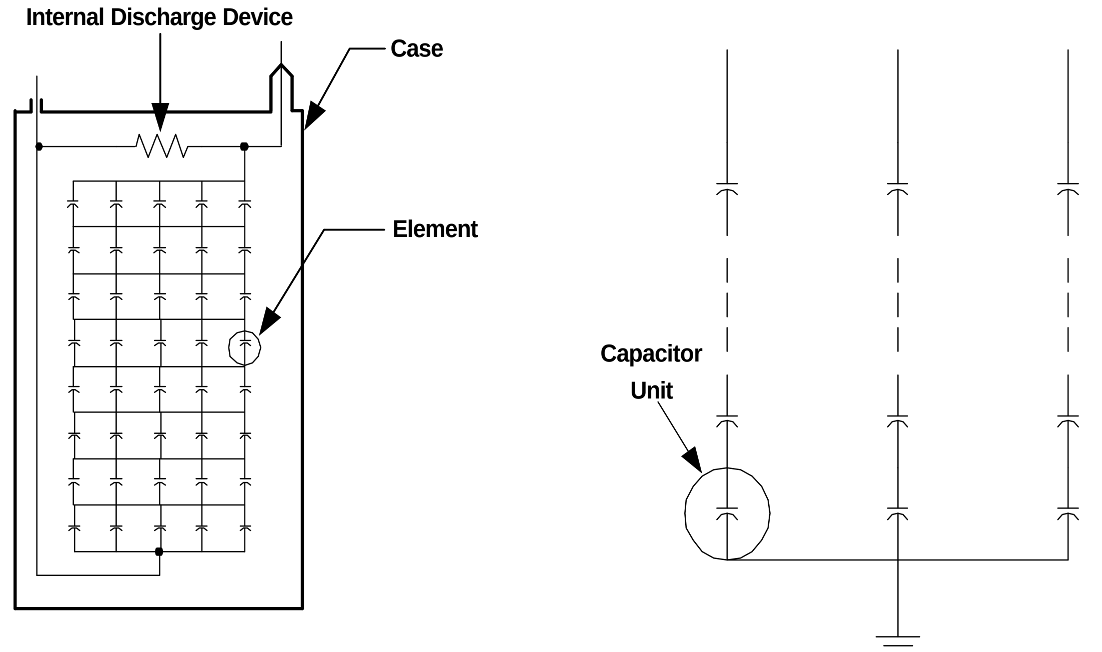


Figure 3a: Fuseless Capacitor Unit **Figure 3b: Fuseless Capacitor Bank**

Figure 3. Fuseless Capacitor Construction

Earlier PG&E shunt capacitor banks used the externally-fused design. Not only was maintenance of the fuses a problem, there were also extensive problems with the capacitor banks, can ruptures, bank tripping, unavailability, and PCB spills. The design team selecting new shunt capacitor bank designs considered all of these issues as well as the advantages of the fuseless design.

GENERAL PROTECTION CONSIDERATIONS

Protection of shunt capacitor banks requires an understanding of the capabilities and limitations of individual capacitor units, associated electrical equipment, and expected power system performance. Protection emphasis is placed in two areas: minimizing fault damage and avoiding false or nuisance bank operations.

The evolution in the internal design and materials of capacitor units has had major consequences on capacitor bank design and protection. Electrical arcing and case ruptures are no longer the major causes behind capacitor bank tripping. Most capacitor bank trips today are caused by animals climbing on the bank or by other causes such as contamination or inadvertent tripping due to human errors.

Capacitor Unit Capabilities and Limitations

IEEE Std 18-1992 [1] specifies the standard ratings for shunt power capacitors connected to transmission and distribution systems. Below are some of the ratings of shunt capacitor units from [1]. However, always consult the latest applicable IEEE and ANSI standards.

- Capacitor units shall not give less than 100 percent and no more than 115 percent of rated reactive power at rated sinusoidal voltage and frequency, measured at a 25^{o}C uniform case and internal temperature.

- Capacitors shall be capable of continuous operation provided that none of the following limitations are exceeded:

  - 110 percent of rated rms voltage, and a crest voltage of 1.2 x √2 of rated rms voltage, including harmonics but excluding transients.

  - 180 percent of rated rms current, including fundamental and harmonic currents.

  - 135 percent of rated reactive power (nameplate kVAR). This rating shall include the following factors and must not be exceeded by their combined effect:

    - Reactive power caused by voltage in excess of nameplate rating at fundamental frequency, but within the permissible voltage limitations.

    - Reactive power caused by harmonic voltages superimposed on the fundamental frequency.

    - Reactive power in excess of nameplate rating caused by manufacturing tolerances.

- Capacitor units rated above 600 Volts shall have an internal discharge device to reduce the residual voltage to 50 Volts or less in five minutes.

Capacitor Bank Components

Figure 4 shows a single line diagram of a PG&E fuseless capacitor design at a 230 kV substation. In this design, there are five capacitor bank steps, and each step is rated 83.52 MVAR. This station is located in the southernmost part of the Bay Area and serves very critical and sensitive loads. Capacitor bank availability cannot be compromised, especially during the summer months.

A number of power system and other components in Figure 4 deserve further discussion.

Each capacitor step has the following components:

- A synchronous (zero voltage) closing circuit breaker to reduce the transient inrush currents during bank energization, and to isolate the bank during system or bank problems.

- A reactor in series with the capacitor bank to reduce the transient inrush currents, and the high magnitude and high frequency transients during back-to-back switching.

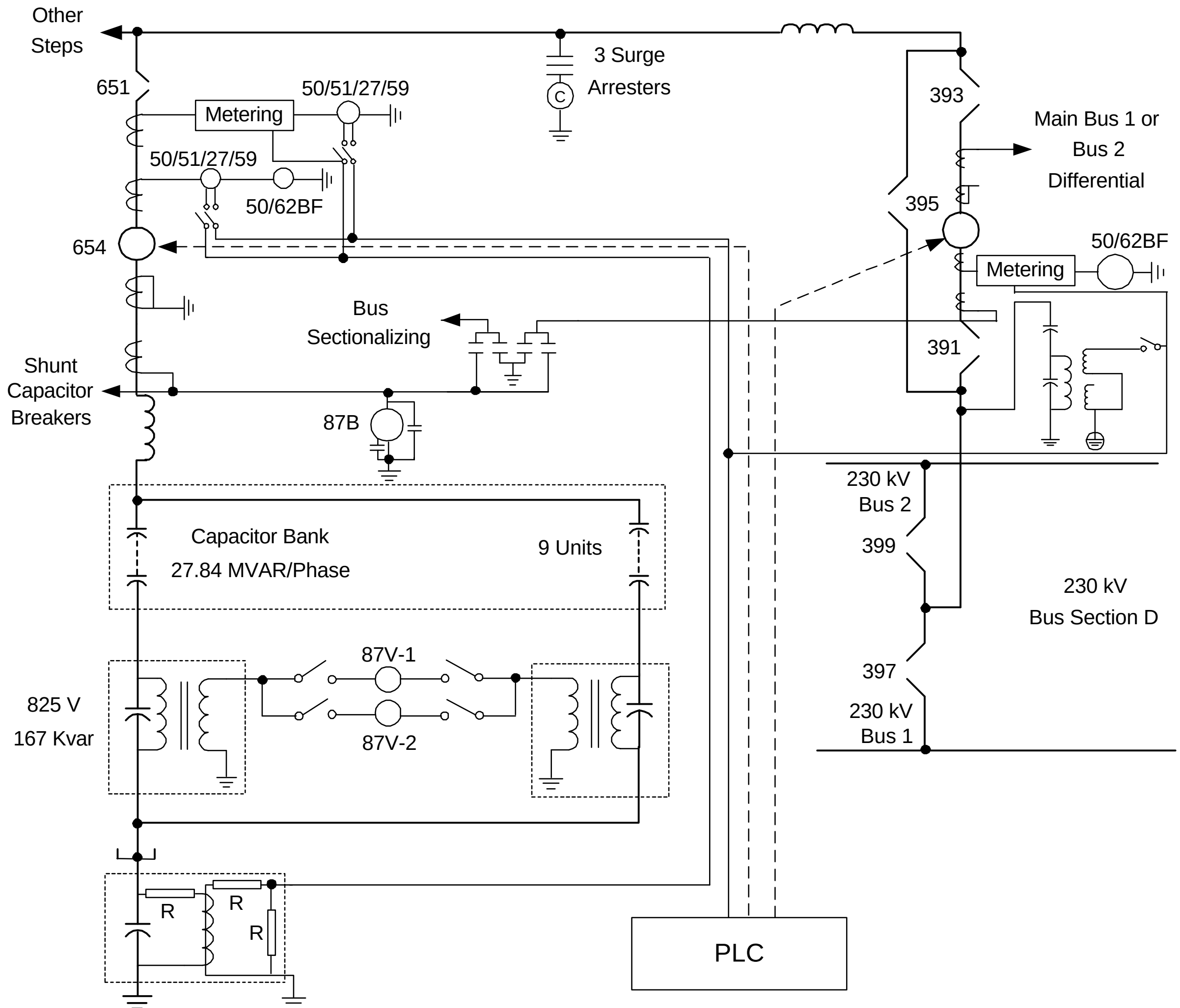


Figure 4: Single Line Diagram of a One-Step Fuseless Capacitor Bank Rated 83.52 MVAR

- Two halves of each phase, each half with a low voltage capacitor with a step-down voltage transformer providing inputs to a differentially connected numerical relay.
- A low voltage capacitor, a current transformer, and a resistive divider in the capacitor bank neutral provide input to a numerical relay for bank unbalance protection.
- A disconnect switch between the breaker and the bus isolates the capacitor step from the power system and permits a safe working clearance point for maintenance purposes.
- Three metal oxide surge arresters reduce voltage surges caused by capacitor switching or lightning and protect the substation equipment.
- A reactor in series with the main circuit breaker to reduce the inrush transients during capacitor energization, and the outrush transients during close-end line or bus faults in the vicinity of the substation.

- A main circuit breaker to provide backup tripping in the event of a failure of one of the capacitor bank breakers. The main breaker disconnect switches bypass the breaker during maintenance, and provide isolation from the power system for a safe working environment.

- All breakers are rated for switching capacitive currents and equipped with synchronous closing controls to reduce the transient overvoltages and overcurrents during capacitor bank switching.

- Numerical relays to provide protection for system faults, system abnormal conditions, and capacitor bank problems. The protection for this installation is discussed in more detail in later sections of the paper.

- A programmable logic controller (PLC) to provide automatic capacitor insertion and removal based on seasonal preprogrammed voltage levels. In addition, the PLC provides a way to balance the circuit breaker operations, control the energization sequences, and perform alarming, and some monitoring, functions.

- Electromagnetic transient program studies (EMTP) were performed to select the optimum values of inrush, outrush reactors, surge arresters, and breakers.

PROTECTION OF FUSELESS SHUNT CAPACITOR BANKS

This discussion focuses primarily on protection for fuseless shunt capacitor bank installations and the advantages that multifunction numerical relays add to this protection. Readers interested in discussion of all aspects of protection issues concerning shunt capacitor banks should consult the latest revision of ANSI/IEEE C37.99-1990, IEEE Guide for Protection of Shunt Capacitor Banks, reference [2].

Because shunt capacitor banks must be available during heavy load periods, the protection design should be reliable and secure, emphasizing both bank and system protection. The protection system should not trip the capacitor bank unnecessarily for system malfunctions, yet should protect the bank adequately even when some relays are unavailable because of failure or maintenance. If a capacitor unit fails, the protection system should remove the capacitor bank from the power system before it is severely damaged and before a system fault develops that could place additional stress on the power system.

Bank protection schemes clear faults within the capacitor bank itself. This protection includes schemes that disconnect a faulted capacitor unit or an element, isolate the bank in the event of a fault that may lead to a catastrophic failure, and alarm to indicate potential bank problems, alerting personnel to take action before a bank trip is necessary.

System protection schemes protect the capacitor bank from stresses imposed on the bank by the power system, and protect the power system and substation equipment from stresses caused during bank switching or normal operation. System protection may include schemes to limit overvoltages and excessive transient overcurrents. Protection schemes provide alarms and means to disconnect the entire bank and prevent abnormal system conditions from damaging the capacitors.

The shunt capacitor bank protection system must guard against the following faults or abnormalities:

- Continuous overvoltage in excess of 110 percent of rated rms capacitor voltage whether this is caused by capacitor unit failures or sustained system overvoltages.
- Overcurrents caused by individual capacitor unit failures or capacitor bus faults.
- Arc-over within the capacitor rack.
- Discharge currents from parallel capacitor units.
- Inrush currents caused by capacitor switching.

Use of conventional overcurrent and overvoltage principles, as well as unbalance and differential relaying principles, can solve many of these problems. Well-planned capacitor bank design can eliminate or minimize most of the problems.

Capacitor Bank Protection

Redundant numerical relays can provide capacitor bank protection with the following functions:

- Overvoltage protection.
- Undervoltage protection (power failure).
- Per-phase capacitor differential protection.
- Neutral unbalance overvoltage protection.

These functions provide protection for the following cases:

- The overvoltage function protects the capacitor against damaging sustained system overvoltages. In addition, it lowers system voltage by removing the capacitor bank from service.
- The undervoltage function prevents damaging transient overvoltages and other problems related to energizing a capacitor bank through a transformer without significant parallel load. This is accomplished by opening the capacitor breakers after five seconds in the event of a loss of bus voltage, a condition that indicates a 230 kV bus fault that was cleared or a system blackout.
- Faulted capacitor element or fault from a capacitor element to a case.
- Bushing failures or faulty connections in the capacitor unit.
- Fault in the capacitor bank other than the capacitor unit, i.e., arcing fault in the bank.
- Continuous overvoltage caused by faulted capacitor elements.
- Rack-to-rack flashovers in two series groups, if connections have not been insulated.

Figure 4 shows the design for the differentially-connected numerical relays. Each phase of a capacitor bank step is split in half. A small capacitor unit (167 kVARs, 825 Volts) near the neutral point of each split phase provides a voltage proportional to the capacitor string current to one of the differential relay inputs. A small step-down voltage transformer connects across this capacitor to reduce the voltage to a level consistent with the design of the numerical relay voltage inputs. This design accomplishes a number of desired goals.

The differential connections shown across the low voltage capacitors remove the need for capacitive voltage transformers (CVTs) on the high side of each step. Earlier PG&E designs used three CVTs on the capacitor side of the circuit breaker to provide voltage to one of the numerical relay differential inputs. The proposed design eliminated the need for three CVTs per capacitor step, resulting in substantial savings.

Another important benefit of the new design is the improvement in protecting capacitor banks from temperature-induced variations in capacitance. Because power capacitors and low voltage capacitors are designed differently, their temperature-induced capacitance variations are different. Designs using high voltage CVTs for one of the differential inputs could suffer from nuisance alarms, misoperations, and reduced sensitivity. In addition, the new design makes the voltage differential protection insensitive to system voltage variations. Table 1 shows the secondary differential voltage as seen by the differential relay, and the percent overvoltage seen by the remaining capacitor series elements, as a function of failed series elements. The alarm is set to operate for three failed capacitor series elements, and the differential trip threshold is set to operate for six failed series elements. The secondary differential voltage is computed using Equation 1.

$$\Delta V = |Vx| - k \bullet |Vy| \qquad \text{(Equation 1)}$$

Where $|Vx|$ and $|Vy|$ are the magnitudes of the secondary voltage inputs to the voltage differential relay. The k constant is set to balance the relay voltage inputs and null the differential voltage. This constant is near one and compensates for capacitance differences caused by manufacturing tolerances. You can compute a preliminary setting for constant k, but it must be adjusted in the field during capacitor bank installation and commissioning. You can also use this constant to compensate for the voltage difference that exists across the low voltage capacitors when the number of strings per phase is odd.

Because the secondary differential voltage computed by the relay is quite small, as shown in Table 1, it is important to apply a relay that has high resolution and accuracy.

Table 1: Percent Overvoltage and Differential Voltage as a Function of Failed Series Elements

Number of Failed Elements	1	2	**3**	4	5	**6**	7	8	9
Percent Overvoltage	1.41	2.86	**4.35**	5.88	7.46	**9.09**	10.77	12.50	14.29
Differential Voltage (Volts)	0.6	1.22	**1.85**	2.51	3.18	**3.87**	4.59	5.32	6.08

The differential connection in numerical relays also has operations and maintenance benefits. When voltage differential protection causes an operation of the capacitor bank, the new protection systems immediately notifies operations and maintenance personnel of the particular phase that caused the operation. The event report also helps them identify the string that has the failed unit or elements. This helps personnel focus on one particular area to find the problem, make necessary repairs, and return the bank to operation. Besides help with troubleshooting after an operation has taken place, event reports from numerical relays also provide personnel with invaluable information for the adjustments usually needed during the initial installation and commissioning period.

Figure 4 also shows the design for the unbalance neutral overvoltage protection. In this design, a small capacitor connects the bank neutral to ground. Any faults within a phase or any capacitor unit element failures cause zero-sequence current to flow through the bank neutral capacitor. A current transformer and a resistive divider help develop a voltage proportional to this zero-sequence current. A multifunction numerical relay detects this voltage unbalance and generates an alarm or a trip, depending on the level of unbalance.

This novel design approach to neutral voltage unbalance protection has two points of particular interest. First, this design eliminates the need for a special protective relay for capacitor bank neutral unbalance protection. Instead, the voltage input from the neutral capacitor resistive divider connects to the synchronism-check input of a multifunction digital relay that provides voltage elements with the needed range. Earlier PG&E designs used a separate solid-state relay for this function. Second, the neutral unbalance protection provides backup to the differential voltage scheme and, in addition, provides protection if a number of equal series elements fail in both halves of one phase. This condition cannot be detected by the differential voltage protection scheme.

Table 2 shows the neutral current and the secondary voltage applied to one of the numerical relay voltage inputs that performs the neutral voltage unbalance function, as a function of failed series capacitor elements.

Because the neutral unbalance voltage presented to the relay is quite small, as shown in Table 2, it is important to apply a relay that has high resolution and accuracy. In addition the relay filtering must be insensitive to third harmonic voltages that may be present across the neutral low voltage capacitors.

Table 2: Capacitor Bank Neutral Current and Voltage as a Function of Failed Series Elements

Number of Failed Elements	1	2	**3**	4	5	**6**	7	8	9
Neutral Current (Amperes)	0.46	0.94	**1.43**	1.93	2.45	**2.99**	3.54	4.10	9.68
Neutral Voltage (Volts)	0.30	0.61	**0.93**	1.25	1.59	**1.92**	2.29	2.66	3.04

The welding process described earlier provides the means to short out a group of parallel capacitor elements in a capacitor unit and allow the unit to remain in operation as long as the other elements or capacitor units are not exposed to overvoltages greater than 110 percent of rated rms voltage.

Both the differential and the neutral unbalance protection provide alarms to alert operations personnel about possible capacitor bank problems.

System Protection

The overall protection for this installation minimizes fault damage, provides high bank availability, and reduces installation and maintenance costs.

Multifunction numerical relays provide the following functions for system protection:

- Overcurrent protection for phase and ground faults between the breaker and the capacitor bank using redundant numerical relays.
- Overvoltage function to protect for sustained system overvoltage that may cause capacitor can failures.
- Breaker failure protection function to allow fault clearing in the event of a failure in one of the capacitor bank breakers.
- Power failure function using undervoltage elements to isolate capacitor banks from the power system in the event of a system blackout. In addition, this feature allows for an orderly capacitor bank reenergization after system voltage is restored to the main 230 kV bus.

A high-impedance bus differential scheme provides capacitor bus protection. Manually switching in and out the appropriate current contributions to the bus differential scheme maintains capacitor bus protection while the main breaker is out-of-service for any reason.

One set of three capacitor voltage transformers provides voltage inputs to the numerical relays and the PLC for protection and control functions. However, designers can now use new technologies to create a directional comparison bus protection scheme that takes advantage of numerical relays already in this installation to provide shunt capacitor bank protection functions.

MONITORING AND CONTROL OF SHUNT CAPACITOR BANKS

The design presented in Figure 4 uses a programmable logic controller (PLC) and digital relays to provide the monitoring and control of the shunt capacitor bank installation. Individual capacitor step circuit breakers provide shunt capacitor bank switching. There are two modes of operation: manual and automatic.

Manual Mode

In the manual mode, operators switch capacitor banks from the control room through step control switches installed on the switchboards. The following permissive conditions must be met before a capacitor step can be switched on or off by the manual control switches.

- The capacitor step must be in manual mode.
- The circuit breaker must be open for at least five minutes before it can be reclosed. This allows the capacitors to be discharged to a safe voltage level through their internal discharge device. If the breaker is not open for five minutes, the programmable logic controller blocks the close circuit and prevents the operator from closing the breaker.

Automatic Mode

In the automatic mode, the PLC controls the switching of the shunt capacitor steps. The PLC is programmed to perform voltage control and event recording, record step operations, balance switching operations, and communicate with a programmable graphics interface (PGI) located in the control room. The PGI is used to adjust voltage set points, and to view the status of capacitor step devices and bank alarms.

To perform automatic step insertion, the PLC compares the control voltage set-point with the measured system bus voltage. System voltage measurement is performed using two transducers. Their difference output of these transducers is compared against set thresholds before the system voltage measurement is accepted as valid. A voltage dead-band is also part of the step switching settings. The dead-band setting is greater than the voltage change caused by the addition or removal of one capacitor step, to avoid hunting by the system. The following must be satisfied in order to insert a capacitor step:

- The capacitor step must be in automatic mode.
- No capacitor step switching has been performed for a two-minute time period.
- Before a step is closed, it must be de-energized for five minutes.
- The main circuit breaker is closed and there is voltage on the bus.

The order of capacitor step insertion is sequenced to balance the number of operations for each step. If all steps have the same number of operations, the insertion is performed in a numerical ascending order. A "Step x Fail to Close" alarm, and a software latch is set if a capacitor step fails to close in five seconds. The software latch prevents further operations, until the problem has been resolved and the operator resets the capacitor step switching via the PGI.

Automatic step removal is performed in a similar fashion as step insertion. The PLC compares the system voltage with the control voltage set-point. If the system voltage is higher than the set-point voltage plus the dead-band setting, the PLC opens the capacitor step in a " First in – First out" order provided no switching action took place in the last two minutes. A "Step x Fail to Open" alarm, and a software latch is set if a capacitor step fails to open in five seconds. The software latch prevents further operations, until the problem has been resolved and the operator resets the capacitor step switching via the PGI.

Rapid insertion of capacitor steps can help system performance in the event of a major disturbance. The PLC monitors the rate-of-change of voltage to perform a rapid insertion of a capacitor step. If the rate-of-change of voltage exceeds four kV per second, and the system voltage falls ten percent below nominal, the PLC issues the commands to insert capacitor steps in two-second intervals. Rapid removal is also performed in the event the system voltage exceeds normal voltage by five percent. Capacitor steps are removed every two-seconds until the system voltage is less than five percent above normal voltage.

A number of different pages on the PGI monitor the operation of the capacitor bank installation. The PGI provides the following screens:

- The *System Status* screen displays the operating status of the 230 kV capacitor steps and the analog meter values for each step.

- The *Single Line Diagram* screen displays the station single line diagram of the substation, the open/close counters, and "Out-of-Service" capacitor steps.
- The *Voltage Set-point* screen displays the current voltage set-points, and dead-bands. In addition, the operator can make changes of the voltage set-points from this screen.
- The *Alarm* screen displays up to 28 alarm messages from the 230 kV capacitor banks, and relays.
- The *Sequence of Events* screen provides access to sequence of events recording for 48 points for the last 50 events.
- The *Maintenance Page* screen allows the operator to remove a step from an automatic sequence, to reset a "Fail to open" or a "Fail to close" lockout condition.

FUTURE PROTECTION AND CONTROL DESIGN ENHANCEMENTS

PG&E's "Substation of the Future" team is looking at future substation designs and substation automation applications as ways of improving system reliability and reducing installation, maintenance, and operating costs. Figure 5 shows a design that is under consideration for future shunt capacitor bank installations.

Capacitor bank protection, monitoring, and control can be further improved by taking advantage of new technologies that are becoming available. Below is a brief list of methods PG&E is considering to further reduce costs and increase system reliability:

- Take advantage of metering provided by numerical relays, and remove metering transducers used in the current design. Present-day numerical relays provide data close to revenue-metering quality, and the use of additional transducers is not necessary.
- Use programmable numerical relay interface buttons for manual control of switching- step operations in addition to the station computer interface.
- Monitor and control switching-step breakers using a locally installed I/O device, which is connected to a protection logic and communication hub via fiber optic cables; to reduce interference from the harsh transients generated in a capacitor bank installation due to inrush, or back-to-back switching transients.
- Use connections from numerical relay communications ports between the protection logic and communication hub to provide data exchange between numerical relays. The hub can then be used for the voltage control, and sequence-of-event recording functions currently performed by the PLC. In addition, the protection logic and communication hub can be used to design a directional comparison bus protection scheme and breaker failure logic.

A substation computer will then be used as the human-machine interface for monitoring, control, and maintenance interlocking of the shunt capacitor steps.

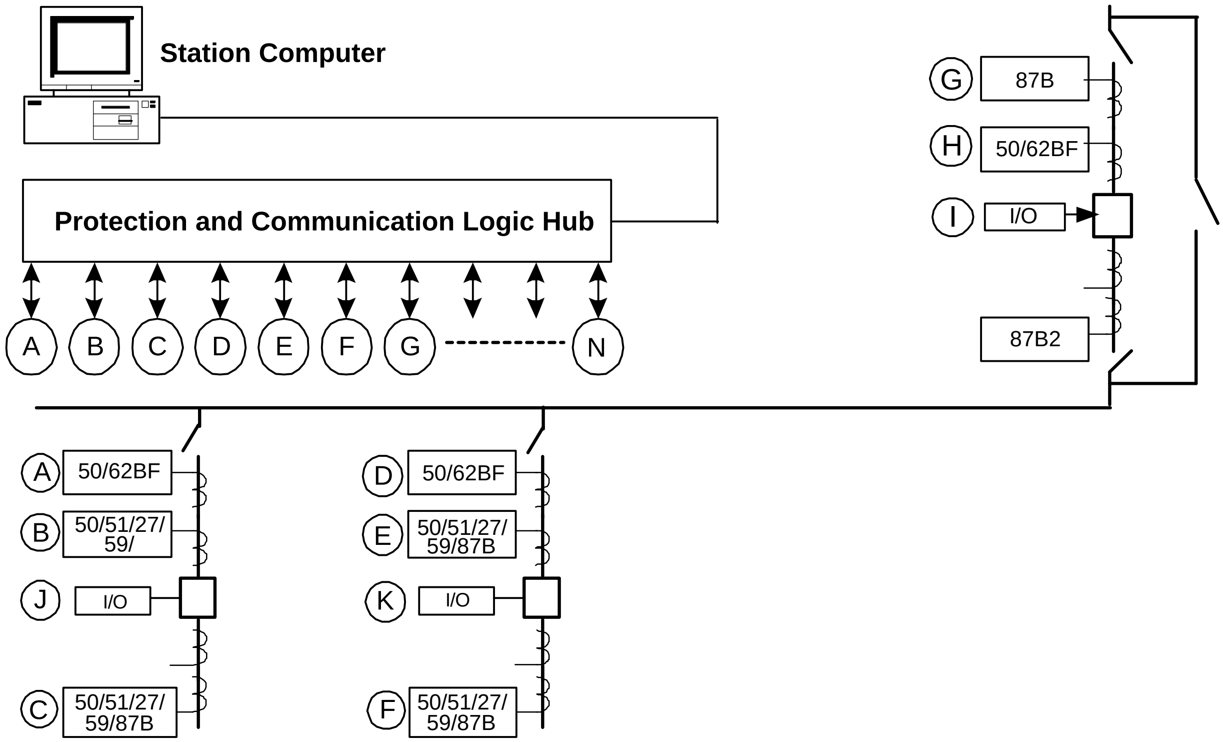


Figure 5: Future Shunt Capacitor Protection, Control, and Monitoring Scheme Design Alternative

CONCLUSIONS

1. Alternative and innovative design approaches for fuseless shunt capacitor bank applications provide sensitive differential voltage unbalance and neutral voltage unbalance protection. These protection methods eliminate the need to install high voltage CVTs, and provide more sensitive and secure differential voltage unbalance protection because the design is insensitive to system voltage variations and temperature-induced capacitance variations.

2. The costs of the protection design, installation, and maintenance are reduced by efficient use of numerical relay inputs, outputs, and protection functions.

3. PG&E adapted the fuseless shunt capacitor bank design as the standard design for their high voltage network because of its efficiency and reliability in monitoring operations, detecting problems, and alerting personnel, as well as its economical installation and maintenance.

4. PG&E plans to design their future shunt capacitor banks using new methods that take advantage of the latest technology to improve and simplify the bus protection design, simplify the control design, and improve the monitoring of the overall installation. These methods eliminate the need for metering and for control handles, reduce the wiring in the yard and control house, and provide isolation through the use of fiber-optic cables.

5. New ways to improve the overall protection and control design for shunt capacitor banks, substantially reduce the initial investment and future maintenance costs.

REFERENCES

[1] ANSI/IEEE Standard 18-1992, IEEE Standard for Shunt Power Capacitors.

[2] ANSI/IEEE C37.99-1990, IEEE Guide for Protection of Shunt Capacitor Banks.

[3] John E. Harder, "Developments in Capacitor Protection," Proceedings of the 11th IEEE/PES Transmission and Distribution Conference and Exposition, New Orleans, Louisiana, 1990.

[4] John E. Harder, "Capacitor Bank Protection," Presented at the Minnesota Power Systems Conference, St. Paul, Minnesota, October 1987.

[5] John E. Harder, "Fuseless Substation Capacitor Banks," Presented at the Pennsylvania Electric Association, Lancaster, Pennsylvania, June 1990.

BIOGRAPHIES

Demetrios A. Tziouvaras was born in Greece and moved to the USA in 1977. He received his B.S. and M.S. degrees in electrical engineering from the University of New Mexico and Santa Clara University, respectively. He joined the System Protection Group of Pacific Gas & Electric Co. in 1980, where he held the position of Principal Engineer and was responsible for the application of new technologies, design standards, and substation automation. He joined the Research & Development Group of Schweitzer Engineering Laboratories in 1998 where he is a Research Engineer. He is a senior member in the Institute of Electrical and Electronic Engineers (IEEE) and a member of the Power System Relaying Committee of the Power Engineering Society of IEEE. He is a member of two subcommittees and chairman of two working groups, one on EMTP Applications to Power System Protection, and the other on Mathematical Models for Current, Voltage, and Coupling Capacitor Voltage Transformers. He has authored and co-authored numerous technical papers and taught seminars in EMTP, protective relaying, and digital relaying at the University of Illinois at Urbana-Champaign and the California Polytechnic Institute in San Luis Obispo, California. His interests include digital relaying modeling, power system protection, and power system transients. He has numerous patents pending.

Malkiat S. Dhillon was born in India. He received his B. S. Degree in electrical engineering from Panjab University, Chandigarh, India, and his M. S. Degree in electrical engineering from California State University, Sacramento. He is a registered electrical engineer in the State of California. He joined the transmission design group of Pacific Gas & Electric co. in 1981 and moved to the System Protection group in 1983. He is senior protection engineer and is responsible for protection of the PG&E 500 kV system. He also works on special projects. In the past he was responsible for design standards, evaluation of new products, and substation automation.

991011 • TP6099-01