Commissioning of Protective Relay Systems

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***Abstract*—Performing tests on individual relays is a common practice for relay engineers and technicians. Most utilities have a wide variety of test plans and practices. However, properly commissioning an entire protection system, not just the individual relays, presents a challenge.**

This paper suggests a process for performing consistent and thorough commissioning tests through many sources: breaking out relay logic into schematic drawings; using SER, metering, and event reports from relays; simulating performance using end-to-end testing and lab simulations; and utilizing other tools, including synchrophasor measurements. We examine and suggest approaches for commissioning several applications: distribution bus protection, short line protection using communications-aided tripping, main-tie-main scheme, line and transformer differential protection. Finally, we propose that, while 100% commissioning certainty may not be possible, we can approach 100% by integrating event report analysis to validate our commissioning strategy.

I. Introduction

Protective relays now perform many functions besides protection. The advantages that modern microprocessor-based relays provide over traditional relays are well documented. These advantages include fault location, event reports, and programmable logic that allow many functions to be included in one device, thus saving hardware and wiring costs. One important complication of the technology shift is the increasing portion of the protection system design that resides in algorithms and logic in relays.

Meanwhile, testing and commissioning practices largely still focus on individual relays, not the protective relaying system. How can we be certain that we are fully testing and commissioning relay systems? Have we improved simplicity and reliability or just shifted the complexity?

II. Certainty in Commissioning With New Technologies

Few would disagree that implementing new technologies with microprocessor-based relays has improved power system protection. This includes improved reliability by finding root cause of system faults, reduced cost of hardware and wiring, fault location, and many other advantages.

Traditional designs, typically electromechanical, have more devices and greatly increased wiring requirements. However, one advantage of single-purpose devices is that all of the functionality, for the most part, can be represented by a single elementary drawing. A technician can have a blueprint of the design and systematically highlight each device and interconnection until the entire system is tested.

Certainty in commissioning protective relaying systems is, perhaps, the most difficult part of implementing new technologies. However, there are many tools and approaches we can use to improve and simplify this process.

A. Tools and Methods for Commissioning Protective Relaying Systems

Some tools and methods that aid in the commissioning of protective relaying systems are listed here:

- I/O contact testing
- Functional element testing
- State simulation testing
- SER, metering, and event report data
- End-to-end tests using satellite-synchronized test sets
- Synchrophasor data
- Logic diagrams that break out programmable logic
- Commissioning in the field
- Lab simulations
- Use of system event reports to validate relay performance as part of the commissioning strategy

B. Developing a Plan

Testing requirements for every system are likely to be different based on the system configuration and protection scheme applied. Develop a test plan that captures all the necessary steps to ensure that a system is tested with reasonable certainty.

Appendix A is a checklist developed for transmission line protection schemes and serves as a template for a customized and complete commissioning testing strategy.

III. Commissioning Examples

A. Fast Bus Protection on a Distribution Bus Using a Protection Logic Processor

Fig. 1 shows a one-line diagram of a distribution bus protection scheme using a fast bus trip scheme.

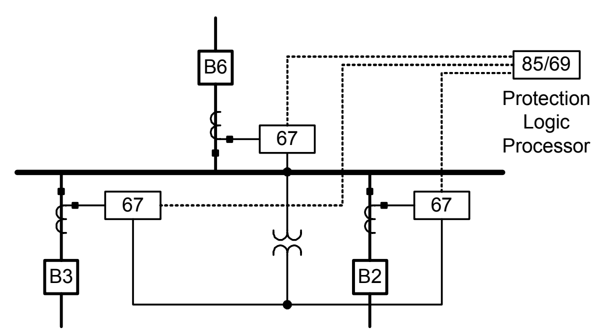


Fig. 1. Fast Bust Trip One-Line Diagram

Most of the logic for the protection of this scheme is developed in the settings of a protection logic processor (85/69 device). Thus, to successfully commission this scheme, we need to verify the performance of the following:

- Directional overcurrent elements (67)
- Performance of the communications path

- CT and VT connections and polarities of the inputs to the 67 devices
- Fast bus trip and block logic settings in relays and protection logic processor
- Breaker trip/dc control circuit

The directional overcurrent elements can be tested and validated by applying test values from system faults (e.g., internal bus fault, external line faults).

CT and VT polarities, phasing, and ratios are usually checked through manual field measurements at commissioning. One improvement is to use synchrophasor data from the relays, if available [1]. Phasor measurements take a precise snapshot of the currents and voltages at the same instant in time.

Commissioning the communications path and logic settings is more complex and requires that the logic be broken out into logic diagrams, like the one shown in Fig. 2.

Ideally, we would like to test the scheme all the way through. The best environment for this is a lab simulation with all three relays and the protection logic processor connected with complete ac voltage and current and the entire communications scheme connected.

For example, individually test directional overcurrent elements (67) for Breakers 2, 3, and 6. Then apply fault simulations for each scenario to verify the internal and external fault logic (expected results are shown in parentheses):

1. Breakers 3, 6 internal, Breaker 2 external (no TRIP).
2. Breakers 2, 6 internal, Breaker 3 external (no TRIP).
3. Breakers 2, 3 internal, Breaker 6 external (no TRIP).
4. Breakers 2, 3, 6 internal (TRIP within 25 ms).
5. Verify Transient Reversal Block logic by applying Test 1, then Test 4 in short intervals, e.g., apply Test 1 for 2 cycles, then Test 4 for 4 cycles, etc. (no TRIP).
6. Verify Disable Fast Bus Trip logic by applying loss of potential (LOP) and relay out of service conditions, then apply Test 4 (no TRIP).

By performing a thorough lab simulation of the complete logic, we can then install and commission this system. In the field, we check the CTs and VTs, verify the integrity of the communications path, and perform breaker trip tests to validate the dc control circuit.

B. Short Line Protection Using Directional Overcurrent Protection in Blocking and Permissive Pilot Tripping Schemes

As shown in Fig. 3, a series of underground distribution lines (Loops 1, 2, 3, and 4) are protected by directional overcurrent protection in a pilot protection scheme. Essentially, this system, even though it is a medium-voltage (15 kV) system, is protected like a transmission system [2].

Each line section uses a permissive overreaching transfer trip (POTT) scheme and a directional comparison blocking (DCB) scheme. The permissive, block, and direct transfer trip signals are transmitted and received between the relays through an optical fiber network using relay-to-relay communications. Two separate fiber paths (A and B) are used.

To successfully commission these schemes, we need to verify the performance of the following:

- Directional overcurrent elements (67)
- Communications paths
- POTT and DCB tripping schemes
- Primary voltage and current magnitude, polarity, and phasing

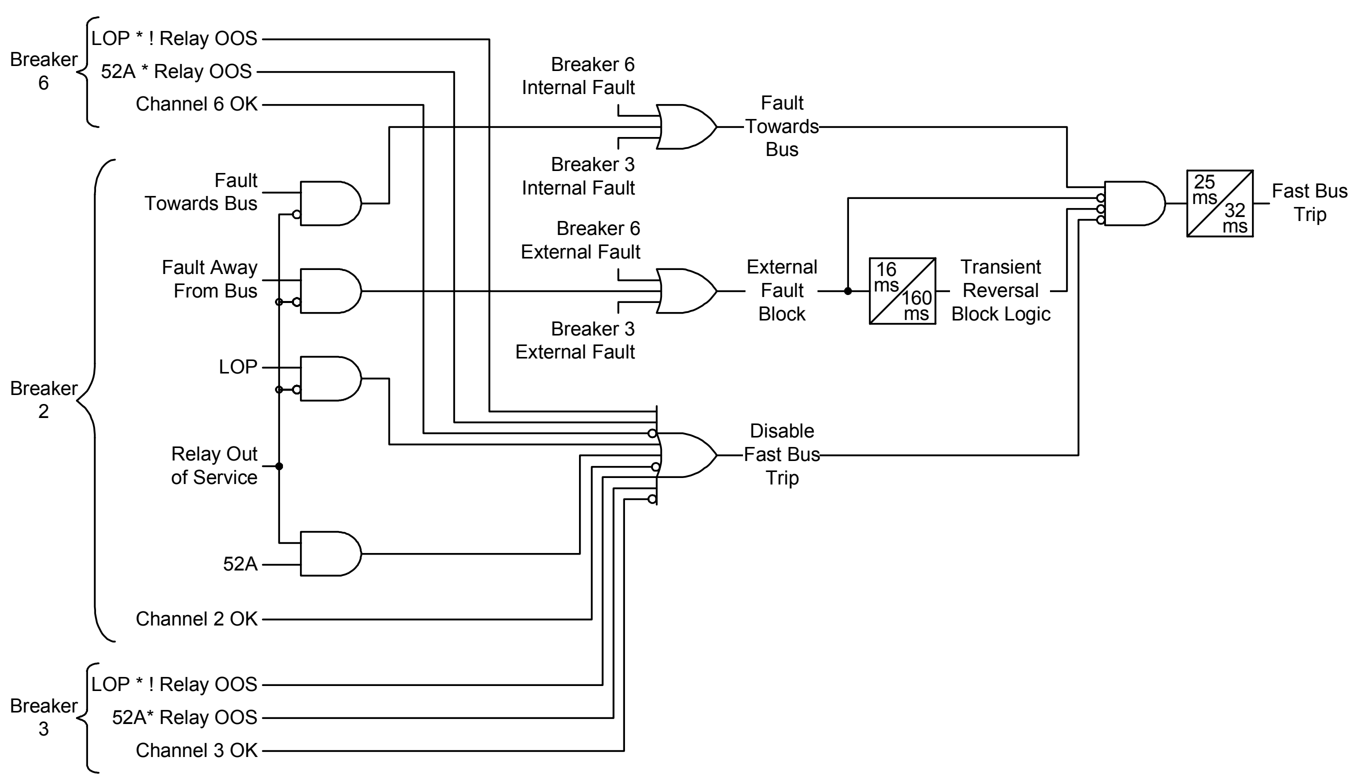


Fig. 2. Fast Bus Trip Logic

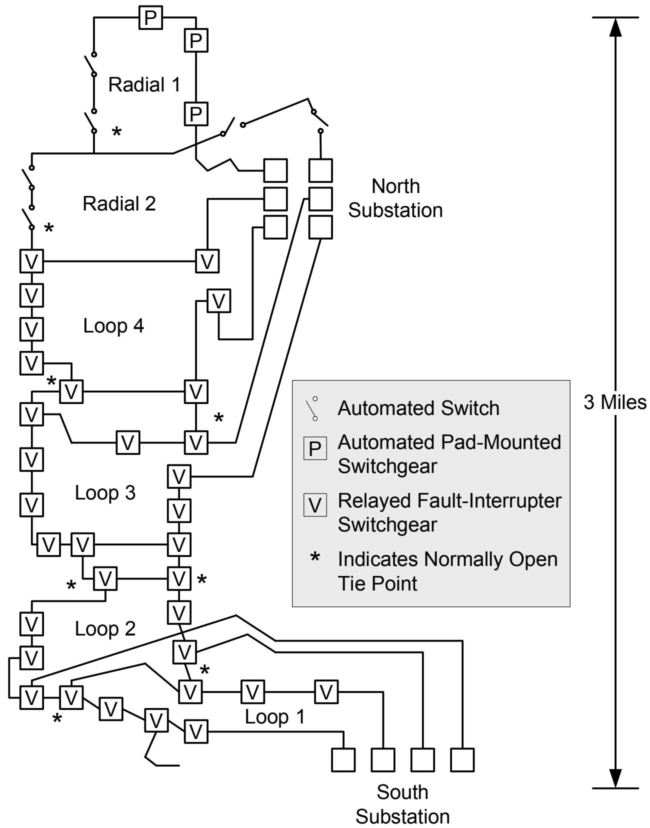


Fig. 3. System One-Line Diagram of Loop Distribution System

1) POTT Scheme

Fig. 4 shows a POTT scheme one-line diagram. As we can see, phase and ground directional overcurrent elements (67P2, 67G2) declare faults in the forward direction.

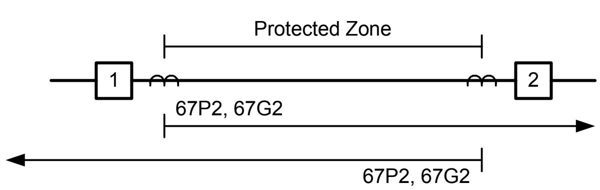


Fig. 4. Basic POTT Scheme Protection

The logic for tripping, as well as transmitting and receiving permissive trip signals, resides within the relay. Fig. 5 shows a control circuit representation of the logic. If a forward fault occurs, 67P2 or 67G2 transmits (KEY) a permissive signal to the remote terminal. If a local forward fault is detected and permissive is received from the remote terminal, trip the local interrupter and send a direct transfer trip to the remote terminal. An open breaker (52B) also transmits a permissive trip signal.

Creating a simple diagram like Fig. 5 is an important step that is often skipped. However, the extra effort allows us to understand and test the logic more systematically.

End-to-end testing is ideal. Forward and reverse faults can be simulated with breaker opened/closed to validate the logic all the way to the TRIP output.

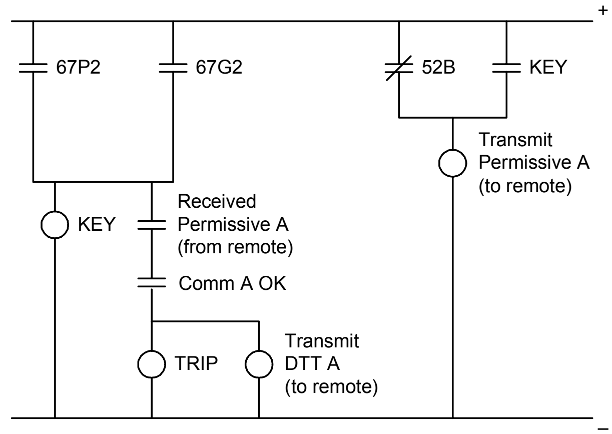


Fig. 5. Control Circuit Representation of POTT Logic

2) DCB Scheme

Fig. 6 and Fig. 7 show the basic DCB scheme one-line diagram and control circuit representation, respectively. The DCB scheme is used in conjunction with the POTT scheme to ensure tripping occurs with no settings changes if the system is run as an open-loop (radial) system.

Forward directional overcurrent elements (67P2T, 67G2T) trip provided no block is received from the remote terminal. Reverse elements (67P3, 67G3) assert the transmit block signal. There is a short 3-cycle delay on the tripping for DCB to allow time for the block to be received.

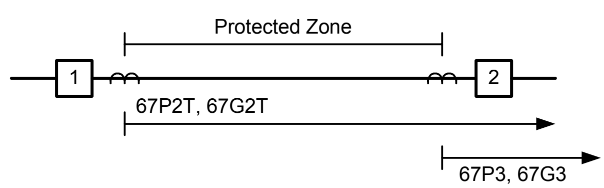


Fig. 6. Basic DCB Scheme Protection

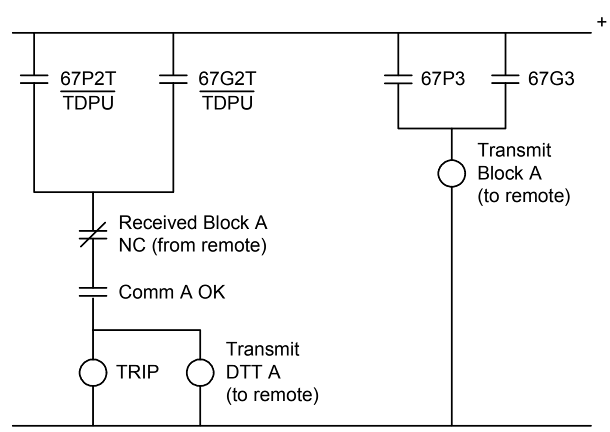


Fig. 7. Control Circuit Representation of DCB Logic

C. Main-Tie-Main Distribution Bus Transfer Scheme

Fig. 8 shows a main-tie-main transfer scheme. When either source voltage is lost, the respective main breaker opens, and the normally open tie breaker closes to restore power to the load.

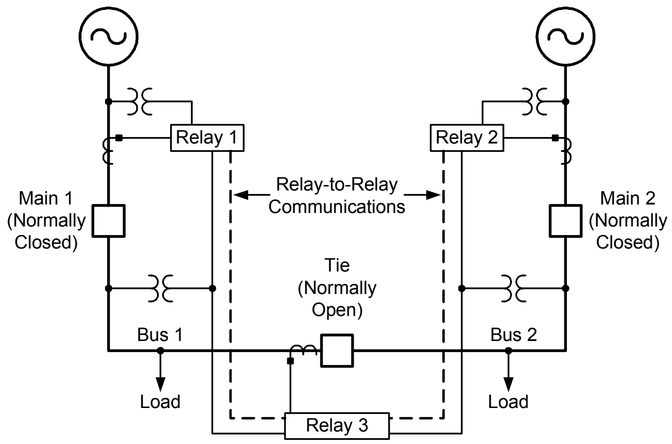


Fig. 8. One-Line Diagram and Relay Interconnect for Main-Tie-Main Scheme

The programmable logic used in this scheme is quite extensive, and logic representations of the scheme must be created to properly test the scheme. Moreover, because many functions are time sensitive, troubleshooting tools like SER reports are critical in validating the logic.

For testing, choose as many operational scenarios as are realistic. For the basic tests, we start with the following:

- Loss of Source 1 – Verify Breaker 1 opens and tie breaker closes. When Source 1 is reenergized, open tie and close Breaker 1.
- Loss of Source 2 – Verify Breaker 2 opens and tie breaker closes. When Source 2 is reenergized, open tie and close Breaker 2.
- Loss of both sources – Verify no transfer occurs.
- Vary the transition time delays between all of the above scenarios.

The challenge is to limit the number of test scenarios. Pick as many as is reasonable based on the system.

Appendix B shows the detailed logic of a very difficult problem that was identified through lab testing and the use of time-aligned SER data.

D. Transformer Differential Protection

Commissioning transformer differential protection schemes involves several levels of testing:

- Hardware tests verify transformer turns ratio, CT turns ratios, and CT polarity.
- Functional tests validate the performance of the relay elements with the installed settings and test the dc control circuits. Trip tests verify that the relay operates the correct lockout relays and breakers.
- In-service or commissioning tests verify the primary and secondary ac current circuits. We must take into account the transformer ratio and connection; the CT ratio, wiring, and connections; and the relay settings.

The last item is, by far, the most challenging aspect of assuring certainty in commissioning. Modern transformer differential relays have settings that compensate for the difference in the secondary currents, adjusting for the transformer connection (e.g., delta-wye) and removing zero-sequence current.

In order to perform commissioning tests, we must apply balanced three-phase currents to the primary system. Some users energize the transformer to the system and begin to apply load. Ideally, we prefer to perform this test without connecting to the power system. For example, use a portable generator or a station service transformer to supply a reduced voltage three-phase power supply to one of the windings of the transformer and apply a short circuit to the remaining winding. An example test setup is shown in Fig. 9.

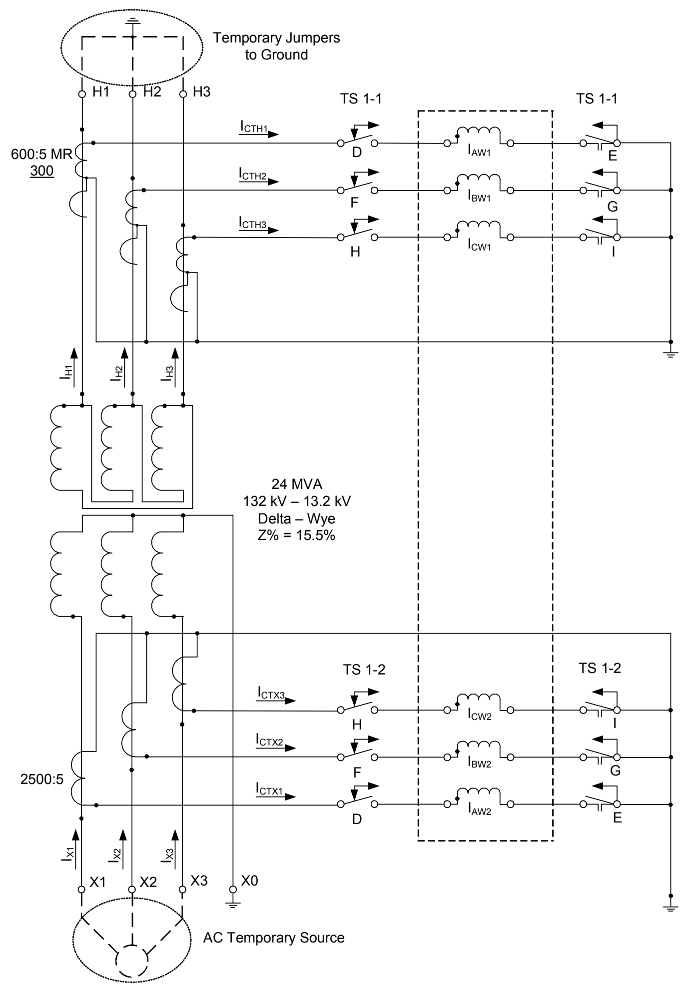


Fig. 9. Three-Line Diagram of Primary Injection Test

Through this procedure, we can check the following:

- The phase rotation and angle of the currents
- Secondary current magnitudes
- The relationship of the high-side currents to the low-side currents
- The operate or differential current (should be nearly zero)

For the transformer shown in Fig. 9, given a 240 Vac source, we can calculate expected relay currents (magnitude and angle). Using relay metering data, we then observe the measured currents, as shown in Table I. If the measured (actual) currents do not match the calculated (expected) currents and/or we observe differential current, we must perform troubleshooting to systematically check CT wiring, connections, and relay settings to correct the discrepancy.

TABLE I
COMMISSIONING TEST WORKSHEET QUANTITIES:
COMPARE EXPECTED CURRENTS WITH ACTUAL CURRENTS

	Expected Currents	Actual Currents
I_{CTX1} (I_{AW2})	246 mA at +150°	0.27 at 149.7°
I_{CTX2} (I_{BW2})	246 mA at +30°	0.25 at –90.5°
I_{CTX3} (I_{CW2})	246 mA at –90°	0.25 at 29.8°
I_{CTH1} (I_{AW1})	205 mA at 0°	0.22 at 0.0°
I_{CTH2} (I_{BW1})	205 mA at –120°	0.21 at –119.7°
I_{CTH3} (I_{CW1})	205 mA at +120°	0.21 at 120.3°

Sometimes it helps to plot the currents, as shown in Fig. 10. Winding 2 B-phase and C-phase currents in this system appear to be reversed.

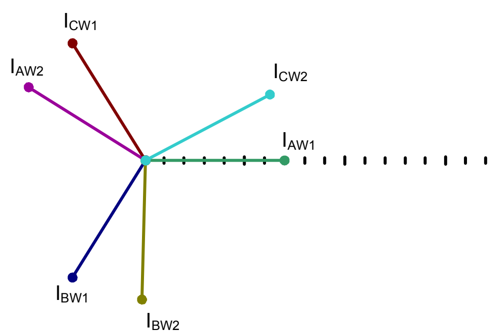


Fig. 10. Plot of Measured Currents During Commissioning Test

Reference [3] includes examples of problems discovered during commissioning and through an undesired operation that could have been avoided through proper commissioning.

E. Transmission Line Protection Using Line Current Differential

Line current differential relaying is unique in that it is a current-only scheme. Key components to commissioning this type of system include the following:

- Verify primary and secondary ac current polarities, phase angle, and phasing
- Verify dc tripping and control circuit
- Check communications paths
- Simulate internal and external faults to validate performance of the line differential element (87L)

Ideally, use end-to-end testing to inject time-synchronized three-phase currents to the relays. This allows us to simulate both internal and external faults. If end-to-end testing is not available, perform one-ended tests using loop-back features in relays or communications equipment. The shortcoming of one-ended tests is that we can only simulate internal faults.

Upon energizing the line, use metering and event reporting features to compare expected with actual currents. Using relay metering data also validates the communications channel.

Fig. 11 shows a screen capture of local and remote metering data as measured at one line end. Alternatively, use real-time synchrophasor data, if available, for the same purpose.

```
=>MET <ENTER>
DIFF RELAY                           Date: 06/05/01    Time: 10:28:50.360
EXAMPLE: BUS B, BREAKER 3

Local                A         B         C        3I0       3I2        I1
I MAG (A Pri)     386.444   385.401   385.597    2.838     1.747   385.813
I ANG (DEG)        -0.10   -119.90    119.80    -2.60    -19.00      0.00

Channel X PRIM       A         B         C        3I0       3I2        I1
I MAG (A Pri)     385.644   387.077   395.563   32.567    30.969   389.172
I ANG (DEG)        179.60     59.50    -56.10    14.80    133.70   -179.00
```

Fig. 11. Screen Capture of Local and Remote Metering Data

F. Transmission Line Protection Using DCB Over Power Line Carrier

Fig. 12 shows a transmission line protection scheme using DCB over power line carrier. When commissioned, the protection system was deemed to be operating properly.

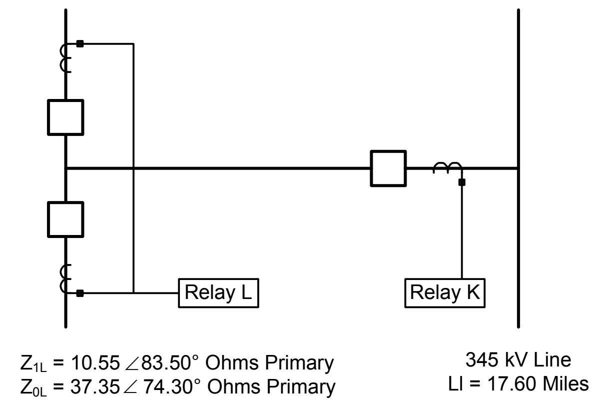


Fig. 12. One-Line Diagram of 345 kV Transmission Line Protection

A B-phase-to-ground fault occurred on the line a few months after commissioning. The relays at each end of the line operated and cleared the fault within approximately 4 to 5 cycles. Presumably, the relays, breakers, and communications scheme all did their job. Are the events worth analyzing? Can we use these events to improve the system? Even after a successful operation, here are some questions we should ask:

1. Were the prefault voltages and currents reasonable? Did the measured load agree with system data, if available?
2. Did the relays operate within the expected time?
3. Did the expected relay elements operate?
4. Did the relay fault location agree with the actual location?
5. Did the power line carrier communications operate as expected?
6. Did the breakers operate in reasonable time?

Analyzing the event reports helps provide the following answers to these questions.

Note: event and metering data give relative phase angles between signals in a relay. Synchrophasors allow comparison of phase angles from multiple relays.

1. The prefault currents are shown in Fig. 13 and Fig. 14. The magnitudes vary from 440 to 510 amperes, primary. There is a slight unbalance (C-phase is high), but this is expected because there are no line transpositions.

Channel	Mag	Angle	Scale	Show	Ref
IR	32.8	338.9	1	0	0
IA	443.2	12.3	1	1	0
IB	454.1	267.7	1	1	0
IC	517.9	137.8	1	1	0
VA	203.8	0.0	1	1	1
VB	199.3	240.7	1	1	0
VC	203.7	121.1	1	1	0
I0	10.9	338.8	1	1	0
I1	469.0	19.2	1	1	0
I2	60.5	250.6	1	1	0
V0	0.3	27.6	1	1	0
V1	202.3	0.6	1	1	0
V2	2.5	298.6	1	1	0

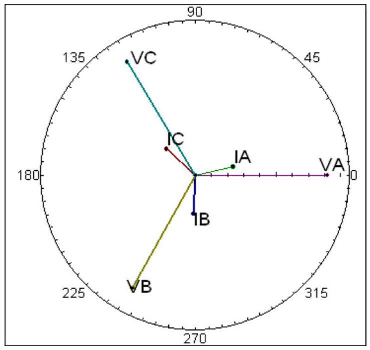


Fig. 13. Prefault Phasors From Relay L

Channel	Mag	Angle	Scale	Show	Ref
IR	42.4	167.9	1	0	0
IA	442.4	190.1	1	1	0
IB	444.0	86.4	1	1	0
IC	510.9	315.8	1	1	0
VA	205.7	0.0	1	1	1
VB	201.4	240.4	1	1	0
VC	204.7	120.8	1	1	0
I0	14.1	167.9	1	1	0
I1	462.7	197.3	1	1	0
I2	60.6	70.7	1	1	0
V0	0.5	32.7	1	1	0
V1	203.9	0.4	1	1	0
V2	2.0	311.5	1	1	0

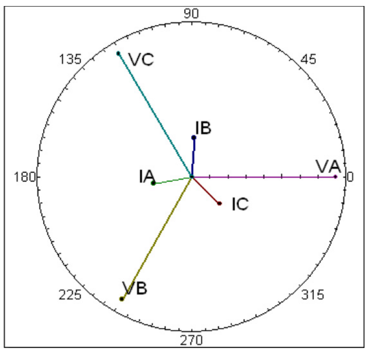


Fig. 14. Prefault Phasors From Relay K

The event reports shown in Fig. 15 and Fig. 16 help us answer the remaining questions.

2. Both event reports show that the 3PT (three-pole trip) asserts within about 1.5 cycles of fault inception, as expected.
3. Both event reports show that Z1G (Zone 1 ground distance element) and 67N2 (ground directional element in DCB scheme) assert. These are expected to operate for the B-phase-to-ground fault.
4. Relay data indicate that fault location was 4.31 miles from Relay L and 13.02 miles from Relay K. This was later confirmed.
5. Both event reports show a momentary pickup of the block trip input (IN3 from Relay L, IN9 from Relay K). This is a concern because the block trip input has a short dropout delay that can delay fault clearing. In this case, the utility is working with the carrier equipment manufacturer to discover root cause.
6. The event report for Relay L shows that the breaker status contacts (IN1, IN2) drop out at Cycle 5.75 or 6. However, the current does not drop out until after Cycle 9! We expect approximately 1.25 cycles of dropout delay due to digital filtering, indicating a slow operating breaker. The breakers in question are an older air breaker design with a history of maintenance issues, requiring frequent maintenance.

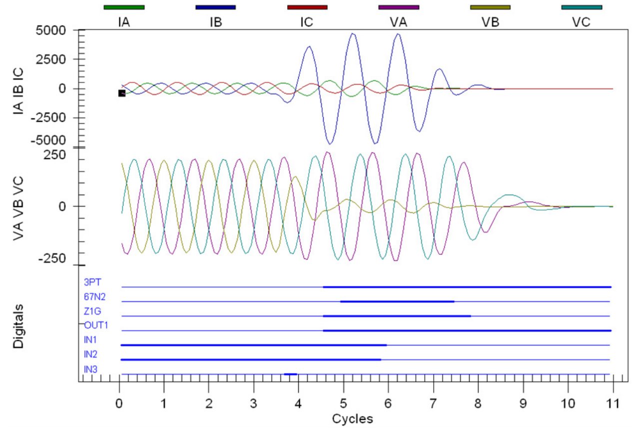


Fig. 15. Event Report for Relay L End: Currents, Voltages, Relay Elements, and I/O Contacts

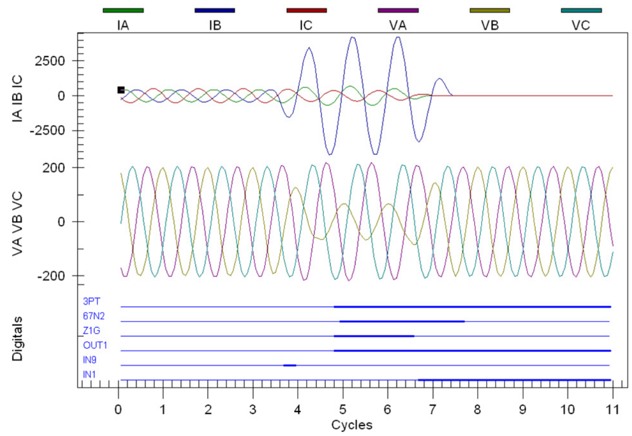


Fig. 16. Event Report for Relay K End: Currents, Voltages, Relay Elements, and I/O Contacts

IV. Conclusions

A number of different tools can improve certainty in commissioning testing: I/O contact testing; functional element testing; state simulation testing; SER, metering, and event report data in relays; end-to-end tests using satellite-synchronized test sets; synchrophasor data; logic diagrams that break out programmable logic; commissioning in field; and lab simulations.

Each application has unique requirements, and it is important to develop a test plan to address the needs properly.

Even careful planning, scrutiny, and extensive testing may not result in 100% certainty. However, using all of the tools available to us, including analyzing event reports after a system is in service, we can continue on a course of constant improvement of protective relay system performance.

V. Appendix A – Line Protection Checklist

Product Information

Relay Model No. ______________________________

Relay Serial No. ______________________________

Relay ID No. ______________________________

Terminal ID No. ______________________________

Application Review Before Commissioning

Primary Protection Functions

- Basic principle of operation described .... ❑
  (POTT, DCB, step-distance, differential, feeder, etc.)
- Distance protection applied .... ❑
  (How many zones, purpose of each described)
- Overcurrent protection applied .... ❑
  (How many levels, purpose of each described
- Backup described (if scheme fails) .... ❑

Other Protection Functions

- Undervoltage applied? .... Yes/No
- Underfrequency applied? .... Yes/No
- Load encroachment applied? .... Yes/No
- Line thermal applied? .... Yes/No
- Power swing block/trip applied? .... Yes/No
- Loss-of-potential enabled? .... Yes/No

Control Functions

- Autoreclosing applied (internal or external to relay) .... ❑
  (scheme described?)
- Synchronism check/voltage checks .... ❑
  (scheme described?)
- Breaker failure applied (internal or external to relay) .... ❑
  (scheme described?)
- Breaker monitor enabled and set .... ❑

Logic

- DC control documentation complete .... ❑
- AC schematic/nameplate documentation complete .... ❑
- Logic diagrams complete .... ❑
- Logic design tested and simulated .... ❑

Before Commissioning

Physical

- Properly mounted .... ❑
- Clean .... ❑
- Undamaged .... ❑
- Testing correct relay .... ❑
  (visibly verified—look under/around panel as needed)

Electrical

- Case grounded .... ❑
- Connections tight .... ❑
- Wiring orderly
  - Labels visible and legible .... ❑
  - No broken strands or wires .... ❑
  - Neat .... ❑
  - Clearances maintained .... ❑

Test Switches

- CT test switches open (CT shorted) .... ❑
- PT test switches open .... ❑
- TRIP output test switches open .... ❑
- Breaker failure (external) test switches open .... ❑
- DC power test switches closed and relay powered up .... ❑

Relay Status

- Enable LED on .... ❑
- Push target reset—all LEDs illuminate .... ❑
- No warnings or failures on **STATUS** command .... ❑

Jumpers

- Password protection enabled .... Yes/No
- **OPEN/CLOSE** command enabled .... Yes/No
- ______________________________ .... Yes/No
- ______________________________ .... Yes/No

Commissioning

Settings

- Correct settings on correct relay .... ❑
- In-service settings saved and stored .... ❑

Protection Functions Check

- Functional tests described .... ❑
- DC supply voltage does not exceed relay rating .... ❑
- Test voltages and currents do not exceed relay .... ❑
  continuous ratings
- Relay operates in expected time (details) .... ❑
- Relay correctly does not operate for out-of-section or .... ❑
  external faults (details)

Protection Communications

- Relay connected to correct pilot channel .... ❑
- Channel functioning correctly .... ❑
- End-to-end testing required and described? .... ❑

Auxiliary Power (Source Voltage)

- Battery source is correct and in good condition .... ❑
- Battery monitor enabled .... ❑

NOTES:

Information Security

Passwords enabled (check jumper) .... ❑

Passwords changed and documented .... ❑

Level 1 ______________

Level 2 ______________

Appropriate people notified of password change .... ❑

Communications channel security requirements described ❑

Data Communications

Metering/targeting data to SCADA/communications processor checked .... ❑

Remote engineering access established.............................. ❑

Date, Time, and Reports

Synchronized date/time input... ❑

Date and time correct .... ❑

Relay HISTORY/SER buffers cleared (e.g., HIS C).......... ❑

Alarms

Alarm contact connected to remote monitor .... ❑

Alarm contact connected to local monitor.......................... ❑

AFTER COMMISSIONING TESTS AND
BEFORE RELAY PLACED IN SERVICE

Voltages from correct PT; PT test switches closed .... ❑

Current from correct CT; CT test switches closed .... ❑

Breaker auxiliary contacts from correct breaker(s) .... ❑

Polarities and phase rotation correct .... ❑

Plot phasors from **METER** command or event report........ ❑

Enter magnitude and phase angle for each measured quantity:

IA ______________

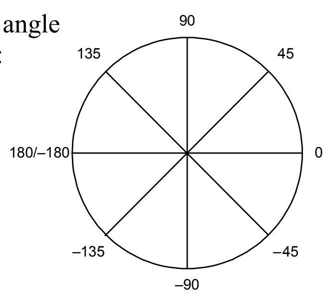
IB ______________

IC ______________

VA ______________

VB ______________

VC ______________



Polarity and phase rotation of V and I as expected .... ❑

Nominal unbalance (I2 / I1 < 5%, V2 / V1 < 5%) .... ❑

Nontrip I/O test switches closed.. ❑

No trips asserted (targets reset, no voltage on test switch).. ❑ (unlatch all trips)

Trip circuit to correct breaker or test switch closed .... ❑

Breaker failure trip to correct lockout or test switch closed ❑

52A contact(s) closed .... ❑

ENGINEERING SIGN OFF

Designer: ____

Setter: ____

Tester: ____

Checker: ____

APPENDIX B

Using SER data in a lab simulation identified a problem in the main-tie-main bus transfer scheme.

A. Test Scenario: Loss of Both Sources at Same Time, Return of Source 1 (S1), and Delayed Return of Source 2 (S2)

Test conditions were applied in four stages:

- Normal operation – Healthy voltage (greater than 90%) and normal load current on both sides (10 seconds).
- Loss of voltage from both sources – Voltage drops to 0 (less than 10%) (15 seconds).
- Voltage and current on S1 return to normal, and S2 remains 0 (1.5 cycles).
- Voltage and current on S2 return to normal (30 seconds).

B. Expected Operation

The loss of voltage on both sides should result in no action. The return of voltage on S1 will result in the transfer scheme beginning to time for a transfer operation. Before the timer times out, voltage on S2 will return to nominal. Breakers M1 and M2 should remain closed throughout the duration of the test, and the tie breaker should remain open.

C. Actual Operation

The scheme failed in two ways. First, M2 tripped. Second, once M2 tripped, the tie breaker failed to close.

D. Troubleshooting the Scheme

The only way to determine the root cause of the failure is to examine the logic in detail. Therefore, comprehensive logic diagrams are an absolute necessity. Fig. 17, Fig. 18, and Fig. 19 show the original logic.

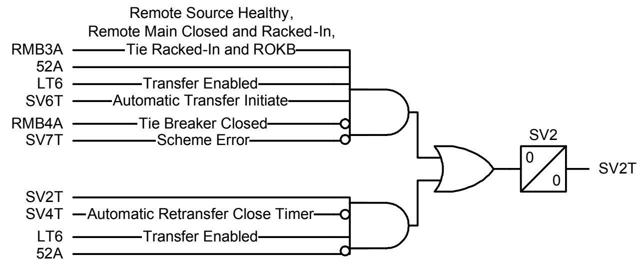


Fig. 17. Old Main Breaker Trip From Automatic Transfer Logic

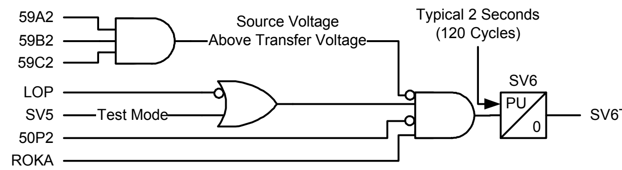


Fig. 18. Old Main Breaker Transfer Initiate Logic

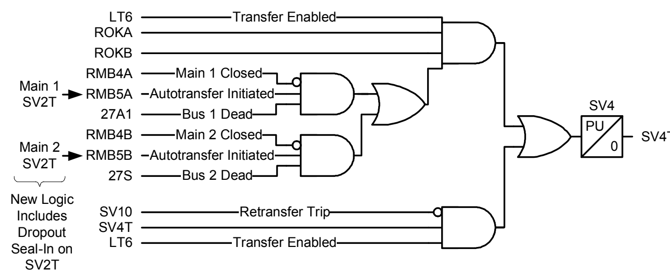


Fig. 19. Old and New Tie Breaker Automatic Transfer Close Logic

The sequence of events, as shown in Fig. 20, tells the story in detail. The scheme tried to initiate a rollover upon the return of S1, but before the transfer was finished, the voltage on S2 returned, and the scheme locked up.

	A	B	C	D	E	F	G	H	I	J	K	L
1	S27											
2												
3	MAIN 1				TIE				MAIN 2			
4												
5	Time	Element	State		Time	Element	State		Time	Element	State	
6												
7	8:40:34.381	3P59	Asserted	S1 healthy	8:40:34.384	3P59	Asserted	B1 healthy	8:40:34.382	3P59	Asserted	S2 healthy
8	8:40:34.401	RMB3A	Asserted	S2 healthy * M2 closed	8:40:34.388	RMB3A	Asserted	S1 healthy * M1 closed	8:40:34.399	RMB3B	Asserted	S1 healthy * M1 closed
9					8:40:34.392	RMB3B	Asserted	S2 healthy * M2 closed				
10												
11	8:40:44.368	3P59	Deasserted	S1 dead	8:40:44.370	3P59	Deasserted	B1 dead	8:40:44.368	3P59	Deasserted	S2 dead
12					8:40:44.370	59S1	Deasserted	B2 dead	8:40:44.372	SV6	Asserted	S2 dead intitiate transfer
13	8:40:44.376	SV6	Asserted	S1 dead timer start	8:40:44.378	RMB3A	Deasserted	S1 dead or M1 open				
14	8:40:44.388	RMB3A	Deasserted	S2 dead or M2 open	8:40:44.378	RMB3B	Deasserted	S2 dead or M2 open	8:40:44.385	RMB3B	Deasserted	S1 dead or M1 open
15	8:40:46.376	SV6T	Asserted	2 sec					8:40:46.372	SV6T	Asserted	2 sec
16												
17	8:40:54.383	SV6T	Deasserted	S1 - 1 ph								
18	**8:40:54.387**	**3P59**	**Asserted**	S1 healthy	**Time Reference=0**							
19					8:40:54.389	3P59	Asserted	B1 healthy				
20				.6 cycles ----------------->	8:40:54.397	RMB3A	Asserted	**S1 healthy * M1 closed**				
21									8:40:54.410	SV2T	Asserted	Trip M2 (S1 healthy M1 closed)
22								1.38 cycles ------------>	8:40:54.410	RMB3B	Asserted	**S1 healthy * M1 closed**
23				1.86 cycles -------------->	8:40:54.418	RMB5B	Asserted	**Auto Transfer Initiated**				
24					**NOTE: If M2 opens before RMB5B deasserts, close Tie**				8:40:54.418	SV6T	Deasserted	S2 - 1 ph (Too late, SV2 Sealed in)
25												
26								1.88 cycles ------------>	8:40:54.418	TRIP	Asserted	Trip M2
27				2.13 cycles --------->	8:40:54.422	59S1	Asserted	B2 healthy	8:40:54.422	3P59	Asserted	S2 Healthy
28									8:40:54.422	SV2T	Deasserted	stop auto transfer
29					8:40:54.430	RMB3B	Asserted	S2 good and M2 closed				
30					8:40:54.430	RMB5B	Deasserted	No Auto Transfer				
31	8:40:54.437	RMB3A	Asserted	S2 healthy * M2 closed								
32					8:40:54.455	27S	Asserted		8:40:54.455	27S	Asserted	B2 dead
33								4.38 cycles --------------->	8:40:54.460	52A	Deasserted	**M2 open (2.5 cycle breaker)**
34				4.86 cycles ---------------->	8:40:54.468	RMB4B	Deasserted	**M2 open**				
35	8:40:54.474	RMB3A	Deasserted	S2 Healthy and M2 Open								
36									8:40:54.589	TRIP	Deasserted	unlatch trip M2
37												

Fig. 20. Time-Aligned SER Data From Main 1, Main 2, and Tie Relays

Initially, all voltages are healthy (3P59 indicates local voltage, RMB3A or RMB3B indicates remote healthy sources). At 8:40:44.368, all voltages go dead (below 10% threshold). This initiates the transfer sequence (SV6T). At 8:40:54.383, S1 returns healthy. However, S2 is not yet back, so as soon as RMB3B asserts (i.e., S1 healthy), the M2 trip (SV2T) asserts. Two cycles later, S2 returns healthy, but the M2 trip has already been asserted. Tie Breaker T does not close because S2 has returned healthy before the transfer occurs.

1) Problems and Troubleshooting:

- Problem 1: Breaker M2 should not have tripped.
  - If S2 had come back at the same time as S1, then the M2 trip would not have asserted, based on the element operate and processing times.
  - In other words, Problem 1 would not have happened if S2 returned healthy less than 1.38 cycles after S1.
- Problem 2: After M2 tripped, Breaker T did not close.
  - The breaker simulator in this scheme uses a 2.52-cycle breaker operate time.
  - It takes 4.86 cycles from when S1 becomes healthy to when the tie recognizes that M2 is open (including the 2.52-cycle breaker trip time).
  - For the tie to close, M2 must be sensed open by the tie before S2 voltage is sensed healthy.
  - In other words, Problem 2 only happens if S2 comes back approximately 1.38 cycles to 4.86 cycles after S1.

2) Solutions:

- Supervise tripping of M2 until S1 is sensed healthy for some qualifying time. Logically, we move the RMB3A (or RMB3B) from the SV2T logic to the SV6T logic (SV6T pickup delay = 120 cycles).
- Latch the main breaker trip to ensure the tie closes. Logically, we add a dropout delay greater than the breaker operate time to SV2T (e.g., 12 cycles). This ensures that the transfer is forced to occur even if the transfer conditions (SV6T) reset before the breaker is actually open.

The updated logic is shown in Fig. 21 and Fig. 22.

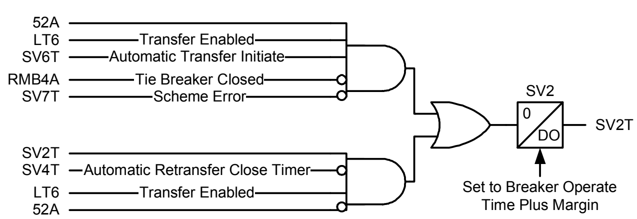


Fig. 21. New Main Breaker Trip From Automatic Transfer Logic

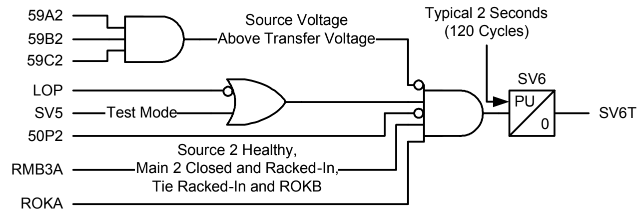


Fig. 22. New Main Breaker Transfer Initiate Logic

VI. References

[1] C. Araujo, F. Horvath, and J. Mack, "A Comparison of Line Relay System Testing Methods," presented at the 33rd Annual Western Protective Relay Conference, Spokane, WA, October 2006.

[2] J. R. Fairman, K. Zimmerman, J. W. Gregory, and J. K. Niemira, "International Drive Distribution Automation and Protection," presented at the 27th Annual Western Protective Relay Conference, Spokane, WA, October 2000.

[3] D. Costello, "Lessons Learned Through Commissioning and Analyzing Data From Transformer Differential Installations," presented at the 33rd Annual Western Protective Relay Conference, Spokane, WA, October 2006.

VII. Biographies

Karl Zimmerman is a senior application engineer with Schweitzer Engineering Laboratories, Inc. in Belleville, Illinois. His work includes providing application support and technical training for protective relay users. He is an active member of the IEEE Power System Relaying Committee and is the chairman of the Working Group on Arc-Flash Protection. Karl received his BSEE degree at the University of Illinois at Urbana-Champaign and has over 20 years of experience in the area of system protection. He is a past speaker at many technical conferences and has authored over 20 papers and application guides on protective relaying.

Previously presented at the 2008 Texas A&M
Conference for Protective Relay Engineers.

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