Multifunction Relays and Protection Logic Processors in Distribution Substation Applications

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Original edition released November 2005

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***Abstract*—Digital technology has evolved, giving rise to the development of multifunction relays that provide several protection functions simultaneously, in addition to performing control, measurement, and communications functions. For these reasons, multifunction relay applications go beyond traditional protection and solve specific protection and control problems. These devices can be used extensively in distribution substations—which, in general, lack bus differential protection, breaker-failure backup, and automatic transformer restoration systems—as well as for loss-of-coordination conditions caused by simultaneous faults. These limitations of traditional protection and control schemes impact power system restoration time and deteriorate primary equipment lifetime. The purpose of this paper is to describe problems found in distribution systems that lack the schemes mentioned above, and to recommend solutions based on the application of multifunction relays and protection logic processors.**

Keywords: Fast bus tripping, simultaneous faults, breaker failure backup protection, distribution systems.

I. Introduction

Electric power supply reliability in a distribution system is measured as the availability of electric power to the customers. To improve this availability, it is important to take the following factors into account:

1. Normal operation of the distribution system: service interruptions must be minimized.
2. Fault prevention: distribution systems must be designed to minimize faults. This requires an adequate trade off between cost and reliability.
3. Reduction of the negative consequences of faults: protection must be adequate to minimize equipment damage and the number of circuits that lose service as a result of faults.

In designing distribution protection, control, and metering systems, we need to deal with conflicts between the reliability requirements mentioned above. A limiting factor is technology: old relay designs had limited control and communications capabilities; often, modern multifunction relays are applied following traditional philosophies, which results in not using the relays to their full potential. For example, it is still common today to find operation and control philosophies that prioritize service continuity over primary equipment wear.

The application of multifunction relays in distribution protection, control, and metering systems provides better technical solutions to existing problems, with lower cost and higher reliability. Multifunction relays, combined with protection logic processors through programmable logic, reduce and simplify wiring, and help resolve protection, control, and operation problems at no additional cost. Applications that benefit from using a combination of multifunction relays and protection logic processors are:

- Bus protection.
- Breaker failure backup protection.
- Protection for simultaneous faults.
- Automatic restoration of electric power to an unfaulted transformer.

II. Bus Protection

Distribution substations typically have four to eight feeders connected to the bus (see Fig. 1). During a bus fault, it is possible to have a fault current between 4000 and 8000 A. The fault must be cleared as soon as possible to avoid equipment damage, particularly to protect power transformers.

The use of bus differential protection is extremely expensive at medium voltage (13.8, 23, and 34.5 kV). Application of overcurrent relays for bus protection has been limited because of the need for a current transformer winding from each feeder; this solution also compromises feeder-protection coordination. The most common practice is to clear bus faults with transformer backup protection, which has a time delay to coordinate with feeder protection. For this reason, bus faults are not cleared instantaneously; clearing times are typically between 0.6 and 1.0 seconds. However, because of the potential costs of bus faults, it is very important to clear these faults instantaneously.

With the traditional bus protection philosophy mentioned above, the power transformer, which is the most important and expensive element in the substation, can experience reduced operating life because of high fault current and the number and duration of bus faults. Theoretical overcurrent limits for power transformers are defined in ANSI C57.92-1962 [1] standard, which gives information about the transformer short-term thermal overload capacity and does not consider mechanical wear. ANSI-IEEE C57.109-1993 [2] standard considers both the thermal and mechanical wear. Analysis of these documents indicates that power transformer lifetime can be extended with bus protection schemes that clear faults instantaneously.

Another drawback of present bus protection schemes is the long service restoration time. If, in the typical substation shown in Fig. 1, Fault F1 occurs, Circuit Breaker A will trip. Once Circuit Breaker A is open, the operator ignores whether the service interruption is due to a bus fault or the result of a backup protection operation for a feeder fault (Fault F2). Consequently, the operator's strategy is to open the eight feeder circuit breakers to locate the fault and to start the restoration process. Once all circuit breakers are open, Circuit Breaker A is closed again, as a test, to identify whether there is a bus fault. If Circuit Breaker A trips again, there is a bus fault, but in this process the transformer is again exposed to fault current, and load continues to be out of service. For the substation depicted in Fig. 1, we estimate that it takes about ten minutes to identify a bus fault; this period does not include the total load restoration time.

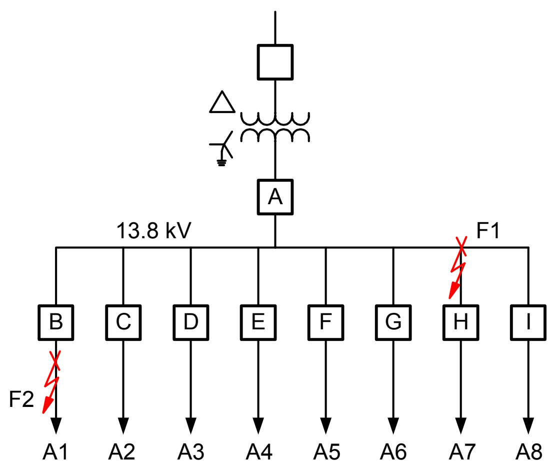

Fig. 1. Typical distribution substation.

An economical solution to this type of fault, other than bus-differential protection, is a high-speed bus-tripping scheme. This scheme can be implemented using the multifunction relay of the transformer low-voltage-side breaker and the feeder multifunction relays, combined with a protection logic processor. The protection logic processor makes tripping decisions based on relay information collected through communications channels.

Fig. 2 shows a 13.8 kV distribution substation equipped with the relays and protection logic processors required to implement fast bus tripping through programmable logic. Fig. 3 shows a fast bus tripping logic diagram. This logic uses the phase (50P) and ground (50G) instantaneous overcurrent elements of the transformer low-voltage-side multifunction relay; these elements are set to detect a bus fault. The output logic variables from the instantaneous overcurrent elements are sent via communications (TMB2A) to the protection logic processor and are used as tripping signals. The logic also uses the phase (50P) and ground (50G) instantaneous overcurrent elements of the feeder relays; these elements are set with a pickup current above the feeder maximum load current. The tripping output logic variables of the feeder instantaneous overcurrent elements are sent via communications (TMB2A) to the protection logic processor and are used as blocking signals. The following discussion analyzes operation of the fast bus tripping scheme for both bus and feeder faults.

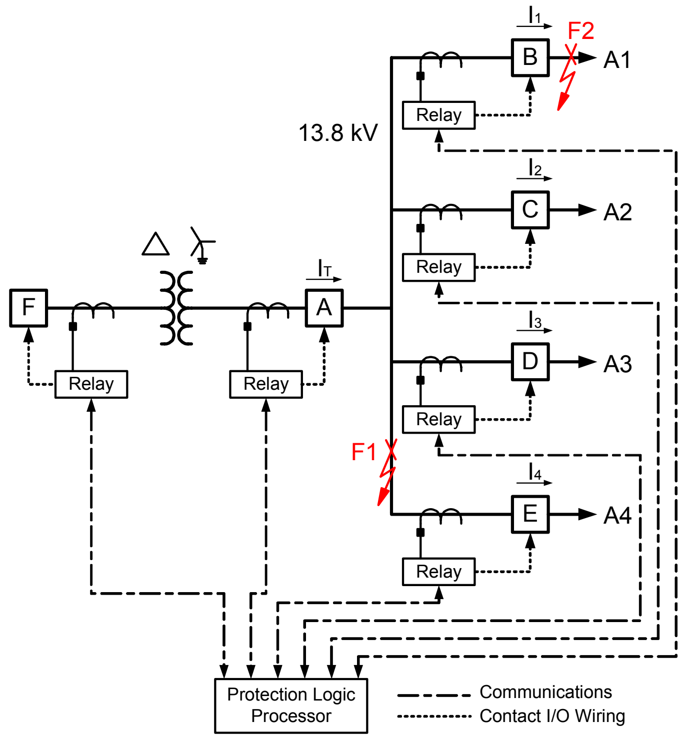

Fig. 2. Distribution substation equipped to implement fast bus tripping and breaker failure backup protection (50BF).

1. Fault F1 at the bus. During this fault, feeder overcurrent elements do not pick up, so no blocking signals are sent to the protection logic processor. However, the phase and/or ground instantaneous overcurrent elements of the transformer low-voltage-side multifunction relay pick up (I_T is greater than 50P and/or 50G). Transformer relay output signals apply to an OR gate and get a three-cycle security delay to convert into the SV1T signal, which applies to an AND gate, as shown in Fig. 3. As the blocking signals are not asserted (R2P5…R2P8 = 0) and signal SV1T is high (SV1T = 1), the logic declares the fault to be at the main bus. For this reason, the protection logic processor sends tripping signals to all the feeder relays and to the transformer low-voltage-side relay to open all the circuit breakers associated with the bus.
2. Fault F2 at Feeder A1. The A1 feeder relay instantaneous overcurrent elements pick up for this fault (I_1 is greater than 50P and/or 50G) and send a blocking signal to the protection logic processor (R2P5 = 1). The transformer multifunction relay phase and/or ground instantaneous overcurrent elements also pick up (I_T is greater than 50P and/or 50G); after three cycles, logic variable SV1T goes high (SV1T = 1). Based on this information, the protection logic processor AND gate does not send any tripping signal to the relays. The fault is then declared to be at Feeder A1, and the fast bus tripping logic does not operate.

The fast bus tripping scheme clears faults in three cycles plus the circuit breaker operating time. This accounts for an overall fault-clearing time much shorter than that of traditional schemes. In addition, this logic allows discrimination between a bus fault and a feeder fault, and the ability to issue an alarm. The alarm provides the operator with the necessary information to quickly and safely restore service to the loads.

III. Breaker Failure Backup Protection (50BF)

At medium-voltage level distribution substations, such as 13.8 kV, protection philosophies do not consider local backup protection, so breaker-failure backup (50BF) protection is not applied. This causes long breaker operation times and selectivity problems. For example, when there is a feeder fault (see Fig. 2) and the breaker fails to operate, the most common practice is to clear the fault with the transformer backup protection. This protection is coordinated with the feeder protection, which has a very large operating time (i.e., seconds) that depends on the magnitude of the fault current. In addition, transformer breaker tripping causes service interruption to all feeder loads. This means that the effect of a breaker failure on selectivity is similar to the result of a bus fault.

As a result, the transformer wears faster and the restoration time is large, as explained before for the fast bus tripping scheme. Because traditional schemes do not provide information about the type of fault, operators need to discriminate between bus faults and feeder backup protection operations.

The protection scheme can be improved by using a combination of multifunction relays and a protection logic processor (see Fig. 2) to implement the breaker failure backup logic (50BF) presented in Fig. 4. This logic uses phase (50P) and ground (50G) instantaneous overcurrent elements from the feeder and the transformer low-voltage-side multifunction relays; these overcurrent elements serve as fault detectors. Feeder fault detector pickup current must be set up above the feeder maximum load current; the transformer low-voltage-side fault detectors must have a pickup current greater than the transformer normal operating current. The logic requires a timer to coordinate the scheme with the feeder protection; the timer is setup with an operating time equal to the sum of the relay and breaker operating times, and the fault detector reset time, plus a security margin. We will analyze feeder and bus faults in the circuit depicted in Fig. 2 to explain the operation of the breaker failure logic.

When Fault F2 occurs at Feeder A1 (see Fig. 2), the A1 feeder primary protection trips, so the breaker failure backup logic shown in Fig. 4 starts (enables the AND gate). The logic operation is supervised by the two current detectors, which, through an OR gate, create the other input to the AND gate. If the feeder primary protection tripped (SV13 = 1), but there is still fault current at the feeder (50P = 1 and/or 50G = 1), the circuit breaker must have failed to operate. Consequently, the logic sends a second tripping signal to the circuit breaker, which, after a time delay, becomes the logic variable SV10T. If the circuit breaker does not trip at this time, and the A1 feeder primary protection and the current detectors remain operated after a time delay set in the SV12T logic variable, the protection logic processor receives information. The protection logic processor communicates with the feeder relays and with the transformer low-voltage-side relay to have them trip all the circuit breakers associated with the bus.

When Fault F1 occurs at the bus (see Fig. 2), the transformer low-voltage-side relay operates, either due to the fast bus tripping protection scheme or to the backup protection scheme. This initiates the breaker failure backup protection logic shown in Fig. 4. The logic operation is similar to that explained in the case of Fault F2. The only difference is that in this case the protection logic processor also sends a signal to the transformer high-voltage-side relay, which trips the high-voltage circuit breaker.

The breaker failure backup logic (50BF) clears the fault in a much shorter time than transformer backup protection schemes, whether it is on the low-voltage-side (feeder backup protection), or on the high-voltage-side (transformer backup protection). This reduces transformer wear and improves transformer lifetime. In addition, the breaker failure backup logic quickly identifies a bus fault and issues an alarm. With this information, the operator may take immediate action, which reduces substation restoration time.

IV. Protection Against Simultaneous Faults

The need to improve service availability has increased the complexity of distribution network topology. In distribution systems, during preventive or corrective maintenance works, or in abnormal network conditions, switching operations often leave several circuits fed from a single source. Furthermore, limitations on the rights of way make it necessary to use double-circuit overhead lines or single-circuit lines that run close to each other. All these factors have increased the frequency of distribution system faults that involve more than one circuit. These faults are known as simultaneous faults.

During simultaneous faults in distribution systems, the transformer low-voltage-side backup protection may misoperate. This impairs protection selectivity and affects service availability in circuits not involved with the fault. The cause of this possible misoperation is that the transformer low-voltage-side overcurrent relay measures the total fault current (sum of the currents on all the faulted circuits) plus the load currents from the unfaulted circuits, while the overcurrent relay of each faulted feeder measures only the feeder fault current. As a result, the transformer low-voltage-side inverse-time relay measures a current that is greater than the current measured by the inverse-time feeder relay; then, the transformer relay may trip faster than the feeder relay.

It is important to remember that the most critical condition for coordinating these two inverse-time overcurrent relays occurs at the maximum fault current (the same current value for both relays). This is the condition for which both curves have the minimum separation, corresponding to a typical coordination interval between 0.2 and 0.4 seconds.

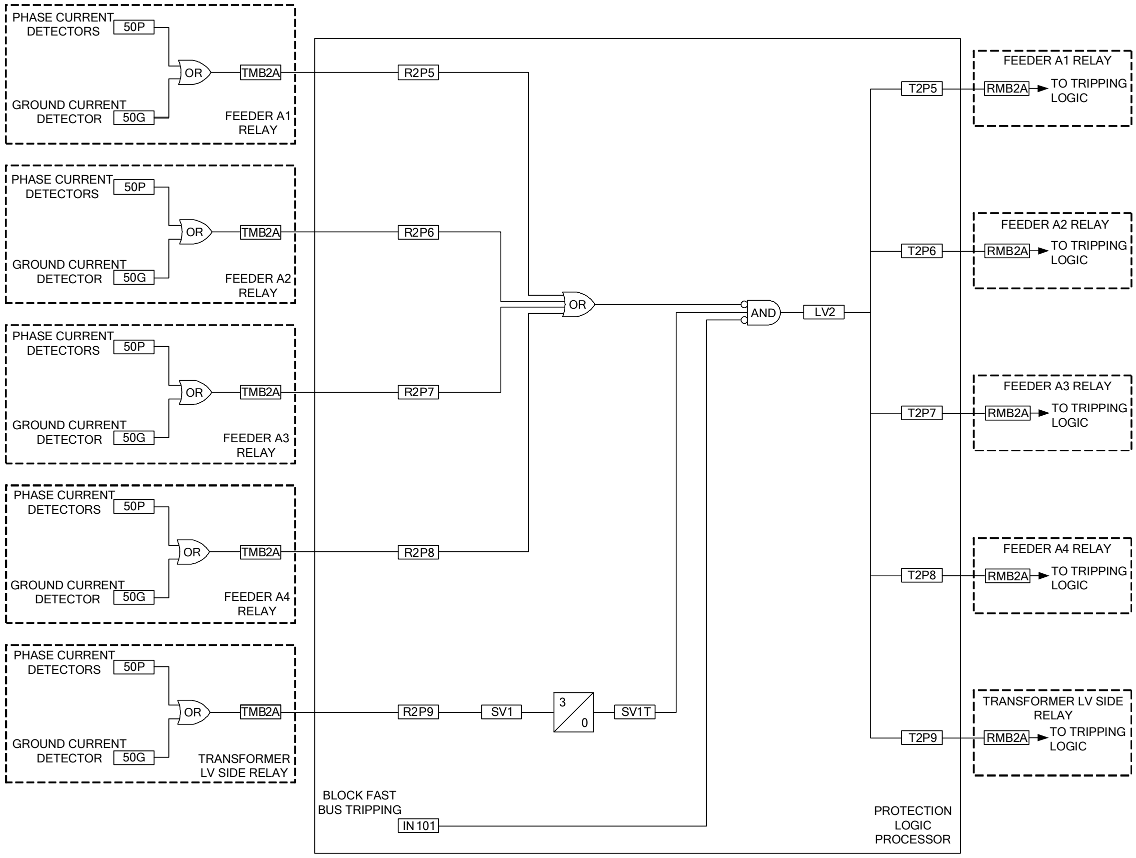

Fig. 3 Fast bus tripping protection logic.

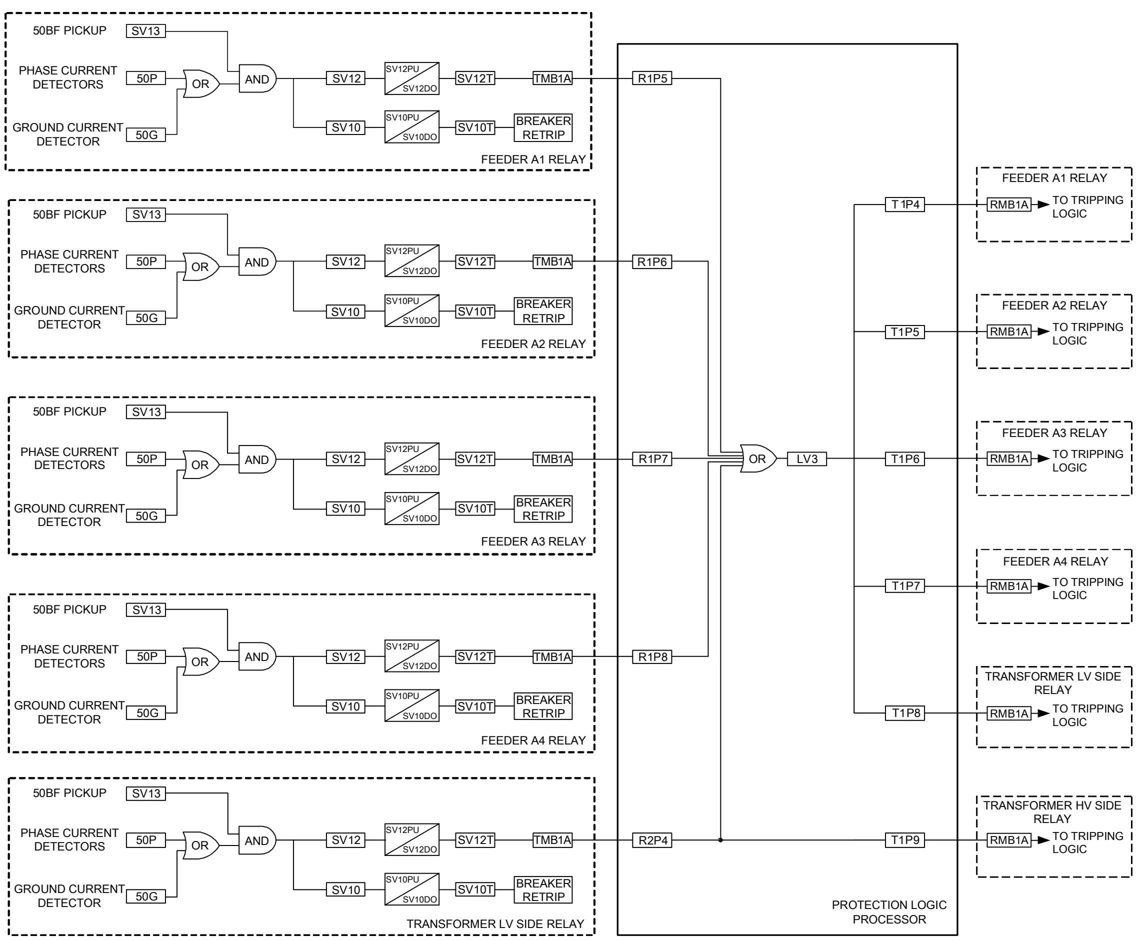

Fig. 4. Breaker failure backup protection logic (50BF).

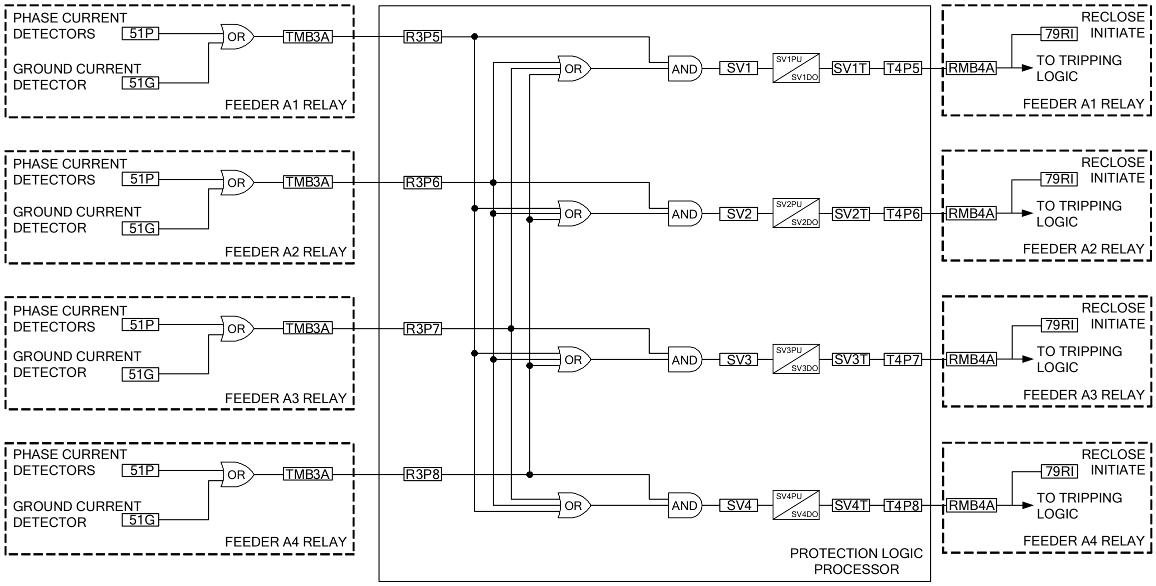

Fig. 5. Logic for protection against simultaneous faults.

Fig. 5 depicts the logic diagram of a protection scheme that solves the problem of misoperation due to simultaneous faults. When a simultaneous fault occurs, for example, in Feeders A1 and A2, the 51P and/or 51G elements of these feeders operate and send this information to the protection logic processor. The protection logic processor, after a security delay of three cycles, declares that the two feeders have a simultaneous fault, by activating the logic variables SV1T and SV2T. Each one of these variables starts the tripping logic of the corresponding feeder relay. The almost instantaneous breaker operation at the faulted feeders guarantees coordination with the transformer low-voltage-side relay. Because the type of fault is already known, at the time of tripping the feeder breakers, we can also start a reclosing logic to attempt automatic power restoration.

In the same way as with the fast bus tripping and breaker failure protection schemes, in this case the operator receives an alarm stating the type of fault. With this information, the operator can take the appropriate actions to guarantee fast service restoration.

V. Automatic Restoration of Electric Power to an Unfaulted Transformer

In some distribution substations (see Fig. 6), a single source feeds two transformers through one circuit breaker. The transformers lack circuit breakers on their high-voltage-side. Instead, they have motor-driven disconnects. In a traditional protection and control scheme, for an internal fault on either one of the transformers, the faulted transformer protection operates and sends a tripping signal to the main circuit breaker through a lockout relay (86T). This operation interrupts service to the load of both transformers until personnel arrive at the substation to restore the lockout relay (86T), isolate the faulted transformer, and restore electric power to the unfaulted transformer. For this reason, the restoration time depends on the personnel travel time to the substation.

Using multifunction relays and a protection logic processor, it is possible to automatically isolate the faulted transformer and to restore the unfaulted transformer. Fig. 7 depicts the automatic restoration logic. The protection logic processor receives signals 86T1 and 86T2 indicating the operation of transformer lockout relays. The protection logic processor also receives signals indicating the status of the main circuit breaker and of the motor-driven disconnects located at the high-voltage-side of each transformer. The high-voltage-side multifunction relay of each transformer controls the corresponding motor-driven disconnect and the closing circuit of the main circuit breaker. The transformer high-voltage-side multifunction relays maintain communication with the protection logic processor.

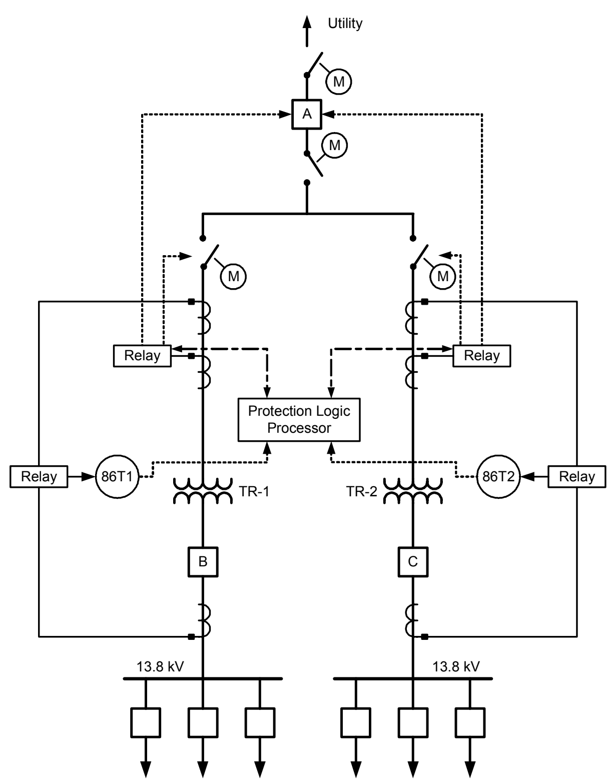

Fig. 6 Distribution substation with only one main circuit breaker on the high-voltage side of two transformers.

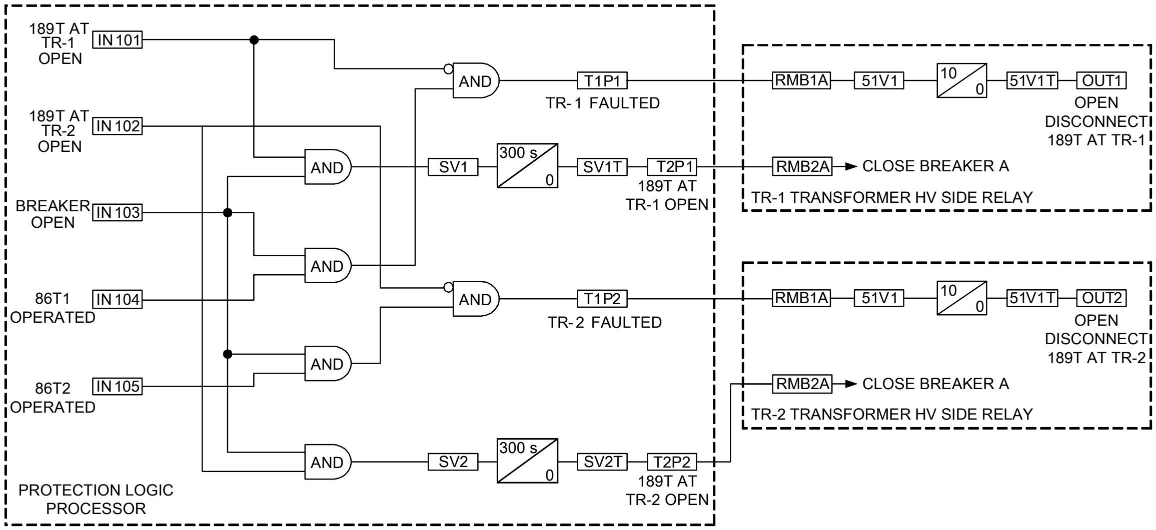

Fig. 7. Logic for automatic restoration of electric power to an unfaulted transformer.

When an internal fault occurs at Transformer TR-1 (see Fig. 6), the transformer differential relay (87T) operates and, via the 86T1 lockout relay, trips the main high-voltage-side breaker and the faulted transformer low-voltage breaker, and also sends this information to the protection logic processor. The protection logic processor (see Fig. 7) confirms that the main circuit breaker is open (IN103 = 1) and that the faulted transformer is Transformer TR-1 (detects that 86T1 operated, IN104 = 1). The protection logic processor sends a signal (T1P1) to the transformer high-voltage-side relay to open the motor-driven disconnect, which isolates the faulted transformer automatically. After this, the protection logic processor checks (through SV1T) for the following 300 seconds that the faulted-transformer high-voltage-side disconnect keeps open (IN101 = 1) and that the main circuit breaker is also open (IN103 = 1). Once the 300-second timer expires, the protection logic processor sends a signal (SV1T = 1) to the TR-1 high-voltage-side relay, for this relay to send a closing signal to the main circuit breaker; this operation restores electric power to Transformer TR-2.

VI. Conclusions

1. The use of multifunction relays combined with a protection logic processor in distribution substations allows engineers to design protection and control schemes that reduce fault and service restoration times.
2. The reduction of fault-clearing time increases the transformer lifetime and reduces voltage sag duration. This, together with a shorter restoration time, improves power quality and electric service reliability.
3. Fast bus tripping protection logic reduces bus fault clearing time from seconds to cycles. Service restoration time is also reduced.
4. Breaker failure backup protection logic (50BF) reduces the duration of faults where the feeder circuit breaker or the transformer low-voltage-side relay fails to operate. It also reduces the service restoration time.
5. The logic for protection against simultaneous faults prevents transformer low-voltage-side breaker misoperations. This improves service quality by avoiding unnecessary service interruptions to the unfaulted feeders.
6. The logic for automatic restoration reconnects electric power to an unfaulted transformer in distribution substations having two transformers that share the main circuit breaker. This reduces service restoration time from hours to minutes.

VII. References

[1] ANSI C57.92-1962, *American National Standard Guide for Loading Oil-immersed Distribution and Power Transformers.*

[2] IEEE Std. C57.109-1993, *IEEE Guide for Liquid-Immersed Transformer Through-fault-current Duration.*

VIII. Biographies

David Sánchez Escobedo received his BSEE from the University of Guanajuato, México in 1994. He worked for four years in Guadalajara at Comision Federal de Electricidad (the Mexican electric utility company) in the Protection Department, in charge of commissioning services, electrical substation maintenance, relay settings calculation, and relay testing. Between 1996 and 1998, he was an Electrical Engineering graduate student at the University of Guadalajara. In 1998, he worked as a professor for the Autonomous University of Guadalajara. Between 1998 and 2000, he also worked for INELAP-PQE as a protection systems design engineer. He joined Schweitzer Engineering Laboratories, S.A de C.V. in August 2000. As a member of the SEL Engineering Department, he designs protection panels, integrated systems, and modular control houses, and also conducts training for utilities and other industries on SEL products.

Eliseo Alcázar Ramírez received his BSEE degree from the Oaxaca Technological Institute in 1998. Between 1999 and 2001, he was the director of the Protection, Control and Metering Department of the Southeastern Distribution Division of Comision Federal de Electricidad in Tehuantepec, Mexico. Between 2001 and 2004, he was the director of the Protection Office of the Southeastern Distribution Division of Comision Federal de Electricidad. During this time, he was engaged in activities of supervision, maintenance, improvement, and commissioning of protection, control, and metering systems. His expertise includes fault analysis, short-circuit studies, protection coordination, and protection system design for electric power systems. Since April 2004, he has worked as a protection engineer for Schweitzer Engineering Laboratories, S.A de C.V., in Monterrey, Mexico. His activities include protection, control, and metering system design and commissioning, as well as technical support and training for engineers from utilities and other industries on SEL products.

Oscar Arturo Márquez Villanueva received his BSEE degree in 1984 from the Instituto Tecnológico de Aguascalientes. Between 1985 and 1999, he worked at Comision Federal de Electricidad in transmission system protection. In addition, between 1988 and 1991, he taught at the Electromechanical Engineering School of the University of Colima. He was the instructor of the course named "Extra-High Voltage Lines" at the Western Training Center of Comision Federal de Electricidad between 1991 and 2000. In 1999 and 2000, he also worked for INELAP-PQE as the Commissioning Services Manager. Since 2000, he has worked for Schweitzer Engineering Laboratories, S.A. de C.V. in Monterrey, Mexico, as a protection engineer. He designs protection panels, integrated systems, and modular control houses, and also conducts training for utilities and other industries on SEL products.

Héctor Jorge Altuve Ferrer received his BSEE degree in 1969 from the Central University of Las Villas, Santa Clara, Cuba, and his Ph.D. in 1981 from Kiev Polytechnic Institute, Kiev, Ukraine. Between 1969 and 1993, Dr. Altuve was a professor of the Electrical Engineering School at the Central University of Las Villas. From 1993 to 2001, Dr. Altuve served as a Ph.D. Program professor at the Mechanical and Electrical Engineering School of the Autonomous University of Nuevo León, in Monterrey, Mexico. Between 1999 and 2000, he was the Schweitzer Visiting Professor at Washington State University's Department of Electrical Engineering. In 2001, he joined Schweitzer Engineering Laboratories as a Senior Research Engineer based in Monterrey, Mexico. In November 2001, Dr. Altuve became the General Director of Schweitzer Engineering Laboratories, S.A. de C.V., the SEL subsidiary in Mexico. His main research interests are in power system protection, control, supervision, and metering. He is an IEEE Senior Member and a Distinguished Lecturer of IEEE Power Engineering Society.

Alexis Martínez del Sol was born in Cienfuegos, Cuba in 1964. He received his Ph.D. in Electrical Engineering in 1997 from the Central University of Las Villas, Cuba. From 1987 to 1999, he worked for the Electrical Engineering School of the Central University of Las Villas, where he served as an Assistant Professor and Director of the Electric Power Department between 1997 and 1999. Since 1999, he has worked as a Level C Professor-Researcher of the Mechanical and Electrical Engineering Department at the University of Guadalajara. His research area is the control, design, and protection of electric motors.

20051115 • TP6229-01