Securing Sequence-Current Differential Elements

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SECURING SEQUENCE-CURRENT DIFFERENTIAL ELEMENTS

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INTRODUCTION

Protection engineers are very familiar with the concept of the impact of current transformer (CT) saturation on current differential protection during an external fault. Saturation of one CT during an external fault will create a "false" differential current that could cause an undesired relay trip. This basic principle is applicable whether the protected element is a power transformer or a transmission line.

Much less known and understood is the impact of CT saturation on current differential protection when considering negative- or zero-sequence current differential elements. The main advantage of sequence-current differential elements (87L0 or 87L2) is that they substantially improve the sensitivity of the relay or its capability to respond to resistive faults. This advantage relieves the need for segregated phase-current differential elements to detect resistive faults and allows them to be optimized for multiphase faults. This paper uses the alpha or current-ratio plane to explain and demonstrate why sequence-current differential elements tend to be much less stable than phase-current differential elements when external faults with CT saturation occur.

First, we will review differential characteristics implemented in the current-ratio plane and their relation to the conventional percentage differential principle. Then, we will present an original analysis, describing why the two mathematical operations involved in the computation of zero- and negative-sequence currents can render the corresponding sequence-current differential elements completely unstable even at moderate levels of CT saturation during an external fault. Finally, we will introduce a CT saturation mitigation technique for these sequence-current differential elements that makes them much more secure and reliable.

REVIEW OF THE ALPHA-PLANE CHARACTERISTICS OF LINE CURRENT DIFFERENTIAL PHASE AND SEQUENCE ELEMENTS

Roberts et al. [1] introduced the concept of the digital characteristic implemented into the current-ratio plane for line current differential elements as shown in Figure 1. Basically, the concept consisted of computing the ratio of the remote current, I_R, (phase or sequence current) over the local current, I_L, and verifying that the ratio lay inside the shown stability area. When no internal fault exists, the ratio is close to the minus one point (–1,0). There are two settings for this characteristic, the radius of the greater arc (typically between 6 and 10) and the angle subtended by the arc (typically between 160 and 210 degrees). This newly defined characteristic is an improvement with respect to the so-called "rainbow" characteristic [2] because of its total digital implementation and the additional control over the angle that was set to a fixed value of 180 degrees in the original concept.

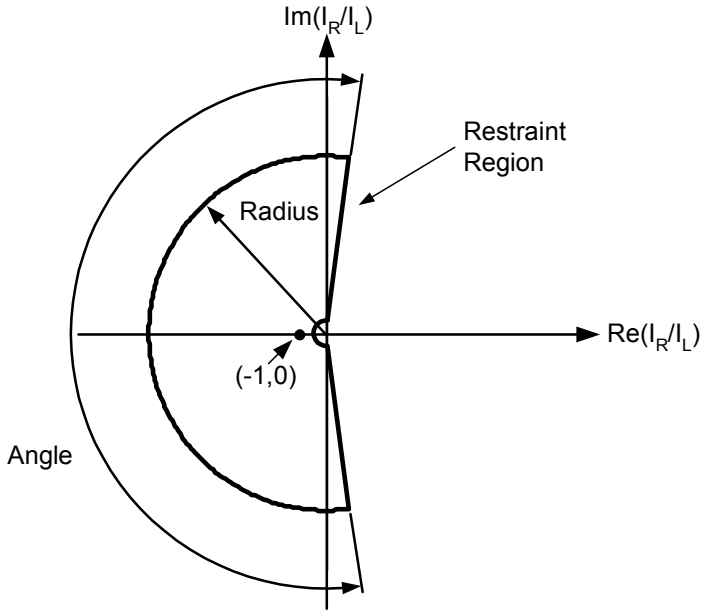


Figure 1 Current Differential Restraint Characteristic on the Alpha Plane

It should be remembered that the technique of mapping a conventional percentage differential characteristic into the current-ratio plane is an old concept [3] that has been used to study the performance of differential characteristics. Closed-form solutions that represent conventional percentage differential characteristics on the alpha plane were developed [1]. Closed-form solutions apply to specific instances of operate and restraint current quantities. No closed-form solution was found for other operate and restraint quantities. If a closed-form solution cannot be found, it is still possible to find the equivalent alpha-plane representation of any current differential relay [4].

As an example, the operate characteristic shown in Figure 2 can be mapped to the alpha-plane characteristics shown in Figure 3 and Figure 4 through the use of the technique described in [4]. For comparison, Figure 3 and Figure 4 also show the restraint region depicted in Figure 1 with typical dimensions of Radius = 6 and Angle = 195 degrees.

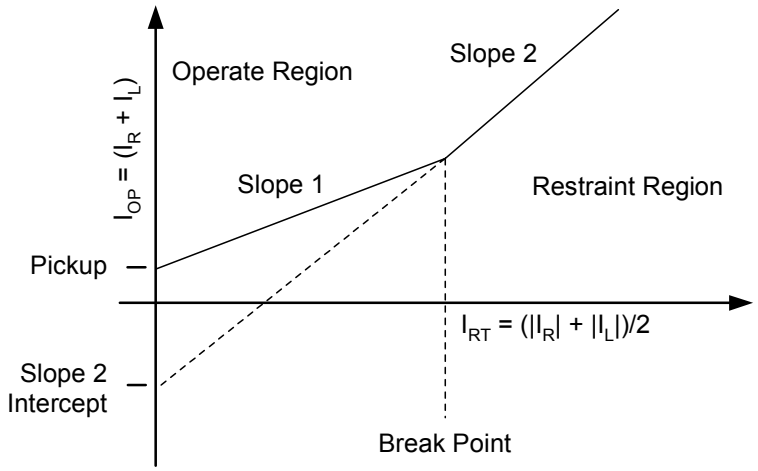


Figure 2 Traditional Dual-Slope Current Differential Operate Characteristic

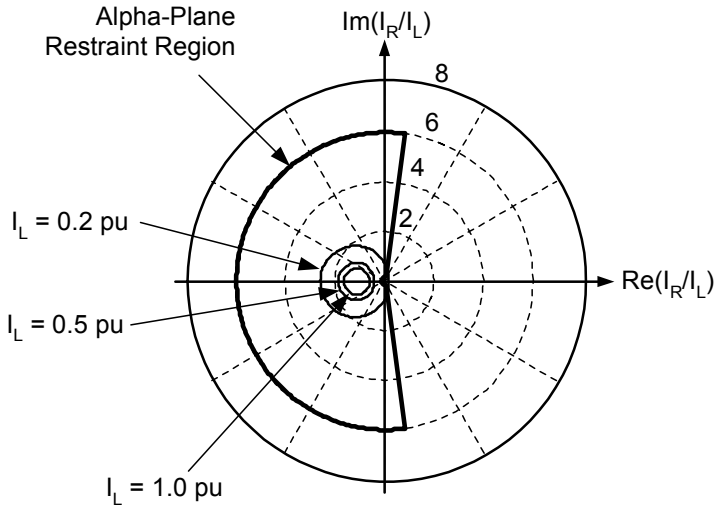


Figure 3 Restraint Region Created by 30 Percent Slope 1 of Figure 1 With 0.2 PU Pickup

Notice in Figure 3 that as local current, I_L, increases from the pickup setting of 0.2 per unit to 1.0 per unit, the restraint region shrinks. Thus, the characteristic shown in Figure 1 gives decreasing tolerance for errors when local current increases, the opposite effect expected for the 30 percent slope.

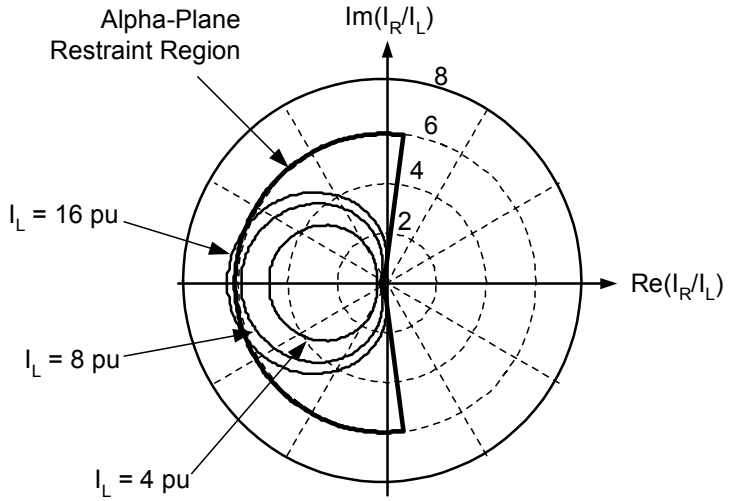


Figure 4 Restraint Region Created by 150 Percent Slope 2 of Figure 1 With 2.0 PU Break Point

Figure 4 shows that as local current increases from 4 per unit to 16 per unit, the restraint region increases in size, as expected. Paradoxically, as the local CT saturates, the measured local current decreases and the restraint region shrinks, making misoperation more likely.

In all cases, the alpha-plane restraint region shown is more tolerant of measurement errors.

PROPERTIES AND JUSTIFICATION OF LINE CURRENT DIFFERENTIAL RELAY SEQUENCE ELEMENTS

This paper addresses certain security concerns regarding negative- and zero-sequence current differential elements. The easiest way to secure an element is to turn it off or exclude it. Therefore, the existence of these elements must be justified.

The main reason to include sequence-current differential elements in a relay is to allow the relay to use a large, static restraint region, such as that shown in Figure 1, for the phase-current differential elements. This large restraint region makes the phase-current differential elements very secure, so they can also be designed for very high-speed operation.

Consider a relay with a negative-sequence current differential element. That element will reliably detect ground and phase-to-phase faults. The phase-current differential element need not detect ground or phase-to-phase faults. It can instead be optimized for fast, secure, and reliable operation during three-phase faults. That optimization includes the use of a large, static restraint region on the alpha plane.

Similarly, a relay with a zero-sequence current differential element can contain phase-current differential elements optimized to detect phase-to-phase and three-phase faults, again with a large, static restraint region. Table 1 shows the required fault type coverage of phase-current differential elements when supported by zero- and negative-sequence current differential elements.

Table 1 Fault Types That Phase Current Differential Element Must Detect

Fault Type	Required Phase Element Coverage Alone	Required Phase Element Coverage When Supplemented by Zero-Sequence Element	Required Phase Element Coverage When Supplemented by Negative-Sequence Element
Phase to Ground	X		
Phase to Phase to Ground	X		
Phase to Phase	X	X	
Three Phase	X	X	X

To help quantify this argument, consider a ground fault on the system depicted in Figure 12. We set the source angle at 15 degrees to deliver 1,000 A of load current. We then applied a 1,000 A ground fault at midline. The ground fault gave the currents and current ratios shown in Table 2.

Table 2 Phase Currents and Ratios During 1,000 A Ground Fault

Phase	Current at S (Amps)	Current at R (Amps)	IS/IR
A	532 ∠–178°	1502 ∠–7.2°	2.8 ∠171°
B	992 ∠56°	992 ∠–124°	1 ∠180°
C	992 ∠–66°	992 ∠114°	1 ∠180°

Figure 5 shows the sequence network diagram for this situation. Inspection of Figure 5 shows that a large fault resistance creates zero- or negative-sequence current that is small compared to positive-sequence current, I1. Phase current is, therefore, dominated by I1. As positive-sequence current flows past the fault point and exits the right side of the line, so does phase current. This produces the A-phase outflow condition shown in Table 2. Outflow creates a phase-current ratio that lies in the left half of the alpha plane. A phase-current differential element with a restraint region shown in Figure 1 will restrain for this internal fault.

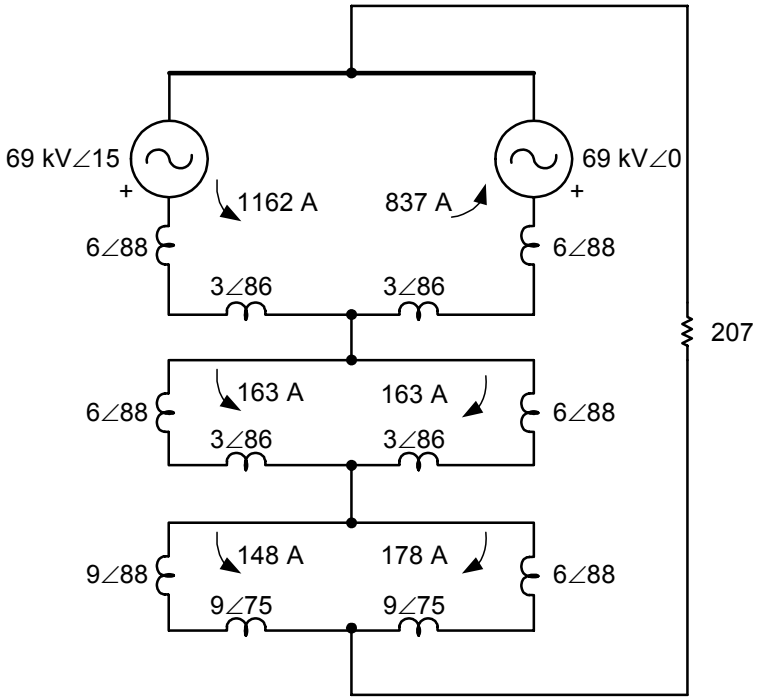


Figure 5 Sequence Network for Midline Fault on System of Figure 12

Notice that for balanced sources the sequence connection diagram of Figure 5 cannot produce outflow in either the zero- or negative-sequence networks. The zero- and negative-sequence current ratios lie either at the origin (zero infeed) or in the right half of the alpha plane, depending on fault location and source impedances. This is outside the restraint region shown in Figure 1, so zero- and negative-sequence current differential elements will operate for such high-resistance faults.

EFFECT OF CT SATURATION ON A CURRENT PHASOR COMPUTED DIGITALLY

When a CT saturates, the corresponding current phasor, as computed by a digital filtering system, undergoes transformations both in magnitude and phase angle with respect to the true or non-saturated current phasor.

Consider a fault of 20,000 A with an X/R ratio of 11.3 where the current is processed through a CT with the following characteristics.

ANSI voltage: 400 V
Turn ratio: 240
Burden: 2 ohms (purely resistive)

The corresponding saturated secondary current, together with the true current, is shown in Figure 6. Also shown are the magnitudes of both currents as would be acquired by a numerical cosine filtering system. Note that a full-cycle Fourier filter would exhibit similar results. Obviously during the saturation interval, the acquired current magnitude falls short of the true value.

Figure 7 shows the ratio of the saturated current phasor magnitude over the true current phasor magnitude, as a cosine filter filtering system would acquire these magnitudes. Figure 8 shows the phase advance of the saturated current phasor with respect to the non-saturated current phasor.

Figure 7 exhibits a minimum ratio of approximately 0.4, and Figure 8 exhibits a maximum phase angle advance of approximately 57 degrees.

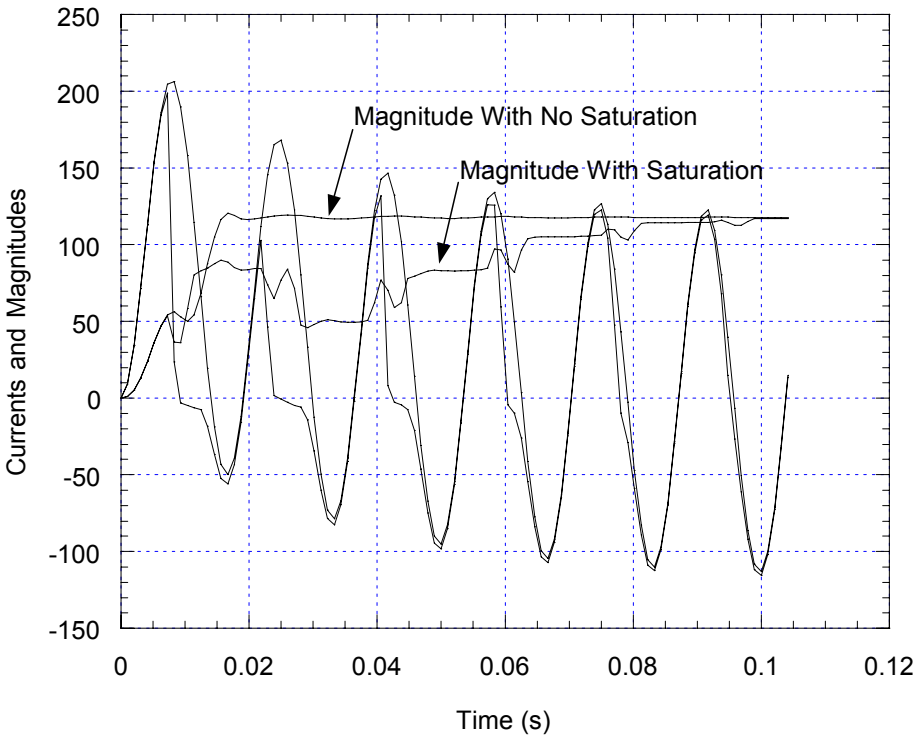


Figure 6 CT Saturation Effect on a Current Phasor Magnitude

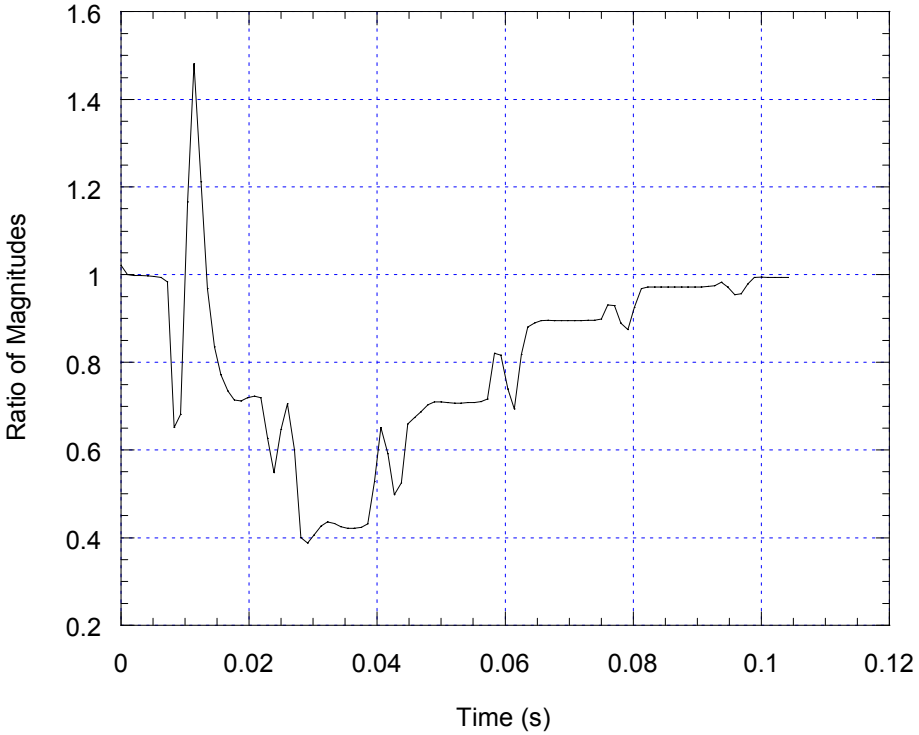


Figure 7 Ratio of Magnitudes of Saturated to True Current Phasor

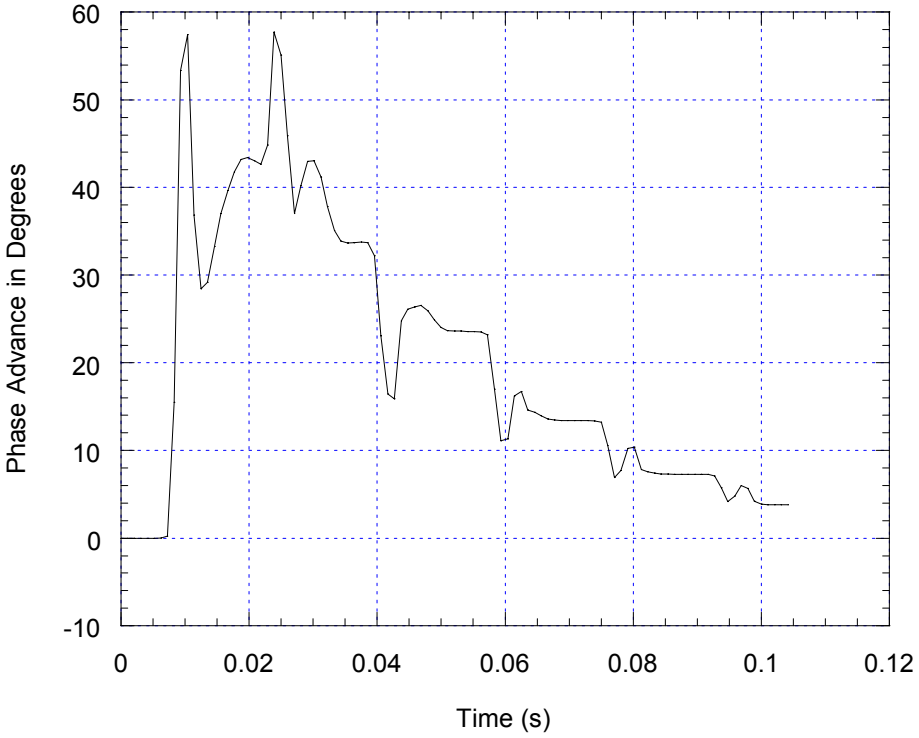


Figure 8 Phase Advance of Saturated to True Current Phasor

We can, with the example of fault current considered (20,000 A, X/R = 11.31), vary the saturation level by changing the CT burden resistance. The time-to-saturate, or the time at which

saturation starts, decreases as the resistive burden increases. As the resistive burden increases, we can record the minimum magnitude ratio and the maximum phase advance. If we plot these two quantities as a function of the time-to-saturate, we obtain the two graphs shown in Figure 9 and Figure 10. On the same graphs, the experience has been repeated with X/R ratios of 6.3 and 25.1.

Figure 9 provides the magnitude ratio for the three X/R ratios considered as a function of the time-to-saturate. As shown, these ratios vary from close to 0 to 1 as the time-to-saturate increases from a few milliseconds to a few cycles. Figure 10 shows the equivalent phase-angle advance of the saturated current phasor. The phase-angle advance goes from beyond 90 to zero degrees as the time-to-saturate varies across the same interval. For both the magnitude and the phase angle, a greater X/R ratio has the effect of making the situation worse in terms of magnitude ratio and phase-angle advance. Note also that the phase-angle advance goes well beyond 90 degrees.

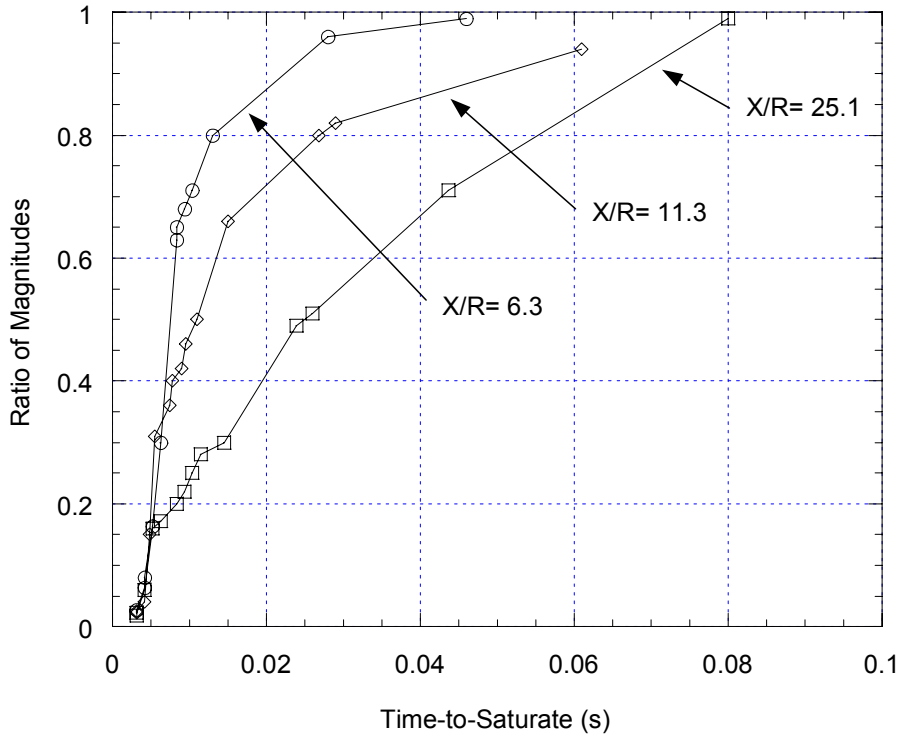


Figure 9 CT Saturation Effect on a Phasor Magnitude

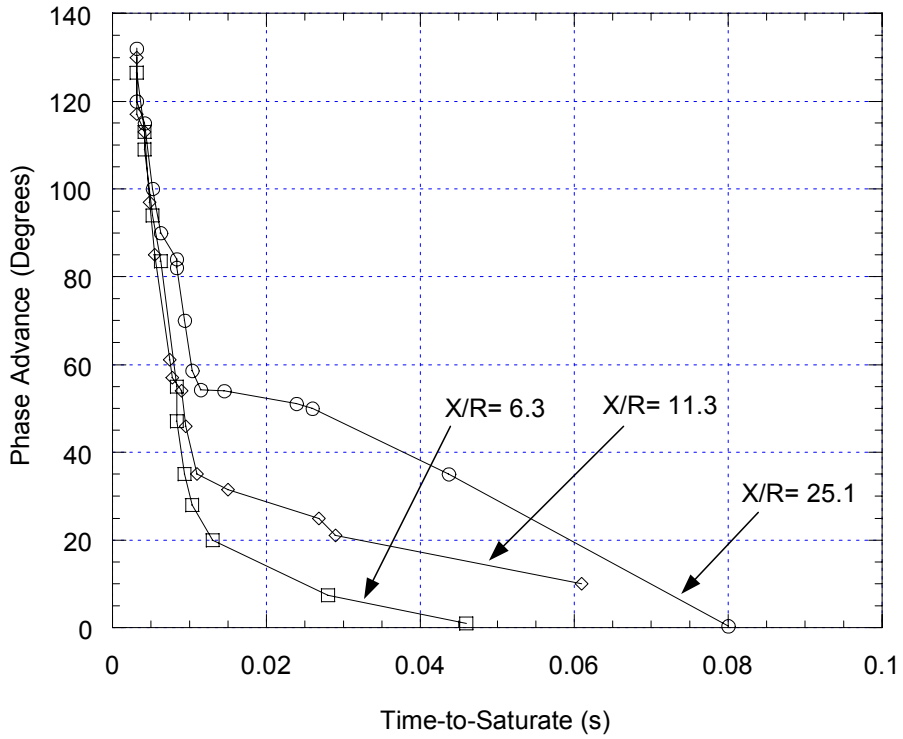


Figure 10 CT Saturation Effect on a Phasor Phase Angle

THE CONCEPT OF A SATURATED CURRENT PHASOR

In digital relays, where phasors are computed through a filtering process, the previous paragraph has shown, that depending upon the level of saturation, the phasor of the saturated current can be defined as a linear transformation on the non-saturated current phasor. This transformation involves a magnitude reduction accompanied by a positive rotation of the phase angle. Saturation is a transient phenomenon, and the parameters of this transformation will vary with time until the magnitude reduction and the phase-angle advance end with disappearance of the saturation. A saturation level can be defined, however, by the minimum magnitude ratio and the maximum phase-angle advance reached during the time the saturation takes place.

Four levels of saturation, from low to extreme, are proposed as convenient definitions. Assuming a true current phasor, IA, the limits of the transformation to be applied to the true phasor to obtain the saturated current phasor, IA_sat, are defined as shown in Table 3 for the four defined levels of saturation.

Table 3 Phasor Transformation as a Function of Saturation Level

Saturation Level	Transformation
Low Saturation	IA_sat = (1–0.9) ∠(0–10)° IA
Moderate Saturation	IA_sat = (0.9–0.5) ∠(10–45)° IA
High Saturation	IA_sat = (0.5–0.2) ∠(45–85)° IA
Extreme Saturation	IA_sat = (<0.2) ∠(>85°) IA

When a CT saturates, the saturation level then will be defined as the one for which the minimum magnitude ratio found in transient state does not get below the ratio defined for the particular saturation level. Alternatively, the maximum phase advance found in transient state should not get above the phase advance defined for the same saturation level.

The concept of a "saturated current phasor" as a linear transformation of the true phasor allows taking into account saturation in equations that model numerical relays in steady state.

IMPACT OF SINGLE CT SATURATION ON AN 87L PHASE ELEMENT

For a numerical line current differential relay, the impact of a single CT saturation during an external fault on a phase current differential element (87LA, 87LB, or 87LC) is easily understood if Figure 1, Figure 9, and Figure 10 are considered. In the situation where there is no saturation, the location of any of the three phase-current ratios, I_R/I_L, will be inside the stability area close to the minus one point (–1,0). If saturation is present on one side of the line, the magnitude of the saturated current phasor will be reduced and it will undergo a rotation in proportion to the saturation level that could go beyond 90 degrees. As a consequence of the transformation imposed on the saturated current phasor during the time interval the saturation occurs, the magnitude of the current ratio will depart from the stable position [close to (–1,0)] and go to values ranging from 0.2 to 5 (depending on how the ratio is performed) for cases of high saturation and an even greater range for extreme situations. Alternatively, the current-ratio phase angle will depart from the stable position around 180 degrees and will undergo a rotation that will bring it to values close to ±90 degrees for a level of high saturation and beyond for extreme saturation cases.

With a conventional percentage differential principle, one can increase the percentage slope to cope with high levels of CT saturation. This is done at the expense of characteristic sensitivity, because, as the slope increases, the stability area increases also. With the characteristic implemented in the current-ratio plane of [1], the user has two settings that compensate for the expected level of saturation: the greater arc radius, R, and the angle, α. As an example, a radius R between 8 and 10 and an angle between 180 and 210 degrees will sustain high to extreme levels of saturation as defined in Table 3.

This paper will show that the same procedure is not applicable to sequence elements. Situations exist in which a sequence element will become unstable even at moderate levels of saturation, and no characteristic exists (whether conventional or in the current-ratio plane) that will stabilize the element.

PERFORMANCE OF SEQUENCE ELEMENTS DURING EXTERNAL FAULTS WITH SINGLE CT SATURATION

Impact of a Distorted Phase Current on the Corresponding I0 or I2 Phasor

During an external ground fault, the zero- and negative-sequence currents measured at both extremities of a transmission line will be opposed in phase as shown in Figure 11. When the corresponding sequence differential current is computed, the result will be close to zero and the corresponding current-ratio plane elements, 87L0 and 87L2, will not operate.

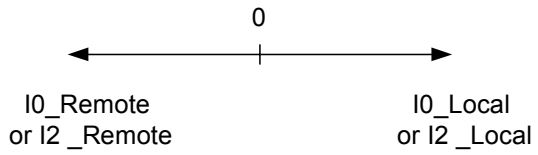


Figure 11 Sequence Currents During an External Fault

During the same external fault, the faulted phase CT could saturate. What, then, is the impact of a saturated CT on both sequence elements? To answer this question, consider the 120 kV single-line network of Figure 12 and assume external application of an A-phase-to-ground fault on the line at R. What happens to the local I0 and I2 current phasors at different levels of saturation of the A-phase current?

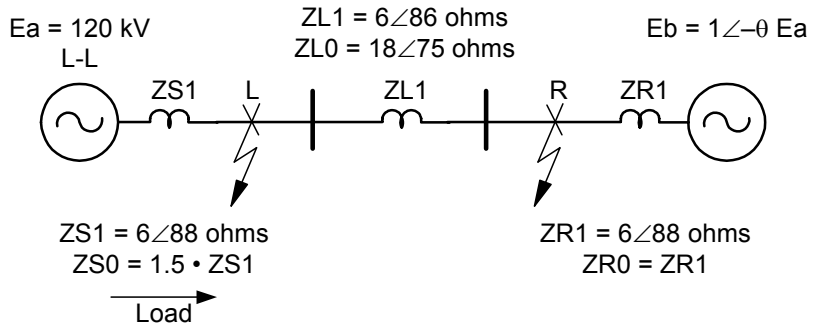


Figure 12 Single-Line Network

From the Appendix, using notation from [5], the A-phase fault current phasor IA at location R can be computed as follows (all variables are identified in the Appendix):

$$IA = ILD + C1 \cdot I1F + C1 \cdot I2F + C0 \cdot I0F \tag{1}$$

From Equation (1), both local sequence phasors can be computed:

$$I0 = IA - ILD - 2C1 \cdot I1F \tag{2}$$

$$I2 = IA - ILD - (C1 + C0) \cdot I1F \tag{3}$$

Alternatively, three times the sequence current phasors can also be expressed in terms of the phase current phasors as:

$$3I0 = IA + IB + IC \tag{4}$$

$$3I2 = IA + a^2 IB + a \cdot IC \tag{5}$$

When the A-phase current is saturated, one can determine I0_sat and I2_sat from Equations (2) and (3):

$$I0\_sat = IA\_sat - ILD - 2 \cdot C1 \cdot I1F \tag{6}$$

$$I2\_sat = IA\_sat - ILD - (C1 + C0) \cdot I1F \tag{7}$$

Obviously, I0_sat and I2_sat depend upon IA; the transformation imposed on IA by the saturation; the load current ILD; the pure fault current at the fault location I1F; and the network

current distribution factors, C1 and C0. Given the transformation imposed on IA to obtain IA_sat, we want to determine the corresponding transformation imposed on I0 and I2 to obtain I0_sat and I2_sat. Equations (6) and (7) are so general in nature that we can draw no conclusion from a simple examination of the two equations. We will proceed, rather, by working out a particular example.

For the circuit of Figure 12 with a load angle of 40 degrees, the steady-state current phasors during the fault have been resolved through use of the superposition principle and the single-phase-to-ground sequence network and equations found in the Appendix. These currents are shown in column 1 of Table 4. Three levels of saturation have been imposed on the fault current, IA, according to Table 3 and are given below:

Low saturation $\Rightarrow$ IA_sat= $0.9 \angle 10°$ IA
Moderate saturation $\Rightarrow$ IA_sat= $0.5 \angle 42°$ IA
High saturation $\Rightarrow$ IA_sat= $0.2 \angle 85°$ IA

After the transformations resulting from the saturation have been imposed on the A-phase phasor, the corresponding saturated sequence current phasors, 3I0_sat and 3I2_sat, are computed. The results are shown in Table 4.

From Table 4, it is possible to compute the transformation imposed on the true local sequence, I0 and I2, by the saturated current phasor, IA_sat, to obtain I0_sat and I2_sat. The results are shown in Table 5.

Analysis of Table 5 indicates the following:

1. At moderate and high levels of saturation, the rotation imposed on I0 is, respectively, 178 degrees and –144 degrees. These rotations are far greater than the rotation of IA_sat with respect to IA. There is a possibility, therefore, with a local sequence phasor to end up with an amplification of the rotation imposed on the true phase current phasor by the CT saturation.

2. In the example considered, for the sequence element 87L0, there is no way the element can be stabilized, as could be the case of the A-phase current differential element. To stabilize the element, the stability area would have to cover zones with angle zero in the current-ratio plane. This is practically impossible to achieve, whatever the characteristic used, whether one uses the conventional or the current-ratio plane method of stabilizing the element.

3. In all three levels of saturation, the negative-sequence element can be made stable. We cannot conclude, however, that 87L2 is stable by definition. The general analysis in the next few pages will demonstrate that the same level of instability can occur with a negative-sequence element.

Table 4 Performance of Sequence Elements to Single CT External Saturation

Local Current Phasors	Low Saturation	Moderate Saturation	High Saturation
IA = 6869 ∠–79°	IA_sat = 6182 ∠–69°	IA_sat = 3434 ∠–37°	IA_sat = 1373 ∠6°
IB = 2690 ∠–144°	IB = 2690 ∠–144°	IB = 2690 ∠–143°	IB = 2690 ∠–143°
IC = 4578 ∠93°	IC = 4578 ∠93°	IC = 4578 ∠93°	IC = 4578 ∠93°
3I0 = 3912 ∠–106°	3I0_sat =2788 ∠–94°	3I0_sat = 955 ∠68°	3I0_sat = 3261 ∠108°
3I2 = 7137 ∠–113°	3I2_sat =5905 ∠–109°	3I2_sat = 2367 ∠–127°	3I2_sat = 2820 ∠173°

Table 5 Sequence Element Transformations Caused by Single CT External Saturation

Low Saturation	Moderate Saturation	High Saturation
3I0_sat = (0.71 ∠12°) • 3I0	3I0_sat = (0.24 ∠174°) • 3I0	3I0_sat = (0.83 ∠–146°) • 3I0
3I2_sat = (0.83 ∠4°) • 3I2	3I2_sa t= (0.33 ∠–14°) • 3I2	3I2_sat = (0.39 ∠–74°) • 3I2

Generalized Analysis

In the previous paragraph, an example has been provided with the analysis of a single A-phase to-ground external fault. Let us now extend the analysis to any type of external fault. Let us assume that any type of external fault could occur, but that only the A-phase CT would saturate. Let us define two vectors, IS0 and IS2, as follows:

$$IS0 = IB + IC \tag{8}$$

and:

$$IS2 = a^2 \cdot IB + a \cdot IC \tag{9}$$

so that from Equations (4) and (5), we have the following:

$$3I0 = IA + IS0 \tag{10}$$

$$3I2 = IA + IS2 \tag{11}$$

Obviously, IS0 and IS2 are the two vectors added to the phasor, IA, to obtain 3I0 and 3I2. Equations (10) and (11) are general by definition and could apply to any type of external fault. In the rest of the text, IS refers interchangeably to either IS0 or IS2.

We want to determine now, for the most general situation, the conditions that IS has to fulfill with respect to IA so that a sequence element (87L0 or 87L2) will become irremediably unstable. To do so, and as a first example, we have defined IA as a unit phasor and represent IS in Figure 13 with a phase angle lag of about 120 degrees with respect to the faulted phasor, IA. By adding IA to IS0 or IS2, we obtain the local zero-sequence or negative-sequence phasor, I0 or I2. Let us assume that the A-phase current undergoes saturation and is subjected to a reduction in magnitude to 0.4 and a phase advance of 60 degrees. The corresponding saturated phasor is then IA_sat. The new zero-sequence and negative-sequence phasor resulting from the saturation of A-phase is shown as I0_sat or I2_sat. For the example shown, one can see that I0_sat or I2_sat undergoes a rotation of practically 180 degrees with respect to the original position of I0 or I2 when the original rotation imposed by the saturation on IA was only 60 degrees.

The latest example has shown that, for any type of external fault, it is possible to find locations of IS (IS0 or IS2) with respect to IA that will make the corresponding element, 87L0 or 87L2, unstable during a moderate saturation of the A-phase current.

Let us go a step further and give IS two magnitude levels of 0.1 and 0.5 successively, and let us vary the phase angle of IS from 0 to 360 degrees with respect to IA. Let us impose on the A-phase current phasor the three levels of saturation defined in the previous paragraph, and let us compute the corresponding rotation of I0_sat or I2_sat with respect to I0 or I2.

The resulting rotation of I0_sat or I2_sat with respect to I0 and I2, respectively, is shown in Figure 14 and Figure 15. In both figures, the angular stability limits have been set to ±90 degrees. In both situations, one can see that there exists a range for the angle of IS where the rotation of the sequence phasor resulting from phasor A saturation becomes larger than the angular stability limit of 90 degrees and the corresponding sequence element becomes unstable. Comparing Figure 14 and Figure 15 also, it is obvious that as the magnitude of IS increases, the sequence element, 87L0 or 87L2, is more likely to become unstable.

This second example has demonstrated that, in the most general case, it will be possible to find positions for IB and IC when IA saturates that will make 87L0 and 87L2 unstable at moderate or high levels of saturation.

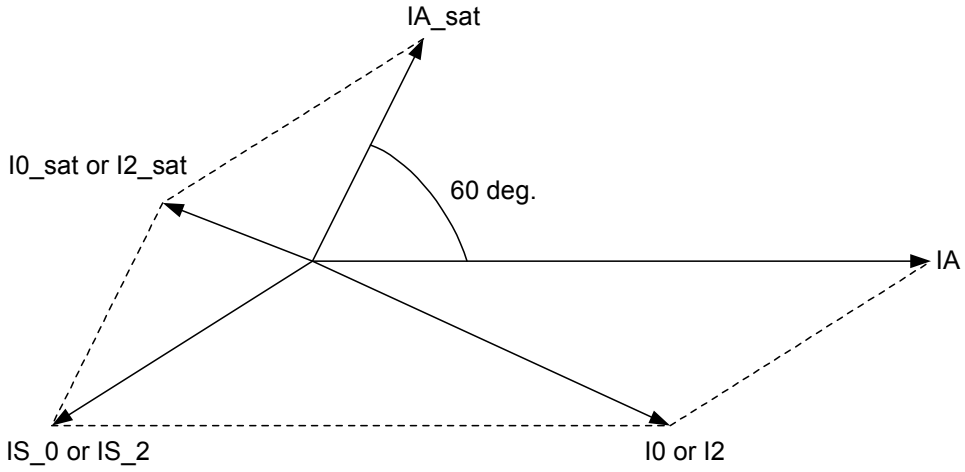


Figure 13 Principle of Sequence Phasor Rotation

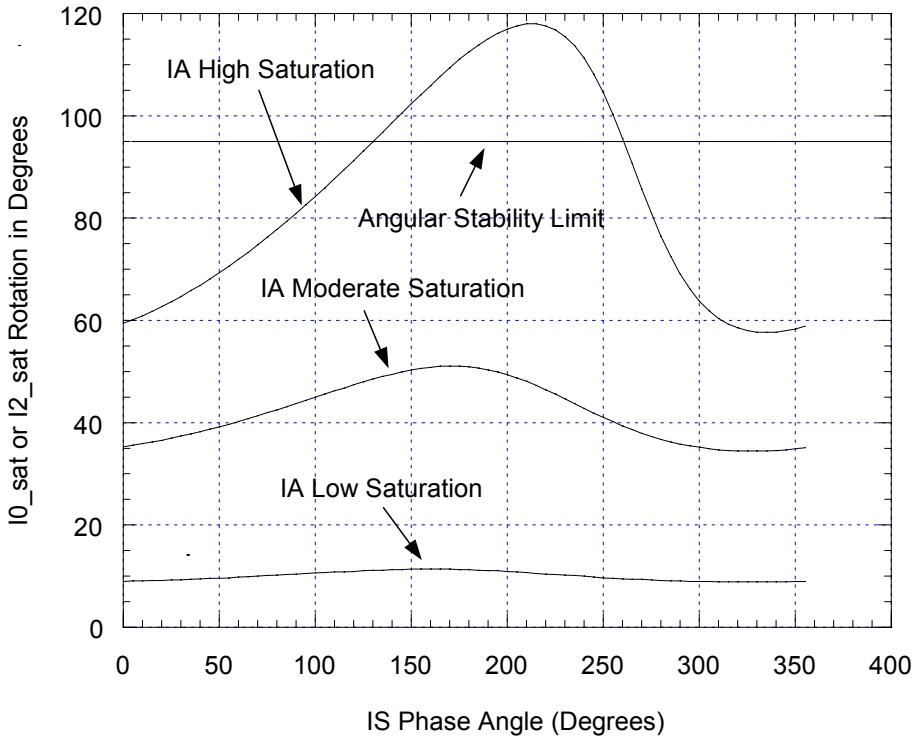


Figure 14 Rotation of Sequence Phasor (I2 or I0) as a Function of IA Saturation Level (|IS|= 0.1)

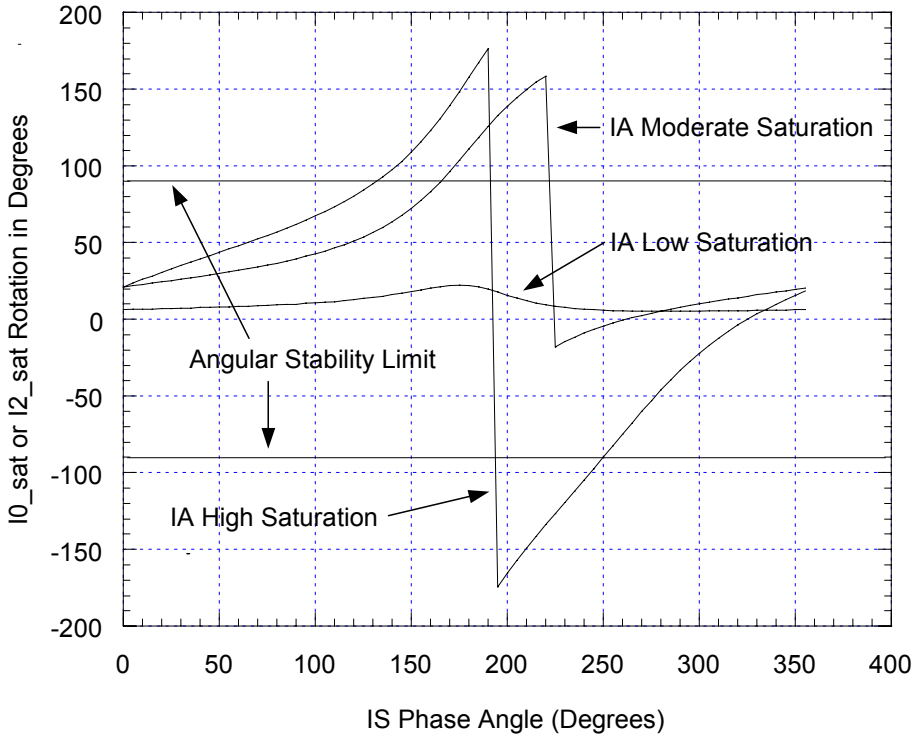


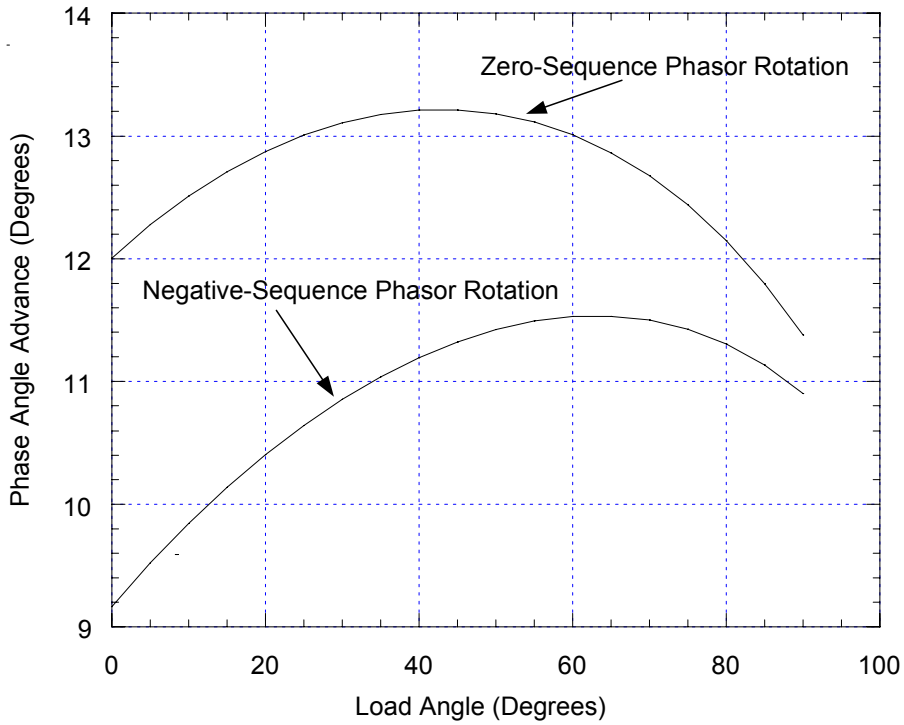
Figure 15 Rotation of Sequence Phasor (I2 or I0) as a Function of IA Saturation Level (|IS|= 0.5)

Impact of the Load Current on the Stability of the 87L0 and 87L2 Elements

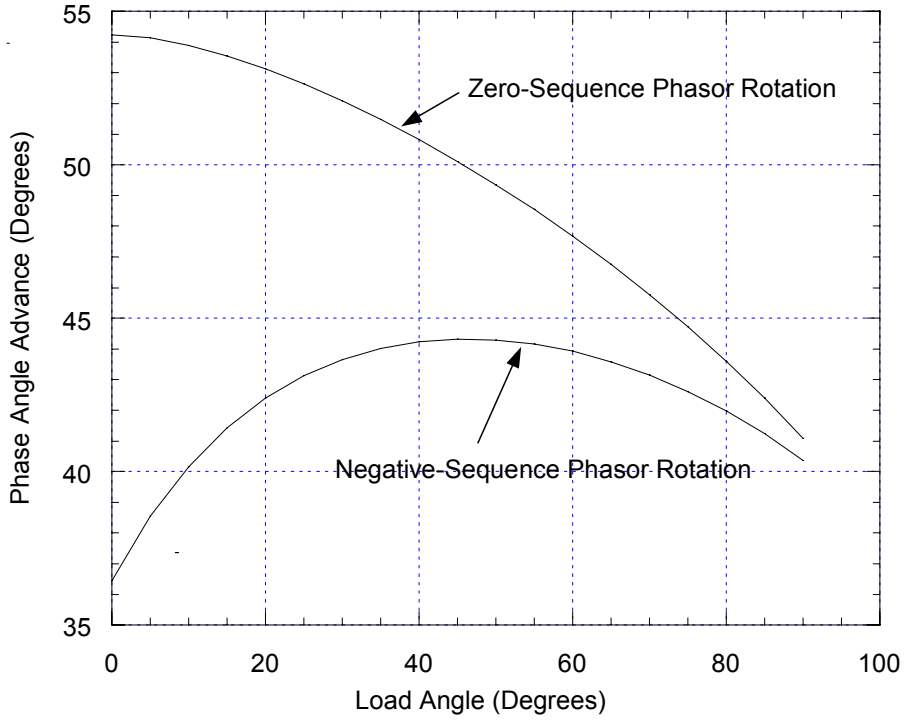
To evaluate the impact of the load on the stability of the 87L0 and 87L2 elements, we varied the load angle, θ, from 0 to –90 degrees on the network of Figure 12 and applied the same A-phase-to-ground external fault at locations L and R.

Figure 16 a, Figure 16 b, and Figure 16 c represent the local phase angle rotation of I0 and I2 resulting from the three previously defined levels of saturation imposed on the A-phase current for a fault at L. Note in this situation that the load current is in opposition to the fault current. Obviously, in this case, there is only one situation in which the zero-sequence element becomes unstable at low load (for the high-saturation situation). In all other cases, the sequence elements remain stable and become more stable as the load angle increases. Also, 87L2 is more stable than 87L0 if we judge only by the amount of phase-angle rotation.

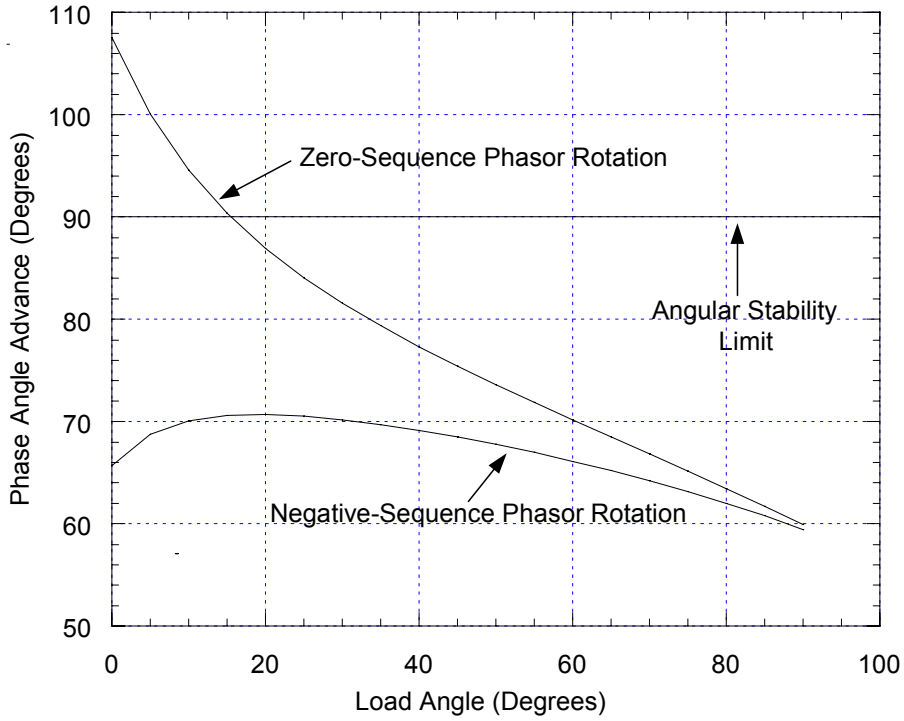
In Figure 17, we created the same plots with a fault at R. This situation is different from the previous case; the sequence element 87L0 becomes unstable starting at medium saturation with a load angle of 30 degrees. The instability increases with the load level. The 87L2 element is close to instability at high load (above 30 degrees) and at high saturation. This second example demonstrates that 87L2 tends to be more stable than 87L0 in all cases, if we judge by the sequence current I0 or I2 phase-angle rotation.



a) Low saturation ⇒ IA_sat = 0.9 ∠10° IA

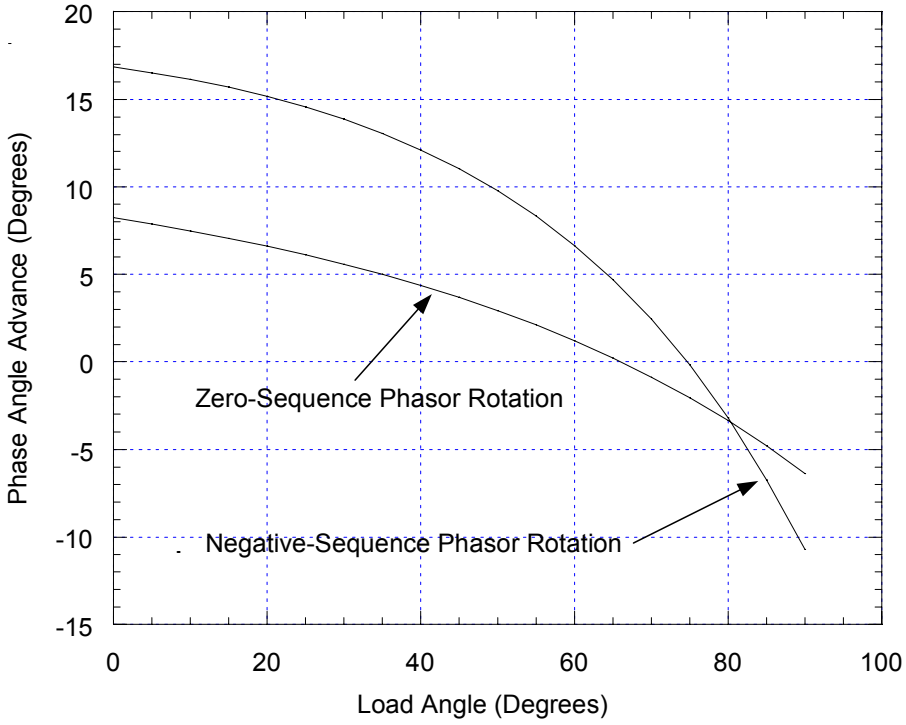


b) Moderate saturation ⇒ IA_sat= 0.5 ∠42° IA

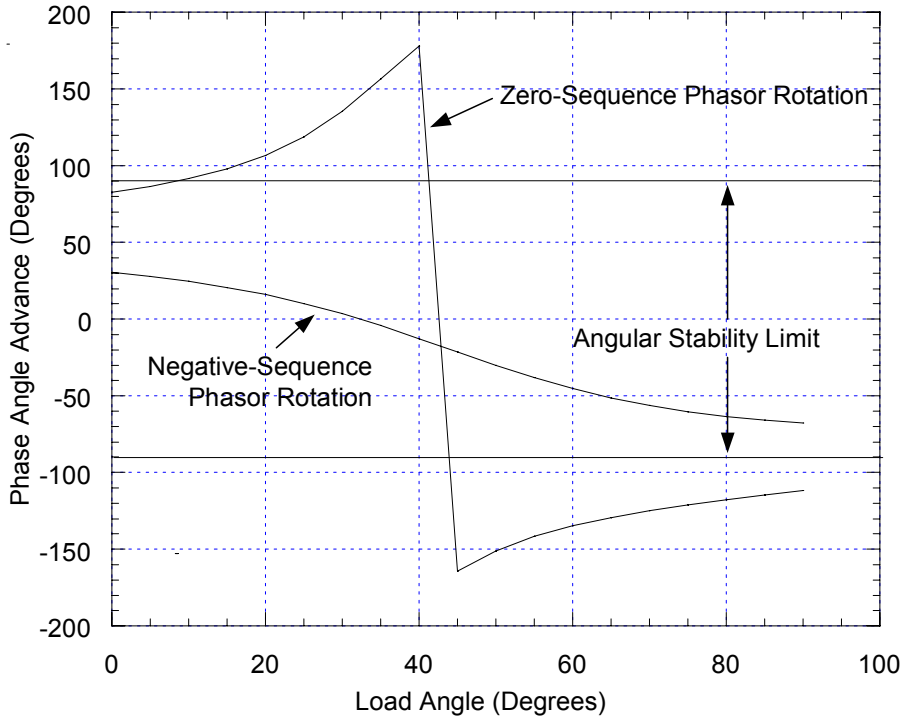


c) High saturation ⇒ IA_sat= 0.2 ∠85° IA

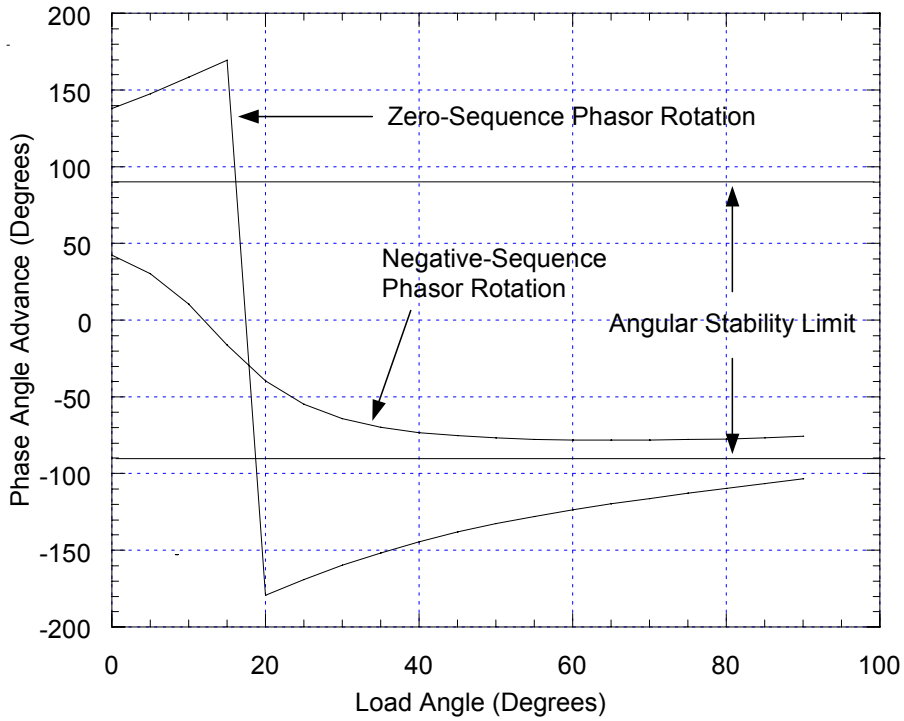
Figure 16 Rotation of Sequence Phasors for a Fault at L as a Function of the Load Angle



a) Low saturation ⇒ IA_sat= 0.9∠10° IA



b) Moderate saturation ⇒ IA_sat= 0.5∠42° IA



c) High saturation ⇒ IA_sat= 0.2 ∠85° IA

Figure 17 Rotation of Sequence Phasors for a Fault at R as a Function of the Load Angle

Transient Simulation Verification

To verify the theoretical results obtained through use of a steady-state analysis together with the use of saturated current, we again simulated the network of Figure 12. We used the same load angle of 40 degrees and an applied A-phase-to-ground fault at location R for transient state analysis through use of the electromagnetic transient program (EMTP). We processed the faulted A-phase current through a CT model so that it underwent moderate saturation. Based solely on the phase-angle rotation determined in the previous steady-state analysis, only the zero-sequence element, 87L0, should go unstable. The negative-sequence element, 87L2, should remain stable.

Figure 18 shows the true A-phase current and the same current undergoing saturation. Figure 19 shows the ratio of the magnitudes of the saturated phasor over the true phasor. Figure 20 shows the saturated phasor corresponding phase angle with respect to the true phasor.

From an examination of Figure 21, Figure 22, and Figure 23 representing the current ratio-plane trajectories for the A-phase, negative-sequence, and zero-sequence element, respectively, it is obvious that only the zero-sequence element, 87L0, goes irremediably unstable. These are the results that we would have expected from the steady-state analysis, and they demonstrate that the concept of using a saturated current phasor in steady state leads to conclusions identical to the ones obtained through use of a transient analysis.

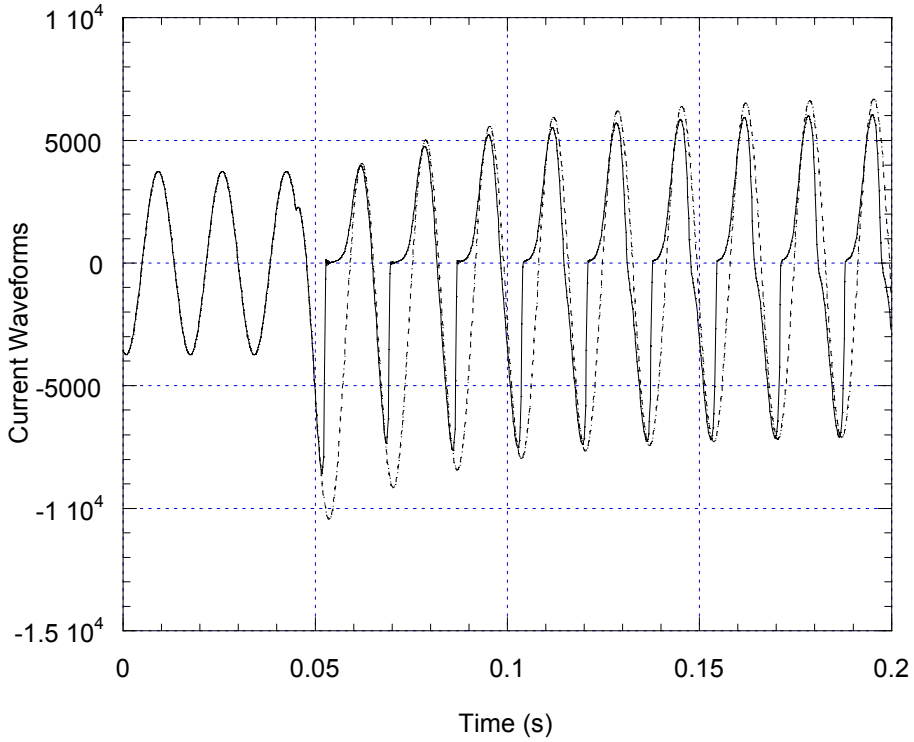


Figure 18 Saturated A-Phase Current

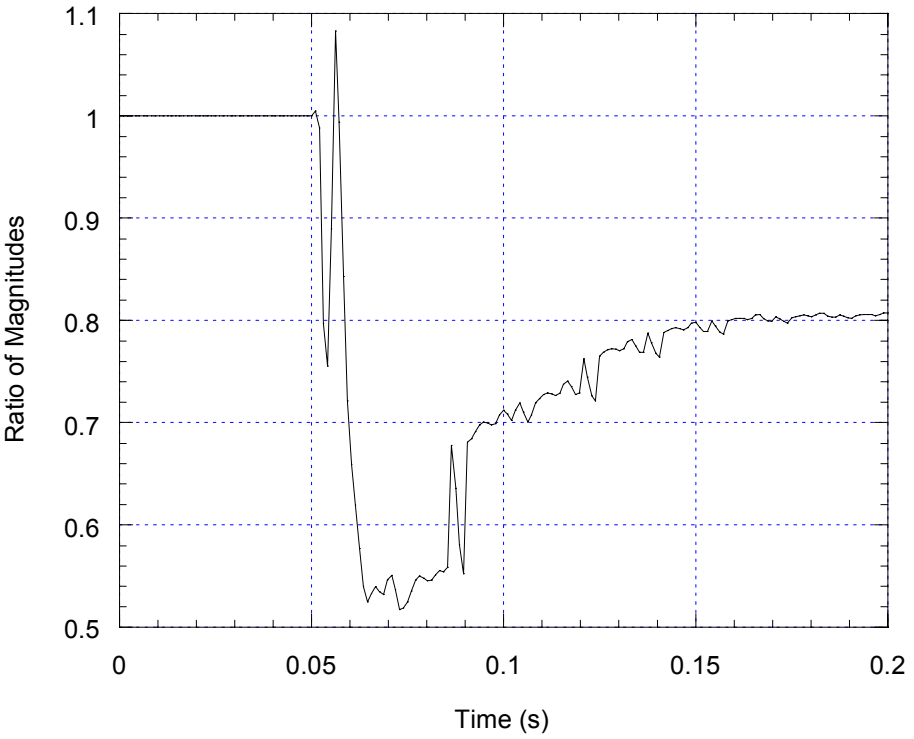


Figure 19 Ratio of Magnitudes of IA_sat Over IA

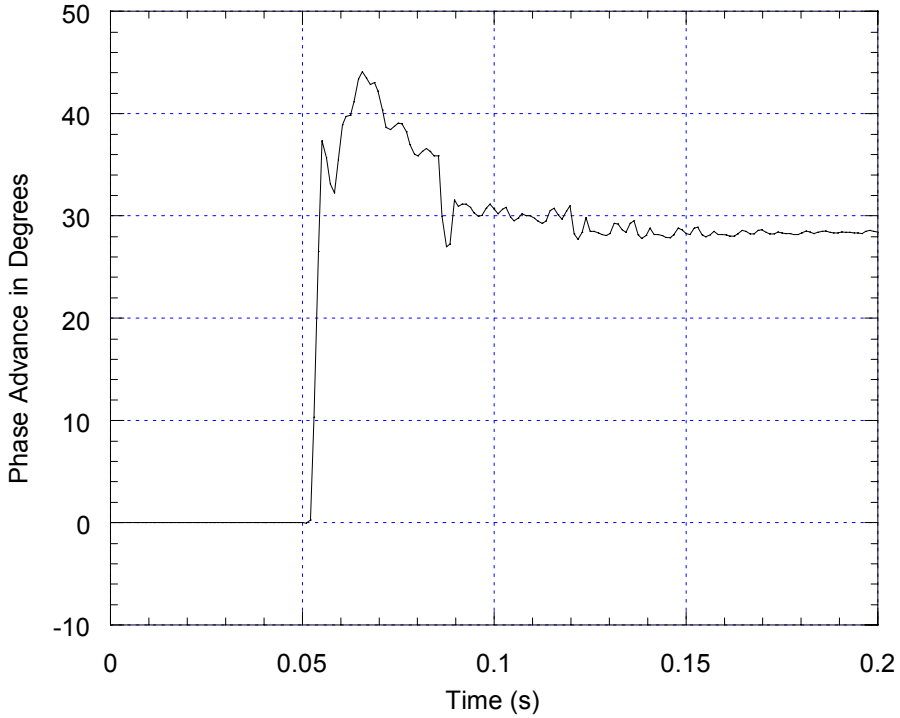


Figure 20 IA_sat Phasor Phase Advance With Respect to IA

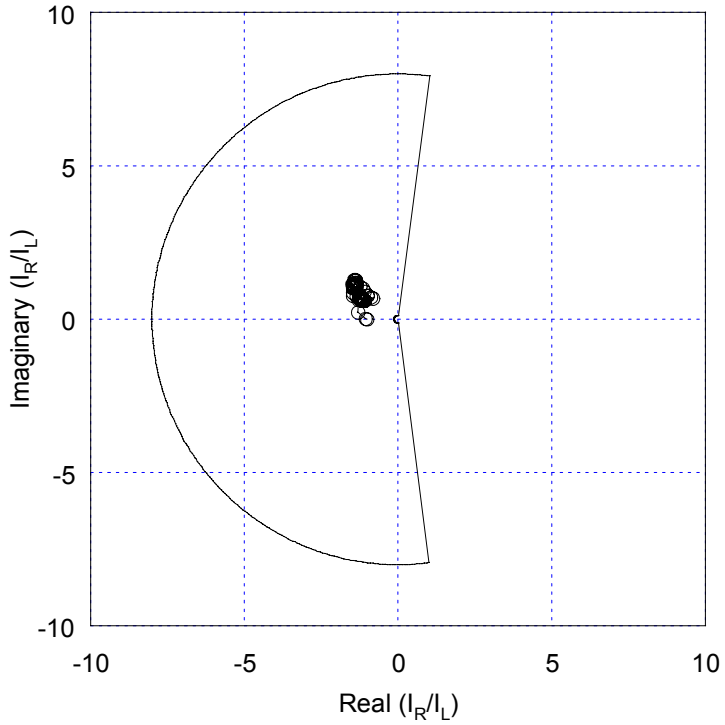


Figure 21 Current-Ratio Plane Trajectory of A-Phase Element

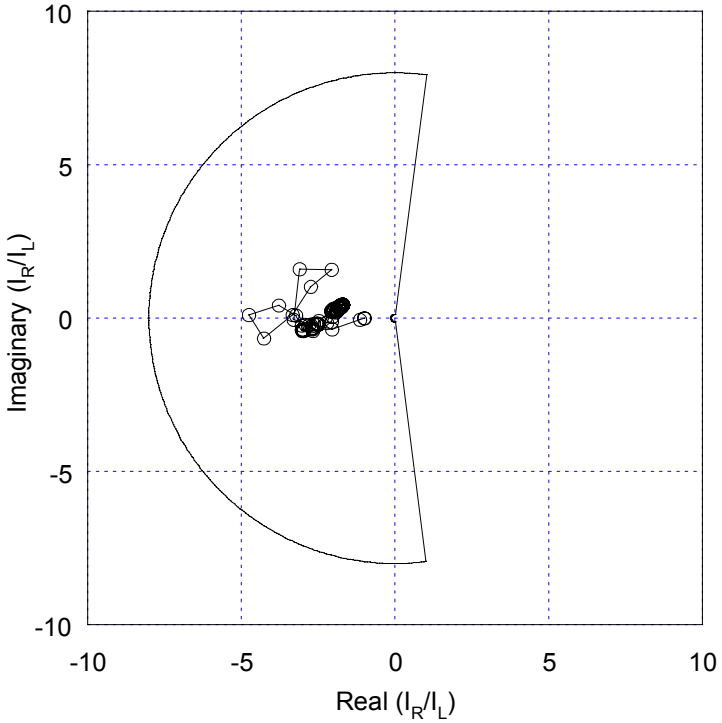


Figure 22 Current-Ratio Plane Trajectory of Negative-Sequence Element

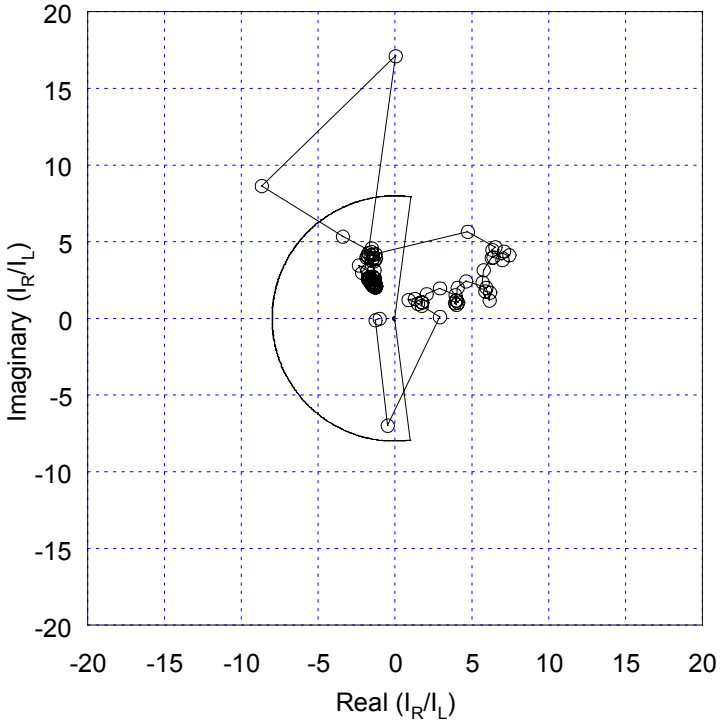


Figure 23 Current-Ratio Plane Trajectory of Zero-Sequence Element

SECURING SEQUENCE-CURRENT DIFFERENTIAL ELEMENTS DURING SATURATION OF A SINGLE CT

Problem Statement

The preceding analysis and simulations show the futility of applying phasor processing to the problem of stabilizing zero-sequence and negative-sequence current differential elements during an external phase-to-ground fault. In other words, further processing of the fundamental quantities will not lead to a robust sequence-current differential element when considering external ground faults. Nevertheless, the case presented earlier for including these elements in a current differential relay is compelling. The resulting impact on phase-element security and speed cannot be ignored.

Description of Mitigation Technique

Because further processing of the fundamental portion of the current waveforms has been demonstrated to be unfruitful, we concentrated on processing the nonfundamental portions, specifically the dc and harmonic components. The technique we chose for securing sequence-current differential elements during external ground faults combines harmonic and dc restraint as shown in Figure 24.

Filters extract the second-harmonic and dc component of each of the local and remote phase currents. The sum of the maximum harmonic and dc components creates an error estimate. This is an estimate of the maximum 3I0 or 3I2 difference current that can be generated by CT saturation. The error estimate is subtracted from the 3I0 and 3I2 difference current, and the result is processed through a very fast inverse-time overcurrent element. The output of the time-overcurrent element enables the corresponding sequence-current differential element. When enabled, the sequence elements are processed through use of the same alpha-plane restraint region shown in Figure 1.

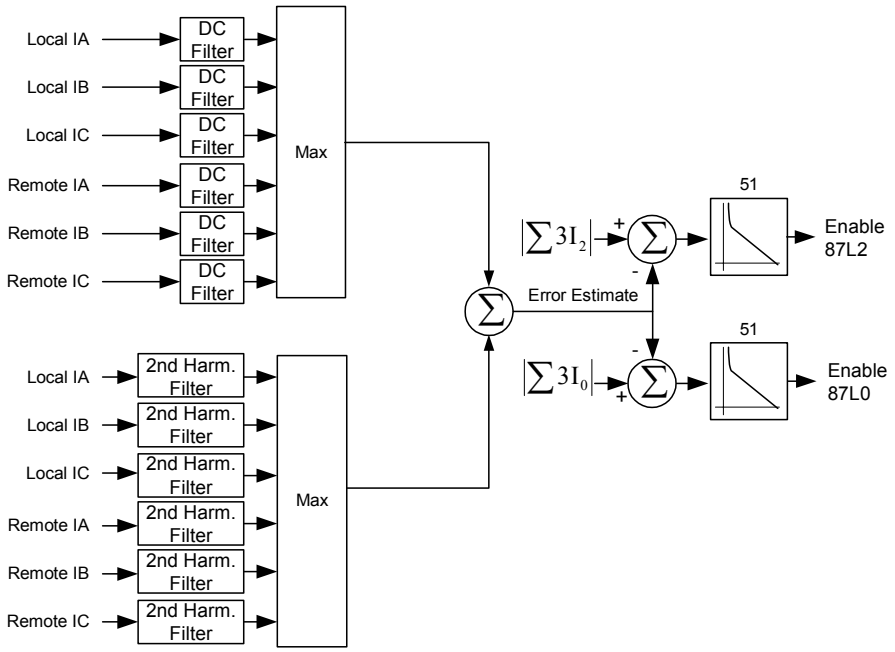


Figure 24 CT Saturation Security Supervision for 87L2 and 87LG Elements

Case Studies

Transient Simulation of the Mitigation Technique

We applied the CT saturation security supervision of Figure 24 to the transient simulation of the A-phase-to-ground fault of Figure 12. Figure 25 shows the time-variation of the zero-sequence current-ratio magnitude. Figure 26 shows the time-variation of the zero-sequence current-ratio phase angle. Figure 27 shows the time-variation of the error estimate of Figure 24 together with the zero-sequence current differential current. During the time the error estimate is greater than the differential current plus the pickup setting, the 87L0 element is blocked because the output of the time-overcurrent element (TOC) is zero. After the differential current becomes greater than the error signal plus the pickup setting, the output of the overcurrent element enables the 87L0 element. One can see by comparing Figure 25 and Figure 26 to Figure 27 that, by the time the 87L0 element enables, the current ratio magnitude and the angle are within the characteristic stability area. Therefore, the 87L0 element has been prevented from operating for this external fault.

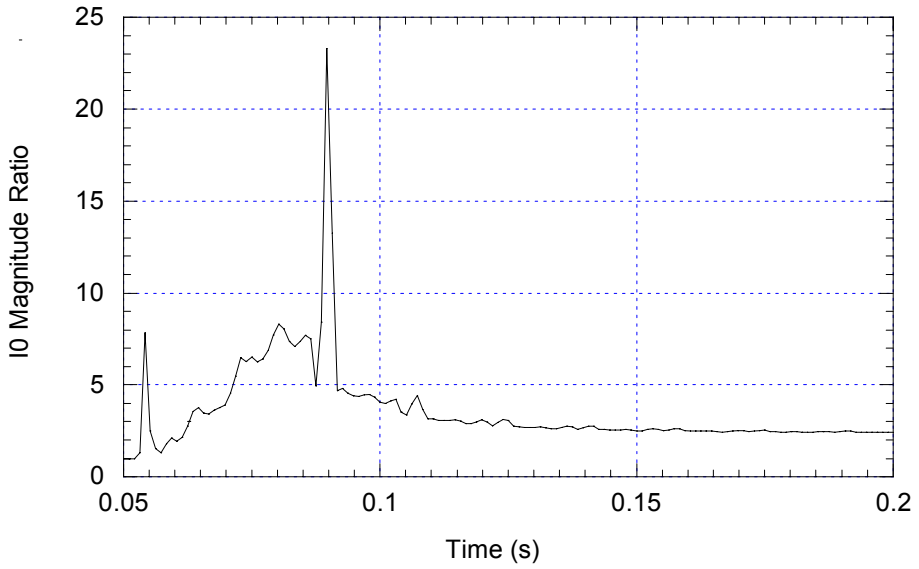


Figure 25 I0 Magnitude Ratio

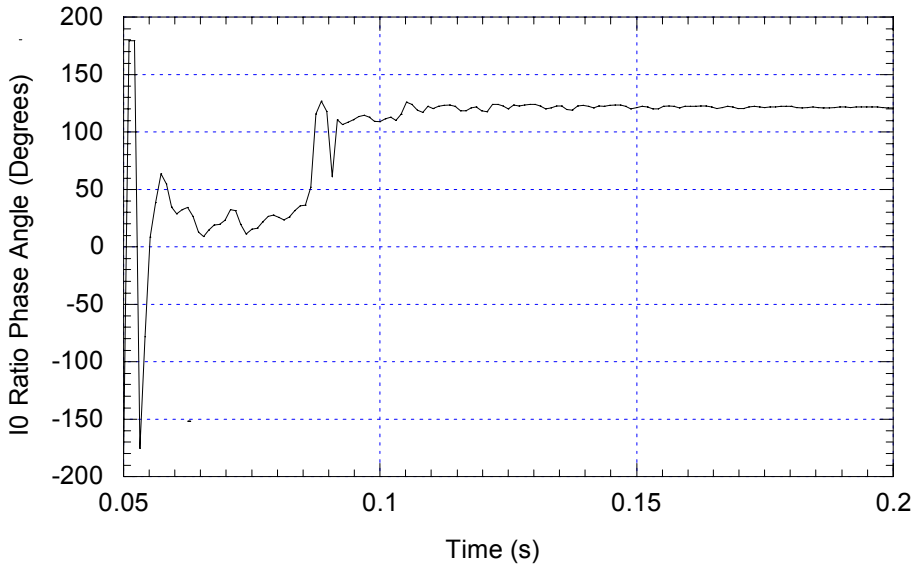


Figure 26 I0 Ratio Phase Angle

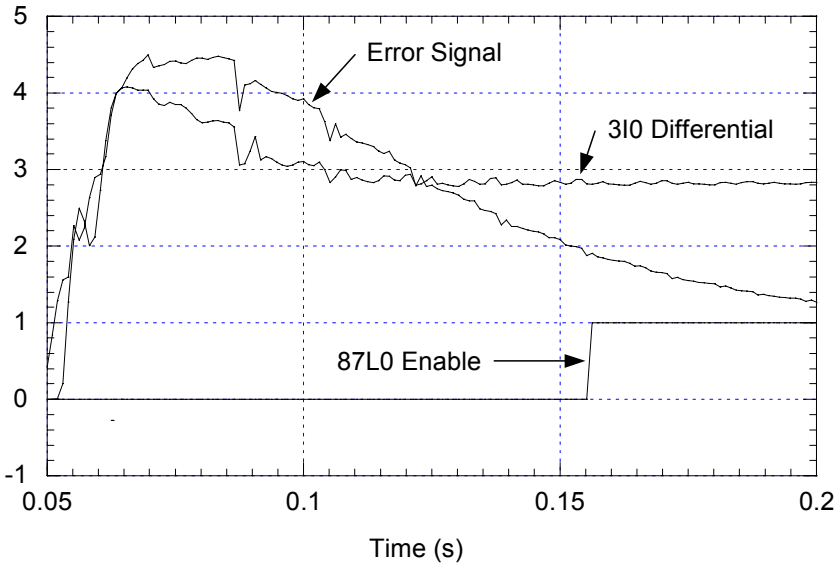


Figure 27 3I0, Error Signal, and 87L0 Enabling Logic

CONCLUSIONS

1. Including zero-sequence and/or negative-sequence current differential elements in a relay allows the phase current differential elements to be optimized for security and speed during multiphase faults.

2. The phasor of a saturated current will exhibit a reduction of its magnitude and an advance of its phase angle with respect to the true phasor when processed by a digital filtering system. The reduction in the magnitude can be as low as 5 percent of the true magnitude, and the phase-angle advance can be as high as 120 degrees in extreme cases of saturation.

3. The concept of the saturated current phasor allows studying the impact of CT saturation on the steady-state characteristic equations of relays.

4. The impact of a saturated fault phase current on the corresponding local zero-sequence or negative-sequence current, I0 or I2, will be the cause for a rotation of this same phasor. There could be an amplification effect in the rotation of the sequence phasor, i.e., the sequence-phasor rotation could be greater than the rotation of the saturated current phasor.

5. Because a saturated sequence phasor rotation could be as high as 180 degrees, there is a tendency for both the 87L0 and 87L2 elements to become completely unstable and cause misoperation even at moderate levels of saturation. When using a conventional percentage differential characteristic or a characteristic embedded in the current-ratio plane, there is no way the element can be rendered stable.

6. The rotation of a sequence phasor resulting from the saturation of a faulted phase current is a complex equation that depends upon the relative position of the two other phase current phasors during the fault. The position of the two non-saturated phase current phasors depends in turn upon the network characteristics: sources and line positive-sequence and zero-sequence impedance, fault-type, fault location, and load angle.

7. As a general rule, the greater the level of saturation of a phase current, the greater the rotation of the corresponding local sequence current, I0 or I2, and as a consequence, the greater the instability of the 87L0 or 87L2 elements.

8. Tests performed on typical network configurations show that the 87L0 element has a tendency to be much more unstable than the 87L2 element.

9. The impact of load current on the stability of the 87L0 and 87L2 elements during CT saturation stresses and confirms the already established fact that the 87L2 element is more stable than 87L0.

10. Because an 87L0 or 87L2 could become irremediably unstable during an external fault with CT saturation, it is necessary to restrain these elements during CT saturation.

11. The main purpose of an 87L0 or 87L2 element is to detect resistive faults. Because CT saturation is very unlikely to occur during a resistive fault, restraining 87L2 or 87L0 during CT saturation does not impair the overall performance of a line current differential relay.

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APPENDIX: RESOLUTION OF AN EXTERNAL SINGLE-A-PHASE-TO-GROUND FAULT THROUGH USE OF THE SEQUENCE NETWORK

For the single-line network of Figure 28, the single-phase-A-to-ground external fault at R current phasors can be found by resolving the Figure 29 network equations through use of the superposition principle. These equations, using notation from [5], are:

$$Z1M = ZS1 + ZL1 \tag{A1}$$

$$Z1N = ZR1 \tag{A2}$$

$$Z0M = ZS0 + ZL0 \tag{A3}$$

$$Z0N = ZR0 \tag{A4}$$

$$ZS0M = \frac{2Z1M \cdot Z1N}{Z1M + Z1N} + \frac{Z0M \cdot Z0N}{Z0M \cdot Z0N} \tag{A5}$$

$$C1 = \frac{Z1N}{Z1M + Z1N} \tag{A6}$$

$$C0 = \frac{Z0N}{Z0M + Z0N} \tag{A7}$$

$$Ef = Ea - ILD \cdot Z1M \tag{A8}$$

$$ILD = \frac{\left(1 - e^{-j\Theta}\right)Ea}{Z1M + Z1N} \tag{A9}$$

$$I1F = \frac{Ef}{ZS0M + 3Rf} \tag{A10}$$

$$I2F = I1F \tag{A11}$$

$$I0F = I1F \tag{A12}$$

$$I1 = C1 \cdot I1F \tag{A13}$$

$$I2 = C1 \cdot I1F \tag{A14}$$

$$I0 = C0 \cdot I1F \tag{A15}$$

$$a = 1\angle 120° \tag{A16}$$

$$IA = ILD + I1 + I2 + I0 \tag{A17}$$

$$IB = a^2 \cdot ILD + a^2 \cdot I1 + a \cdot I2 + I0 \tag{A18}$$

$$IC = a \cdot ILD + a \cdot I1 + a^2 \cdot I2 + I0 \tag{A19}$$

$$3I0 = IA + IB + IC \tag{A20}$$

$$3I2 = IA + a^2 \cdot IB + a \cdot IC \tag{A21}$$

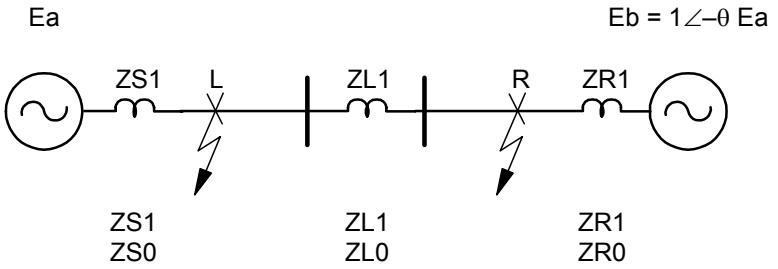

Figure 28 Single-Line Network

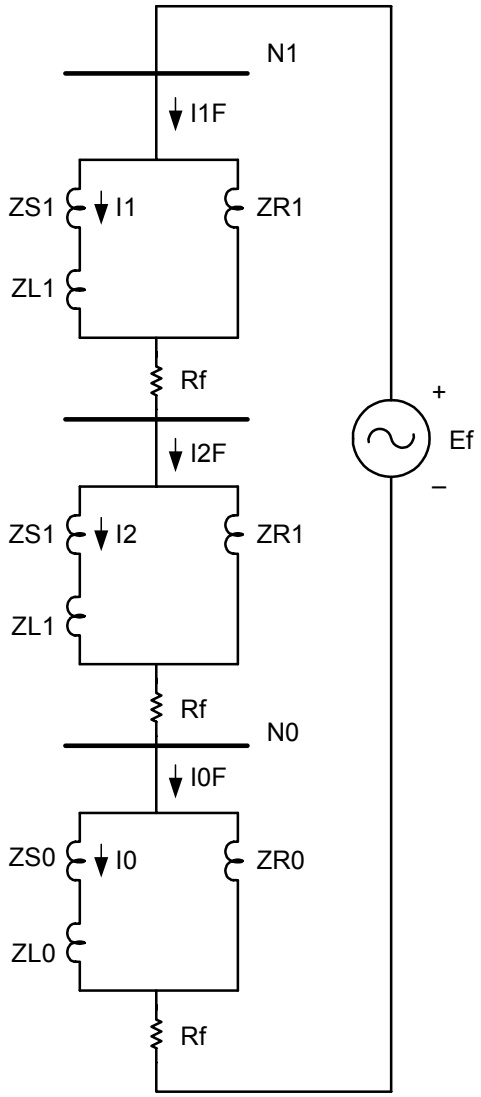

Figure 29 A-Phase-to-Ground Fault at R Pure-Fault Sequence Network

BIOGRAPHIES

Gabriel Benmouyal, P.E. received his B.A.Sc. in Electrical Engineering and his M.A.Sc. in Control Engineering from Ecole Polytechnique, Université de Montréal, Canada in 1968 and 1970, respectively. In 1969, he joined Hydro-Québec as an Instrumentation and Control Specialist. He worked on different projects in the field of substation control systems and dispatching centers. In 1978, he joined IREQ, where his main field of activity was the application of microprocessors and digital techniques to substation and generating-station control and protection systems. In 1997, he joined Schweitzer Engineering Laboratories in the position of Principal Research Engineer. He is a registered professional engineer in the Province of Québec, is an IEEE Senior Member, and has served on the Power System Relaying Committee since May 1989. He holds over six patents and is the author or co-author of several papers in the field of signal processing and power networks protection.

Tony J. Lee received his B.S. degree in electrical engineering from Washington State University in 1987. Mr. Lee then worked for Texas Instruments in Dallas, Texas from 1987 through 1991, when he joined Schweitzer Engineering Laboratories, Inc. as a hardware design engineer. He presently holds the position of Research Engineering Manager at SEL. Mr. Lee holds four U.S. patents, several foreign patents, and has several patents in process.