

A New Phasor Current-Based Channel Asymmetry Compensation Method Without External Time Sources for Line Current Differential Relays

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Abstract—The reliable operation of line current differential (87L) protection schemes requires accurate alignment of local and remote current measurements. In the absence of reliable external time sources, communications channel asymmetry, defined as the difference between local-to-remote and remote-to-local propagation delays, poses a significant challenge to maintaining accurate data alignment and ensuring the dependability and security of the 87L scheme. Prior work by the authors introduced an adaptive Kalman filter-based approach to estimate and compensate sudden asymmetry changes, primarily caused by communications channel path-switching events, without relying on external time references. However, modern packet-based communications systems that use multiprotocol label switching (MPLS) transport to replace older time-division multiplexed (TDM) systems often experience gradual variations in channel delay. These variations may arise from queue build-up in intermediate routers, congestion on specific network paths or dynamic routing optimization. Under such conditions, techniques that rely on detecting abrupt delay changes become ineffective.

To address the challenge, this paper introduces a phasor-based channel asymmetry compensation method that works without external time sources and relies only on locally measured and remotely received current phasors. The proposed method estimates channel asymmetry by identifying a consistent phase shift in the remote current phasors across all three phases relative to the local phasors. Secure asymmetry estimation is ensured through supervision mechanisms, including disturbance detection and loss of 87L supervision. Once a channel asymmetry is detected, the asymmetry is quantified from the magnitude of the phase shift and used to correct the misalignment of the remote current phasors. The proposed method does not require voltage measurements, line parameters, or user-defined settings, resulting in a self-contained solution capable of accurately tracking gradual asymmetry drift in modern packet-based networks for two-terminal lines. Real-world testing demonstrates that the proposed method effectively achieves precise time alignment during varying channel delay conditions, thereby ensuring the security and sensitivity of the 87L element.

I. INTRODUCTION

The current line differential (87L) scheme offers simple, dependable and secure power line protection. In this scheme, there are two devices at terminal ends of a line or cable that are being protected and each of the devices computes differential quantities, namely differential operate and restraint currents, to classify a power system fault as internal (inside the zone of protection) or external (outside the zone of protection). The two devices are connected through a communications link and exchange time-stamped data samples to estimate the

differential currents [1]. The communications link may comprise a pair of fiber-optic cables that carry the data samples each way. During every transmission interval, the device on one end of the power line transmits the data encoded, according to IEEE C37.94, *IEEE Standard for N times 64 kbps Optical Fiber Interfaces between Teleprotection and Multiplexer Equipment* [2], to the device at the other end. The device that is receiving the data decodes the data and uses the time stamps to measure the link delay and align the received data with the locally sampled data. Once aligned, the device computes the differential currents and decides whether to operate (declare a trip) or to restrain. It is crucial to precisely align the data to ensure that the estimated differential currents are accurate. This precise alignment can be achieved by relying on a high-precision external time source (global, synchronized time) or by using stable, internal crystal oscillators (local, asynchronous time). By using the internal crystal oscillators to generate time stamps, it is possible to avoid any dependency on the status of an external time source. Improving the reliability of the overall 87L scheme by minimizing the impact of loss of external time source is the main motivation behind the technique proposed in this paper [3].

Devices that do not rely on an external time source to perform data alignment typically use the ping-pong method. This method exchanges data samples that are time-stamped using the internal (local) time of the device. This method works similarly to how one converts time stamps from a different time zone to their local time zone based on the time offset. The receiving end relay uses the time stamps of the received data to estimate the clock offset. As explained in Section II of this paper, this clock offset estimation method assumes that the communications channel is symmetrical, i.e., the time taken for the data to travel between the two devices is the same in both directions. An asymmetrical channel creates an error in the clock offset calculation that results in data misalignment and fictitious differential currents.

Channel asymmetry becomes especially important in schemes using data multiplexers where advantages, such as long-distance communications, time distribution, path redundancy, and transfer tripping, are leveraged. Therefore, when the channel becomes asymmetrical, protective relays can either place the 87L scheme in a high-security mode or inhibit the 87L scheme entirely. However, with these fallback methods, the user loses either sensitivity or dependability. To

enhance the dependability of 87L protection over an asymmetrical communications channel, an adaptive Kalman filter-based approach was introduced [4]. This method can quickly and precisely detect and compensate for channel asymmetry that can result due to path-switching conditions. However, the method detects channel asymmetries introduced during path switching that typically results in a step change in the channel delay.

This limitation becomes increasingly relevant with the widespread adoption of multiprotocol label switching (MPLS)-based 87L transport schemes where the channel delay and asymmetry can vary slowly and accumulate over time, depending on network congestion [5]. 87L scheme over MPLS has become popular because it offers various advantages, such as network convergence (allowing teleprotection, SCADA, synchrophasors, and other network traffic on a single network), high-aggregated bandwidth with flexibility to reroute traffic based on network congestion, multiple hot standby channels, and the ability to leverage existing Ethernet infrastructure. Therefore, a method that can ensure continuous 87L operation under changing channel delay and asymmetry conditions while being independent of any external time sources and the underlying communications scheme is desirable in achieving a reliable 87L protection scheme.

In this paper, we propose a novel technique using local and remote current phasor measurements to achieve precise, real-time estimation and compensation of channel asymmetry without relying on any external time sources. This technique helps maintain sensitivity and dependability of the 87L scheme with MPLS-based implementations. To provide a complete and coherent perspective, we examine how modern communications networks introduce channel asymmetries in Section II, review existing channel delay estimation techniques in Section III, and introduce a phasor current-based asymmetry compensation method in Section IV. In Section V, we validate the proposed method through real-world results, which demonstrate its effectiveness under practical operating conditions.

II. CHANNEL ASYMMETRY IN MODERN COMMUNICATIONS NETWORKS

In this section, we explore different sources of channel asymmetry and their characteristics.

A. Sources of Asymmetry and Their Characteristics

The channel asymmetry in applications that use direct point-to-point fiber-optic communications between the relays or time-division multiplexing synchronous optical networks (TDM SONET) is typically very small and of no concern.

Fig. 1 shows 87L serial communications, IEEE C37.94, over an MPLS network using virtual synchronous networking (VSN) [6] [7]. The channel asymmetry in these applications can be attributed to the use of jitter buffers to achieve constant bit rate between the multiplexer and the relay. As the bit rates vary beyond the tolerance of the buffer, the difference in the pointer lever of the jitter buffer creates varying channel asymmetry over time, as shown in Fig. 2. The jitter buffer sizes can vary

between different manufacturer implementations (0.1–5 ms [6]). A smaller jitter buffer means lower channel latency. Gradual accumulation of channel asymmetry can be observed based on the network conditions in one of the paths, say the forward path, while the reverse path (or return path) delay is constant. Further, these buffers must be monitored and reset if the allocated buffer size is reached. Resetting the jitter buffer typically results in loss of 87L communications.

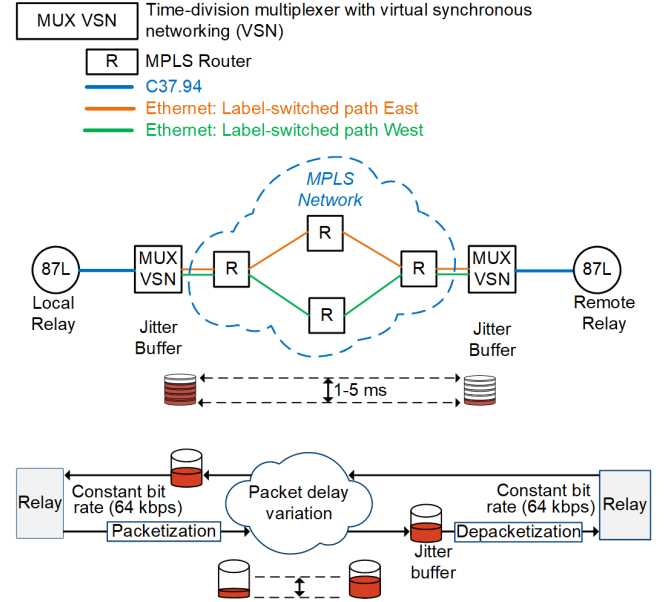


Fig. 1. Serial 87L communications over MPLS network using VSN.

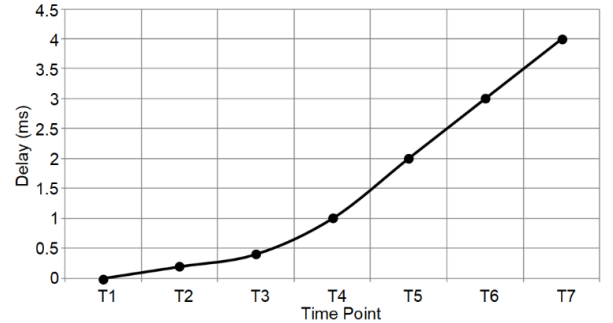


Fig. 2. Gradual increase in asymmetry due to increase in jitter buffer pointer levels.

Fig. 3 shows 87L Ethernet communications over an MPLS network [8]. Traditional MPLS networks can have longer network latency in one direction than in the other due to congestion and queue build up. Modern MPLS networks use quality of service prioritization to reduce latency and loss of packets on congested networks. The routing of transmit and receive paths are configured to use the same network nodes to minimize asymmetry. Changing router and queue conditions may result in fluctuating asymmetry. Fig. 4 provides a representation of the characteristics of channel asymmetry under dynamic latency variation. In these applications, typically, the 87L relays depend on external time synchronization for accurate estimation of the one-way channel delay and alignment of 87L data. A loss of the external time source longer than the holdover period can result in the loss of 87L protection.

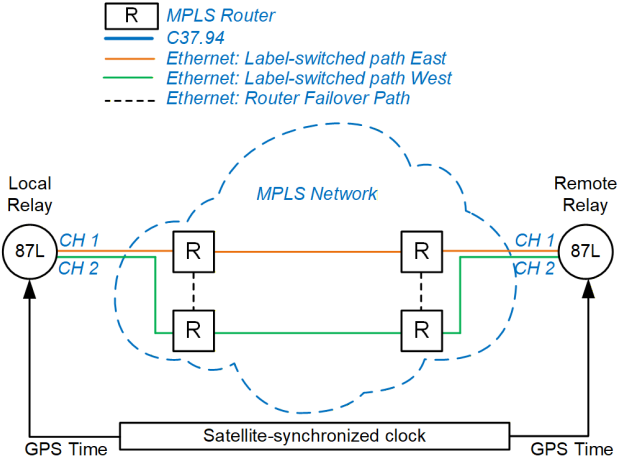


Fig. 3. Ethernet 87L communications over MPLS network.

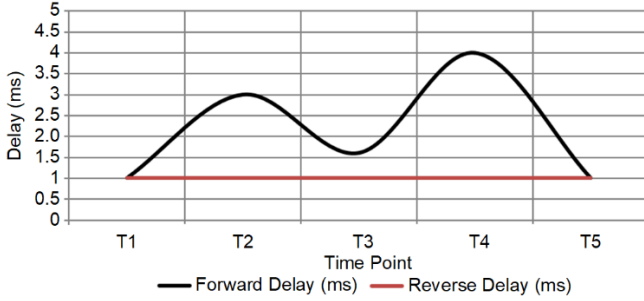


Fig. 4. Dynamic latency varying condition.

III. REVIEW OF EXISTING CHANNEL DELAY ESTIMATION METHODS

In this section, we review the existing channel delay estimation methods along with their advantages and disadvantages and evaluate the impact of unprecise data alignment, as a result of channel asymmetry conditions, on the 87L protection.

A. Time-Based Synchronization Methods

87L protection requires current measurements from both terminal ends of a transmission line to be accurately aligned in time before differential calculations are performed. Traditional implementations through deterministic TDM-based channels could compensate for communications delays, using channel-based synchronization methods. However, packet-switched MPLS networks introduce variable delay and jitter, making dedicated service provisions, such as MPLS or external time synchronization, necessary for reliable 87L operation [9] [10].

In modern utility networks, Global Navigational Satellite Systems (GNSSs) provide a common time reference to protection relays at each line terminal. The relays synchronize their internal clocks, using GNSS (in this paper, we focus on GPS-derived signals) either directly or through IEEE 1588-2008 *Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems* Precision Time Protocol (PTP), distributed across the MPLS network [11]. Current samples are then time-stamped using this common reference before being exchanged between terminals. By using synchronized time stamps, rather than packet arrival

times, the relays can accurately align measurements despite variations in MPLS network latency, including cases where the path changes across the MPLS network. This ensures that the differential algorithm compares samples representing the same electrical instant, thereby maintaining protection security and dependability.

Accurate synchronization is critical because timing errors directly translate into phase-angle errors in measured currents. Such errors can result in false differential current calculations, leading to incorrect relay operation or failure to detect faults. Consequently, GPS-referenced synchronization, often combined with PTP and synchronous Ethernet (SyncE), is a key enabling technology for deploying 87L protection over MPLS communications networks. In the absence of GPS, PTP, or other common time references, the 87L protection may experience sample synchronization errors due to clock drift and variable communications delays. In MPLS networks, these timing inaccuracies can reduce protection sensitivity, increase the risk of misoperation, and ultimately, may force the differential element to block or rely on backup protection schemes.

B. Channel-Based Synchronization Methods

Applications that do not have external time for synchronization rely on channel-based synchronization. Channel-based synchronization methods typically use the ping-pong method to determine round-trip channel delay. The local relay (R1) sends a message to the remote relay (R2). R1 maintains a time stamp ($t_{TX(R1)}$) of when the packet was sent to R2. R2 responds to the message from R1. The response also includes any delay (typically referred to as hold time) between the reception and transmission of the response packet ($t_{HOLD(R2)}$). R1 captures the time of arrival ($t_{RX(R1)}$) of the packet received from R2. The channel round-trip delay is calculated, as shown in (1). To align the remote phasor with the local phasor, the one-way channel delay is calculated as one-half of the round-trip channel delay, as shown in (2). Note that this delay will be later referenced as $T_{receive}^{calc}$.

$$T_{\text{Round trip}} = T_{RX(R1)} - T_{TX(R1)} - T_{HOLD(R2)} \quad (1)$$

$$T_{\text{one-way}} = \frac{T_{\text{Round trip}}}{2} \quad (2)$$

The advantage of channel-based synchronization is that it does not depend on external time sources. On the downside, the channel-based synchronization inherently does not have the ability to determine channel asymmetry. This becomes an issue with applications involving 87L communications over multiplexed channels or Ethernet. Not accounting for channel asymmetry can result in data misalignment and fictitious differential currents, which can cause the 87L element to misoperate.

C. Channel Asymmetry Compensation Without External Time Sources

1) Enhanced Channel-Based Synchronization Methods

The conventional channel-based synchronization method assumes that the 87L communications channel is symmetrical. When the channel becomes asymmetrical, there is a

misalignment of data due to the inaccurate clock offset estimation. The magnitude of this error is directly proportional to the magnitude of the channel asymmetry. As modern crystal oscillators are stable, if the clock offset estimation is accurate (i.e., the channel is symmetrical), there should be no sudden changes in the clock offset. The method proposed in [12] accumulates the uncompensated raw clock offset to compute a mean historical raw clock offset that gets compared with the latest estimated raw clock offset to declare a channel asymmetry when there is a significant difference between the latest and mean clock offsets. Although this is a simplified implementation, the speed of asymmetry detection depends on the length of the averaging window (for example, 5 power-system frequency cycles). This is because when there is a path-switching event, there can be momentary interruptions of traffic (an invalid clock offset estimate), and the averaging has to reinitialize so that average of valid clock offsets can be estimated. Additionally, there can be errors when there are rapid path-switching conditions. To solve such shortcomings, the technique proposed in [4] introduces an adaptive Kalman filter that declares a channel asymmetry when there is a sudden change in the trend of the estimated clock offset of at least 100 μ s over 4 ms. Once a channel asymmetry is declared, using the predicted system state, the proposed method estimates the channel asymmetry as the magnitude of the jump in the clock offset. By compensating the channel asymmetry in the estimated raw clock offset and filtering the compensated clock offset to minimize the peak-to-peak noise, the proposed method becomes quickly adaptive to channel delay conditions. However, since this method assumes that a sudden change in the channel delay corresponds to a channel asymmetry condition, it is limited to 87L applications using data multiplexers, as such applications result in sudden changes in the channel delay caused by the path switching of the data multiplexer. Additionally, this method cannot detect steady-state channel asymmetries, such as those present at the device power-up.

2) Phasor-Based Asymmetry Compensation Methods

In the absence of an external time source, the methods relying on the clock offset information obtained from the internal crystal oscillator require a sudden channel-switching (path switching) event to declare a channel asymmetry. However, in modern packet-based networks that implement an 87L scheme over MPLS, such a path-switching event may not occur, and the channel asymmetry can slowly build up over time, as presented in Section II.A. Therefore, to ensure reliable channel asymmetry detection in such Ethernet-based 87L schemes, load current-based phasor comparison techniques have been proposed [13] [14] [15]. These techniques are effective for two-terminal applications, as shown in Fig. 5, and operate on the core principle of Kirchhoff's current law, where under normal steady-state operating conditions, it is expected that the current entering a line (positive sequence current, I_{1_local}) should equal

the current exiting the line (positive sequence current, I_{1_remote}), as shown in (3). Note that if the line is a cable where charging current compensation cannot be neglected, then the charging current compensation is performed on the local and remote currents prior to comparing them for 87L protection.

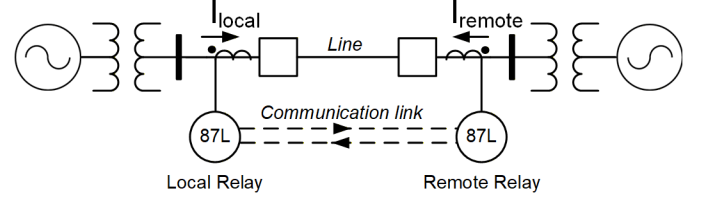


Fig. 5 Simplified two-terminal 87L application.

$$\begin{aligned} \overrightarrow{I_{1_LOCAL}} &= -\overrightarrow{I_{1_REMOTE}} \text{ or} \\ \angle I_{1_LOCAL} &= \angle I_{1_REMOTE} - 180^\circ \end{aligned} \quad (3)$$

From the perspective of the local 87L relay, to align the remote current phasors with the local current phasor, the relay estimates the receiving channel delay ($T_{receive}$), as the one-way channel delay shown in (2). When there is a channel asymmetry, the error in the estimated receive channel delay (ΔT_{error}) and the resulting error in the alignment of the current phasors (θ_{error}) are shown below in (4) and (5) respectively, where ω is the system operating frequency in rads.

$$\Delta T_{error} = T_{receive}^{actual} - T_{receive}^{calc} \quad (4)$$

$$\theta_{error} = \omega \cdot \Delta T_{error} \quad (5)$$

Since the remote current phasors for all three phases are transmitted in the same communication link, the θ_{error} appears uniformly across all three phases. Therefore, the positive sequence phasor can be represented as follows in (6),

$$\begin{aligned} \overrightarrow{I_{1_remote}} &= e^{-j\theta_{error}} \cdot \\ &\frac{1}{3} \cdot [IA_{remote} + aIB_{remote} + a^2IC_{remote}] \end{aligned} \quad (6)$$

where $a = 1 \angle 120^\circ$.

For sinusoidal quantities, a time misalignment directly translates into an angular deviation (θ_{error}) proportional to system frequency. Fig. 6 illustrates the misalignment (θ_{error}) in the positive sequence phasor for different levels of channel asymmetry for a 60 Hz nominal power system. Depending on the direction of the channel asymmetry (RX delay > TX delay or RX delay < TX delay), the remote phasor can be misaligned in the clockwise or anticlockwise direction by half of the actual asymmetry value.

Since the θ_{error} is directly proportional to the channel asymmetry, the local 87L relay can compensate for the θ_{error} by applying a rotation angle (θ_{rotate}) to the remote positive sequence current phasor, which can be derived by rewriting the θ_{error} equation in terms of current phasors, as shown in (7).

$$\begin{aligned} \theta_{rotate} &= \angle I_{1_local} - \angle (\overrightarrow{I_{1_remote}} \cdot e^{-j\theta_{error}}) \\ &= (\angle I_{1_local} - \angle I_{1_remote}) + \theta_{error} \\ &\Rightarrow \theta_{rotate} = \pi + \theta_{error} \end{aligned} \quad (7)$$

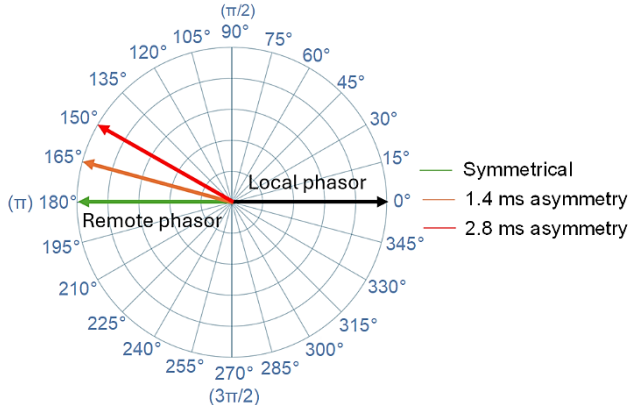


Fig. 6 Effect of channel asymmetry on local and remote phasors.

Although the process of compensating the channel asymmetry using the calculated θ_{rotate} is simple, it may not be reliable under conditions like single-phase CT errors, steady-state load unbalances, and power system faults. As an example, consider a single-phase CT error during a balanced steady-state system condition, where there is an error (α) on the A-phase current measurement. Applying small angle approximation to the Taylor series, it can be seen that the angle of the remote positive sequence current phasor can be $1/3$ of the error (α), as shown in (8) and (9), which can be falsely assumed as the channel asymmetry.

$$\vec{aI_{\text{remote}}} = \frac{1}{3}$$

$$\begin{aligned} & \bullet [IA_{\text{remote}}e^{j\alpha} + aIA_{\text{remote}}e^{-j120^\circ} + a^2IA_{\text{remote}}e^{j120^\circ}] \\ &= \frac{IA_{\text{remote}}}{3} \cdot [2 + e^{j\alpha}] \\ &= \frac{IA_{\text{remote}}}{3} \cdot [2 + \cos\alpha + jsin\alpha] \end{aligned} \quad (8)$$

$$\angle I_{\text{remote}} = \tan^{-1}\left(\frac{\sin\alpha}{2 + \cos\alpha}\right) \approx \frac{\alpha}{3} \quad (9)$$

To avoid sole reliance on current phasor measurements, voltage phasors can be additionally used to determine the channel asymmetry [16]. In this method, the locally measured voltages and currents along with the user-provided line impedance parameters are used to calculate the midpoint line voltage at either terminal of the line. The two relays then exchange this calculated midpoint and compare the received midpoint line voltage with the locally calculated value to determine channel symmetry. However, this method is challenged when the voltage measurement is unreliable (loss of potential condition) or if the line impedance is inaccurate.

D. Impact on 87L Performance

1) Impact on 87L Security

When using channel-based synchronization methods that are independent of an external time source, channel asymmetry introduces a timing error that produces an apparent phase-angle error between the local and remote current phasors. As channel asymmetry increases, the resulting phase error increases. This error results in a non-zero operating current, which is not fault-related but is introduced by a communication timing error. The magnitude of this false operate current increases with load

current magnitude, increasing the risk of undesired operation, particularly under heavy load or external fault conditions. Channel asymmetry therefore impacts 87L security. With sensitive settings (low pickup and low slope), the false operate current may cause the operating point to enter the trip region during external faults or heavy load conditions.

2) Impact on 87L Sensitivity and Dependability

Channel asymmetry also impacts sensitivity and dependability. Increasing the slope setting or otherwise desensitizing the differential characteristic improves security by accommodating the false operate current (Fig. 7). However, this reduces sensitivity to internal faults, especially in applications with limited fault current (e.g., weak infeed or inverter-based resources).

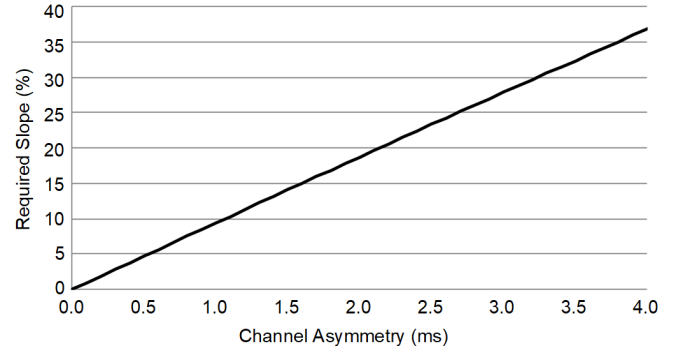


Fig. 7 Required slope vs. channel asymmetry [4].

Alternative to increasing the slope, relays may block the 87L element when external time is lost. Such measures reduce dependability and availability of 87L protection.

Therefore, to maintain both security and dependability, the relay should mitigate the underlying timing error rather than compensate through conservative settings. Channel asymmetry detection and compensation methods correct the clock offset estimate during asymmetry events and maintain proper alignment of local and remote data. This ensures that the operate current remains low during through-load and external fault conditions, while preserving sensitive settings for internal faults. This functionality is especially important when an external time source is unavailable or when the relay operates in fallback (channel-based) synchronization mode. By detecting channel asymmetry and applying appropriate asymmetry compensation, the 87L element maintains secure and dependable operation without requiring excessive desensitization or blocking.

IV. PROPOSED PHASOR-BASED ASYMMETRY COMPENSATION METHOD

The proposed method, shown in Fig. 8, uses the local and remote current phasors (and is independent of external time reference) to detect channel asymmetry. The current phasors used by the proposed method are already available in modern line current differential digital relays and are typically estimated using digital filters [17]. The proposed method leverages the assumption that under normal operating conditions, the local and remote current phasors are separated by approximately 180 degrees. Rather than solely relying on the

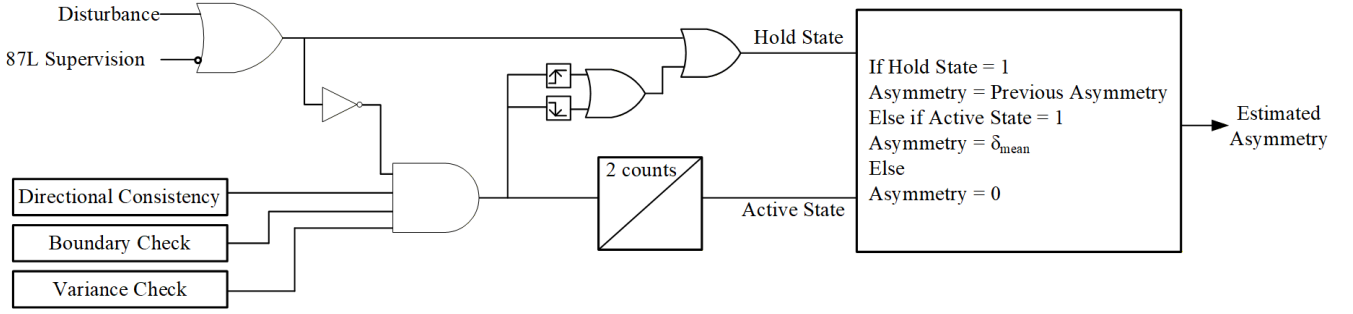


Fig. 8 Logic diagram of the proposed method.

positive sequence current, the proposed method performs a three-phase spatial consistency check to specifically identify channel asymmetry events. The proposed design is comprised of two primary operational states, namely, an active state (active asymmetry detection, estimation and compensation) and a hold state (continuous compensation with a frozen estimated asymmetry and no active asymmetry detection). When there is no detected channel asymmetry (i.e., asymmetry is 0), the proposed design does not perform asymmetry compensation. Depending on the system design (whether channel asymmetry is possible or not), the user can choose to enable or disable the proposed phasor current-based asymmetry detection and compensation.

To obtain a time-invariant steady-state baseline, the proposed method computes a referenced remote current angle for each individual phase ($\angle I\Phi R_{ref}$), when there is sufficient current to ensure reliable phasor estimates, as shown in (10). Then, using the referenced remote current angle, the proposed method computes a per-phase-angle error ($\delta I\Phi R$) assuming that for a symmetrical synchronized channel, the referenced remote current angle should be 180 degrees. This phase-angle error represents the spatial deviation from the 180 degrees baseline, which occurs during a channel asymmetry condition, as shown in (11).

$$\angle I\Phi R_{ref} = \angle I\Phi R - \angle I\Phi L \quad (10)$$

$$\delta I\Phi R = \angle I\Phi R_{ref} - 180^\circ \quad (11)$$

A. Active State

When there are no system disturbances (change in load flow, internal faults or external faults) or loss of 87L communications, the proposed method performs a multiphase, multiconsistency check to detect channel asymmetry. Once detected, the proposed method estimates the channel asymmetry based on the phase-angle error, as shown in (11).

First, the algorithm checks for directional consistency to see if all three remote current phasors shifted in the same angular direction. This can be performed by checking the sign of the estimated phase-angle error, as shown in (12).

$$\text{sign}(\delta IAR) = \text{sign}(\delta IBR) = \text{sign}(\delta ICR) \quad (12)$$

Second, the algorithm performs boundary validation to verify if the individual phase-angle errors, converted to time domain, are within the practical boundaries to filter out jitter and unrealistic timing leaps. The maximum limit will depend on the maximum possible asymmetry in the

87L communications scheme, while the minimum limit will depend on the accuracy of the current measurements, as shown in (13).

$$\text{Minimum Limit} \leq \frac{\delta I\Phi R}{\omega} \leq \text{Maximum Limit} \quad (13)$$

Finally, the algorithm performs a variance check to verify that the spatial deviation of individual phase errors is strictly within a boundary, shown in (14) and (15).

$$\delta_{mean} = \frac{\delta_A + \delta_B + \delta_C}{3} \quad (14)$$

$$I\Phi_{dev} = \delta I\Phi R - \delta_{mean} \leq 2^\circ \quad (15)$$

If the conditions in (12), (13) and (15) are true and stay true for two consecutive processing intervals, the proposed method declares a channel asymmetry. When there is a detected channel asymmetry, the remote current phasor for each phase is rotated by the estimated mean phase-angle error to compensate for the channel asymmetry. This compensated remote current phasor is then used to estimate the differential operate and restraint currents for the 87L element, as shown in (16).

$$\vec{I\Phi}_{remote_{new}} = \vec{I\Phi}_{remote_{old}} \cdot e^{-j\delta_{mean}} \quad (16)$$

B. Hold State

To preserve the alignment baseline during power system disturbances, such as power system faults or channel interruptions, the algorithm enters a hold state where the estimated channel asymmetry is frozen to the value that was last estimated when the asymmetry detection was active. The remote current phasor compensation uses the frozen estimated phase-angle error. The algorithm enters a hold state when any of the following conditions becomes true.

1. Disturbance detection: A sensitive disturbance detection is used to detect disturbances on the system such as external fault, internal fault, and changes in power flow that can comprise of changes in the consumer load demand or the direction of the power flow.
2. Loss of 87L scheme supervision: when there are channel interruptions, a data integrity check failure, or an accumulated events of spurious channel or 87L element, there is a loss of 87L scheme supervision.
3. Change in channel symmetry: When the proposed algorithm transitions between a symmetrical channel declaration and an asymmetrical channel declaration,

there is a momentary transition guard, which protects against race conditions

V. PERFORMANCE EVALUATION AND TESTING

To validate the proposed method, a 12 kV power system with two-terminals interconnected by a cable, as shown in Fig. 9, was modelled in RTDS/RSCAD for real-time HIL testing. The cable is protected by an 87L scheme whose communications link is IEEE C37.94 optical fiber connected through data multiplexers. These data multiplexers are time synchronized through a satellite-synchronized clock and the two 87L relays are free-running on their internal crystal oscillators. The relays exchange data required to perform line current differential calculations through the IEEE C37.94 communications link and perform data alignment using the channel-based synchronization method (ping-pong technique) described in Section III.B. The data being exchanged comprise instantaneous charging current compensated samples. These compensated samples are then filtered to obtain phasors, which are used by the proposed method to estimate and compensate for any channel asymmetry. The proposed method was validated under various channel asymmetry events and power system conditions, as discussed in this section.

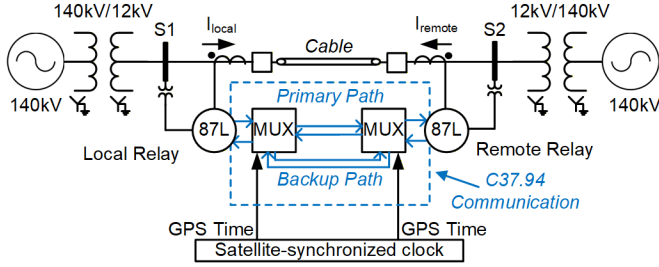


Fig. 9 The power system used to validate the proposed method.

A. Steady-State Power Flow

The validation of the proposed method begins with a simple case where there is a steady-state active power flow from terminal S1 to S2. The source angle at S1 was adjusted to result in a 1 pu load current through the power cable. During the steady power flow, at $t = 0$ s, a channel asymmetry was simulated such that the one-way channel delay changes gradually from 0 ms (symmetrical) to 4 ms (asymmetrical) over a period of 1 s. Prior to $t = 0$ s, the estimated 87L restraint current is approximately 2 pu and the estimated 87L operate current is approximately 0 pu. At $t = 1$ s, the estimated 87L restraint current stays approximately at the same level as observed at $t = 0$ s, but the uncompensated operate current increases from approximately 0 pu to 1.4 pu while the compensated operate current stayed close to 0 pu. After $t = 1$ s, the channel was made symmetrical by changing the channel delay from 4 ms (asymmetrical) back to 0 ms (symmetrical). Typically, the communications system will issue an alarm for such high-magnitude asymmetries, and the system operator intervenes to perform remedial actions. This asymmetry simulation is performed primarily for clear demonstration of the effectiveness of the proposed method.

As illustrated in Fig. 10, following the inception of channel asymmetry, as the estimated phasors settle and the asymmetry exceeds the minimum limit, the proposed method detects the channel asymmetry around $t = 0.05$ s, as indicated by the assertion of ASYMT digital (ASYMT = 1). When ASYMT is asserted, the proposed method estimates the channel asymmetry (ASYM analog) using the equations presented in Section IV. With this estimated asymmetry, the false operate currents are shown to be significantly reduced within 0.1 pu (I_{op} analog, 87IOPA: 87L operate current for A-phase without asymmetry compensation and 87IRT[p]: 87L operate current for A-phase with asymmetry compensation, where [p] = A, B, C). Note that only the A-phase operate current is shown for illustration, and B-phase and C-phase operate currents are similar to the A-phase operate current. Additionally, when there is a change in the asymmetry detection status (channel transition between symmetrical and asymmetrical conditions), the proposed method issues a momentary hold (assertion of ASYMHLD digital) to ensure that the asymmetry is estimated under stable channel conditions. The tracking of the actual asymmetry is illustrated in Fig. 11 (zoomed). It can be seen that the estimated asymmetry has an error of ± 100 μ s. Fig. 12 illustrates that with the proposed method, an 87L misoperation can be avoided (no 87OP – 87 operate assertion), therefore, the 87L element can be secured. Note that 87OP asserts if there is an 87L trip for any one of the three phases.

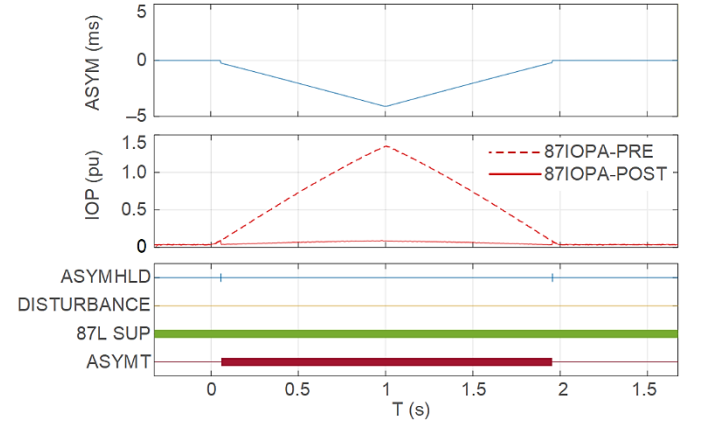


Fig. 10 Steady-state power flow—S1 to S2: proposed method response.

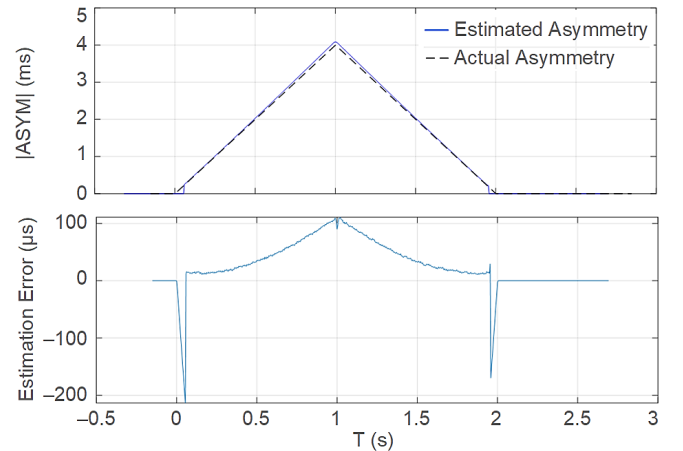


Fig. 11 Steady-state power flow—S1 to S2: asymmetry estimation error.

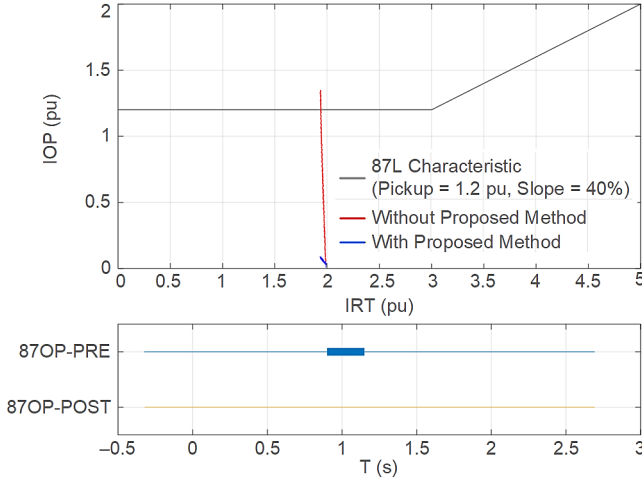


Fig. 12 Steady-state power flow—S1 to S2: 87L characteristic (A-phase).

B. External Fault

While precise data alignment under steady-state conditions is essential, a more challenging case would be to verify the effectiveness of the proposed method during power system faults that typically result in transient, high-current conditions. When a severe fault occurs outside the protected zone, it results in massive magnitudes of fault current flowing through the protected line and these currents often accompany a decaying DC offset that saturates the magnetic core of CTs. As the CT saturates, the secondary current waveforms get distorted, resulting in false phase-angle shifts. Such fictitious phase-angle measurements will result in erroneous channel asymmetry estimates, and it may become essential for the proposed method to block the channel asymmetry estimation. Hence, the proposed method—instead of blocking the asymmetry estimation (as explained in Section IV) during an external fault, due to a detected disturbance under an external fault condition—places the estimation on hold and retains the latest asymmetry estimate. This will be helpful in cases where there is an external fault during an asymmetrical channel condition. To illustrate the effectiveness of the proposed estimation and hold scheme under external faults, two fault types are chosen; namely, a single line-to-ground fault and a three-phase fault.

1) Single Line-to-Ground Fault

In this case, a bolted A-phase-to-ground fault is simulated at terminal S2 when $t \approx 0.9$ s. Similar to the previous case, a linearly increasing asymmetry is triggered at $t = 0$ s. As illustrated in Fig. 13 and Fig. 14, the proposed method detects and accurately estimates the channel asymmetry, and when there is an external fault, there is a detected disturbance that places the asymmetry estimation on hold. As the external fault clears after 10 cycles, the disturbance detection resets and the proposed method resumes estimation of the channel asymmetry. Fig. 15 shows that the duration of the false 87L operation is shorter compared to the previous case. This is because, during external faults, there is typically sufficient restraint current, and the false operate currents primarily arise due to saturated CTs.

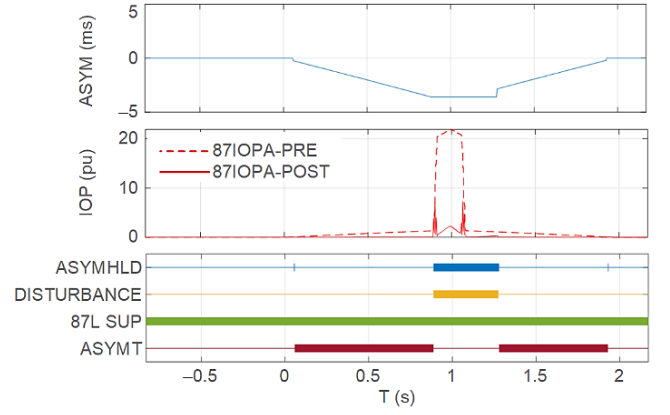


Fig. 13 External AG fault—S1 to S2: proposed method response.

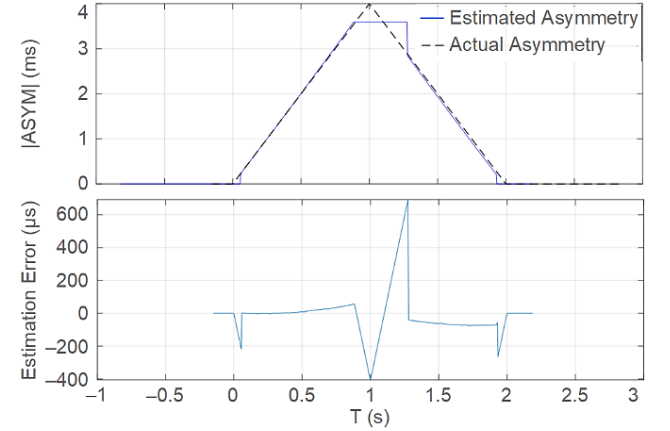


Fig. 14 External AG fault—S1 to S2: asymmetry estimation error.

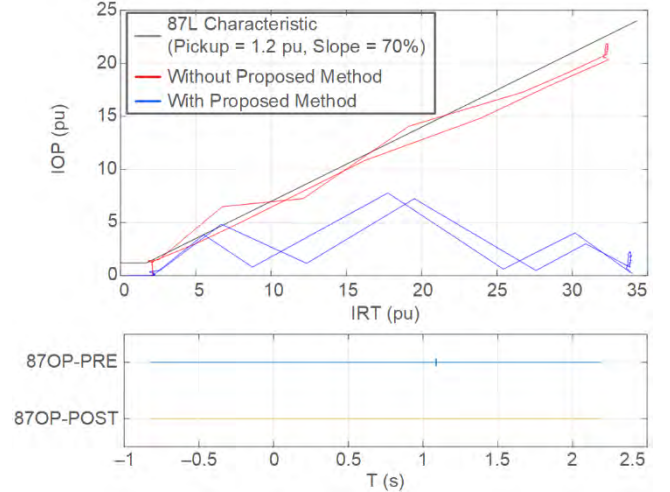


Fig. 15 External AG fault—S1 to S2: 87L characteristic (A-phase).

2) Three-Phase Fault

During a single line-to-ground fault, it was observed that the proposed method effectively rejected isolated single-phase-angle errors. Similarly, for a three-phase fault, it is expected that the proposed method will reject multiphase errors. Compared to a single line-to-ground fault, it becomes more important to block the channel asymmetry estimation during a three-phase fault, because it is possible that the CTs saturate evenly across the three phases and fool the multiphase consistency check.

In this case, a bolted three-phase fault is simulated at terminal S2 when $t \approx 0.9$ s. In Fig. 16 and Fig. 17, it can be seen that the proposed method accurately estimates the channel asymmetry, and when there is an external three-phase fault, the method blocks updates to the estimated channel asymmetry.

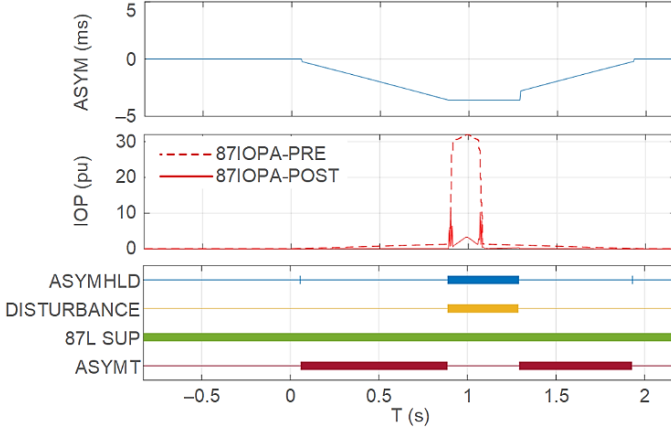


Fig. 16 External ABC fault—S1 to S2: proposed method response.

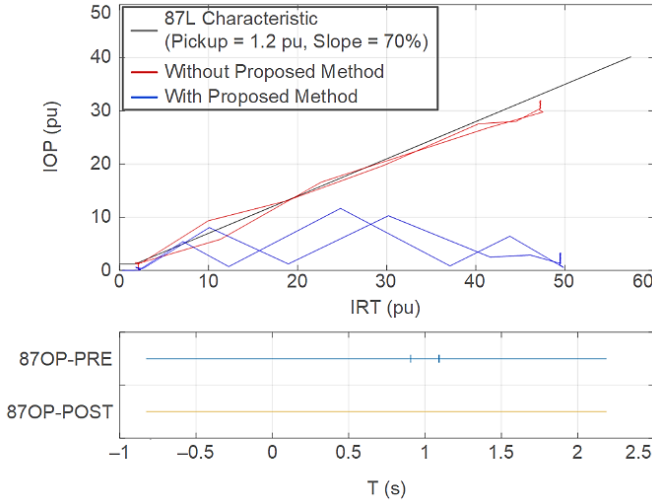


Fig. 17 External ABC fault—S1 to S2: 87L characteristic (A-phase).

C. Internal Fault

While it is necessary to ensure that the 87L scheme is secure under channel asymmetry conditions, it is vital that the 87L scheme is dependable, sensitive, and fast for internal faults that may occur during an asymmetrical channel condition. As opposed to an external fault (where a channel asymmetry can generate fictitious operate currents), for an internal fault, the proposed method can estimate the true operate current, thereby, improving the dependability of the 87L scheme. Fig. 18 shows that, with the proposed method, the actual operate current can be maintained during an asymmetrical channel condition.

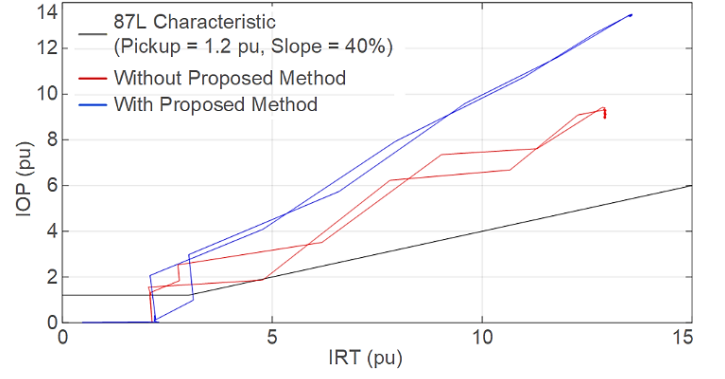


Fig. 18 Internal ABC fault—S1 to S2: 87L characteristic (A-phase).

D. Power Swing

When generators at opposite ends of a line oscillate mechanically against each other, the power angle across the line tends to continuously vary over time. Since this is a symmetrical three-phase phenomenon that results in an even phase shift across three phases, it is important to verify the security of the proposed method during power swing events. To simulate a power swing event, the remote source is modeled as a dynamic source (synchronous machine with excited and governor models), while keeping the local source as a static source (voltage source behind a Thevenin impedance). An internal resistive three-phase fault is simulated to trigger a system disturbance, and the proposed method is validated. Fig 19 shows that the proposed method does not falsely estimate any channel asymmetry during or after the disturbance.

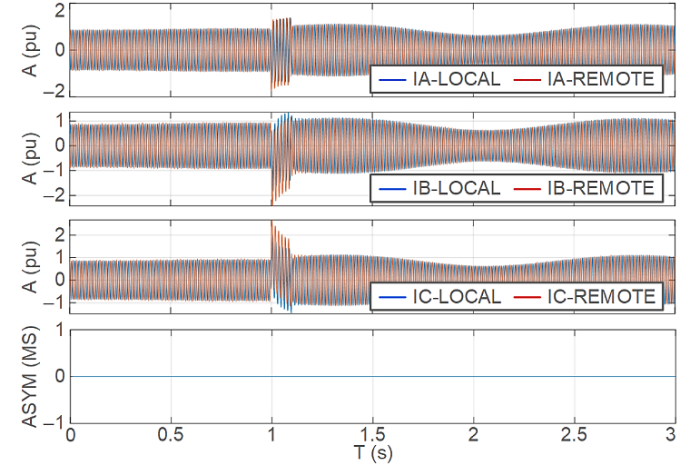


Fig 19 Power swing: three-phase analogs.

E. Corrupted Packet

As the compensations performed by the proposed method directly affect the 87L element, it is imperative that the proposed method estimates and compensates for channel asymmetry using error-free data. In this case, during a channel asymmetry condition, the 87L packet that is transmitted from the remote relay is corrupted. Fig. 20 illustrates that when there is a corrupted packet (87L SUP status is deasserted), the proposed method enters the hold state and stores the value of the latest estimated channel asymmetry, while the 87L element is blocked during this duration. The differential quantities

during the duration when the received packet is corrupted get replaced with NaN (invalid data). The method continues to estimate the asymmetry once the relay starts receiving valid packets.

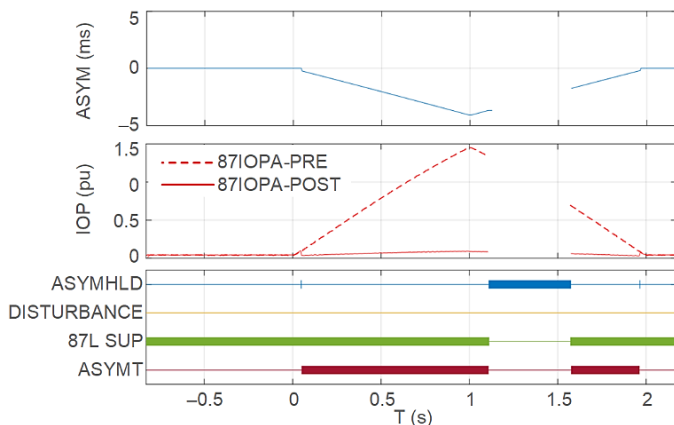


Fig. 20 Corrupted packet: proposed method response.

VI. CONCLUSION

This paper presents a novel phasor current-based channel asymmetry detection and compensation method for line current differential (87L) protection that operates without external time sources. Unlike traditional channel-based synchronization methods that assume symmetrical communications delays, or previous approaches that rely on detecting sudden delay changes, the proposed technique continuously estimates asymmetry using locally measured and remotely received current phasors based on the expected 180 degrees phase relationship between local and remote currents under normal operating conditions. By applying a three-phase consistency check, the method can reliably identify and compensate for channel asymmetries commonly encountered in modern MPLS-based communication networks.

Real-time, HIL testing demonstrates that the proposed method accurately tracks the channel asymmetry, reduces any fictitious differential operating current, and maintains the security and dependability of the 87L scheme. The method requires no voltage measurements or line parameter settings, making it a self-contained solution. As utilities continue migrating toward packet-switched communications infrastructures, the proposed method offers a practical and robust means of preserving 87L element security, sensitivity, and availability, minimizing dependence on external time synchronization.

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