Sizing CTs for 87Z Applications in Space-Constrained Switchgear: Practical Methods to Assess Their Adequacy and Sensitivity

Michael Kozich
Rehlko

Anushka M. Dissanayake, Marcos Donolo, Osama Ansari, Vinod Yedidi,
Jay Hartshorn, and Angelo D'Aversa
Schweitzer Engineering Laboratories, Inc.

Presented at the
53rd Annual Western Protective Relay Conference
Spokane, Washington
October 27–29, 2026

Sizing CTs for 87Z Applications in Space-Constrained Switchgear: Practical Methods to Assess Their Adequacy and Sensitivity

Michael Kozich, *Rehlko*
Anushka M. Dissanayake, Marcos Donolo, Osama Ansari, Vinod Yedidi, Jay Hartshorn, and Angelo D'Aversa,
Schweitzer Engineering Laboratories, Inc.

***Abstract*—Determining the minimum current transformer (CT) performance required for dependable high-impedance differential (87Z) protection remains a practical challenge, particularly as utilities and manufacturers seek to reduce CT size, cost, and footprint. This challenge is driven in part by an industry trend toward compact switchgear footprints, which reduces the available space for CT installation and can limit the size and performance of the CTs that can be accommodated. This paper investigates the minimum C-class CT suitable for 87Z applications and provides guidelines for selecting CTs to ensure reliable operation.**

The paper presents practical methods for estimating internal-fault voltage-pulse width and minimum detectable fault current directly from CT excitation curve data. The proposed techniques enable protection engineers to assess CT suitability, determine minimum CT requirements, and evaluate 87Z sensitivity numerically. The methods are validated using CTs of multiple C-classes through high-current testing over a wide range of fault-current magnitudes, including both symmetrical and asymmetrical fault conditions. Experimental results show strong agreement between estimated and measured pulse widths and sensitivity limits. The proposed methods provide accurate, repeatable, and straightforward tools that reduce testing effort, time, and cost while supporting the application of lower-class CTs in modern high-impedance differential protection schemes.

I. Introduction

The technology landscape is constantly evolving, with modern systems becoming smaller, more cost-effective, and increasingly efficient. Traditionally, the power system industry has adopted new technologies gradually due to the importance of reliability and the preference for proven solutions. This conservative approach has been particularly evident in substation and switchgear design. Recent growth in data centers and the push to reduce facility footprint are driving more compact and space-constrained designs. As a result, long-standing design practices and assumptions must be reevaluated to ensure they continue to provide value while supporting modern design objectives.

Protection of power systems relies heavily on current transformers (CTs), which provide the input signals necessary for protective relays to detect and isolate faults. These relays must analyze current waveforms quickly and accurately to ensure that faults are cleared before they escalate into equipment damage or broader system disturbances. In switchgear applications, CTs are commonly required not only for feeder protection but also for bus differential protection schemes that monitor the total current entering and leaving the protection zone.

High-impedance differential (87Z) protection schemes are widely applied for bus differential protection due to their simplicity, sensitivity, and inherent security against external faults [1]–[8]. These schemes operate by summing CT secondary currents and placing a stabilizing resistor (Rs) in its path. Under normal and external fault conditions, the summation current produces minimal voltage on Rs and a large voltage during internal faults [2] [3]. Metal-oxide varistors (MOVs) are used to limit overvoltage during fault conditions [2] [4].

The CT voltage rating (C-class in ANSI) and MOV clamping voltage determine the signals measured by the relay and, consequently, the effectiveness of 87Z protection [2]. Typical 87Z protection algorithms use the voltage across the Rs, the current through Rs, or both as operating quantities. During internal faults, the voltage across Rs typically resembles a square-wave pulse due to the combined effects of CT saturation and MOV clamping. Higher C-class CTs and lower MOV clamping voltages produce wider voltage pulses, while the MOV clamping voltage also affects the pulse peak magnitude. Wider pulses result in a higher voltage magnitude measurement, improving sensitivity.

CTs with voltage rating below C200 generally do not provide sufficient pulse width for fundamental-frequency- or rms-based 87Z elements. Consequently, industry practice has traditionally recommended the use of C200-class CTs or higher [3] [4]. Higher-class CTs provide greater volt-time capability, resulting in stronger and more sustained voltage signals during internal faults [2]–[8]. Accordingly, CTs with voltage rating of C200 or higher remain the preferred choice for high-impedance differential applications, particularly in systems with high fault-current levels or where maximum protection margin is required.

In practice, however, modern switchgear constraints challenge these traditional requirements. Bus differential protection schemes often require multiple CTs within a single breaker cell, including separate CTs dedicated to feeder protection and bus protection. In reduced-footprint switchgear designs, physical space limitations can prevent the use of larger, higher-class CTs and may preclude configurations such as double-stacking CTs on the bus stub insulation tube [9].

Double-stacking CTs on both bushings is also frequently employed in tie-breaker applications and may become impractical in compact switchgear designs. These constraints may require engineers to specify lower-C-class CTs (e.g., C100 or below) in applications where higher-class CTs would traditionally be specified.

At the same time, practical system considerations, such as staged expansions, retrofit projects, and multiowner infrastructure, often lead to nonideal CT configurations, including mismatched ratios or mixed performance characteristics [6]. High-impedance schemes are particularly sensitive to such conditions, and traditional guidance generally discourages their application where CT performance is limited or inconsistent [6].

To address the aforementioned challenges, this paper reexamines the relationship between CT performance and 87Z protection behavior under practical application constraints. The objective is to determine whether lower-C-class CTs can provide dependable 87Z operation and to quantify the resulting tradeoffs in protection sensitivity and performance. To this end, the paper:

- Investigates the performance of high-impedance differential protection schemes using lower-C-class CTs.
- Quantifies the impact of CT characteristics on internal fault detection sensitivity and protection dependability.
- Provides practical design and application guidance for implementing 87Z protection with lower-class CTs.

By bridging traditional protection theory with modern switchgear constraints and relay capabilities, this paper enables more flexible and practical application of 87Z in real-world systems.

The remainder of this paper is organized as follows. Section II discusses the time-domain sample-based waveform recognition element (SBWFRE) for 87Z applications and its advantages. Section III presents a method for determining whether a selected CT can dependably detect high-current internal faults by estimating the voltage-pulse width using CT excitation curve data for lower-class CTs. Section IV describes a method for estimating the minimum fault-current sensitivity of 87Z schemes using CT excitation curve data. Section V presents high-current experimental results that validate the proposed methods. Finally, Section VI concludes the paper and presents practical guidelines for the application of lower-C-class CTs in 87Z protection schemes.

II. Time-Domain 87Z

A typical single-phase version of an 87Z scheme for a bus with three feeders is shown in Fig. 1. The CTs associated with a particular phase are connected in parallel and are supervised by the 87Z relay through a Rs, an MOV, and a bypass relay connected across the CT secondary circuit. The Rs, typically 2 kΩ, develops the operating voltage used by the relay and is often implemented as a voltage divider (R1 and R2) to lower the voltage presented to the relay input (Rs = R1+R2). During normal load and external fault conditions, the CT secondary currents sum to approximately zero, producing little voltage across Rs. During an internal fault, the differential current develops a voltage across Rs that is used by the relay to detect and isolate the fault.

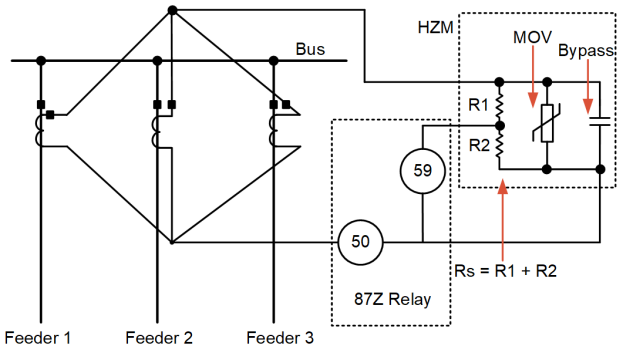

Fig. 1. Single-phase diagram showing typical 87Z connections

The relay settings are typically defined in terms of the voltage across the entire Rs. The relay internally accounts for the voltage-divider ratio and calculates the corresponding voltage and current thresholds used by its protection algorithms.

An MOV is included to limit the voltage across the CT secondary circuit to a safe level during internal faults. Depending on the application, the MOV clamping voltages may range from approximately 800 V to 2 kV. Because sustained fault currents can cause significant energy dissipation in the MOV, a bypass relay is also provided. Following fault detection, the bypass relay closes to divert current away from the MOV and Rs, limiting thermal stress and protecting the high-impedance circuit. Some high-impedance modules (HZMs) include an internal high-speed MOV bypass function; however, an external lockout or auxiliary bypass relay is often recommended to provide additional protection and redundancy.

As mentioned earlier, although C200 or higher CTs are generally preferred for 87Z protection applications, protection engineers and switchgear manufacturers may choose lower-class CTs in certain situations, such as compact-footprint switchgear designs, where reduced size and lower cost are important considerations. Lower-class CTs may still provide dependable performance when time-domain elements are used, such as those employing high sampling rates or bipolar peak detectors. The 87Z logic discussed in [2] consists of one phasor-based algorithm and two time-domain algorithms. The phasor-based algorithm operates on phasor quantities estimated by processing signal samples through digital band-pass Fourier filters. In contrast, the time-domain algorithms operate directly on the raw signal samples.

Time-domain Algorithm 1 uses raw voltage samples to estimate the voltage magnitude and compares the estimated magnitude with a threshold value to determine whether an internal fault is present. Time-domain Algorithm 2, referred to as the SBWFRE, is the primary focus of this paper. Fig. 2 illustrates the SBWFRE logic.

The inputs to the SBWFRE logic are raw voltage and current samples obtained from the analog-to-digital (A/D) converters.

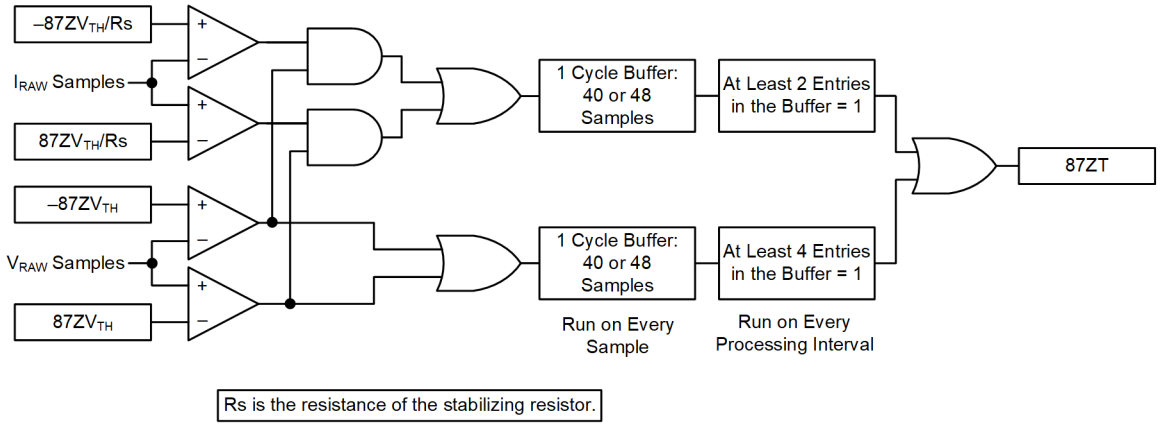

Fig. 2 87Z SBWFRE logic

The 87Z relay samples these signals at a rate of 2,400 Hz, corresponding to 40 samples per cycle for 60 Hz systems and 48 samples per cycle for 50 Hz systems. As shown in Fig. 2, the logic compares the sampled current and voltage values against corresponding positive and negative threshold values to ensure security. The resulting binary signals are then processed through AND and OR gates.

The processed binary quantities are stored in two one-cycle memory buffers. The upper buffer shown in Fig. 2 stores a logic '1' whenever both the current and voltage sampled values exceed their respective thresholds. The lower buffer stores a logic '1' whenever only the voltage sampled values exceed the thresholds.

For the SBWFRE to assert a tripping signal, one of the following conditions must be met:

1. The voltage and current sampled values exceed their respective thresholds for two entries within the most recent cycle as shown in the upper buffer of Fig. 2; or
2. The voltage sampled values alone exceed the thresholds for four entries within the most recent cycle as shown in the lower buffer of Fig. 2).

When either condition is satisfied, the logic asserts the 87ZT bit.

III. Internal-Fault Voltage-Pulse-Width Estimation for High-Current Faults

In the time-domain 87Z schemes, accurately determining the internal-fault voltage-pulse width for high-current faults becomes critical, as the dependability of the protection relies on this width. This section presents a method to estimate the internal-fault voltage-pulse width for fault currents up to 50 times nominal current using the data from the CT excitation curve. The estimated pulse width is then used to determine the minimum CT requirements necessary for dependable 87Z operation.

A. How to Approximate Volt-Time Area Using the CT Excitation Curve

A typical voltage waveform across the Rs for an internal fault is shown in Fig. 3. This event was recorded during a staged 65 kA internal fault using a C100 1200:5 CT. Only the waveform corresponding to a half-cycle fault current is shown. The corresponding CT excitation curve is also shown in Fig. 4. With a sufficiently large sampling rate, the approximate volt-time area of this voltage pulse can be computed using (1).

$$A_{VT} = Ts \sum_{i=0}^{n} y_i \tag{1}$$

where:

Ts is the sampling interval, which is equal to 1/2400 s in this example.

y_i are the sampled values.

n is the number of samples within the boundary.

A_{VT} is computed as 1.07 V • s for the example.

The volt-time area can be computed from the CT excitation curve. The CT excitation curve provides the excitation voltage as an rms value of a sinusoidal signal at a given frequency. The volt-time area of a half-cycle sinusoidal signal with the rms value of V_{rms}, frequency *f,* and period *T* can be calculated as shown in (2).

$$A_{CT} = \int_{t_0}^{t_0+T/2} \sqrt{2}V_{\text{rms}} \sin(2 \bullet \pi \bullet f \bullet t)dt = \frac{\sqrt{2}\text{V}_{\text{rms}}}{\pi \bullet \text{f}} \tag{2}$$

For a 60 Hz sinusoidal signal, this volt-time area is given by $0.0075 \bullet V_{\text{rms}}$. Let $V_{\text{rms}(I_e = 10\text{ A})}$ denote the excitation voltage at an excitation current of 10 A. From Fig. 4, $V_{\text{rms}(I_e = 10\text{ A})} = 142\,V$. The corresponding computed volt-time area using this value is 1.065 V • s, which is close to the experimentally calculated A_{VT}. We empirically found that using $V_{\text{rms}(I_e = 10\text{ A})}$ to compute the half-cycle volt-time area provides a conservative estimate of the volt-time area associated with the internal-fault voltage pulse.

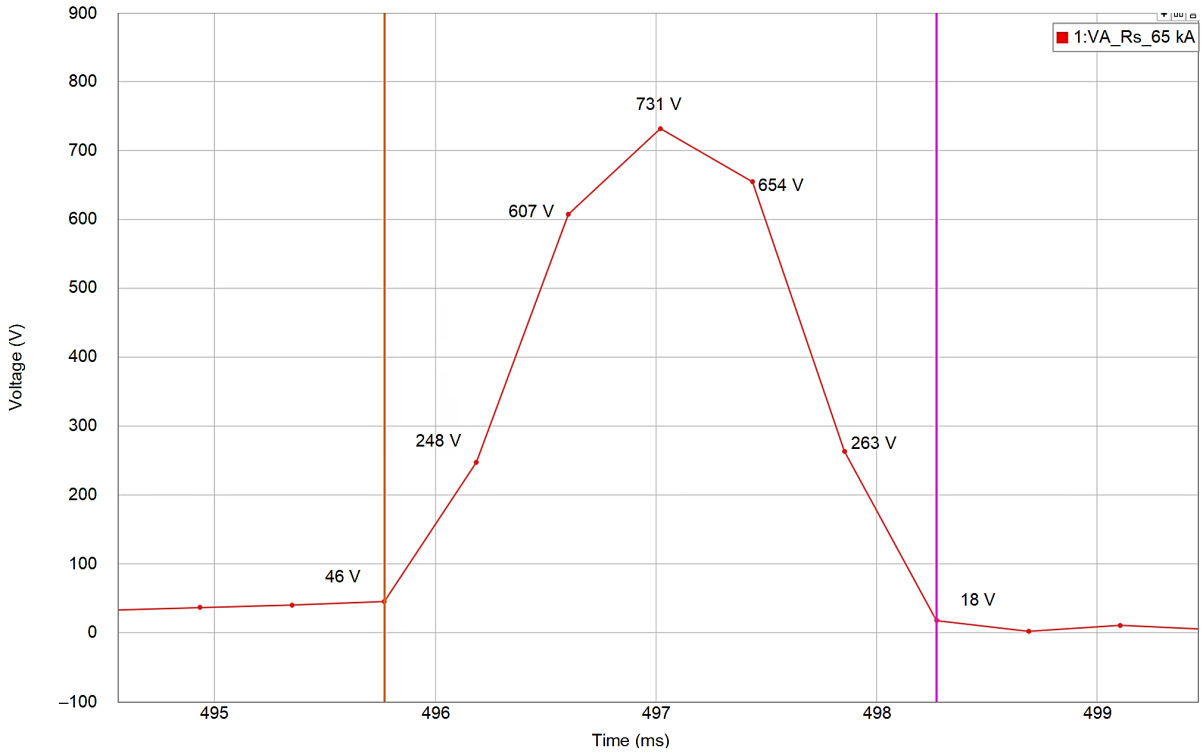

Fig. 3 Voltage pulse of a C100 1200:5 CT for a 65 kA internal fault

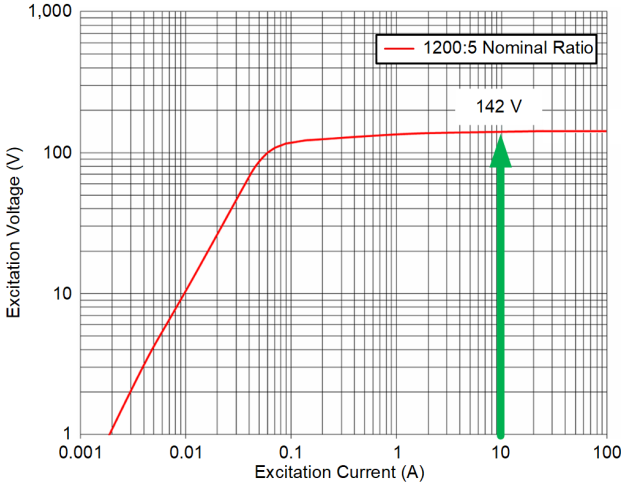

Fig. 4 CT excitation curve of the C100 1200:5 CT at 60 Hz

B. How to Approximate the Voltage-Pulse Width

The volt-time area of an internal-fault voltage pulse can be approximated by a triangle with a peak of 840 V, as shown in Fig. 5. The 840 V peak value is based on experimental observations from the high-current fault tests presented in this paper. This value is specific to the MOV characteristics of the hardware used in the test setup and should not be considered universally applicable. MOVs with different voltage-clamping characteristics may produce different peak voltages under similar fault conditions. In Fig. 5, $87ZV_{TH}$ is the voltage pickup threshold of the SBWFRE in peak value, Δt_{TH} is the pulse width at $87ZV_{TH}$, and Δt_{base} is the pulse width close to zero voltage. Since the estimated volt-time area is known from the $0.0075 \bullet V_{rms(I_e = 10\ A)}$, we can calculate the Δt_{base} as shown in (3).

$$\Delta t_{base}(\text{ms}) = \frac{2 \bullet 0.0075 \bullet 1{,}000}{840} V_{rms(I_e = 10\ A)} = \frac{V_{rms(I_e = 10\ A)}}{56} \quad (3)$$

Now it is straightforward to calculate the pulse width at a given setting value, as shown in (4).

$$\Delta t_{TH}(\text{ms}) = \frac{(840 - 87ZV_{TH})}{840} \Delta t_{base}(\text{ms}) \quad (4)$$

For switchgear 87Z applications, a typical minimum 87Z pickup setting is 200 V, expressed as an rms quantity across the Rs. The SBWFRE, however, operates directly on instantaneous samples rather than rms quantities. Therefore, the rms setting is converted to a peak value by multiplying by √2. An additional factor of 1.5 is applied to maintain secure operation during worst-case asymmetrical faults with significant dc offset. As a result, the corresponding SBWFRE voltage threshold ($87ZV_{TH}$) is 425 V and will be used in the following analysis.

For the $87ZV_{TH} = 425$ V, (4) simplifies to (5).

$$\Delta t_{425\ V}(\text{ms}) = 8.8 \bullet 10^{-3} \cdot V_{rms(I_e = 10\ A)} \quad (1)$$

For this example, the calculated pulse width is $\Delta t_{425\ V} = 1.25$ ms, which is close to the actual measured pulse width of ~1.3 ms. Section V.A compares the pulse width calculated using the proposed volt-area approximation with the pulse width measured experimentally for a range of C50 and C100 CTs. The comparison includes multiple fault-current levels under both symmetric and asymmetric fault conditions. The close agreement between the calculated and measured pulse widths demonstrates the accuracy of the volt-area approximation and validates its use for pulse-width estimation across the tested operating range.

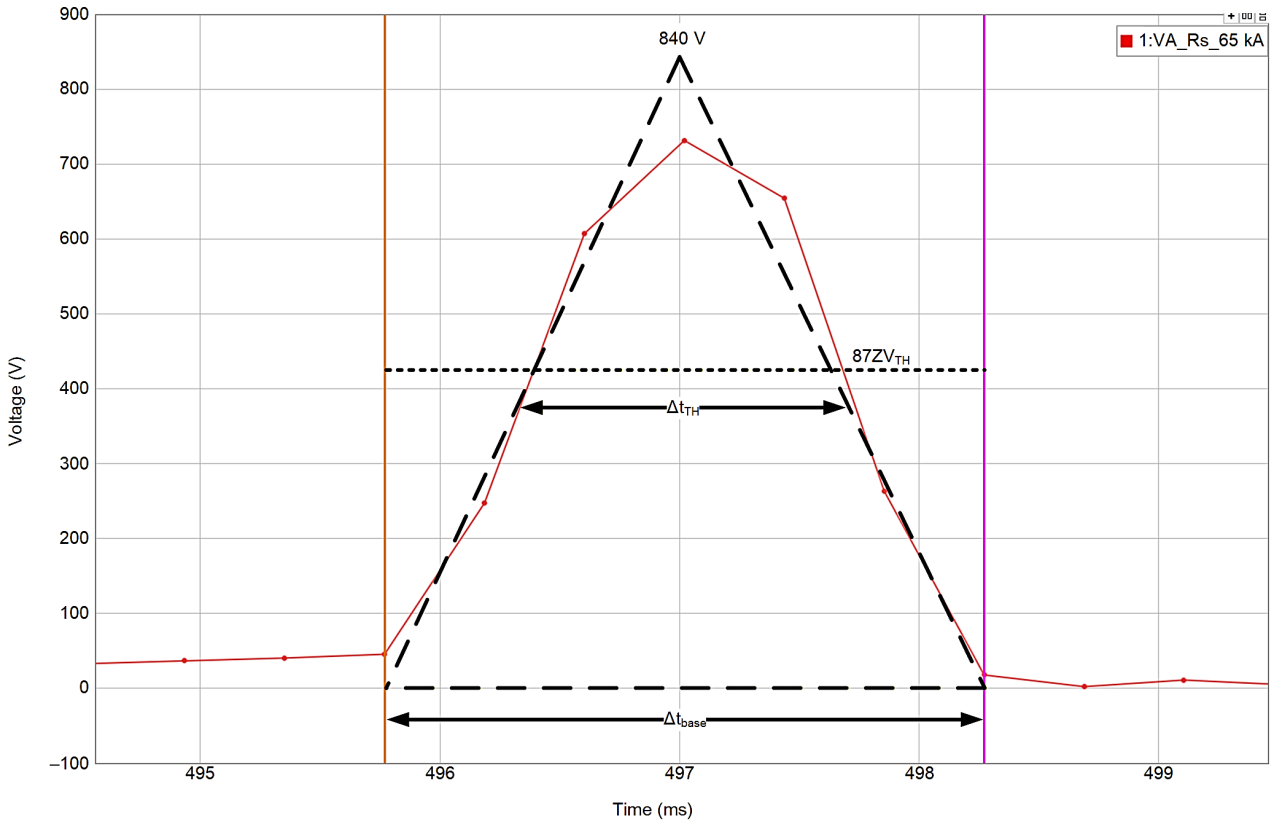

Fig. 5 Volt-time area estimation using triangle approximation

The triangular approximation works for C-class C100 and below. For C-class C200 and above, the voltage pulse begins to flatten at its peak as the fault current grows, resulting in a trapezoidal shape. Therefore, the area approximation must be modified for higher-class CTs.

To approximate the voltage-pulse width of a C50 or C100 CT, evaluate (4). For dependable 87Z operation, the two voltage samples and the corresponding two current samples must exceed their respective 87Z thresholds. At a sampling rate of 2,400 Hz, a voltage-pulse width greater than 0.83 ms (2/2,400 s) at the $87ZV_{TH}$ guarantees that more than two samples are above the pickup threshold. To provide an additional margin and ensure dependable 87Z protection, a minimum voltage-pulse width of 1 ms at the $87ZV_{TH}$ can be established. Based on the analytical results and experimental testing, CTs with an excitation voltage of 140 V or greater at an excitation current of 10 A are suitable for use with the 87Z SBWFRE element.

The voltage-pulse width approximations are based on experimental results obtained with fault-current magnitudes from 50 to 54 times the nominal current. As the fault current increases, CT saturation occurs more quickly, causing the voltage-pulse width to decrease. Therefore, when using C100-class and lower CTs, the maximum fault current should be less than 50 times the nominal current.

IV. Minimum Fault-Current Estimation

Determining the minimum fault current detectable by the 87Z element is typically done by using the CT excitation current (IE) corresponding to the 87Z pickup voltage in rms quantity. For CTs below C200, the 87Z pickup voltage may be close to or exceed the CT knee-point voltage and, in many cases, may not intersect the CT excitation curve at all. Making it impossible to determine IE and scheme sensitivity from data sheet information alone. In such cases, a primary current injection test is traditionally required. As an alternative, this section introduces a method to estimate the minimum detectable fault current directly from the CT excitation curve.

An approximation of the minimum peak voltage required across the Rs to operate the 87Z SBWFRE is developed first. At low fault currents, the MOV does not conduct because the peak voltage ($87Z_{VP}$) across the Rs during a low-level internal fault does not reach the MOV conduction voltage. Under these conditions, the voltage pulse resembles the sketch shown in Fig. 6. To get two samples above the threshold for reliable operation of the 87Z element, it is assumed that the peak must be at least 20 percent above threshold. Therefore, $87Z_{VP} = 1.2 \bullet 87ZV_{TH}$.

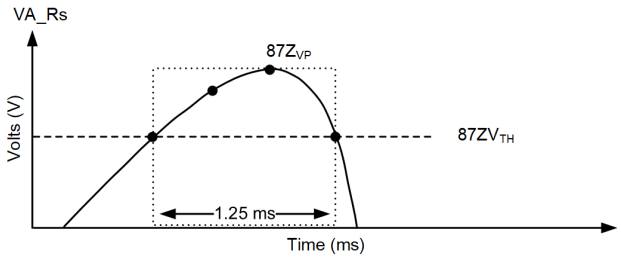

Fig. 6 Voltage across the Rs for low internal fault currents

The volt-time area produced by the peak voltage can then be used to determine the operating point on the CT excitation curve ($V_{rms(min)}$), as shown in (6).

$$V_{rms(min)} = \frac{87Z_{VP} \bullet 1.25}{0.0075 \bullet 1000} = 0.2 \bullet 87ZV_{TH} \quad (6)$$

Here, 0.0075 is derived from (2), and 1.25 ms is the time between four consecutive samples sampled at 2,400 Hz. For $87ZV_{TH} = 425$ V, the $V_{rms(min)} = 85\ V$. From the CT excitation curve, find the IE at ~85 V (IE_{85V}) and apply it to (7) to calculate the minimum primary fault current at which the 87Z SBWFRE operates.

$$IF_{rms(min)} = \left(1.5 \bullet n \bullet IE_{V_{rms(min)}} + \frac{87Z_{VP}}{Rs}\right) \bullet CTR \quad (7)$$

where:

1.5 is a security margin.

n is number of CTs in the scheme per phase.

Rs is the resistance of the stabilizing resistor.

CTR is the CT ratio of CTs.

V. Results

This section discusses the experimental testing performed as part of an extensive validation program conducted over several years. High-current internal fault tests were conducted at KEMA Laboratories to validate the voltage-pulse-width-estimation method for internal faults. Multiple back-to-back high-current tests were performed under both internal and external fault conditions, with currents up to 100 kA and under both symmetrical and asymmetrical conditions. These tests were conducted over a two-day period using the same relay and HZM unit. Upon completion of the testing, no damage or degradation was observed in either the relay or the HZM unit. Both devices continued to operate correctly and demonstrated reliable performance throughout and after the extensive test program.

Laboratory testing of minimum fault-current sensitivity was conducted using a current amplifier system capable of supplying up to 2.5 kA. All CTs tested were 60 Hz and a nominal secondary of 5 A. The Rs was 2,000 Ω.

In addition to the tests presented in this section, comprehensive testing was previously performed at Powertech Labs Inc. (Canada) and the IPSEP Testing and Certification Laboratory (LEC-IPSEP, Argentina). The testing described in this paper built upon those earlier efforts and provides additional validation under a broader range of operating conditions.

A. Internal-Fault Voltage-Pulse-Width Estimation

The schematic of the test setup is shown in Fig. 7, and the actual experimental setup at the KEMA testing facility is shown in Fig. 8. Three CTs were used in the test setup, and current was applied through only one CT for 100 ms. Both symmetrical and asymmetrical faults were tested. The results are summarized in Table I. According to the results, the estimated voltage-pulse width at the setting voltage is close to the measured values.

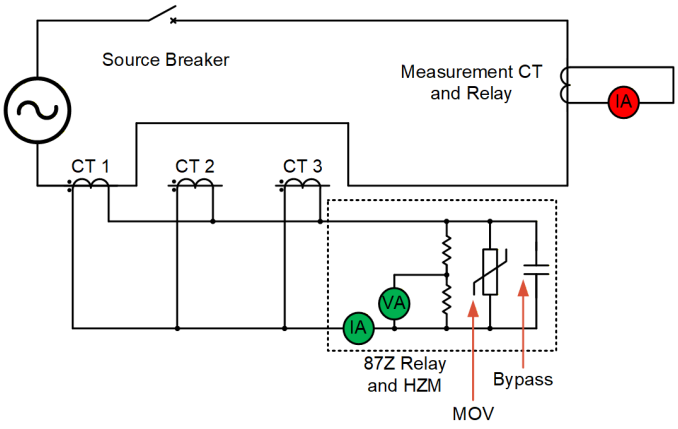

Fig. 7 Schematic diagram of the test setup

Fig. 8 Experimental test setup at KEMA Laboratories

The applied primary fault current, the relay-captured voltage across the Rs, and the differential current for various fault currents with different classes of CTs are shown in Fig. 9 through Fig. 14. The X/R ratio of the asymmetrical fault currents were ~20.

In all tests, the relay issued an 87Z trip in less than one power system cycle (in most cases, within one-quarter of a power system cycle) following the fault inception. The bypass contact operated approximately one cycle after the relay asserted the 87Z trip. This behavior is evident from the voltage across the RS (VA_Rs) dropping to zero and the differential current (I_DIFF_SEC) increasing to the relay clipping limit. The differential current increases because, once the bypass contact closes, the Rs is short-circuited, allowing the CTs to recover from saturation.

Fig. 14 compares the voltage pulse widths produced by different CTs with the same CTR during a 65 kA symmetrical fault, captured at a sampling rate of 4 kHz. The results indicate that CTs with higher excitation voltages at an excitation current of 10 A generate wider voltage pulses. Consequently, these CTs provide greater operating margins and improved dependability.

TABLE I
COMPARISON OF VOLTAGE-PULSE WIDTHS OF DIFFERENT CTS

CT Information	$V_{rms(I_e=10\,A)}$ (V)	**Fault Current and Information**	**Calculated Δt_{TH} (ms)**	**Measured Δt_{TH} (ms)**
C50 400:5	70	20 kA symmetric	0.62	0.6
C50 1200:5 (CT-W)	115	50 kA symmetric	1.01	1.22
		65 kA symmetric		1.2
		165 kA peak, 65 kA rms		1.1
C100 1200:5 (CT-X)	140	65 kA symmetric	1.23	1.2
		165 kA peak, 65 kA rms		1.05 to 1.3
C100 1200:5 (CT-Y)	142	40 kA symmetric	1.25	1.34
		65 kA symmetric		1.3
		100 kA peak, 40 kA rms		1.25 to 1.4
		165 kA peak, 65 kA rms		1.2
C100 1200:5 (CT-Z)	150	65 kA symmetric	1.32	1.43
		165 kA peak, 65 kA rms		1.3

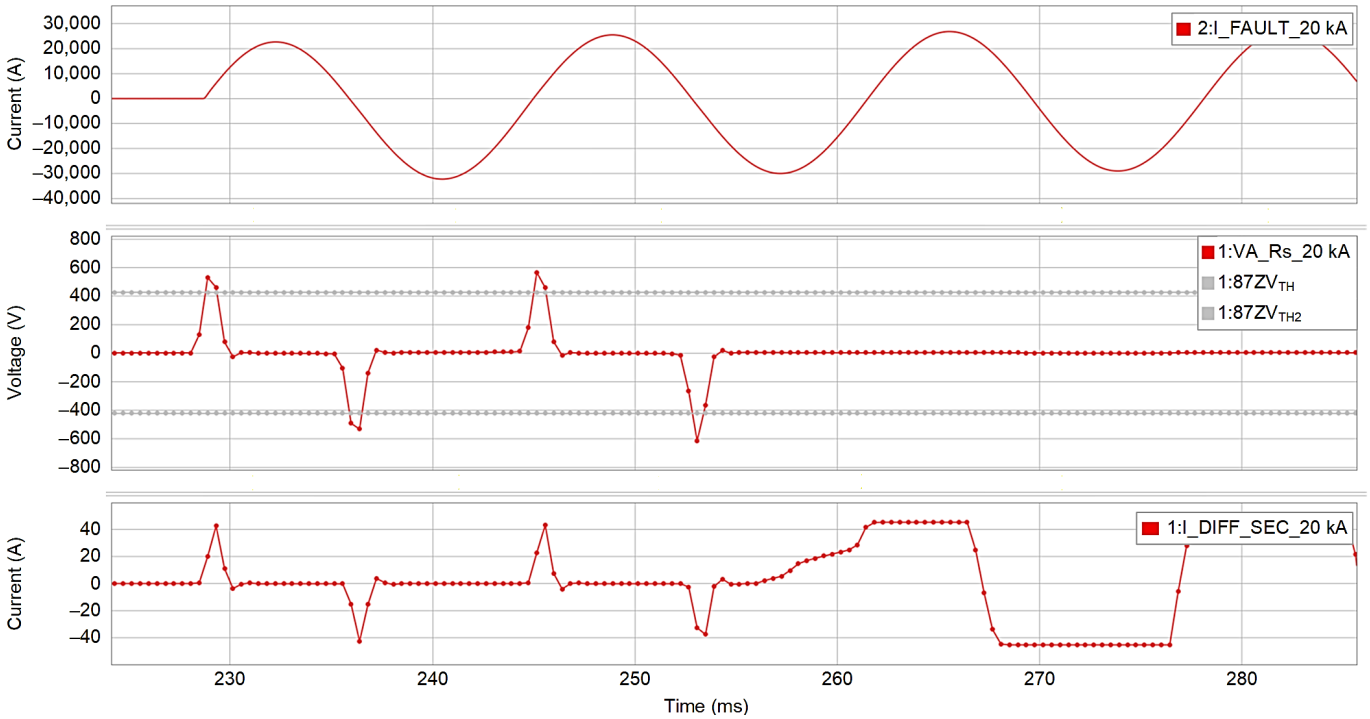

Fig. 9 Primary fault current (top), relay-captured voltage (middle), and differential current (bottom) of a 20 kA symmetrical fault with C50 (400:5) CT (70 V at 10 A excitation current)

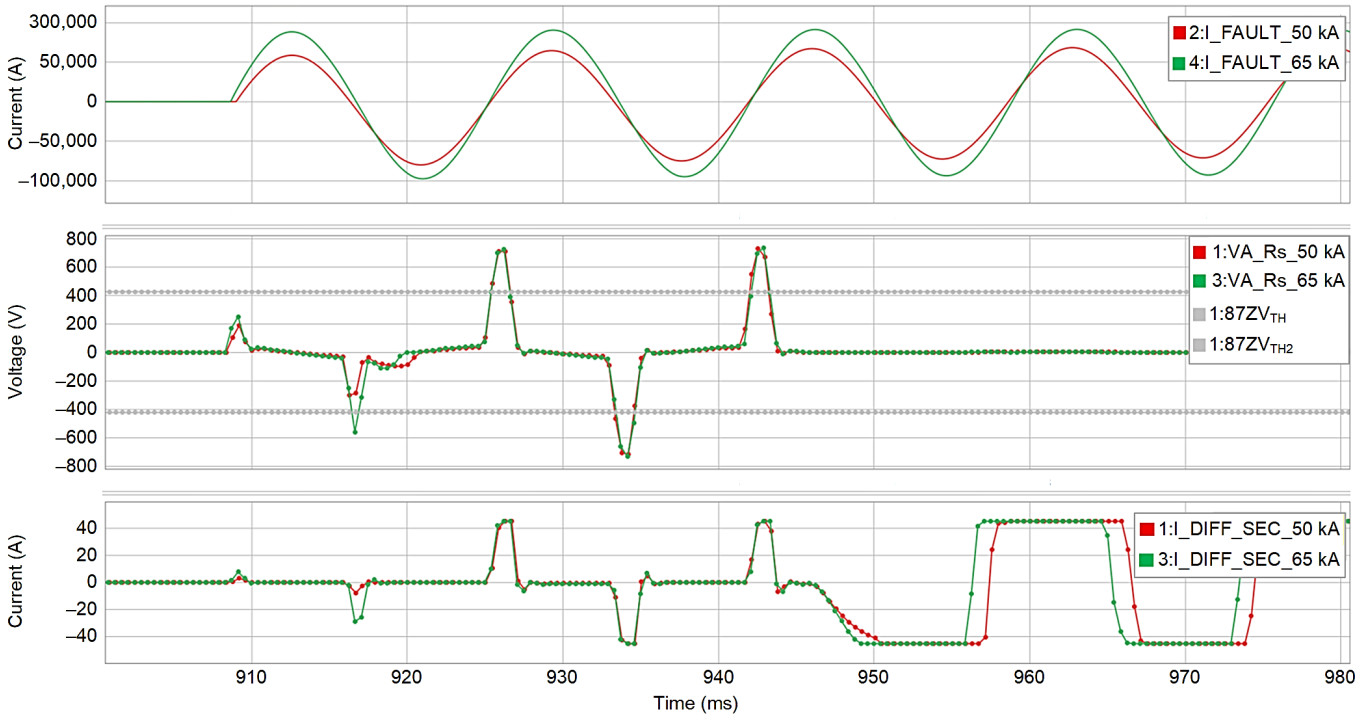

Fig. 10 Primary fault current (top), relay-captured voltage (middle), and differential current (bottom) of a 50 kA and a 65 kA symmetrical fault with C50 (1200:5) CT (CT-W 115 V at 10 A excitation current)

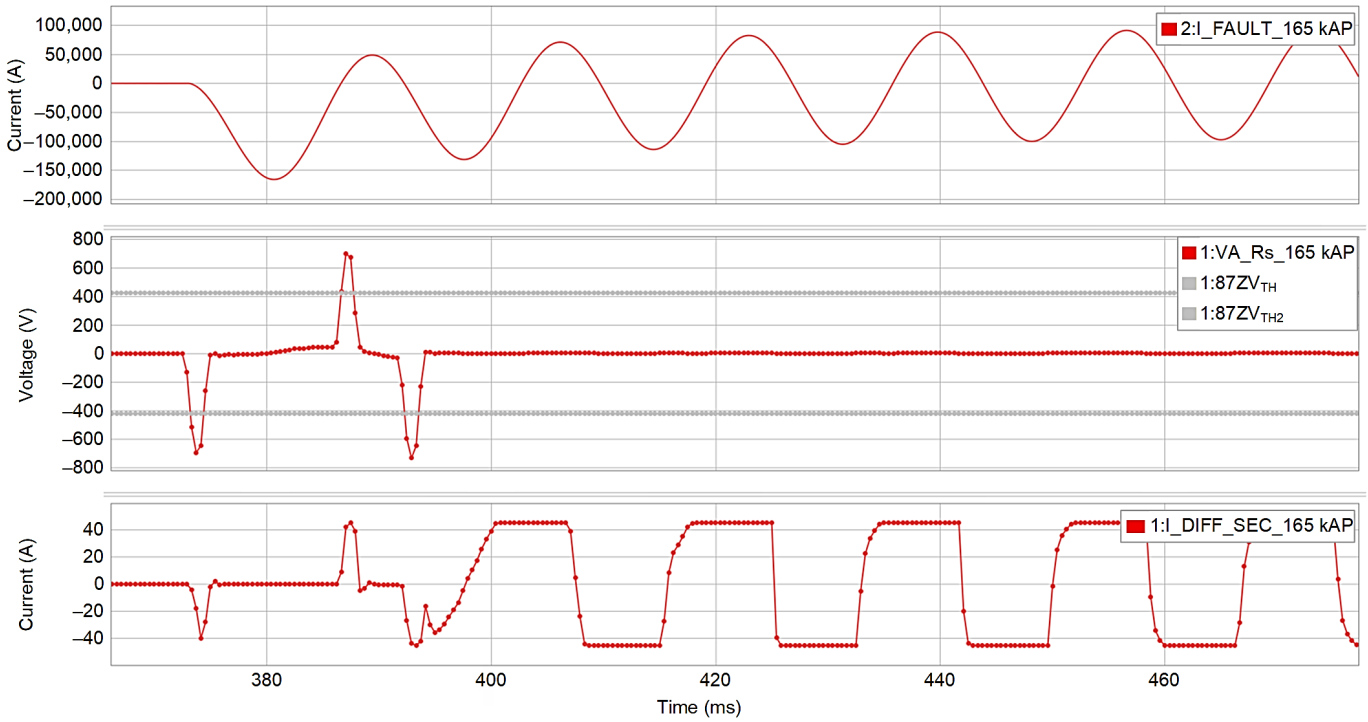

Fig. 11 Primary fault current (top), relay-captured voltage (middle), and differential current (bottom) of a 165 kA peak asymmetrical fault with C50 (1200:5) CT (CT-W 115 V at 10 A excitation current)

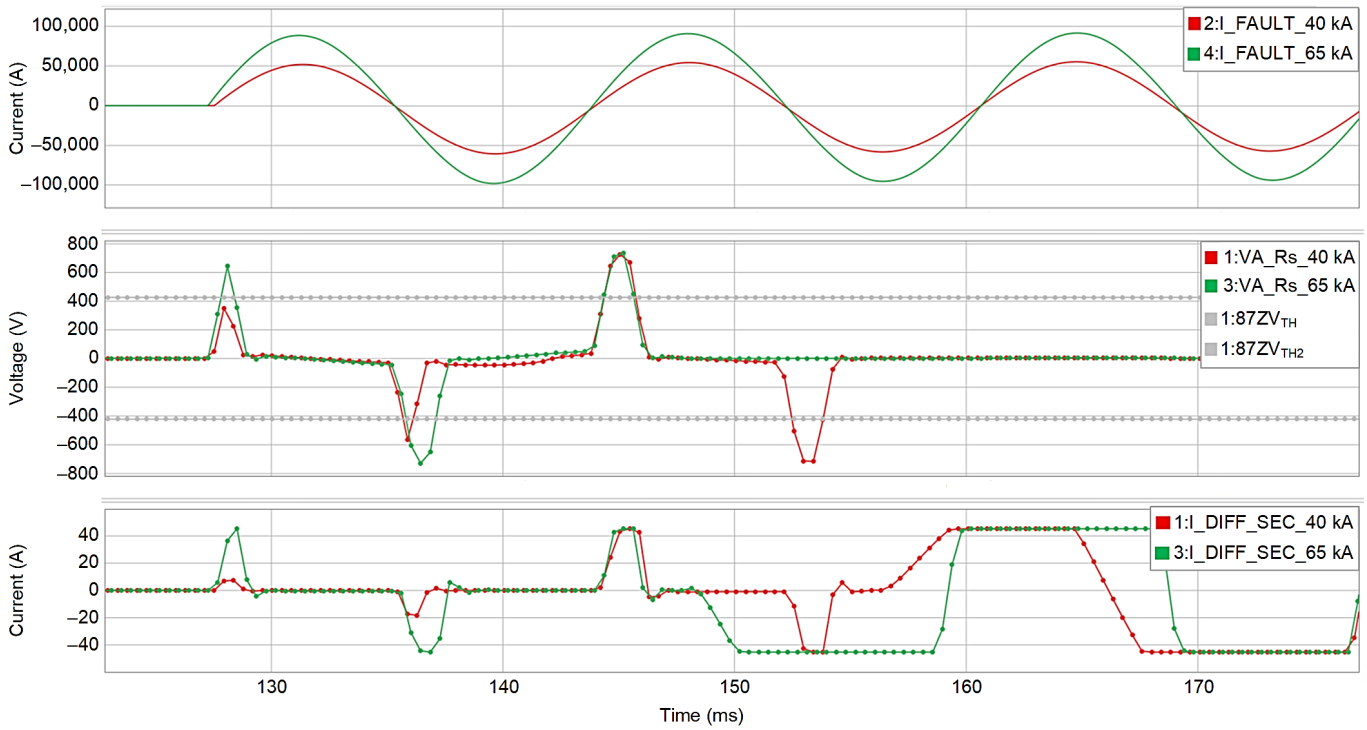

Fig. 12 Primary fault current (top), relay-captured voltage (middle), and differential current (bottom) of a 40 kA and a 65 kA symmetrical fault with C100 (1200:5) CT (CT-Y 142 V at 10 A excitation current)

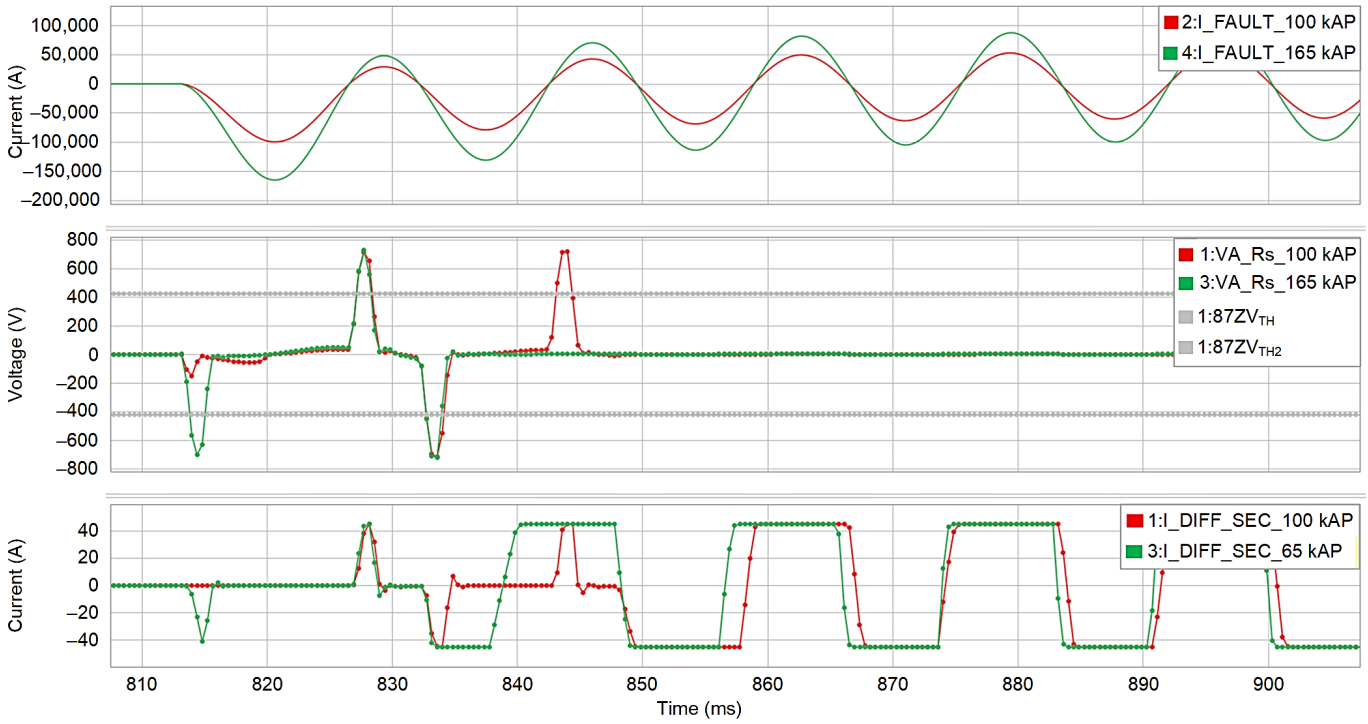

Fig. 13 Primary fault current (top), relay-captured voltage (middle), and differential current (bottom) of a 100 kA peak and a 165 kA peak asymmetrical fault with C100 (1200:5) CT (CT-Y 142 V at 10 A excitation current)

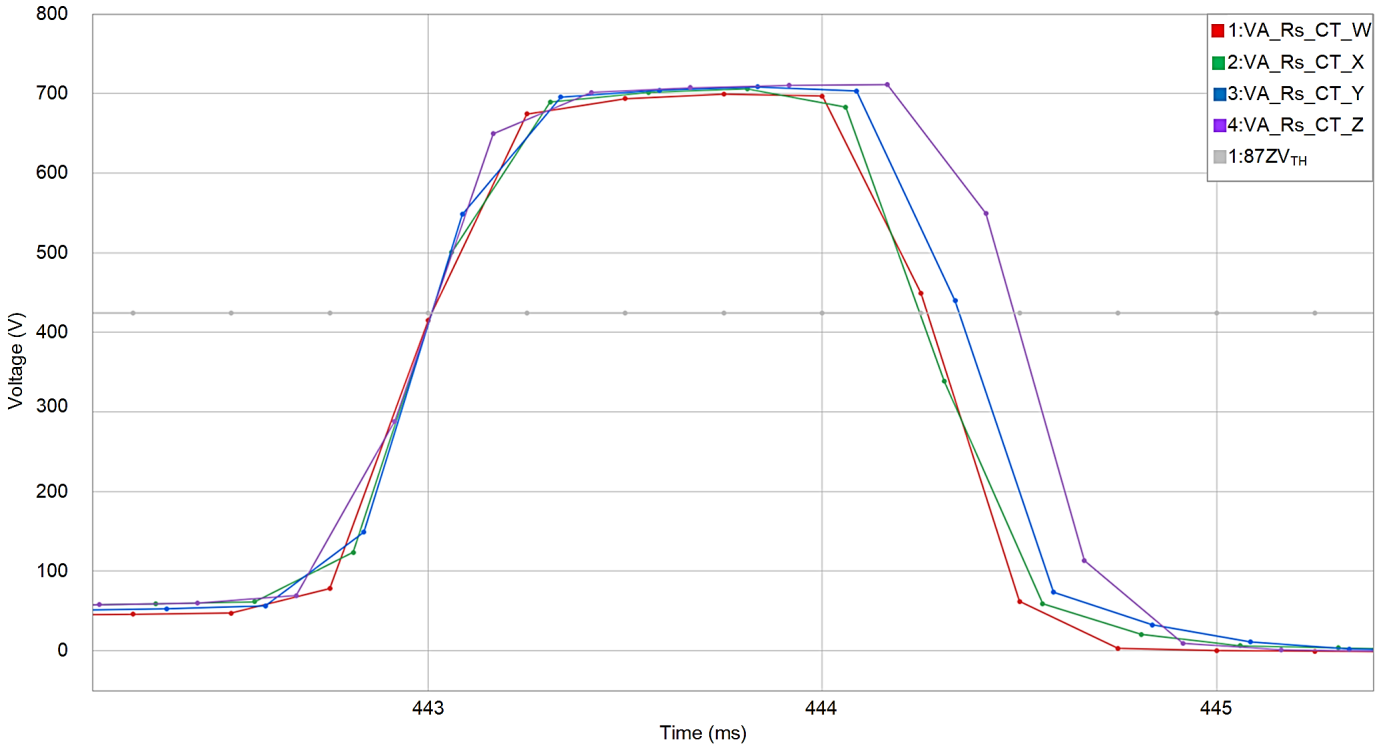

Fig. 14 Comparison of relay-captured voltage for a 65 kA symmetrical fault with different CTs with same CTR (4 kHz sampling)

B. Minimum Fault-Current Estimation

To validate the minimum fault-current estimation method, a test setup similar to that shown in Fig. 7 was used. Current was injected through a single CT while varying the number of CTs connected in parallel to emulate buses with different numbers of feeders. Testing was conducted using two $87ZV_{TH}$ pickup-threshold settings and CTs of different C-classes. The estimated minimum fault current was compared with the measured minimum fault current, the results are summarized in Table II and Table III. Fig. 15 shows the primary current and the voltage across Rs captured during one of the minimum fault-current tests.

As shown in Table II and Table III, the estimated minimum fault current closely matches the actual measured fault current. The results also demonstrate that the 87Z SBWFRE is highly sensitive. Specifically, it can issue an 87Z trip for very low fault currents approximately 150 A of primary fault current or less when three or fewer feeders are connected.

In addition, it was observed that the minimum fault-current estimation method provides the best results when $IE_{V_{rms(min)}}$ is less than 0.1 A. When $IE_{V_{rms(min)}}$ is greater than 0.1 A the estimation becomes less reliable, and an experimental approach should be used to determine the minimum fault current [2].

TABLE II
COMPARISON OF MEASURED AND ESTIMATED MINIMUM FAULT CURRENTS ($87ZV_{TH}$ = 283 V)

CT Information	CTR	$87ZV_{TH}$	$V_{rms(min)}$ (V)	$IE_{V_{rms(min)}}$ (A)	# of CTs	$IF_{rms(min)}$ (A rms – pri)	
						Estimated	Measured
C50 1200:5 (CT-W)	240	283	57	0.028	1	51	40
	240	283	57	0.028	2	61	65
	240	283	57	0.028	3	71	70
C100 1200:5 (CT-X)	240	283	57	0.028	1	51	35
	240	283	57	0.028	2	61	45
	240	283	57	0.028	3	71	60
C100 1200:5 (CY-Y)	240	283	57	0.036	1	54	40
	240	283	57	0.036	2	67	55
	240	283	57	0.036	3	80	75
C100 1200:5 (CT-Z)	240	283	57	0.024	1	49	40
	240	283	57	0.024	2	58	50
	240	283	57	0.024	3	67	80

TABLE III
COMPARISON OF MEASURED AND ESTIMATED MINIMUM FAULT CURRENTS ($87ZV_{TH}$ = 425 V)

CT	CTR	$87ZV_{TH}$	$V_{rms(min)}$ (V)	$IE_{V_{rms(min)}}$ (A)	# of CTs	$IF_{rms(min)}$ (A rms – pri)	
						Estimated	Measured
C50 1200:5 (CT-W)	240	425	85	0.042	1	76	70
	240	425	85	0.042	2	91	115
	240	425	85	0.042	3	106	125
C100 1200:5 (CT-X)	240	425	85	0.042	1	76	65
	240	425	85	0.042	2	91	85
	240	425	85	0.042	3	106	115
C100 1200:5 (CY-Y)	240	425	85	0.05	1	79	65
	240	425	85	0.05	2	97	100
	240	425	85	0.05	3	115	130
C100 1200:5 (CT-Z)	240	425	85	0.033	1	73	65
	240	425	85	0.033	2	85	80
	240	425	85	0.033	3	97	105

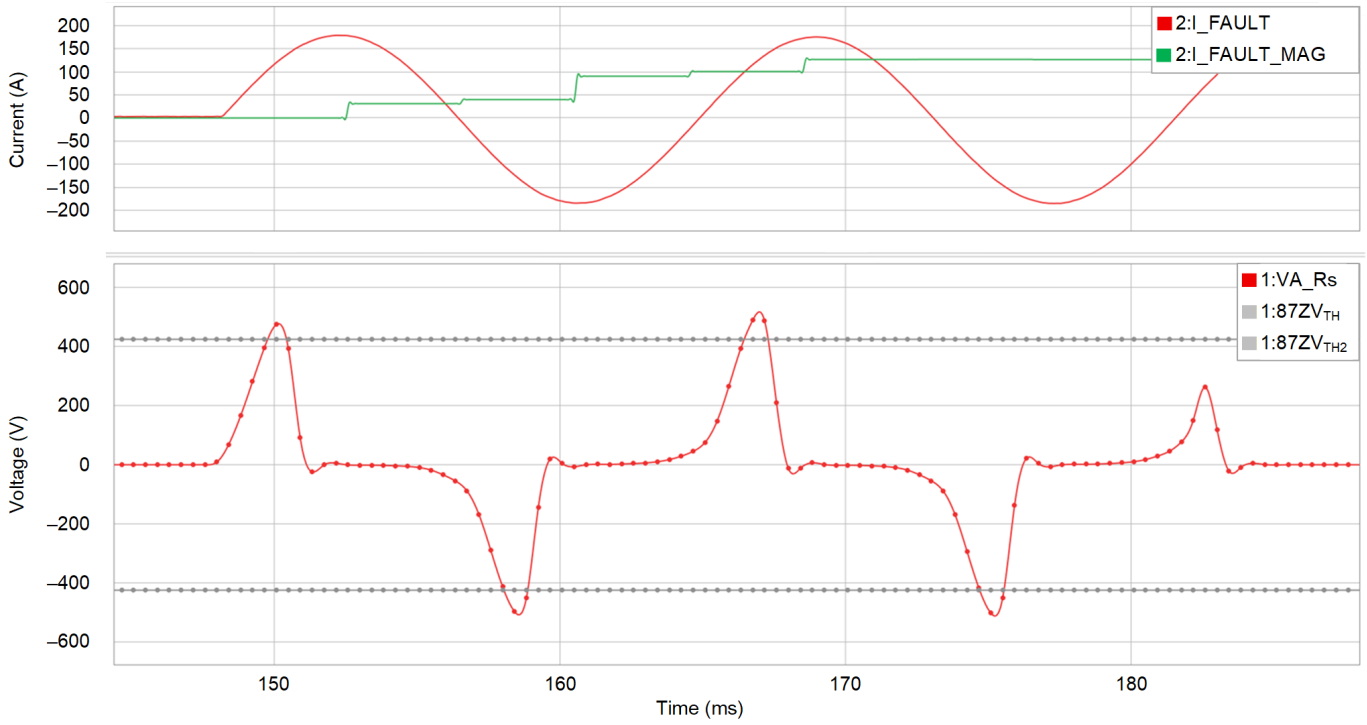

Fig. 15 Primary fault current and voltage across the Rs for 125A primary internal fault with three C50 1200:5 CTs (CT-W, $87ZV_{TH}$ = 425 V)

VI. Conclusion

This paper presents two practical methods for evaluating CT suitability in 87Z applications directly from CT excitation curve data: (1) a high-current internal-fault voltage-pulse-width estimation method and (2) a minimum fault-current sensitivity estimation method. These methods allow protection engineers to accurately evaluate CT performance and assess 87Z dependability and sensitivity during the design phase, well before CTs are procured, while also providing straightforward guidance for CT selection in space-constrained applications.

Extensive laboratory testing, including high-current symmetrical and asymmetrical internal-fault conditions, showed strong agreement between the estimated and measured voltage-pulse widths and minimum fault-current sensitivities. The results demonstrate that the proposed methods provide accurate and practical tools for evaluating 87Z performance and establishing minimum CT requirements.

Whenever possible, C200-class or higher CTs should be used for 87Z protection because they provide the greatest operating margin and dependability. However, lower-class CTs may be used in applications, such as compact-footprint switchgear, where space or cost constraints prevent the use of higher-class CTs. In such cases, careful engineering evaluation is required. Based on the analysis and test results presented in this paper, CTs with 140 V or higher at 10 A excitation current are recommended, and symmetrical fault currents should be limited to less than 50 times the CT nominal current when applying lower-class CTs. These guidelines help ensure dependable operation while maintaining adequate fault sensitivity.

VII. References

[1] K. Behrendt, D. Costello, and S. E. Zocholl, “Considerations for Using High-Impedance or Low-Impedance Relays for Bus Differential Protection,” proceedings of 63rd Annual Conference for Protective Relay Engineers, College Station, TX, 2010, pp. 1–15.

[2] J. Hartshorn, J. LaBlanc, Z. Korkmaz, M. Donolo, M. J. Thompson, H. J. Altuve Ferrer, and D. Costello, “Effect of Stabilizing Resistance, CT Class, and MOV Maximum Clamping Voltage on High-Impedance Differential Scheme Performance,” proceedings of the 50th Annual Western Protective Relay Conference, Spokane, WA, October 2023.

[3] *SEL-587Z High-Impedance Differential Relay Instruction Manual.*

[4] S. E. Zocholl and D. Costello, “Application Guidelines for Microprocessor-Based, High-Impedance Bus Differential Relays,” proceedings of the 62nd Annual Conference for Protective Relay Engineers, College Station, TX, 2009, pp. 451–468.

[5] GE Power Management, “High-Impedance Differential Relaying.”

[6] R. Franklin, H. Nabi-Bidhendi, M. J. Thompson, and H. J. Altuve, “High-Impedance Differential Applications With Mismatched CTs,” proceedings of 71st Annual Conference for Protective Relay Engineers, College Station, TX, 2018, pp. 1–14.

[7] D. Tourn, E. Florena, G. Zamanillo, P. Donolo, A. Dissanayake, and P. Kulkarni, “Signal Processing for High-Impedance Differential Protection Schemes,” IEEE/IAS 59th Industrial and Commercial Power Systems Technical Conference, Las Vegas, NV, 2023, pp. 1–6.

[8] J. LaBlanc and M. J. Thompson, “Redundant Bus Protection Using High-Impedance Differential Relays,” proceedings of the 71st Annual Conference for Protective Relay Engineers, College Station, TX, 2018, pp. 1–13.

[9] *SIEMENS 5kV and 15kV Metal-Clad Switchgear Type GM (SGIM-3258B) Instruction Manual.*

VIII. Biographies

Michael Kozich is a senior staff engineer at Rehlko. Since joining in 2007, he has worked on the paralleling switchgear team, holding various roles, including automation engineering team lead and project engineer. Throughout his career, he has developed expertise in PLC and HMI programming, power system installation, and power system design proficiencies. Michael has a Bachelor of Science in electrical engineering from the University of Wisconsin-Milwaukee. He is passionate about delivering customer solutions.

Anushka M. Dissanayake received the BS degree in electrical and electronic engineering from the University of Peradeniya, Sri Lanka, in 2014, and the PhD degree in electrical engineering from Oklahoma State University, Stillwater, OK, USA, in 2020. Since 2020, he has been with Schweitzer Engineering Laboratories, Inc. (SEL), where he is currently a development lead engineer in the Research and Development division. He holds several patents and has authored multiple technical papers related to power system protection and control. His research interests include power system protection, digital signal processing, and microgrids.

Marcos Donolo received the BSEE degree from Universidad Nacional de Río Cuarto, Argentina, in 2000, the MS degree in electrical engineering, the second MS degree in mathematics, and the PhD degree in electrical engineering from the Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 2002, 2005, and 2006, respectively. Since 2006, he has been with Schweitzer Engineering Laboratories, Inc. (SEL), where he is currently a principal engineer. He holds several patents and has authored numerous papers related to power system protection.

Osama Ansari is a lead power engineer in Research and Development at Schweitzer Engineering Laboratories, Inc. (SEL). He joined SEL in 2021 as an application engineer in the Sales and Customer Service division, focusing on power system protection, and has since transitioned to his current role. Prior to SEL, he worked as a protection engineer at Duke Energy Florida, specializing in distribution protection coordination and settings calculations. He also has experience as a project and commissioning engineer in Mumbai, India, where he commissioned and tested medium-voltage and high-voltage switchgear and transformers. Osama earned his BS in electrical engineering from Sardar Patel College of Engineering, Mumbai, India, in 2014. He holds an MS in electrical engineering from the University of South Florida (2019), an MS in Cybersecurity Operations and Control Management from Harrisburg University of Science and Technology (2024), and an MS in project management from Harrisburg University of Science and Technology (2026). He is an active member of the IEEE.

Vinod Yedidi is a senior engineer in the Research and Development division of Schweitzer Engineering Laboratories, Inc. (SEL). He has been with the company since 2006. Vinod received his MS in electrical engineering from University of Idaho in 2006 and his BS in electrical and electronics engineering from the Jawaharlal Nehru Technological University College of Engineering in Hyderabad, India, in 2002. He has been a member of IEEE for 25 years and is a registered professional engineer in Washington.

Angelo D'Aversa received his BSEE degree from Drexel University in 1990 and an MSEE degree in 1994. After graduation he developed distribution relays for General Electric for nine years. In 1999, he joined Schweitzer Engineering Laboratories Inc. (SEL) as a test engineer and since joining SEL has spent many years developing firmware for a variety of protective relays. Presently, he is a senior engineering director for the Industrial Systems group for SEL.

Jay Hartshorn graduated from University of Idaho in 2013 with a BS in Electrical Engineering. He joined Schweitzer Engineering Laboratories, Inc. (SEL), in 2016 and presently holds the title of development lead engineer in the Industrial and Rotating Machinery group. He holds several patents related to power system protection.

© 2026 by Rehlko and Schweitzer Engineering Laboratories, Inc.
All rights reserved.
20260928 • TP7269-01