Power-Swing Detection Logic for Systems With Low Inertia

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Abstract

Distance protection elements face security problems during power-swing conditions because the swelling power may cause the apparent impedance to encroach on the element operating characteristics. To address this problem, line distance protective relays include a power-swing blocking logic to secure their distance elements during power swings. Avoiding undesired line tripping keeps the transmission network intact and gives the system time to stabilize through inherent transient stability margins and dedicated transient stability schemes, including load and generation shedding, power system stabilizers, and remedial action schemes. From the protection perspective, however, assertion of the power-swing blocking logic hurts protection dependability during power-swing conditions. Symmetrical faults that cannot be detected by using sequence directional elements in a pilot protection scheme are of particular concern. To maintain protection dependability during power swings, it is desirable to remove the power-swing blocking signal for faults that occur during power swings, especially for three-phase symmetrical faults. Characteristics of power swings continue to change as more unconventional low-inertia sources are added to the power system. These sources are modulated by their control algorithms rather than by the inertia of the rotating masses and synchronous machine torques. This paper presents a power-swing blocking and out-of-step tripping logic suitable for systems with low inertia. The presented logic does not require settings and derives its operating parameters from the basic line parameters and distance protection settings. As a result, application of the presented logic does not need transient stability studies. The logic presented in this paper has been implemented and deployed in the field since 2020.

1 Introduction

Large system disturbances, such as loss of generation or load, slowly cleared faults, and relay operations that remove key assets from the system, may result in large power surges. Following the disturbance, the system finds a new equilibrium through oscillations, i.e., power swings. Power swings are therefore natural and unavoidable phenomena that allow the system to find a new power flow pattern and remain stable if conditions allow.

Power swings, however, create problems for distance protection. First, the surge of power may cause the apparent impedance to encroach on the distance element operating characteristic. This encroachment may trigger a misoperation of the underreaching Zone 1 element, time-delayed zones in a step-distance scheme, as well as a pilot scheme that uses the overreaching Zone 2 element as a forward-looking fault detector. This security concern calls for a power-swing blocking (PSB) logic to accompany distance elements in line relays. Second, distance elements may have problems with polarizing signals during power swings, especially during unstable power swings where the equivalent local and remote source voltages can be temporarily out of phase. This situation jeopardizes both security and dependability of distance and phase directional overcurrent elements and calls for a careful design of the distance and directional polarizing logic [1]. Third, protection dependability during power swings remains important. Asymmetrical faults can be detected by using the zero- and negative-sequence directional overcurrent elements in a pilot scheme. Detecting symmetrical line faults, however, as well as providing step-distance protection for the surrounding system, requires distance elements to be operational. This calls for removing the power-swing blocking signal and allowing the distance elements to respond to faults during power swings, even if their performance is not as good during power swings as during routine operation.

Loss of transient stability (a machine or a cluster of machines slips a pole relative to the rest of the system) demonstrates itself as an unstable power swing. When an unstable power swing occurs, a practical remedy to restore transient stability is to separate the system along the boundaries between clusters of machines that are out of synchronism and those that remain in synchronism or have a chance to stabilize given natural stability margins and available system integrity protection schemes. It is often preferrable to separate the system by tripping lines through which the unstable power swing traverses. To perform this function, out-of-step tripping elements are made available in line relays to provide system separation, allowing for an autonomous and distributed out-of-step tripping without a centralized scheme. Using this approach, the power swing, as it traverses though the transmission network, allows selecting lines for separation tripping.

Power-swing blocking elements are based on monitoring either the impedance rate-of-change or the swing center voltage rate-of-change [2]. Historically, the impedance-rate-of-change methods use impedance blinders and apply timers to perform a crude (not continuous) impedance-rate-of-change

measurement. Section 2 provides more information on traditional power-swing blocking elements.

Today, an increasing number of unconventional sources are added to power systems, the majority of which are connected to the system through inverters. Inverter-based sources include photovoltaic, wind, and battery-powered sources, as well as high-voltage direct-current links to systems with conventional or unconventional sources. The new sources change the nature of the grid in many ways. In the context of this paper, the nature of power swings is changing as synchronous generators are replaced with low- or no-inertia sources. These sources use control algorithms to stay synchronized with the rest of the power system instead of relying on mechanical inertia and the push-and-pull of synchronous machine torques, as in traditional power systems. This new behavior calls for revisiting the power-swing element design.

Another motivation for this work is to provide for a setting-less power-swing blocking and out-of-step tripping logic. Performing transient stability studies to set these elements is not easy in traditional systems dominated with synchronous generators. It becomes even more problematic in systems with a large percentage of unconventional sources (transient model availability and accuracy as well as source dependance on internal control parameters).

This paper presents a new design for power-swing blocking and out-of-step tripping logic that is based on continuous measurement of the impedance rate-of-change. Application of the logic does not require transient stability studies, and the logic does not assume that the impedance traverses in a traditional right-to-left or left-to-right path across the apparent impedance plane. The power-swing blocking logic includes a fault-during-a-power-swing module to remove the blocking signal and maintain dependability for faults occurring during power swings. The out-of-step tripping logic follows the trip-on-the-way-out principle. Our design has been implemented in a relay [3] and has been in service since 2020.

2 Traditional Power-Swing Logic

2.1 Blinder-based power-swing blocking logic

Historically, a power-swing blocking logic uses blinders (additional impedance zones) to track the impedance rate-of-change [2]. A two-blinder (one-step) method, as in Fig. 1a, uses an inner blinder and an outer blinder. The inner blinder is set outside of all the distance zones to be blocked, while the outer blinder is set outside of the worst-case load impedance. The method assumes that a power swing enters the outer blinder and only after a time delay (inversely proportional to the swing rate) enters the inner blinder. By comparison, during faults, the apparent impedance jumps inside the inner blinder with no delay. This simple method may fail during resistive faults if the apparent impedance is located between the inner and outer blinders.

A three-blinder (two-step) method attempts to solve this problem by using an additional (middle) blinder placed between the inner and outer blinders, as in Fig. 1b. In this method, a power swing is declared if the impedance stays for some time between the outer and middle blinders and subsequently moves out and stays for some time between the middle and inner blinders.

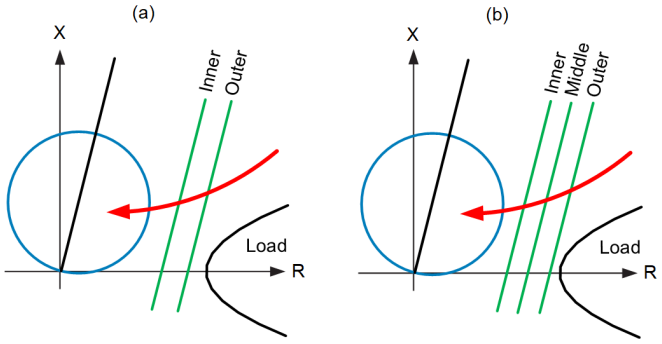

Fig. 1. Blinder-based power-swing blocking logic: two-blinder method (a) and three-blinder method (b).

The blinder-based method is easy to implement in analog relays. It only requires two or three additional impedance zones (blinders) and a simple logic involving a timer(s) and latches.

The blinder-based method is commonly used today because of the industry inertia and familiarity, even though the method is not easy to apply:

1. Blinder coordination is required respective to the distance protection zones and the load impedance. The two or three blinders must be placed between the protection zones and the load impedance and must be spaced apart to allow accurate timing of the traversing impedance (see Fig. 1).
2. Transient stability studies are required to obtain the impedance travel time between the blinders. These studies are time-consuming because they may involve a significant number of system contingencies. The studies also require multiple utility departments to work together and share data and tools. Additionally, the impedance is a nonlinear function of the source angle difference – during a power swing, the impedance rate-of-change depends on where that impedance is located on the apparent impedance plane. Therefore, if the blinders are moved, the timers should be recalculated, at least in theory. Presently, transient stability software packages do not implement protective relay models, which further complicates the task of selecting the blinders and timers.
3. The impedance trajectory during a power swing is not necessarily a horizontal or near-horizontal path (right-to-left or left-to-right). The impedance may traverse along complicated paths, such as approaching vertically and retreating horizontally.
4. The logic can be defeated by faults and switching events. An external fault can move the impedance to an area between the blinders. Fault clearance can move the impedance to a different point. Autoreclosing can change the impedance yet again. Because the logic does not monitor the impedance rate-of-change continuously, it may be defeated by a sequence of events if the impedance jumps from point to point.
5. Some implementations use the positive-sequence impedance in the power-swing blocking logic. This

approach reduces the computational burden in microprocessor-based relays, but it adds another level of application complexity. The distance zones to be blocked work on loop impedances, while the power-swing blocking logic works on the positive-sequence impedance. The two impedances are not the same and can differ considerably during asymmetrical faults and open-pole conditions. This makes the coordination more difficult. Additionally, an evolving fault can move the positive-sequence apparent impedance from one position to another and defeat the blinder-based logic.

2.2 Swing-center voltage-based logic

A swing-center voltage method effectively monitors the slip frequency. The magnitude of the swing-center voltage (a voltage at the point in the power system where the voltage is zero when the equivalent sources are exactly out-of-phase) is proportional to the cosine of the angle between the voltage and current. The derivative of the swing-center voltage magnitude is therefore proportional to the swing rate [4]. The method is relatively easy to implement in microprocessor-based relays [5]. The key advantages of the method are that it does not require using and coordinating blinders and it can operate without a setting defining the expected swing rate.

The method requires solving some implementation challenges, such as accuracy of calculating the rate-of-change especially in the context of noise and off-nominal frequency ripple in the phasors, the issues related to using the positive-sequence quantities, and the impact of switching events on power-swing detection dependability (i.e., avoiding spurious deassertion of the blocking bit during a power swing).

2.3 Out-of-step tripping logic

Historically, the out-of-step tripping logic is based on a single blinder method, preferably supervised with a prior assertion of the power-swing detection logic [2]. Two tripping modes can be used. Tripping when the apparent impedance goes beyond the point of no return (the point after which transient stability cannot be recovered) is referred to as trip-on-the-way-in. Tripping when the apparent impedance has already crossed the line impedance, making it certain that the out-of-step condition has already taken place, is referred to as trip-on-the-way-out. The trip-on-the-way-out application is simple because it does not require complex calculations of the blinder settings required in the trip-on-the-way-in method.

3 Attributes of the New Logic

The new power-swing logic described in this paper has these attributes:

- The logic operates based on the continuous measurement of the impedance rate-of-change (dZ/dt). The continuous measurement removes the need to use blinders and the associated requirement to calculate the blinder settings to coordinate with the distance zones and the load impedance. It also alleviates concerns regarding the impedance trajectory angle as it relates to the position of the blinders (i.e., the method does not assume a right-to-left or left-to-right near-horizonal path).
- The logic operates on a per-loop basis. This allows blocking healthy distance loops and allowing the faulted distance loops to operate (power-swing “unblocking”).
- The logic uses a factory constant for the swing rate threshold and does not require a user setting. There is a considerable difference between the impedance rate-of-change during faults and during power swings. This difference is at least of one order of magnitude, which allows using a factory constant rather than a setting.
- The power-swing blocking logic includes a module to remove the blocking action to maintain dependability of distance protection for faults during power swings.
- The out-of-step tripping logic operates for unstable swings that traversed the line impedance angle through or near the protected line. The logic operates using the trip-on-the-way-out principle and it does not require user settings.

4 Power-Swing Blocking Logic

This section describes the key components of the power-swing blocking logic. Portions of this section and the following sections are taken directly from [3].

4.1 Impedance-rate-of-change measurement

Fig. 2 illustrates a trajectory of an impedance that traverses the impedance plane from right to left during a power swing. The dots represent complex impedance values: *k* is the index of the newest impedance value while *k*–1 is the index of the previous value. The logic processes the input data at a rate of once a millisecond.

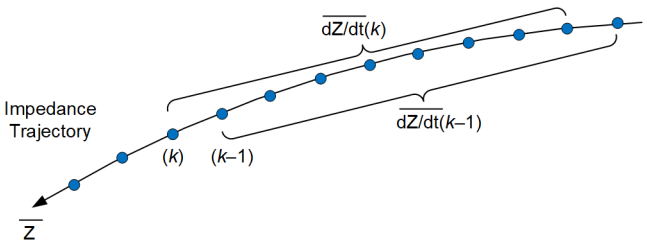

Fig. 2. Impedance-rate-of-change measurement.

The logic calculates the apparent impedance derivative (dZ/dt) as a complex value. This complex value provides information about both the rate and direction of the impedance change. The magnitude of the dZ/dt signal tells the logic how fast the impedance is traversing. The angle of the dZ/dt signal tells the logic the angle (direction on the impedance plane) of the impedance trajectory.

During power swings, the impedance does not change much over a period of just 1 ms. Therefore, calculating the impedance rate-of-change based on just two consecutive samples would yield noisy results. Also, during power swings, the frequency measured by the relay slightly lags the true signal frequency. This lag causes a small ripple in the measured phasors and quantities derived from phasors, such as the apparent impedance. To improve noise rejection when measuring impedance changes during very slow swings and to improve rejection of the off-nominal frequency ripple, the logic calculates the change in impedance by using a data window of two power cycles. The data window of the d/dt

filter is graphically illustrated by parentheses in Fig. 2. We implement the d/dt filter as a first order Walsh filter with a window length of two nominal power cycles (the first order Walsh filter is the best-fit least-square estimator that measures the slope of a signal). Using two cycles of impedance values to measure the impedance rate-of-change provides the logic with well-behaved d/dt values even when the changes in the impedance are very small and the apparent impedance measurement is relatively noisy, such as during off-nominal frequency conditions.

The logic measures the impedance rate-of-change on a per-loop basis (AG through CA).

4.2 Impedance-rate-of-change consistency logic

Power swings exhibit consistent impedance trajectories, while faults and other switching events exhibit sudden jumps preceded and followed by stationary behavior. Our implementation includes the impedance-rate-of-change consistency logic illustrated in Fig. 3. When deciding if the change in impedance at the *k*th processing interval is consistent with a power swing, the logic uses the 5 ms-old change in apparent impedance (*k*–5 ms) as a reference. The new value of the change in impedance (the value at sample *k*) must point in approximately the same direction as the 5 ms-old change (sample *k*–5 ms); the logic allows a trajectory angle difference within ±20 degrees. Also, the new value must not be too different in magnitude from the old value, i.e., the impedance trajectory cannot speed up or slow down too much compared with the 5 ms value in the past. The logic allows a magnitude difference of 1:1.25 (the new value cannot be larger than 1.25 times the old value or smaller than 1/1.25 times the old value).

Fig. 3 depicts the consistent trajectory condition with an enclosed shape. The new impedance-rate-of-change value must be within that shape for the power-swing blocking logic to consider the impedance trajectory consistent. At each processing interval, the 5 ms-old change in impedance creates a small consistency region ahead of the traversing impedance for the new change in impedance. The impedance rate-of-change must be within that small region in the next processing interval for the power-swing blocking logic to consider the impedance trajectory consistent with a power swing.

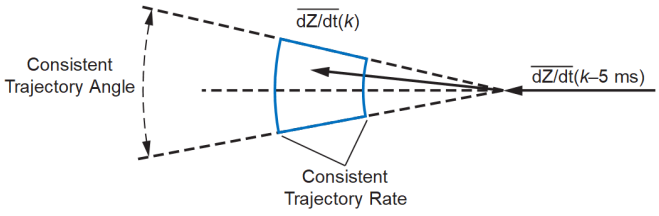

Fig. 3. Illustration of the consistent trajectory principle.

The 5 ms time interval has been selected to further reduce the impact of the off-nominal frequency ripple. The 5 ms interval is close to a quarter of a power cycle (considering both the 60 Hz and 50 Hz systems) and allows for the ripple error to partially cancel.

4.3 Impedance supervisory zones

The power-swing blocking and out-of-step tripping logic use the following three impedance zones:

- *Power-swing impedance supervisory zone* (Z_{PSB}): This zone is used to supervise the power-swing blocking logic. This zone encompasses all distance protection zones that are enabled and configured to be blocked by the power-swing blocking logic. The logic does not declare a power swing until the impedance enters the Z_{PSB} zone. This reduces spurious power-swing blocking assertion during load changes.
- *Power-swing fault-detection zone* (Z_{FLT}): This is a narrow quadrilateral zone placed close to the line impedance and used to reset the power-swing blocking signal when the impedance enters that zone and stays there, i.e., ceases to traverse the impedance plane.
- *Out-of-step tripping zone* (Z_{OOS}): This is a narrow quadrilateral zone used to detect the out-of-step condition when the swing center passes through or near the protected line.

To determine the size of the Z_{PSB} power-swing impedance supervisory zone, the logic inspects the settings of the distance zones that are enabled and configured for power-swing blocking. Fig. 4 shows an impedance contour formed to encompass all the distance zones that are enabled and configured for power-swing blocking. The contour also encompasses the Z_{OOS} out-of-step tripping zone if the out-of-step tripping logic is enabled.

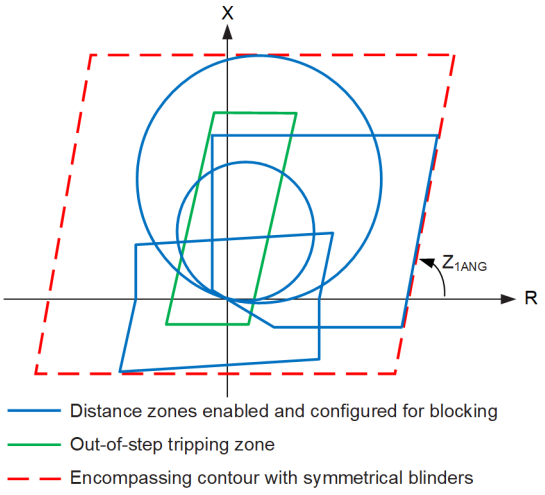

Fig. 4. Contour encompassing all relevant impedance zones.

The encompassing contour has a quadrilateral shape with symmetrical left and right blinders. The logic calculates the size of the contour by using settings of the distance zones, the positive-sequence line impedance magnitude and angle (Z_{1MAG}, Z_{1ANG}), and the basic rules of geometry. The logic establishes the Z_{PSB} power-swing impedance supervisory zone by adding a 15 percent margin around the encompassing contour (see Fig. 5).

The size of the operating characteristics of the distance elements that are enabled and configured for power-swing blocking drives the size of the Z_{PSB} power-swing impedance supervisory zone. Therefore, this zone may encroach on the stable region of power system operation, such as load impedance. This is acceptable because the power-swing

blocking logic declares a power swing based on the continuously measured impedance rate-of-change and not by timing how long the apparent impedance remains in any area of the apparent impedance plane. This is one of the advantages of the presented method. The Z_{PSB} power-swing impedance supervisory zone does not need to be set by the user and it does not need to be coordinated with the load and fault impedance areas (does not need to be located between the load area and the distance zones exposed to power swings, as in Fig. 1).

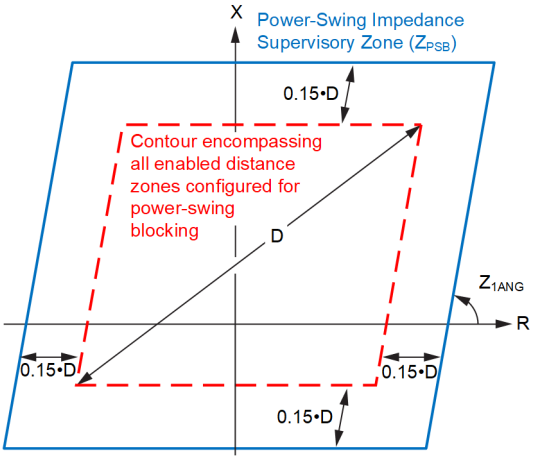

Fig. 5. Power-swing impedance supervisory zone.

The power-swing logic also establishes a fault-detection zone. The Z_{FLT} power-swing fault-detection zone is a narrow quadrilateral shape encompassing the line impedance (see Fig. 6) with the left and right blinders each configured to 15 percent of the line impedance magnitude.

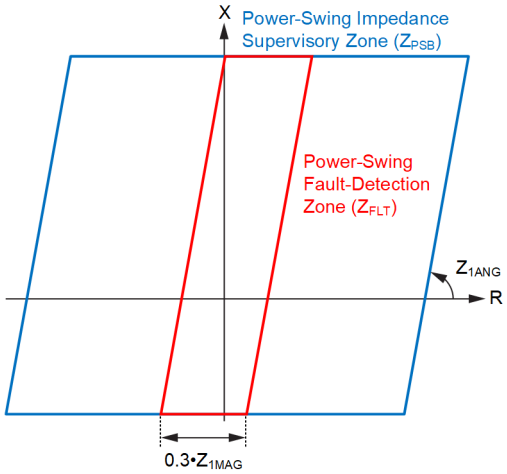

Fig. 6. Power-swing fault-detection zone.

The logic applies the fault-detection zone to detect metallic faults during power swings, as well as to improve security of the power-swing blocking logic and out-of-step tripping logic, as explained later in this section.

The out-of-step tripping logic uses a quadrilateral blinder zone to apply the trip-on-the-way-out operating principle (see Fig. 7). The logic establishes the Z_{OOS} out-of-step tripping zone based on the positive-sequence line impedance settings. The out-of-step tripping logic operates only if the impedance traverses through the line impedance or through less than 50 percent of the line impedance magnitude outside of the protected line. In our design, the out-of-step tripping logic is only concerned with unstable power swings that pass through or near the protected line.

All the impedance zones of the power-swing logic (Z_{PSB}, Z_{FLT}, and Z_{OOS}) are applied on a per-loop basis (AG through CA) and may have different sizes for phase (AB, BC, CA) and ground (AG, BG, CG) loops because of the individual phase and ground distance element settings.

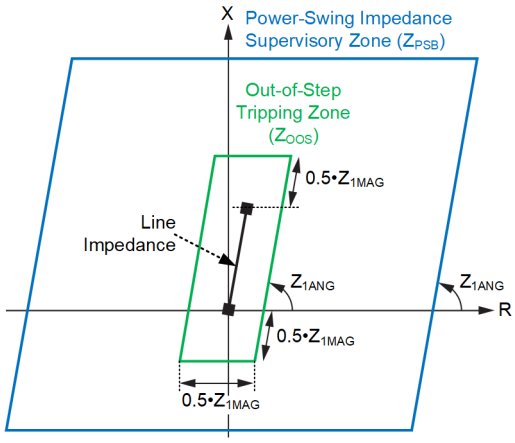

Fig. 7. Out-of-step tripping zone.

4.4 Power-swing blocking logic

Fig. 8 shows a simplified logic diagram of the power-swing blocking logic for the AB loop. The power-swing blocking logic declares a power swing in the AB loop if the following conditions are true:

- The apparent impedance in the AB loop, Z_{AB}, is inside the Z_{PSB} power-swing impedance supervisory zone.
- The apparent impedance in the AB loop, Z_{AB}, is outside the Z_{FLT} power-swing fault-detection zone. This supervision is waived if a power-swing blocking condition is already detected. This supervisory condition increases security of the power-swing blocking logic (prevents spurious power-swing blocking assertion) during faults when the apparent impedance may leap directly into the fault-detection zone.
- The impedance trajectory is consistent with a power swing in terms of the advance angle and rate (see Fig. 3).

The security pickup timer, PU, (e.g., 20 ms) prevents spurious power-swing blocking assertion as a result of transients during faults and switching events. The dependability dropout timer, DO, (e.g., 65 ms) prevents a spurious reset of the power-swing blocking condition in healthy loops because of switching events during power swings, such as inception or clearance of an external fault. The timer in Fig. 8 is an integrating timer: it integrates up when the input is asserted and down when the input is deasserted. This integrating action prevents spurious reset of the power-swing blocking (PSB) bit because of noise and switching events.

If the power-swing blocking logic detects an internal fault (the PSBFLTAB bit asserts), the logic removes the blocking action on a per-loop basis.

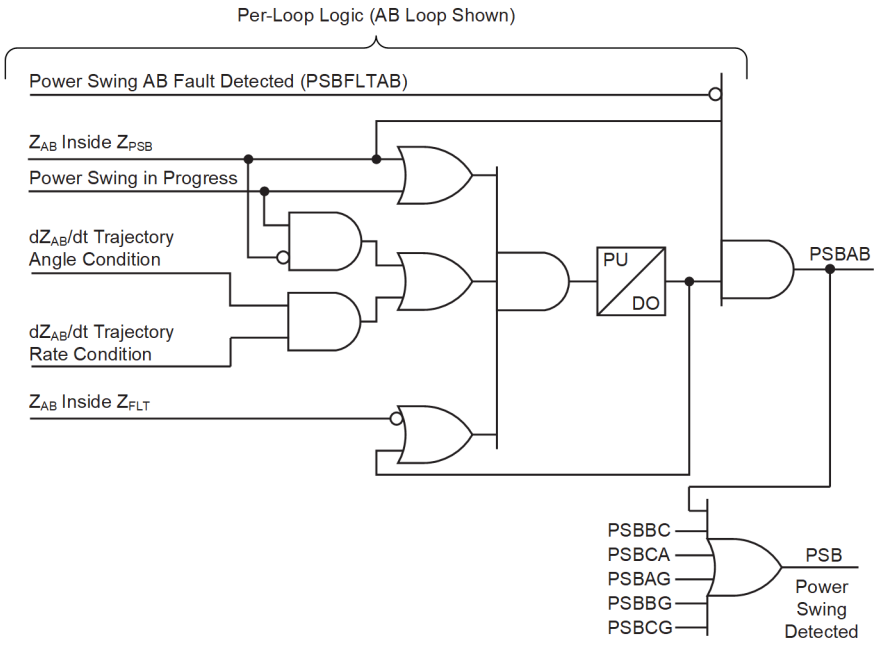

Fig. 8. Simplified power-swing blocking logic.

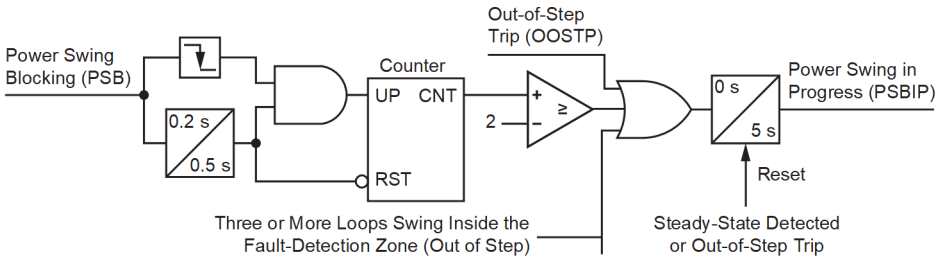

Fig. 9. Power-swing-in-progress logic.

In addition to monitoring the relative impedance rate-of-change (see Fig. 3), the power-swing blocking logic also monitors the absolute impedance rate-of-change and applies minimum and maximum impedance-rate-of-change limits. The minimum limit is a factory constant of 1 Ω secondary per second or 0.25 percent of the measured impedance magnitude per second, whichever is greater. The minimum value of the impedance rate-of-change accounts for the ability of the relay hardware and digital filters to measure small values of the impedance rate-of-change. The maximum limit corresponds to a swing rate of 3 Hz, i.e., the impedance rate-of-change that occurs when traversing across the power-swing impedance supervisory zone in one-third of a second during an unstable power swing. Using a moderate value of 3 Hz to distinguish between power swings and faults improves the power-swing blocking logic security (no undesired power-swing blocking assertions) and therefore the distance protection dependability (no undesired distance element blocking). A power swing may, however, accelerate after some time and reach a swing frequency greater than the 3 Hz design limit. The power-swing blocking logic uses an auxiliary logic (power-swing-in-progress logic), as shown in Fig. 9, to maintain power-swing blocking during such accelerating power-swing conditions.

The logic in Fig. 9 counts how many times the PSB bit (Fig. 8) deasserts in a short time window, and on the second deassertion, the logic declares an ongoing and potentially accelerating power swing. Also, assertion of the out-of-step condition (OOSTP bit) activates the accelerating swing logic. When the accelerating power-swing (power-swing-in-progress, PSBIP) bit asserts, the power-swing blocking logic in Fig. 8 no longer applies the 3 Hz limit and does not require supervision from the impedance zone to engage the timer. Such supervision would not work anyway because the impedance repeatedly enters and leaves the Z_{PSB} power-swing impedance supervisory zone. The logic in Fig. 9 resets the 5 s timer if the power system returns to a steady state (stops swinging) or loses stability (out-of-step trip asserts).

In single-pole tripping and reclosing applications, the open-pole logic inhibits the power-swing blocking logic in the three loops associated with the pole that is open. When the breaker recloses after the single-pole trip, the power-swing blocking logic requires some time to measure the impedance and verify the swing condition. To ensure dependable power-swing blocking, the logic assumes a power swing in the three loops previously blocked by the open-pole condition for 200 ms after the pole has closed if the other three loops declare a power-swing condition (a form of temporary cross-loop blocking).

5 Fault-During-a-Power-Swing Logic

The power-swing blocking logic inherently deasserts when the apparent impedance stops traversing the impedance plane in a manner that is consistent with a power swing.

In addition, the power-swing blocking logic includes a fault-during-a-power-swing detection logic (see Fig. 10). This logic detects metallic faults by verifying that the apparent impedance entered but did not leave the Z_{FLT} power-swing fault-detection zone in Fig. 6. If the apparent impedance does not leave the fault-detection zone within a time interval consistent with the preceding power swing, the PSBFLTAB bit asserts (Fig. 10) and resets the PSBAB bit (Fig. 8). The power-swing blocking logic continuously measures the rate and direction of the traversing apparent impedance. When the impedance enters the fault-detection zone, the logic estimates the time it would take for the traversing impedance to travel across and leave the fault-detection zone, given the impedance trajectory rate and direction at that time. The logic adds a 50 percent margin to the estimate and ensures that the delay (PU) is not shorter than 200 ms.

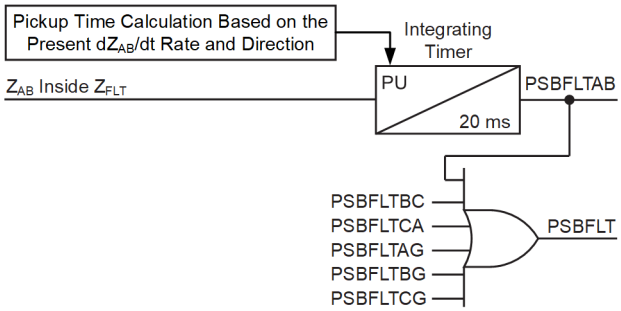

Fig. 10. Simplified fault-during-a-power-swing logic.

6 Out-of-Step Tripping Logic

The out-of-step tripping logic uses the trip-on-the-way-out operating principle and asserts for unstable power swings that have already traversed through the line impedance. The logic uses impedance supervision for the trip signal, and it actuates the circuit breaker when the voltages at both sides of the circuit breaker are not out of phase once the breaker has opened. The out-of-step tripping logic works by continuously measuring the impedance rate-of-change on a per-loop basis (see Section 4). The logic uses this measurement to detect that the apparent impedance has traversed through the impedance plane in a manner consistent with a power swing.

Fig. 11 shows a simplified diagram of the out-of-step tripping logic. The figure emphasizes the AB measurement loop. The logic works by detecting if the apparent impedance traverses through the Z_{OOS} out-of-step tripping zone. While the power-swing blocking bit is asserted, the logic detects if the impedance traverses right-to-left or left-to-right. The logic verifies this condition on a per-loop basis and applies a 100 ms extension timer to compare all six measurement loops.

The out-of-step tripping logic is heavily biased in favor of security. The logic declares an out-of-step condition if 1) at least two of the six measurement loops detect the right-to-left unstable swing and none of the loops detect the left-to-right swing or 2) at least two of the six measurement loops detect the left-to-right unstable swing and none of the loops detect the right-to-left swing.

During single-pole tripping and reclosing intervals, the open-pole logic blocks three of the six measurement loops, and therefore, during single-pole open conditions, the voting logic becomes effectively a two-out-of-three logic.

The out-of-step tripping logic uses a latch to keep the out-of-step trip pending (OOSTP) bit asserted. By design, the out-of-step tripping logic follows the trip-on-the-way-out philosophy and executes the trip command based on the power-swing impedance supervisory zone and based on time. The logic resets the latch, deasserts the OOSTP bit, and asserts the OOST bit for 200 ms either when the apparent impedance in all six loops leaves the Z_{PSB} power-swing impedance supervisory zone or 2 s after the OOSTP bit asserts, whichever comes first.

The out-of-step tripping logic does not have any settings related to impedance, time, or swing rate.

7 Examples of Operation

This section presents several examples of operation by using complex cases obtained from an analog made-to-scale multi-machine power system model. For simplicity, the relay [3] was not connected to trip the breakers; faults were cleared by opening a fault switch rather than tripping breakers.

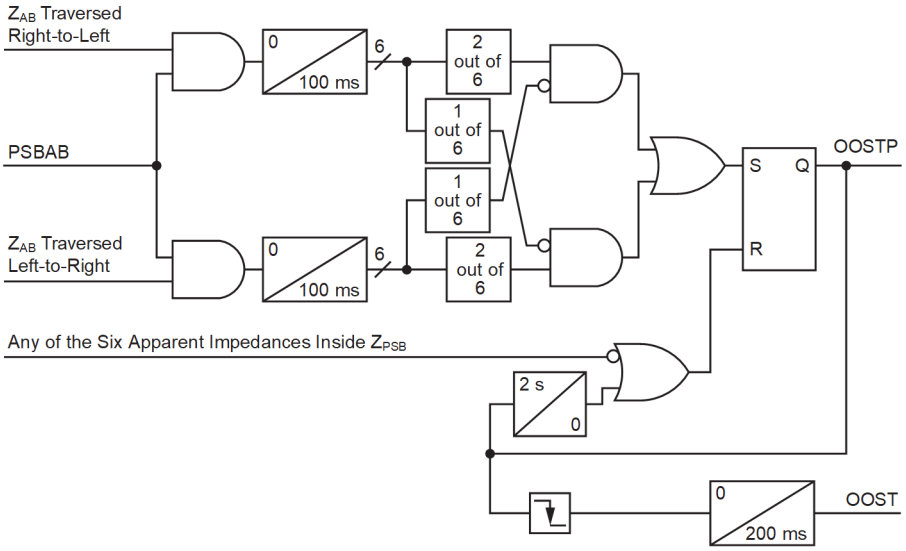

Fig. 11. Out-of-step tripping logic.

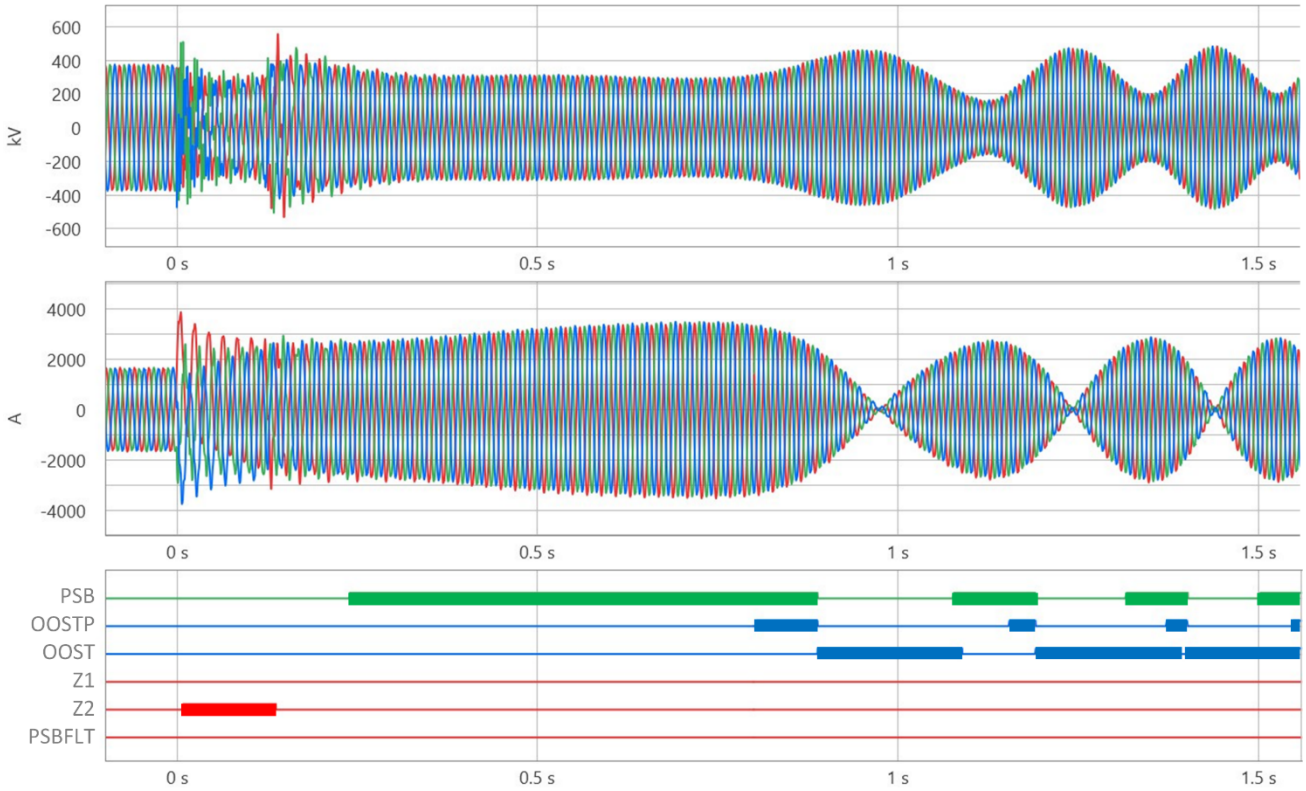

Fig. 12. Unstable power swing following a slowly cleared external fault.

7.1 Unstable power swing following a fault

Fig. 12 shows the voltages, currents, and selected relay bits during an unstable power swing. A bolted three-phase fault occurred at the remote busbar (see Z2 assertion). The system was heavily loaded, and the fault was cleared slowly, in 120 ms (a breaker failure scenario). As a result, this event resulted in a loss of transient stability. The system lost synchronism after about 0.7 s. The unstable power swing has a slip frequency of about 5 Hz (slipping a pole every 0.2 s). The apparent impedance traverses through the protected line impedance. The PSB bit asserts correctly and secures distance protection from a misoperation (the Z1 and Z2 bits do not assert despite the impedance entering their operating characteristics). The PSB bit asserts and deasserts as the impedance swings in and out of the Z_{PSB} power-swing impedance supervisory zone. The OOSTP (out-of-step trip pending) bit asserts each time the system slips a pole (the OOSTP bit can be used to count the pole slips to coordinate individual out-of-step tripping schemes). The OOST (out-of-step trip) bit follows as soon as the apparent impedance exits the Z_{PSB} power-swing impedance supervisory zone after the system slips a pole. The PSBFLT (fault detected during a power swing) bit does not assert because there is no fault during the swing.

7.2 Ground fault during a power swing

Fig. 13 shows the voltages, currents, and selected relay bits during a close-in internal ground fault that occurs during an unstable power swing similar to that in Fig. 12. The fault occurred when the swing current envelope was approaching its maximum.

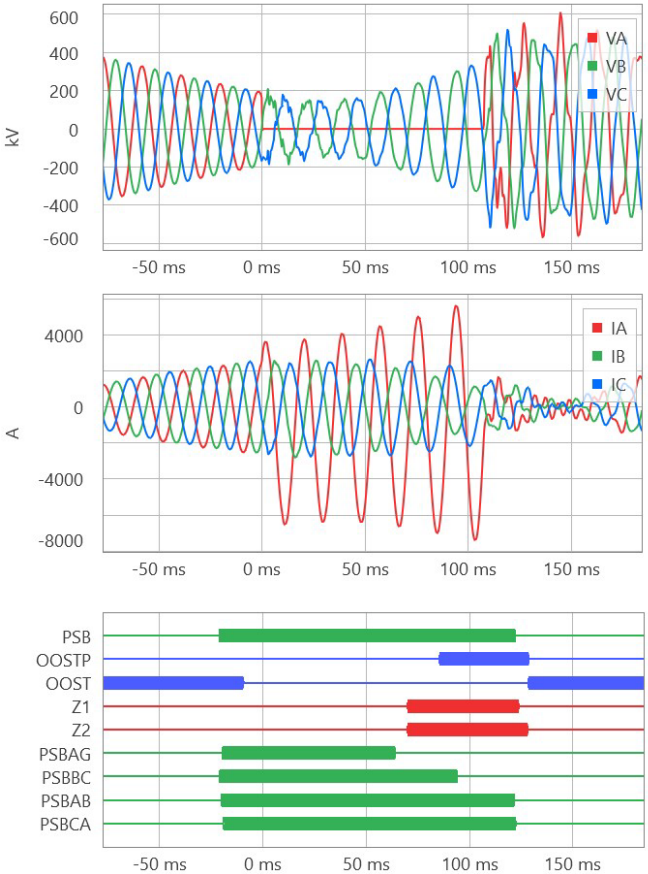

Fig. 13. Internal ground fault during a power swing.

The system slipped a pole before the fault, and therefore, the OOST bit was asserted when the fault occurred. The power-swing blocking logic stays asserted in the healthy loops (see

the PSB bit and the PSBBC, PSBAB, and PSBCA phase loop bits), but it deasserts in the faulted loop (see the PSBAG bit). The PSBBC bit deasserted before the other bits because the Z_{BC} apparent impedance exited the Z_{PSB} power-swing impedance supervisory zone when the system swung away from the out-of-step condition. The PSBAG bit deasserts in about 65 ms because the AG apparent impedance stopped moving. The PSBAG deassertion unblocks the AG distance loops, allowing the distance elements to respond to this close-in forward fault (see the Z1 and Z2 bits). The out-of-step tripping logic detects the pole slip that occurred during the fault (see the OOSTP bit). Detecting the out-of-step condition despite the presence of the fault, blocking healthy distance loops for security, and unblocking faulted distance loops for dependability are advantages of our per-loop implementation.

7.3 Double-line-to-ground fault during a power swing

Fig. 14 shows the voltages, currents, and selected relay bits during a close-in reverse double-line-to-ground fault that occurs during an unstable power swing similar to that in Fig. 12. The fault occurred when the power swing current envelope was approaching its maximum. As a result, there is very little difference in the current magnitudes between the faulted phases, B and C, and the healthy phase, A.

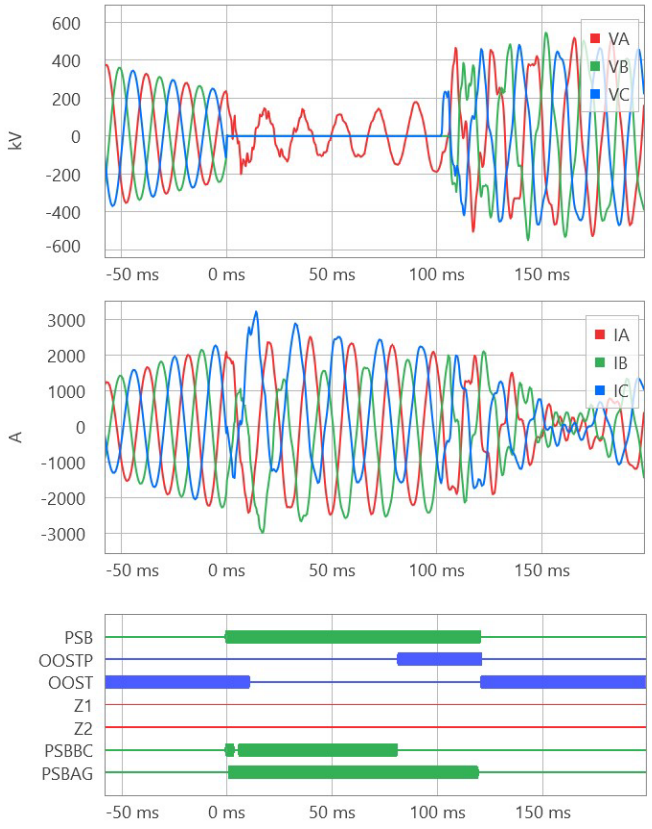

Fig. 14. Reverse double-line-to-ground fault during an unstable power swing.

Note that the power-swing blocking logic deasserts in the BC loop (see the PSBBC bit). This unblocks the distance elements in the BC loop. The distance elements are self-polarized during a power swing and therefore restrain for this reverse fault (see the Z1 and Z2 bits) even though the equivalent sources were almost out-of-phase when the fault occurred. The healthy loops continue to be blocked (see the PSBAG bit).

7.4 Three-phase fault during a power swing

Fig. 15 shows the voltages, currents, and selected relay bits during a forward three-phase symmetrical fault at the remote bus that occurs during an unstable power swing similar to that in Fig. 12. The fault occurred when the swing current envelope was approaching its maximum. As a result, the fault currents are smaller than the pre-fault power-swing currents.

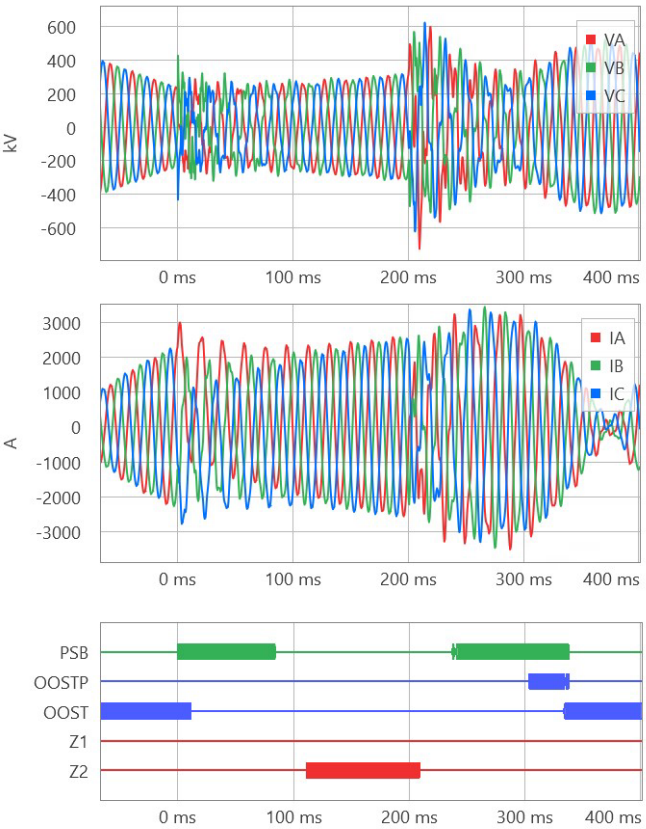

Fig. 15. Forward three-phase fault during an unstable power swing.

Note that the power-swing blocking logic deasserts in all six loops (see the PSB bit). This unblocks the distance elements in all loops. The distance elements are self-polarized during a power swing and avoid issues with memory polarizing and frequency deviations. The distance elements respond correctly – Zone 2 asserts for this fault and Zone 1 restrains (see the Z1 and Z2 bits) – even though the equivalent sources were almost out-of-phase when the fault occurred. The out-of-step tripping logic detects a pole slip that occurs in less than 100 ms after the fault was cleared.

8 Conclusions

This paper presents a power-swing blocking and out-of-step tripping logic that is based on a continuous measurement of the impedance rate-of-change. The continuous measurement allows the logic to track the impedance trajectory irrespective of its location and path on the impedance plane with respect to the distance protection zones and the load. The logic does not require user settings and associated transient stability studies and, instead, derives its internal parameters from the distance element and line impedance settings. The impedance rate-of-change, even in systems with low inertia, is lower by at least an order of magnitude compared with the impedance rate-of-

change during faults. This allows the logic to avoid any settings related to the expected impedance-rate-of-change value during power swings.

The power-swing blocking logic is implemented on a per-loop basis, allowing an inherent unblocking for metallic faults that occur during power swings (the faulted-loop apparent impedance stops moving). The power-swing logic also includes a dedicated fault-during-a-power-swing logic to further enhance distance protection dependability for metallic faults during power swings.

The out-of-step tripping logic is heavily biased for security by monitoring the impedance rate-of-change in all six loops and verifying several conditions before asserting the trip-on-the-way-out bit.

The presented power-swing blocking and out-of-step tripping logic accounts for low-inertia unconventional sources in the system by recognizing that the impedance trajectories during power-swing conditions may exhibit a higher rate of change because of low inertia and may not follow traditional paths on the impedance plane because of the control algorithms modulating the source currents.

The presented logic has been implemented in a relay [3] and has been in service since 2020 with a good track record in the field.

References

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