Distance Element Polarizing Logic for Systems With Low Inertia

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Abstract

Mho distance protection elements operate by comparing the IZ – V operating signal with a polarizing voltage. Ideally, the polarizing voltage should have a non-zero value for all types of faults, including bolted faults close to the relay location. Therefore, preferred polarizing voltage choices include healthy phase voltages (cross-phase polarization), positive-sequence voltage (a form of cross-phase polarization), pre-fault voltage (memory polarization), or a combination thereof. Memory polarization became the prevailing form of polarizing in modern distance relays. However, memory polarization is predicated on sufficient system inertia. In systems with low-inertia generation, such as wind-powered machines and inverter-based sources, memory polarization is known to cause both security and dependability problems for distance protection. Also, memory polarization may be suboptimal in traditional power systems during power swings and in applications to series-compensated lines. This paper presents an advanced distance element polarizing logic for both low-inertia and traditional systems.

1 Introduction

During bolted faults close to a line terminal, the relay faulted phase voltage is very small and therefore is not a reliable reference signal for directional mho distance and directional phase overcurrent protection elements. For unbalanced faults, relay designers have several options for addressing this problem, including negative-sequence polarization for directional overcurrent elements and healthy-phase polarization for mho distance elements. During close-in bolted three-phase faults, however, all three phase voltages are small and unreliable and there is no negative-sequence voltage and current to help determine the fault direction. Analog relays often implement offset distance characteristics to address this problem [1]. Today, most microprocessor-based distance relays use memorized pre-fault voltage as a polarizing signal (memory polarization).

Memory polarization works well if the sources in the system have sufficient mechanical inertia. Because of high inertia, the pre-fault source voltage angle is a reliable proxy for the source voltage angle during the fault. If, however, the source inertia is low, the source voltage angle during the fault may quickly drift away from the source voltage pre-fault angle. This leads to both protection security and dependability problems when using memory polarization. With an increasing penetration of low-inertia wind-powered machines and no-inertia inverter-based sources, cases of distance relay misoperation because of incorrect memory polarization are on the rise [2].

One reason for the increasing rate of misoperations is that most distance relays that are in service today use a relatively simple memory polarizing logic. These simple designs work well in high-inertia power systems powered by large synchronous generators. Modern power systems, however, call for a more robust polarizing logic that is explicitly designed to account for the nature and time constants of today's sources.

This paper presents a new design of a distance polarizing logic suitable for applications in both traditional high-inertia and emerging low-inertia power systems. The design was implemented in 2020 [3] and has been in service since. The paper uses field cases to illustrate the operation of the presented logic.

2 Mho Distance Element Polarizing Basics

A mho distance element compares an operating signal with a polarizing signal by using a 90-degree comparator limit angle [1]. The operating signal, often referred to as IZ – V, comprises the distance element loop voltage (V), loop current (I), and reach impedance (Z_R), as follows:

$$S_{OP} = I \cdot Z_R - V \quad (1)$$

All distance elements, both mho and quadrilateral, use the operating signal (1), even if they do so indirectly. The polarizing signal, in turn, is a design choice. Quadrilateral distance elements are polarized with current. Mho distance elements are polarized with voltage. Directional mho distance elements use one of the following polarizing signals:

- *Self-polarized* elements use the loop voltage as the polarizing signal. During close-in bolted faults, however, the loop voltage is very small and therefore cannot provide reliable polarization. This may result in a loss of security or dependability.
- *Cross-phase-polarized* elements use the healthy phase or phases voltage or the positive-sequence voltage as the polarizing signal. Cross-phase polarization works for close-in bolted faults, except for three-phase faults.

- *Memory-polarized* elements use the pre-fault voltage as the polarizing signal (the polarizing logic extrapolates the pre-fault voltage angle into the fault). This choice provides a non-zero polarizing signal for all fault types, including close-in bolted three-phase faults.

2.1 Positive-sequence voltage polarizing

Most distance elements today use memory polarization: mho distance elements use it for distance comparator polarization, and quadrilateral distance elements may use it to polarize their phase directional comparators. Often, the positive-sequence voltage (V_1) is memorized and used as a polarizing signal, as follows:

$$S_{POL} = V_{1MEM} \quad (2)$$

The signal (2) applies to the AG distance loop because the positive-sequence voltage is calculated by using Phase A as a reference. The signal (2) is phase-shifted by multiples of 30 degrees before it is used to polarize the other five distance loops (BG through CA).

It is inconsequential if the memorized voltage is a positive-sequence voltage or any of the phase-to-ground or phase-to-phase voltages because the pre-fault voltages are symmetrical. However, when a mix of the memorized voltage and the live voltage is used for polarizing [4], i.e., when the memory is allowed to decay with time, then the use of positive-sequence voltage is beneficial because the positive-sequence voltage is non-zero for any bolted fault except the three-phase fault.

2.2 Offset loop voltage polarizing

A mho distance element may also use an offset characteristic to avoid issues with close-in bolted faults. A forward-looking distance element may have its operating characteristic extended in the reverse direction to provide dependability during forward close-in bolted faults or in the forward direction to provide security during reverse close-in bolted faults [1]. By extending (offsetting) the characteristic in the forward or reverse direction, the user predetermines the element response to close-in bolted faults. Offset mho elements were often used in the era of electromechanical and static relays because developing a memory signal when using analog relays was relatively difficult.

An offset polarizing signal is defined by (3) where the loop voltage (V) is offset (augmented) by adding or subtracting the $I \cdot Z_{OFF}$ term as shown in (3a) and (3b).

Offset polarizing signal:

$$S_{POL} = V \pm I \cdot Z_{OFF} \quad (3)$$

Reverse-offset mho element:

$$S_{POL} = V + I \cdot Z_{OFF} \quad (3a)$$

Forward-offset mho element:

$$S_{POL} = V - I \cdot Z_{OFF} \quad (3b)$$

where Z_{OFF} is a small offset impedance with the angle typically equal to the line positive-sequence impedance angle ($\angle Z_{OFF} = \angle Z_R = \angle Z_{1LINE}$).

During close-in bolted faults, the loop voltage is zero (V = 0). The polarizing signal (3) is in phase with the operating signal (1) if using reverse offset (3a) and out of phase with the operating signal if using the forward offset (3b). The former ensures dependability for forward close-in bolted faults, the latter ensures security for reverse close-in bolted faults.

3 Memory Polarization Concerns

Unlike analog relays, microprocessor-based relays can "memorize" pre-fault signals and apply them during fault conditions without adding complexity or reducing reliability. As a result of this convenience, memory polarization became a prevailing way of polarizing directional mho distance elements.

Memory polarization is not free from concerns, however, as summarized in this section.

3.1 Source inertia

The key underlying assumption for memory polarization is that the source voltage angle does not change because of the fault, at least for the initial few hundreds of milliseconds of the fault. As a result, the pre-fault source voltage angle can be used to represent the source angle during the fault. This assumption holds true when the sources have high inertia. Low-inertia sources swing during fault conditions and the pre-fault source angle will not continue to represent the fault angle. When the error between the true source voltage angle and the polarizing voltage angle is greater than the distance comparator limit angle (typically 90 degrees), a distance element is likely to misoperate (a forward fault appears to the distance element as a reverse fault, and vice versa).

Even in systems with high-inertia sources, memory polarization cannot be applied for a long time. Some relays apply memory polarization for a fixed time and switch to cross-phase polarization after the memory timer expires [5]. In this implementation, the memory polarization time needs to be longer than the breaker failure tripping time. Other relays use logic that allows the memory portion of the polarizing signal to decay with time so that eventually the polarizing signal becomes a cross-polarized signal [4].

3.2 Power swings

When the power system swings, the voltage angle changes with time. As a result, the memorized (past) voltage angle is different than the present voltage angle. The faster the swing, the greater the difference between the memorized voltage angle and the present source voltage angle. If a fault occurs during a power swing, the past source angle does not accurately represent the fault current direction because the latter is driven by the present source angle. Memory polarization does not work well if the source angles change considerably during stable power swings. It is not applicable at all during unstable power swings. This problem is solved by either applying memory polarization for a short time following the fault or forcing a switchover from memory polarization to self polarization or cross-phase polarization when the relay detects a power swing.

3.3 Series-compensated line applications

During faults on or near series-compensated lines, the relay voltage and current angles may shift significantly compared with their expected values for a fault in an inductive-resistive network. Series capacitors create a substantial network nonhomogeneity. Unequal bypassing of series capacitors (the response of metal-oxide varistors and triggered air gaps to fault currents) introduces significant series unbalance in the network. As a result, in some cases, using self polarization during faults on or near a series-compensated line may be detrimental and applying memory polarization for a longer time may be necessary. This problem can be solved by monitoring the angle difference between the live and memorized voltages. If the difference is large and series capacitors are located on or in the vicinity of the protected line, the relay may force memory polarization and not allow self-polarization.

3.4 Frequency measurement errors and frequency deviation

Proper memory polarization requires that the polarizing logic has not only locked to the pre-fault source voltage angle but has also applied that angle while using the present (fault) value of the frequency. In other words, memory polarization requires that the frequency during the fault and the frequency assumed or applied by the memory polarization logic match. If there is a frequency deviation, the polarization is not accurate and may result in a misoperation. For example, if the frequency difference is 2 Hz, the memory polarizing signal (2) and the operating signal (1) slip at 2 revolutions per second times 360 degrees per revolution = 720 degrees per second, or 90 degrees every 125 ms. After 125 ms of a standing 2 Hz frequency deviation, the polarizing error is 90 degrees, which may result in a misoperation. The greater the frequency difference, the shorter the safe application of memory polarization.

The following phenomena and their combination can lead to frequency errors:

- The system frequency changes, such as during a disturbance in systems with low-inertia sources, but the relay-measured frequency lags because of inherent and intentional delays in the frequency measurement logic.
- The system frequency is unchanged, but the relay measures the frequency with a significant error because of transients and limitations in its frequency measurement logic.

When the relay applies a frozen pre-fault phase angle while using the pre-fault frequency, but the frequency changes during the fault, a polarizing error occurs. This problem has two solutions: 1) the memory duration is limited to a duration that guarantees the angle error is safely below 90 degrees, considering the greatest possible frequency deviation, and 2) the relay measures frequency during the fault and uses it to adjust the pre-fault angle to represent the changing angular position of the source. The latter approach has a limit – frequency cannot be measured by using voltage signals during close-in bolted three-phase faults. If one assumes the worst-case of unavoidable frequency measurement errors, then limiting the duration of the memory polarization is the only method to guarantee the security of memory-polarized distance elements.

We can estimate the longest safe usage of memory for polarization as follows. We assume that the relay cannot measure frequency and therefore uses the pre-fault frequency when applying memory polarization. At the same time, as the worst-case assumption, the system experiences a rapid change in frequency defined by the maximum rate-of-change-of-frequency (ROCOF). We assume that the frequency starts changing immediately after the fault inception. If so, the polarizing angle error after time (t) is:

$$\Theta_{\mathrm{ERROR}} = \frac{1}{2}(360^{\mathrm{o}} \cdot \mathrm{ROCOF}) \cdot \mathrm{t}^2 \qquad (4)$$

We assume the highest acceptable angle error is 90 degrees, and we solve (4) for time:

$$\mathrm{t_{MAX}} = \sqrt{\frac{2 \cdot 90^{\mathrm{o}}}{360^{\mathrm{o}} \cdot \mathrm{ROCOF}}} = \frac{1}{\sqrt{2 \cdot \mathrm{ROCOF}}} \qquad (5)$$

For example, for the frequency rate of change of 5 Hz/s, we obtain the maximum memory polarization duration of 316 ms. If memory is applied for longer than 316 ms and the system frequency drifts at 5 Hz/s or faster, a distance element may face security issues. Our design limits the memory duration to 0.3 s. This duration is long enough to maintain directional integrity of protection during breaker failure conditions yet short enough to avoid security issues because of frequency excursions, even if the relay cannot measure frequency and use it in the polarizing logic.

3.5 Ring-down voltages

Transmission line distance relays typically use line-side voltage transformers (VTs). When a transmission line that includes line-side reactors is tripped, the relay voltages in the disconnected phases are subject to a ring-down effect. The voltages decay relatively slowly and exhibit frequency that is several hertz below the nominal system frequency. If the relay uses these voltages for frequency measurement and for memory polarization, then the relay may have issues after the line is reclosed. After reclosing, the relay voltages and currents are at the system frequency, while the relay frequency and memory are locked to the ring-down frequency that is considerably different than the system frequency. This difference may lead to security problems, as explained in Subsection 3.4. Modern relays refrain from using ring-down voltages for frequency measurement based on either explicit ring-down detection logic [6] or the breaker status signals (open-pole detection logic).

3.6 Polarizing signal validation and usage

Today's low-inertia power systems demand a more intentional application of polarization in distance protection elements. Specifically, the following aspects must be considered:

- The polarizing signal validation requires the relay to establish that it has locked to the pre-fault voltage angle and frequency. Only after the relay confirms that it is locked to the pre-fault voltage can it use the memory to polarize the distance elements. Use cases for polarizing signal validation include line energization, reclosing after a fault, off-nominal frequency conditions, and power swings. These conditions can occur in

combination; for example, a line may be energized when the system is at off-nominal frequency while the relay is connected to line-side VTs.

- The duration of the memory polarization must be limited to avoid issues with frequency. In this context, one must assume that the relay will not be able to measure frequency, at least during some fault conditions (a close-in bolted three-phase fault, for example). If so, correction for frequency excursion may be impossible, and limiting the duration of the memory polarization will be the only practical way to avoid protection security issues.
- When the relay polarizing logic decides not to use memory for any reason, it needs to decide how to polarize the distance elements and if it needs to allow the distance elements to remain functional if a suitable polarizing signal is not available.

The rest of this paper presents a new polarizing logic that is designed to address the requirements and concerns outlined in this section.

4 New Polarizing Logic Design

The polarizing logic comprises the following main modules:

1. *Frequency measurement*. Several functions of a typical distance relay require frequency measurement, including frequency compensation (or tracking) in the phasor measurement subsystem and frequency protection elements. We use frequency to improve the operation of the phase-lock loop used in the polarizing logic.
2. *Positive-sequence voltage measurement*. This module addresses the problem of ring-down voltages and accounts for a single-pole open condition during the single-pole tripping and reclosing interval.
3. *Phase-lock loop*. This module tracks (follows and locks to) the live positive-sequence voltage.
4. *Supervision*. This module comprises a state machine that controls how the polarizing signal is selected, validated, and used depending on the application and system conditions.

The following subsections provide more information on each of these modules.

4.1 Frequency measurement

The polarizing logic uses a phase-lock loop (PLL) to track and lock to the live voltage. In general, a PLL has the ability to track frequency. In our design, however, the supervisory logic temporarily opens the PLL feedback loop to prevent the PLL from following the voltage angle during the fault, and by doing so, the logic applies the concept of memory polarization. When the PLL is freewheeling with the feedback loop open, the PLL cannot track frequency. Therefore, our design provides the PLL with the measured frequency. By feeding the PLL with the frequency signal, we allow the PLL to lock to the pre-fault angle, use it as a polarizing reference, and yet simultaneously follow the frequency if the voltage is large enough to permit frequency measurement during the fault. This decoupling of the angle and frequency measurements is essential for the polarizing logic as per the fundamental equation (6) in the rotating angle reference in radians:

$$\Theta_{(t)} = \Theta_{(MEM)} + 2 \cdot \pi \cdot \int_{0}^{t} f_{(t)} dt \qquad (6)$$

where $t = 0$ is the fault inception time, $\Theta_{(t)}$ is the present polarizing angle, $\Theta_{(MEM)}$ is the memorized pre-fault angle, and $f_{(t)}$ is the present frequency.

Our design uses the frequency measurement method [7] implemented in device [3].

4.2 Positive-sequence voltage measurement

Fig. 1 shows the positive-sequence voltage phasor (V_{1P}) derivation for use in the polarizing logic. V_{1P} excludes voltages from open phases and is separate from the general-purpose positive-sequence voltage (V_1).

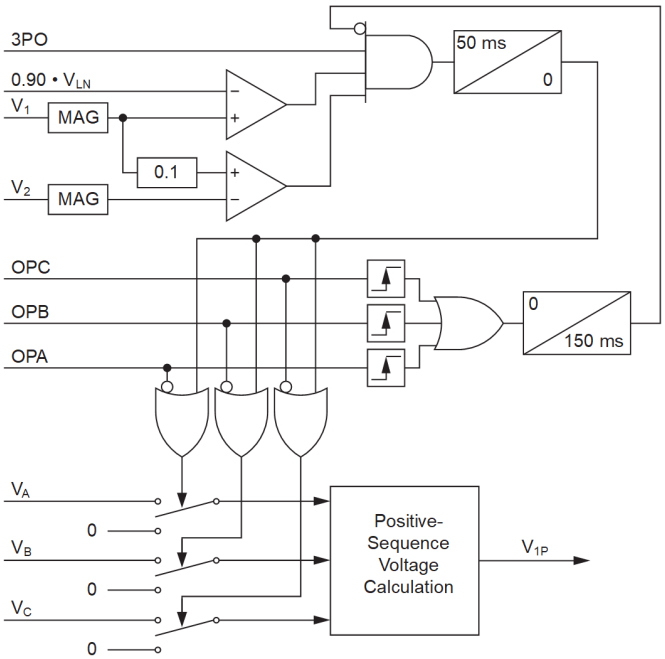

Fig. 1. Positive-sequence voltage logic.

The logic uses the open-pole bits (OPA, OPB, and OPC) to remove voltages in open phases to avoid corrupting the V_{1P} voltage with ring-down voltages after tripping one or all breaker poles. The open-pole bits may lag the primary contacts of the breaker but only by a brief period (milliseconds). Such a short time exposure to the ring-down voltages is acceptable given the intentional inertia built into the PLL. Therefore, the logic in Fig. 1 does not require a dedicated ring-down detection algorithm. The V_{1P} calculation takes into consideration how many voltages are effectively used to derive the positive-sequence voltage, and it applies scaling that ensures the V_{1P} voltage magnitude does not change with the number of open poles.

If all three phase voltages (V_A, V_B, and V_C) are present, the logic uses them even if the breaker is open. This situation occurs if the line is energized by the remote terminal or if the relay is connected to the bus-side VTs. To allow the measurement of the V_{1P} signal when the breaker is open, the

measured voltage must be near nominal (the positive-sequence voltage, V_1, above 90 percent of the nominal phase-to-ground voltage, V_{LN}) and balanced (the negative-sequence voltage, V_2, below 10 percent of the positive-sequence voltage, V_1) for at least 50 ms. In addition, the breaker must be completely open (3PO bit asserted) and must not have been opened recently and therefore subjected to the ring-down voltages (rising-edge detectors for the OPA, OPB, and OPC bits with the 150 ms dropout timer).

4.3 Phase-lock loop

Fig. 2 shows a simplified diagram of the polarizing logic PLL. The logic is based on the concept of a synchronous reference frame and uses a PLL with a proportional (P) controller to generate a replica voltage of the live input voltage. The logic calculates the locking error (E) and uses the controller to advance or retard the output voltage (V_{1PLL}) with the goal of aligning it with the live input voltage (V_{1P}). V_{1P}, in turn, is obtained by using the logic in Fig. 1. The relay supplies the frequency-controlled oscillator in the PLL with the frequency signal (f) from the frequency measurement logic, augmented with the controller output (Δf). Therefore, the controller's role is to track and lock the angle and adjust for small frequency deviations. A positive Δf value speeds up the oscillator and advances the phase angle of the output voltage; a negative Δf value slows down the oscillator and retards the phase angle of the output voltage. The close-loop control allows phase locking of the output voltage V_{1PLL} to the input voltage V_{1P}. Once the output voltage is locked, the distance elements can use it for memory polarization. The gain of the controller allows locking within a few hundred milliseconds. A start-up logic (not shown) allows fast locking during line energization to make memory polarization available as soon as possible after the breaker closes. The supervisory logic monitors the locking error E to detect if the PLL is locked. If the PLL is locked, the output voltage V_{1PLL} is a valid replica of the live input voltage V_{1P}, and the distance elements can use it for polarizing in place of the live input voltage. The supervisory logic controls the PLL by 1) closing the control loop to allow locking and 2) opening the control loop to force the oscillator to freewheel. By doing so, the logic applies memory polarization. When freewheeling, the oscillator provides a memorized value of the voltage phase angle at the present value of the power system frequency. The frequency security filter suppresses changes in frequency resulting from transients to ensure they do not corrupt the polarizing voltage.

During fault conditions, the logic in Fig. 2 responds in one of the following three ways:

1. The positive-sequence voltage phasor V_{1P} remains sufficient for reliable measurement of the angle. In this scenario, the supervisory logic allows the PLL to slowly relock to the live voltage. In the first few tens of milliseconds, the polarizing voltage is fully memorized, and after several hundred milliseconds, the PLL relocks to the live fault voltage. In this scenario, the relay measures the power system frequency and uses it in the polarizing quantity. This is a preferred scenario, and it applies to all faults except close-in bolted three-phase faults.
2. The positive-sequence voltage phasor V_{1P} collapses to zero because of a close-in bolted three-phase fault. In this scenario, the supervisory logic forces the controller input to zero (the PLL is freewheeling), which makes the output voltage V_{1PLL} a fully memorized voltage. The polarizing voltage has a fixed frequency equal to the pre-fault frequency because the relay does not measure frequency if the positive-sequence voltage V_1 is zero. Limiting the duration of the memory polarization secures the distance elements in case the fault frequency is considerably different than the pre-fault frequency.
3. In applications to series-compensated lines, if the polarizing logic detects a voltage inversion, the logic forces the PLL to freewheel for a duration of 1 s to extend the memory duration and ensure proper directional operation of the distance elements. When in this polarization state, the logic stops using memory polarization if the frequency is significantly different than nominal or if the relay cannot measure frequency.

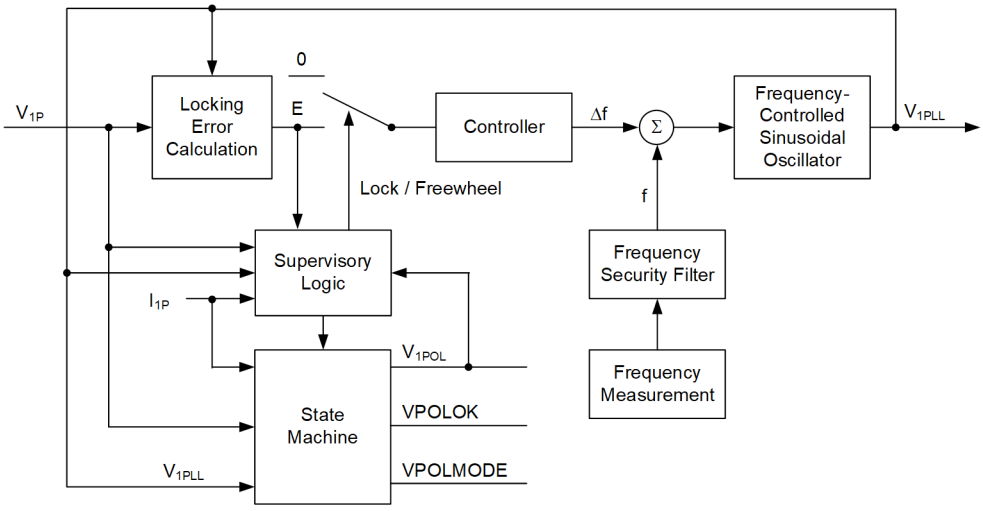

Fig. 2. Polarizing logic PLL.

4.4 Controlling the polarizing signal

The polarizing logic includes a state machine to control the polarizing voltage while explicitly addressing several fault and system conditions (Fig. 3). The state machine controls the following output signals:

- V_{1POL} is the polarizing voltage routed to the distance and phase directional overcurrent protection elements. This signal is referenced to Phase A and applies directly to the AG distance protection loop. The other five distance protection loops shift this signal by multiples of 30 degrees. Because the magnitude of the polarizing voltage does not matter, the voltage has a fixed magnitude equal to the nominal phase-to-ground voltage.
- The VPOLOK bit signifies that polarization is available. When VPOLOK deasserts, the relay blocks the distance and phase directional protection element.
- VPOLMODE is an analog signal provided for the ease of post-event analysis. It has values ranging from 0 to 6 that signify the polarizing method in use.

The state machine in Fig. 3 can be better understood with the following description. When the line breaker is open, the open-pole bits suppress all three voltages in the V_{1P} calculation (see Fig. 1) and the state machine remains in the *Polarizing Not Available* state. When the breaker closes and the line is healthy, the "V_{1P} is sufficient" condition asserts and the state machine transitions to the *Self-Polarized* state. In this state, the PLL tracks and eventually locks to the live voltage (see Fig. 2). A start-up logic (not shown) allows fast locking during line energization.

When the "PLL is locked" condition asserts, the state machine transitions to the *PLL Locked* state. In this state, the memory voltage is fully established. The logic detects a fault by using a disturbance detector and the "PLL unlocked" condition to transition to the *Memory-Polarized* state. The logic limits the memory action to 0.3 s, as explained in Subsection 3.4.

After the memory time expires, the state machine proceeds to verify the live voltage level. If the "V_{1P} is sufficient" condition is true, the state machine returns to the *Self-Polarized* state. In all cases but the close-in bolted three-phase fault, the memory will have already decayed and the transition from the *Memory-Polarized* state to the *Self-Polarized* state will not change the polarizing quantity.

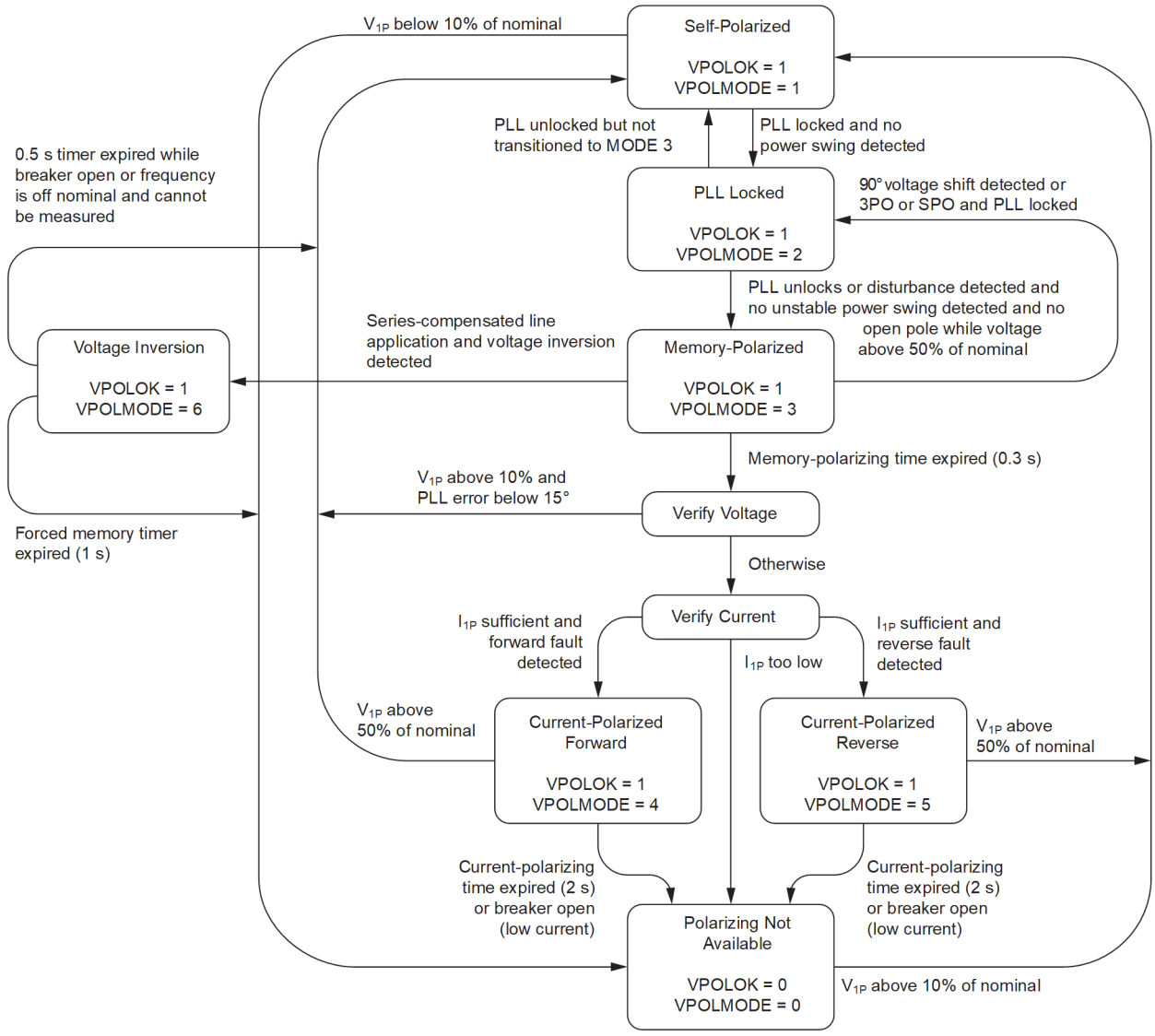

Fig. 3. Polarizing logic state machine.

If the voltage is too low, however, which is the case for close-in bolted three-phase faults that are not cleared in 0.3 s, the state machine proceeds to verify the positive-sequence current phasor I_{1P}. While in the preceding *Memory-Polarized* state, the logic was able to reliably determine the direction of the three-phase zero-voltage fault (forward or reverse) by measuring the angle between the polarizing voltage and the positive-sequence current. If the fault direction is forward and the V_{1P} voltage is still too low, then the logic uses the $+I_{1P}$ current phasor for polarizing (*Current-Polarized Forward* state, (3a)). If the fault direction is reverse and the V_{1P} voltage is still too low, then the logic uses the $-I_{1P}$ current phasor for polarizing (*Current-Polarized Reverse* state, (3b)). The logic shifts the current by the angle of the line positive-sequence impedance as per (3) to obtain the angle of the system voltage adequate for polarizing, as well as by multiples of 30 degrees depending on the distance loop. When in the *Current-Polarized* state, the logic starts a timer and terminates current-based polarizing after 2 s (three typical step-distance time-coordination steps plus margin). Current polarization allows time-delayed operation of directional distance elements and the phase directional element for close-in bolted three-phase faults.

By limiting the memory action to a safe interval of 0.3 s and using self polarization with voltage or current later into the fault, the distance polarizing logic provides dependable and secure polarization for instantaneous tripping, as well as time-delayed tripping, even under frequency changes as fast as 5 Hz/s and with zero voltage at the relay location during the fault.

If the relay detects a power-swing condition, the logic favors self polarization over memory polarization. When the power-swing blocking element [8] detects an unstable or accelerating power-swing condition, the polarizing logic forces self polarization.

In applications without series compensation, upon entering the *Memory-Polarized* state, the logic monitors for a step change in the angle between the live voltage and the memory voltage. If the logic detects a voltage shift greater than 90 degrees, the state machine exits the *Memory-Polarized* state and reverts to the *Self-Polarized* state. This step enhances security in applications in which the memorized voltage differs too much from the live voltage. This can happen when the local system is very weak relative to the remote system, and as a result, the local relay effectively locks to the remote source voltage rather than the local source voltage.

In applications with series compensation, upon entering the *Memory-Polarized* state, the logic monitors for a voltage inversion. If the logic detects a voltage shift greater than 20 degrees, the logic extends the memory usage from the normal 0.3 s to 1 s. After the 1 s timer expires, the logic reverts to the *Polarizing Not Available* state. This step improves the security of distance elements if the fault voltage is inverted because of series compensation.

5 Examples of Operation

The polarizing logic presented in the previous section has been implemented in relay [3] and has been in service since 2020. This section presents examples of operation in the field.

5.1 Internal fault with successful autoreclosing

Fig. 4 presents the relay voltages, currents, and the mode of polarization for an internal CG transient fault. The ultra-high-speed relay [3] asserted the trip command in 10 ms and the protection system cleared the fault in 32 ms (2 cycles) by tripping Pole C of the two-cycle breaker. The reclose attempt was successful, and the line was fully restored to service 500 ms after the fault inception. Prior to the fault, the polarizing logic was locked and ready to apply memory polarization (VPOLMODE 2 in Fig. 3). When the fault happened, the logic applied memory polarization (VPOL-MODE 3). The memory polarization was replaced by self polarization in 72 ms because the PLL was locked and the open-pole condition asserted following the trip. During the single-pole open interval, the logic was ready to apply memory polarization should a second fault have occurred. When the line was reclosed, the logic applied memory polarization and kept it for the maximum duration of 0.3 s.

This case shows oscillations because of the low inertia of the nearby sources. The oscillations are visible in the measured frequency. During the event, the frequency deviation with respect to the pre-fault frequency is as high as 0.1 Hz. The system oscillates at about 1.6 Hz (oscillation period of about 0.63 s). Fig. 4 shows the granularity of the frequency measurement and how well the method [7] implemented in relay [3] measures the power system frequency.

Fig. 4 also shows the positive-sequence voltage (V_1) angle and the angle of the positive-sequence voltage derived by accounting for open poles (V_{1P}) and used in the PLL. The angles are referenced to the pre-fault angle and frequency. The two angles are the same if all poles are closed. When Pole C is open and the remote terminal recloses at about 0.35 s after the fault inception, the remote terminal drives the Phase C voltage, and that affects the V_1 angle (the angle difference between V_1 and V_{1P} is about 20 degrees). The PLL, however, tracks the local Phase A and Phase B voltages only and is unaffected by both the transients and the incorrect angle of the Phase C voltage. Fig. 4 illustrates the importance of removing voltages from phases with an open-pole condition when measuring frequency and deriving the live voltage for tracking in the polarizing logic.

The plot in Fig. 4 also shows the polarizing voltage (V_{1POL}) angle. Shortly after the fault inception, this angle reflects the pre-fault angle as desired (memory polarization). Subse-quently, the polarizing voltage tracks the live voltage. As expected, when the system swings, the polarizing voltage lags the live voltage because of the swing. The inertia built into the PLL makes the PLL output lag the PLL input during swing conditions. The PLL tracks the live voltage closely despite the oscillations. In this case, the angle difference between the live voltage (V_{1P}) and the polarizing voltage (V_{1POL}) is less than 2 degrees and the state machine declares the PLL locked because the angle difference is so small; VPOLMODE is 2.

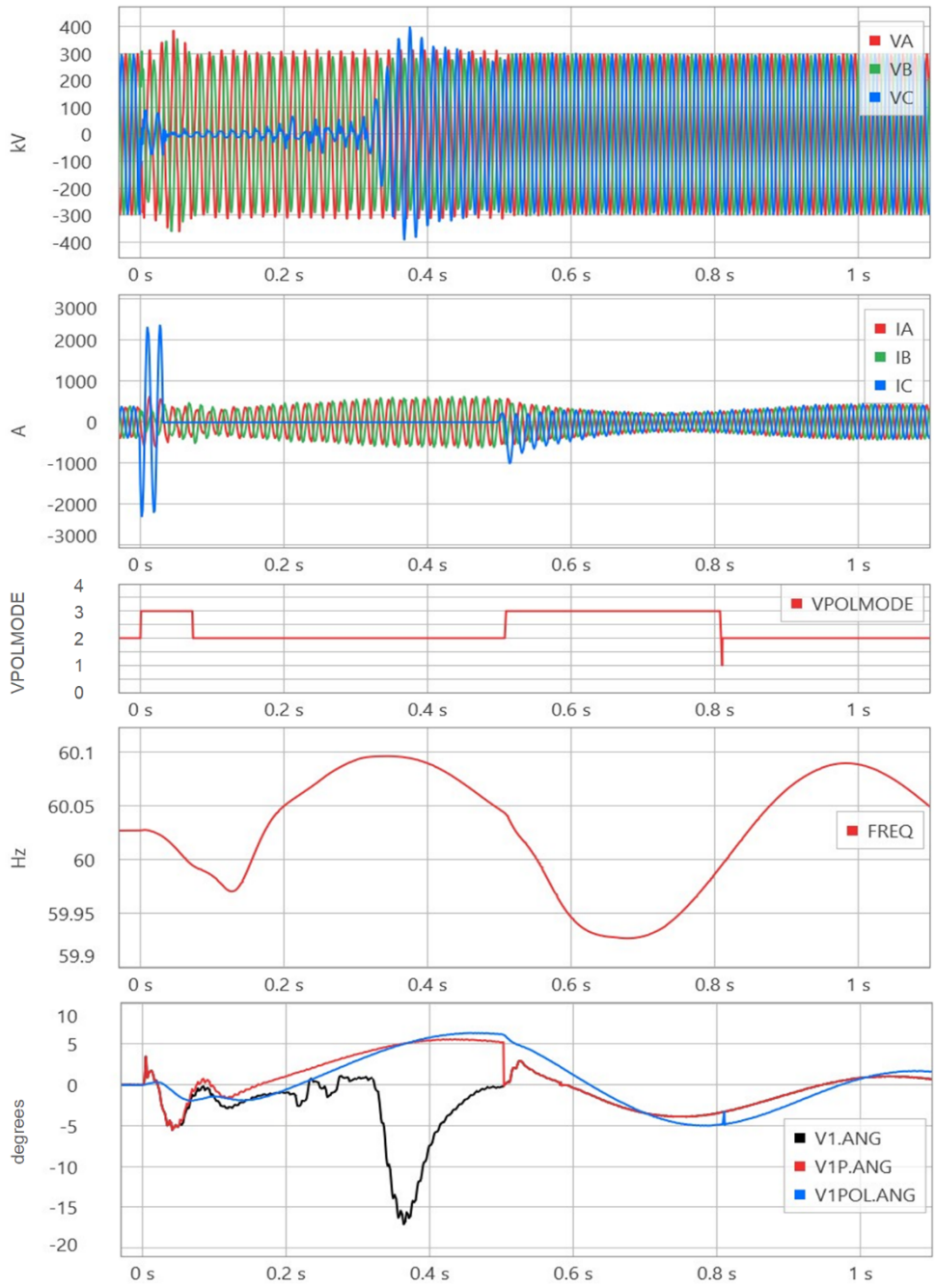

Fig. 4. Field record 1: single-pole trip with successful reclosing.

5.2 External fault with unsuccessful reclosing

Fig. 5 presents the relay voltages, currents, and the mode of polarization for a permanent external fault in the reverse direction. Because it is an external fault, the relay did not trip, and no open-pole condition asserted. Therefore, the logic applied memory polarization for the entire 0.3 s. The PLL was locked at the end of the 0.3 s interval, and the logic returned to VPOLMODE 2 (PLL locked). Therefore, when the reclosing took place, the logic applied memory polarization (VPOL-MODE 3) and kept it again for 0.3 s. During the time between the fault and reclosing on that permanent fault, the polarizing logic was locked to the live voltage. This lock increased the protection security in case the system frequency started to drift.

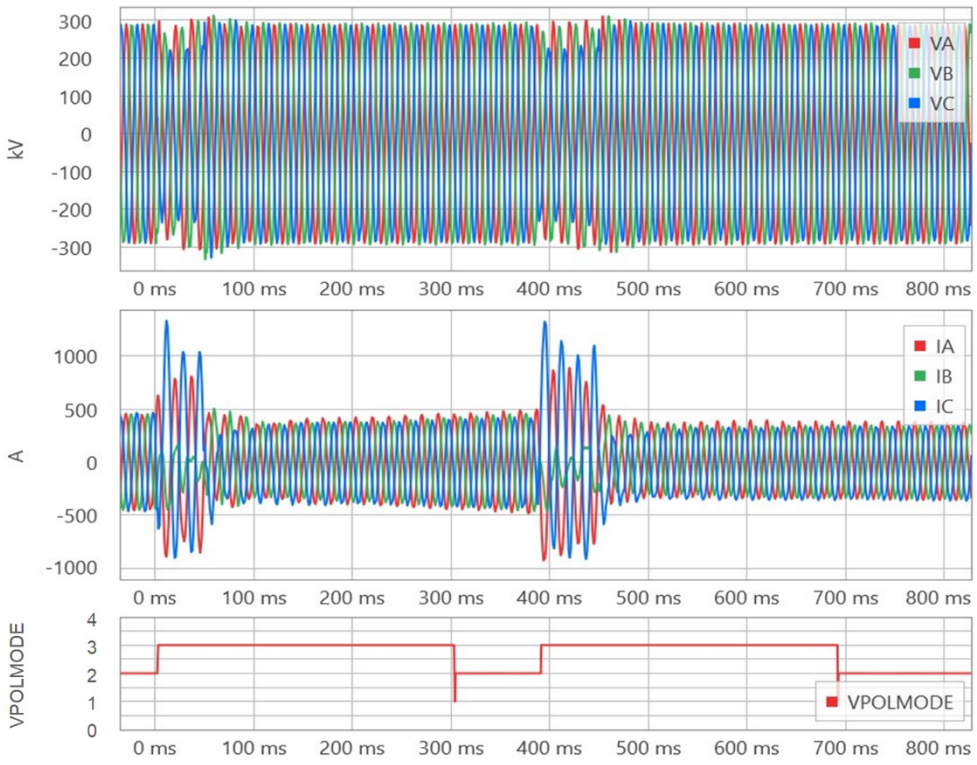

Fig. 5. Field record 2: external fault with unsuccessful reclosing.

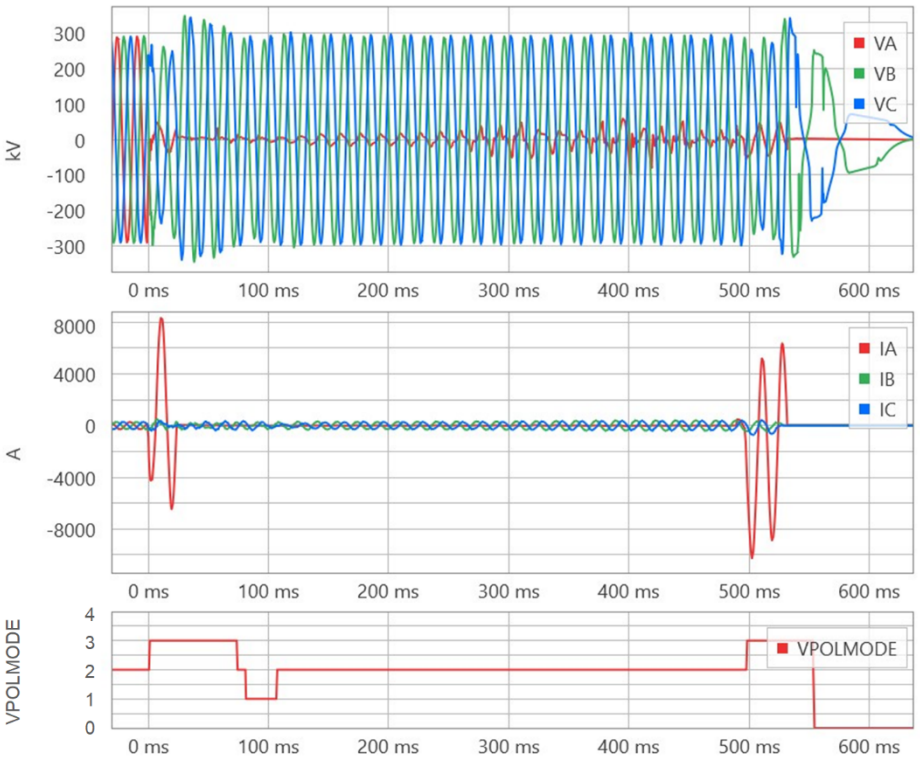

Fig. 6. Field record 3: internal fault with unsuccessful reclosing.

5.3 Internal fault with unsuccessful reclosing

Fig. 6 presents the relay voltages, currents, and the mode of polarization for an internal permanent AG fault. The ultra-high-speed relay [3] asserted the trip command in 2.1 ms by using an incremental-quantity distance element (TD21), and the protection system cleared the fault in 24 ms (1.5 cycles) by tripping Pole A of the two-cycle breaker. The reclose attempt was unsuccessful, and the line was tripped and locked out. Prior to the fault, the polarizing logic was locked and ready to apply memory polarization (VPOLMODE 2). When the fault occurred, the logic applied memory polarization (VPOLMODE 3). The memory polarization was removed in 74 ms once the open-pole condition asserted following the trip. The

polarizing logic state machine returned to VPOLMODE 2 (PLL locked) for a brief time and transitioned to VPOLMODE 1 (PLL locking). The PLL relocked very quickly, and the logic entered VPOLMODE 2 in 105 ms following the fault inception. From that time on, the logic was ready to apply memory polarization should a second fault have occurred. When the line was reclosed, the logic applied memory polarization and kept it for 56 ms (the relay tripped again, and the open-pole condition terminated the *Memory-Polarized* state before the 0.3 s timer expired). After the second (three-pole) trip, all three voltages were removed and the logic transitioned to the *Polarizing Not Available* state (VPOLMODE 0). When the line was eventually reclosed, the relay relied on the switch-onto-fault logic before the polarizing logic established a valid polarizing signal for the distance protection elements.

6 Conclusions

This paper presents a distance polarizing logic suitable for systems with low-inertia generation including wind-powered machines and inverter-based sources. To address the new characteristics of such low-inertia systems, the angle and frequency tracking and locking parts of the polarizing logic must accommodate the need for much shorter time constants today than in the past. Memory polarization cannot be applied for too long because fast frequency excursions can jeopardize distance protection security. Measuring frequency and using it to adjust the polarizing signal is desirable, but it cannot guarantee proper operation during close-in bolted three-phase faults. These faults yield voltages that are too small and unreliable to be used for frequency measurement. This paper advocates switching to offset polarization during such faults instead of extending the use of memory for too long. Our new design applies either a forward or reverse offset depending on the initial direction of the fault. The logic applies reverse offset to ensure distance protection dependability for forward faults. The logic applies forward offset to ensure distance protection security for reverse faults.

The presented approach uses a synchronous frame reference with a phase-locked loop to track and lock to the live voltage. The logic uses a state machine to explicitly control how the polarizing signal is selected, validated, and used depending on the application (such as protecting series-compensated lines) and present conditions (such as time since the fault inception, voltage inversion, power swing, and open-pole condition). The state machine allows the users to better understand the logic when testing or performing event analysis. A state machine is also a good foundation for the relay designers because it allows adding new conditions and states as we learn more about the behavior of modern power systems.

The presented approach has been in service for three years at the time of writing and it performs exceptionally well, including in parts of the grid that have significant percentages of wind and inverter-based generation.

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