Development and Implementation of a Control System for an Independent Phase-Controlled Capacitor

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1 Introduction

A utility-owned distribution substation was experiencing voltage unbalance on the 27.6 kV distribution buses. The 115 kV source to the substation is on the same tower structure as another 500 kV line. The mutual coupling between the two transmission lines results in voltage unbalance on the 115 kV line during high-power flow conditions on the 500 kV line [1]. The unbalance manifests as negative-sequence voltage at the 27.6 kV substation buses, which can result in the overheating of motor loads. Fig. 1 shows the simulation results for the 27.6 kV negative-sequence voltage for various 500 kV and 115 kV power flows. The graph shows that the negative-sequence voltage at the 27.6 kV buses increases when the power flow on the 500 kV line increases in either direction.

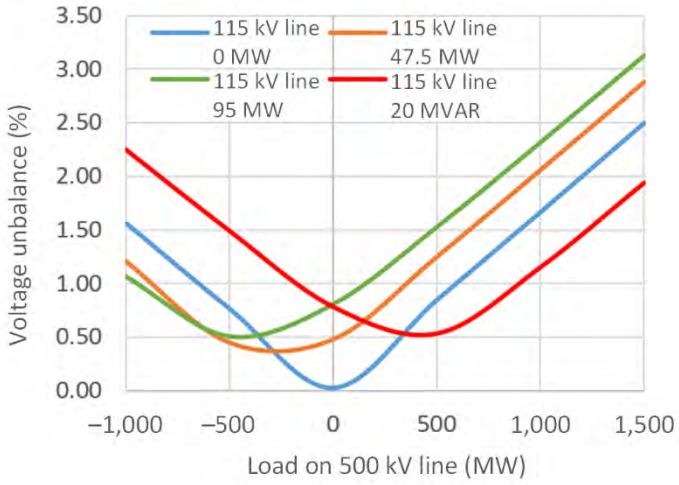

Fig. 1. Negative-Sequence Voltage on the 27.6 kV Bus for Different 500 kV Flows

The utility installed a multistage delta-connected capacitor bank, and a control system collectively called the independent phase-controlled capacitor (IPCC). The IPCC can counteract the negative-sequence voltage by switching in different stages of capacitors in different phases to cancel out the negative-sequence voltage on the 27.6 kV bus. The IPCC can also provide symmetrical voltage support by switching capacitors in all three phases simultaneously. Priority is given to the unbalanced voltage compensation.

Legacy equipment failures and the lack of spare parts necessitated the replacement of the legacy controller with a modern system while retaining original power system equipment, such as capacitors, inductors, switches, and instrument transformers.

1.1 Substation Layout

The distribution substation is fed from a single 115 kV source. Two step-down transformers feed two 27.6 kV distribution buses connected via a normally closed bus tie. Details are shown in Fig. 2. There are several distribution feeders on each bus that are not shown in this figure. The IPCC is connected on dedicated feeder circuits and can be isolated via breakers. The IPCC resides within the substation perimeter.

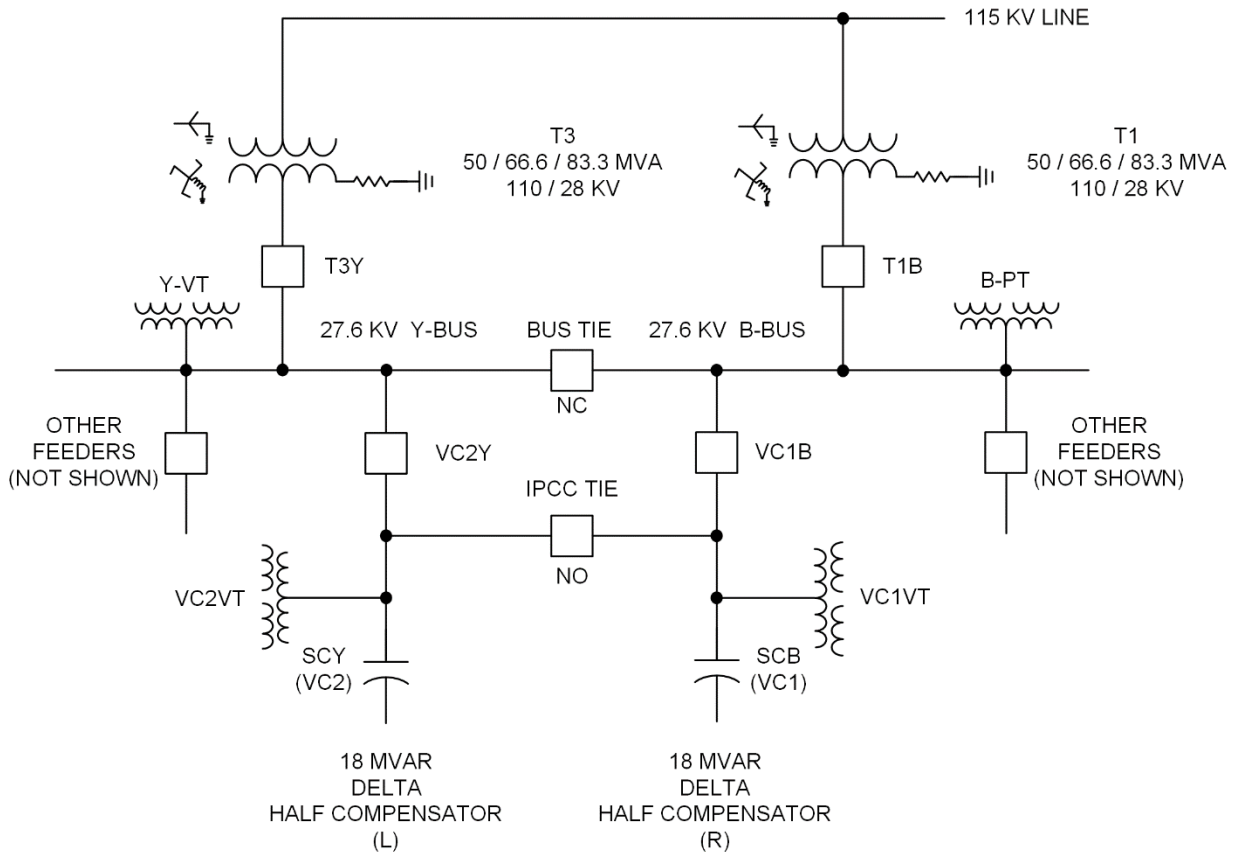

Fig. 2. Utility Substation Layout

1.2 IPCC Configuration

The IPCC capacitor bank is a delta-connected capacitor bank rated at 36 MVAR with 12 MVAR per phase, which can be switched in four stages (or 3 MVAR per stage per phase). The capacitor stages are switched in/out using vacuum switchers VS1-VS12 [2]. The capacitors are evenly distributed between the Y-bus and the B-bus (see Fig. 2 and Fig. 3) to maintain symmetry as much as possible. An IPCC tie breaker can be closed if either the Y- or B-bus is out of service so that the IPCC stages associated with the bus that is out of service can be transferred to the in-service bus and switched in as necessary. The IPCC tie and the bus-tie breakers are interlocked so that both cannot be closed simultaneously. The IPCC detail is shown in Fig. 3. The drawing does not show grounding switches or discharge voltage transformers (DVTs) present in the system that measure voltage across each capacitor for protection; these details are provided in Section 4.1 of this paper.

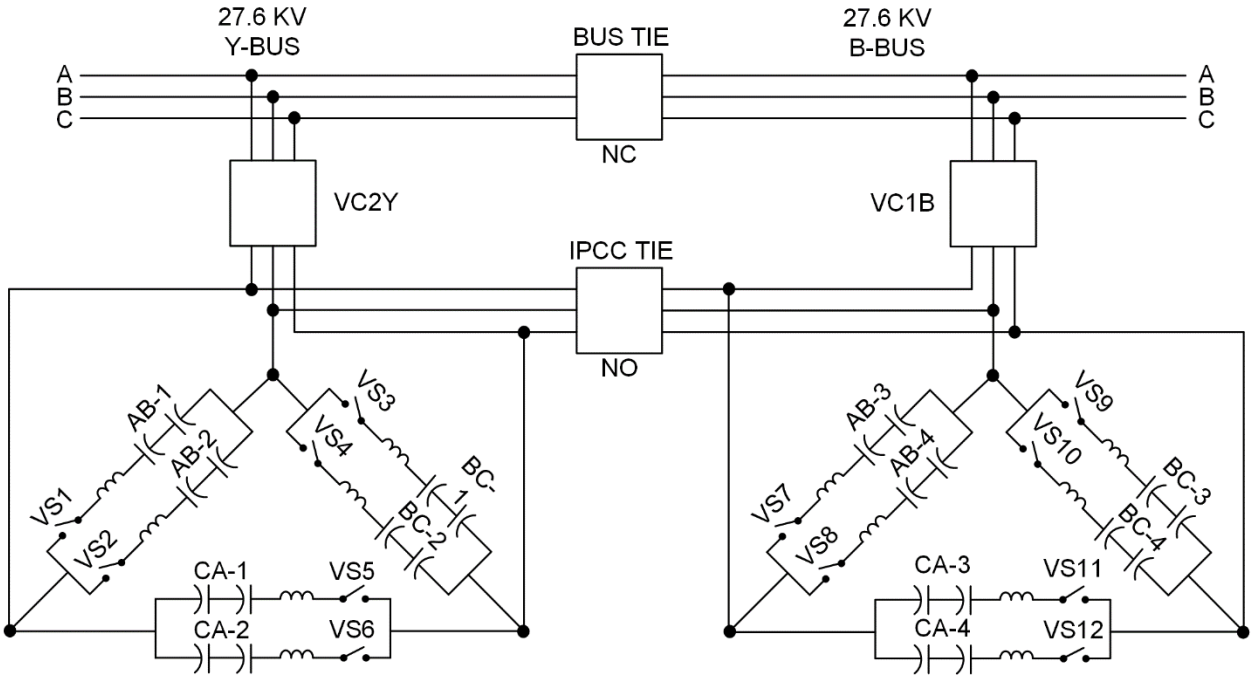

Fig. 3. IPCC Detail

1.3 Unbalanced Voltage Compensation Principle

The equivalent sequence network with one interphase capacitor closed is similar to a phase-to-phase fault circuit with fault impedance, as shown in Fig. 4.

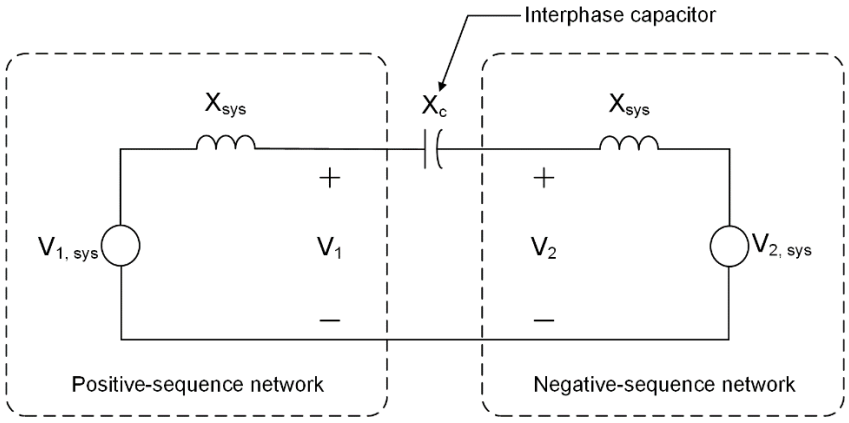

Fig. 4. Single-Phase Equivalent of the Capacitor

The positive-sequence voltage change caused by switching one interphase capacitor is provided by Equation (1).

$$\frac{\Delta V_1}{V_{1,sys}} \approx -\frac{X_{sys}}{X_c + 2 \bullet X_{sys}} \tag{1}$$

where:

ΔV_1 is the change in positive-sequence voltage.

$V_{1,sys}$ is the equivalent positive-sequence system voltage.

X_{sys} is the Thevenin equivalent of the system impedance.

X_c is the capacitance inserted in the system.

The negative-sequence voltage change caused by switching one interphase capacitor is provided by Equation (2).

$$\frac{\Delta V_2}{V_{1,sys}} \approx \frac{X_{sys}}{X_c + 2 \bullet X_{sys}} = -\frac{\Delta V_1}{V_{1,sys}} \quad (2)$$

where:

ΔV_2 is the change in negative-sequence voltage.

$V_{1,sys}$ is the equivalent positive-sequence system voltage.

X_{sys} is the Thevenin equivalent of the system impedance.

X_c is the capacitance inserted in the system.

The change in negative-sequence and positive-sequence voltage is equal in magnitude but opposite in direction. It can also be deduced that the negative-sequence voltage magnitude change, caused by switching in/out one interphase capacitor, is the same as the change caused by switching out/in two capacitors, one in each of the other two interphases.

2 Control Algorithm

The algorithm is designed to operate in the following sequential manner.

1. If the system negative-sequence voltage percentage goes outside the bandwidth for a certain amount of time determined by the user, a switching operation is performed, as determined in the numbered bullets 2, 3, and 4.

$$V2[\%] > V2P[\%] \quad (3)$$

where:

$V2[\%]$ is the system negative-sequence voltage.

$V2P[\%]$ is the user-set negative-sequence voltage threshold, which is $V2P_{normal}$ or $V2P_{contingency}$, depending on system conditions.

The set point is determined by the state of the system. If the system is single-ended (i.e., if one of the main breakers is open) or if it is a split-bus condition (i.e., if the bus-tie breaker is open), then $V2P_{contingency}$ is used. If the system configuration is normal, then $V2P_{normal}$ is used. $V2P_{normal}$ is greater than $V2P_{contingency}$, because switching the operation in a weaker system yields in larger switching transients.

2. The average phase-to-phase voltage is calculated, as shown in Equation (4). The deviation of each phase-to-phase voltage from the average voltage is determined using Equations (5), (6), and (7).

$$Vavg = \frac{Vab + Vbc + Vca}{3} \quad (4)$$

$$Dab = Vab - Vavg \quad (5)$$

$$Dbc = Vbc - Vavg \quad (6)$$

$$Dca = Vca - Vavg \quad (7)$$

where:

Vavg is the average of the three phase-to-phase voltages.

Dab is the deviation of Vab from the average voltage.

Dbc is the deviation of Vbc from the average voltage.

Dca is the deviation of Vca from the average voltage.

3. The voltage deviation is sorted according to their magnitude and assigned by maximum deviation, medium deviation, and minimum deviation. These are designated as Dmax, Dmid, and Dmin.

4. The capacitor switching is carried out based on the logic that follows. The total compensation (symmetrical + asymmetrical) at any given time is calculated in Equation (8).

$$\begin{bmatrix} Cab \\ Cbc \\ Cca \end{bmatrix} = K \begin{bmatrix} Cn \\ Cn \\ Cn \end{bmatrix} + \begin{bmatrix} Kab \\ Kbc \\ Kca \end{bmatrix} Cn \quad (8)$$

where:

Cab, Cbc, and Cca are the total capacitors in each interphase.

Cn is the capacitance of one branch/stage.

K represents the stages of symmetrical compensation that are switched in at any instance of time. The range of K is $0 \le K \le 4$. It is assumed that K = KY + KB, where KY is the capacitor branches on Bus Y half of the IPCC and KB is the capacitor branches on Bus B half of the IPCC.

Kab, Kbc, and Kca are the capacitors for asymmetrical compensation in each interphase, and the range of these values is $-K \le (Kab, Kbc, Kca) \le 4 - K$.

Whenever the negative-sequence voltage exceeds the setting, there are two possible state transitions.

- Switch in/out a capacitor branch corresponding to Dmax.
- Switch out/in capacitor branches corresponding to Dmid and Dmin.

For example, the current state can be assumed as [1, 0, 0]. If the negative-sequence voltage exceeds the setting, and if it is determined that Vbc is too low compared to Vab and Vca, then there are two state transition candidates.

- [1, 0, 0] → [1, 1, 0], which means switching on a capacitor branch (BC).
- [1, 0, 0] → [0, 0, –1], which means switching out two capacitor branches (AB, CA).

The control strategy is to minimize |Kab| + |Kbc| + |Kca| when choosing a state transition. The same strategy applies in recovering states when the controller restarts.

After choosing the state transition, the total capacitor branches that need to be switched on must be calculated by adding K to Kab, Kbc, and Kca. The sums are denoted as Nab, Nbc, and Nca.

$$Nab = K + Kab \quad (9)$$

$$Nbc = K + Kbc \quad (10)$$

$$Nca = K + Kca \quad (11)$$

Nab, Nbc, and Nca are adjusted by executing the following sequentially so that Nab, Nbc, and Nca are feasible.

- A switching operation should be performed by the controller if $0 \le Nab \le Mab$, $0 \le Nbc \le Mbc$ and $0 \le Nca \le Mca$, where Mab, Mbc, and Mca are the available branches after deducting the branches that are tagged out from the total number of capacitor branches.
- If min(Nab, Nbc, Nca) < 0, the controller should increase the lesser of KY and KB (i.e., switch in one branch on all three phases on the bus), which has the lower number of branches switched in.
- If Nab > Mab, Nbc > Mbc, or Nca > Mca, the controller should decrease the larger of KY and KB (i.e., switch out one branch on all three phases from the bus), which has the higher number of capacitor branches switched in.
- If Nab, Nbc, and Nca are still not feasible, the controller should alarm and recover KY and KB to the values before the previous adjustments. No switching is performed in this part of the sequence. The control goes back to the beginning of the sequence.

Note that Nab, Nbc, and Nca are always updated whenever KY and KB change.

An example sequence of operations, using the control algorithm described in this section, is provided in the Appendix.

3 Algorithm Validation Using Electromagnetic Transients Program (EMTP) Modeling

Prior to development of the code and implementation in the field, validation was required in a simulated environment. To achieve this, the power system and the control algorithm were modeled using an electromagnetic transient analysis program and simulations were performed. The simulation starts at zero power flow on the 500 kV transmission line. The power flow is increased up to the maximum line rating, ramped down to zero, increased up to maximum line rating in the opposite direction, and finally ramped down to zero again. The two objectives of the control algorithm are as follows.

- It should be convergent (i.e., upon a full cycle of switching, it should come back to its original state).
- It should not hunt or have multiple switching operations.

Fig. 5 shows the results of the simulations. The first graph shows the 27.6 kV bus phase-to-phase voltages as they change with the power flow in the 500 kV line. The second, third, and fourth graphs show the switching of the four stages of the interphase capacitors. At the end of the simulation, it is seen that the state of the capacitors is the same as it was at the beginning of the simulation.

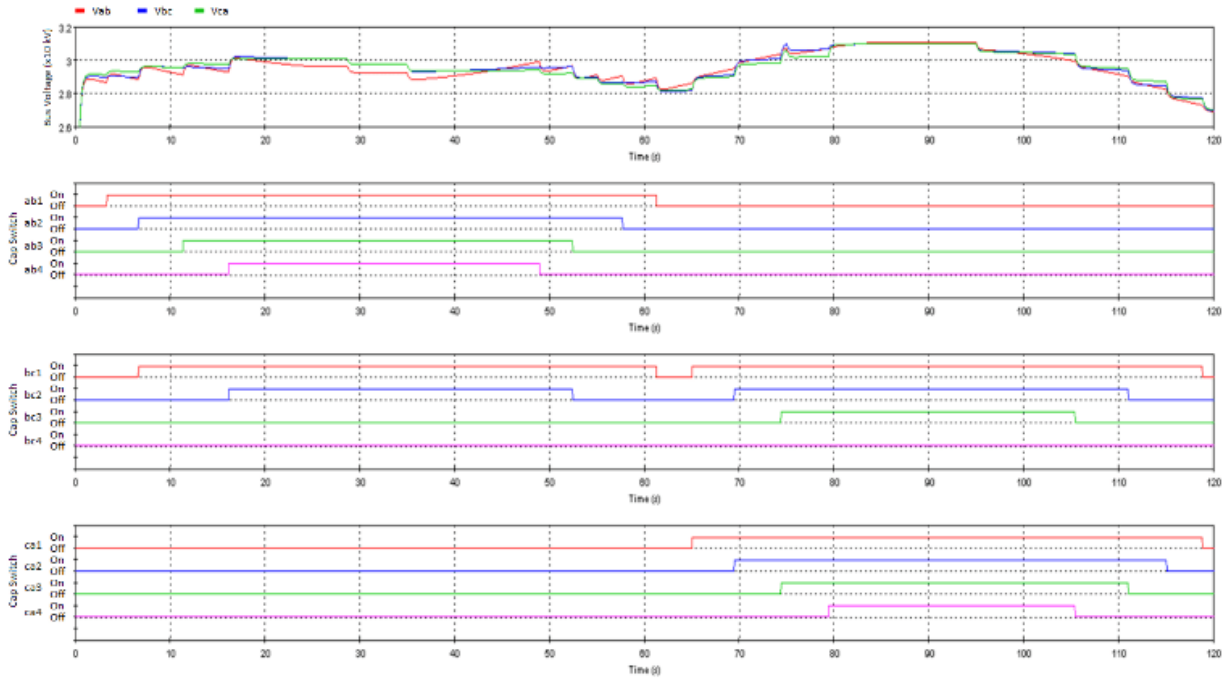

Fig. 5. EMTP-RV Simulation of the IPCC Algorithm

4 Implementation

The new IPCC controller is a set of two independent controller devices working in active/hot-standby configuration. Both the controllers evaluate the inputs and make decisions, but only the active controller executes the command. Four serial channels are used for communications between the main and alternate controller.

A proprietary peer-to-peer protocol is used on COM1 and COM2 for exchanging high-speed signals, such as operating modes and communications failures.

Distributed Network Protocol 3 (DNP3) is used on COM3 and COM4 to exchange information to synchronize the human-machine interface (HMI) screens and controller states. DNP3 links are also used

to send commands from supervisory control and data acquisition (SCADA) to the active controller. Fig. 6 shows the communications architecture of the new system.

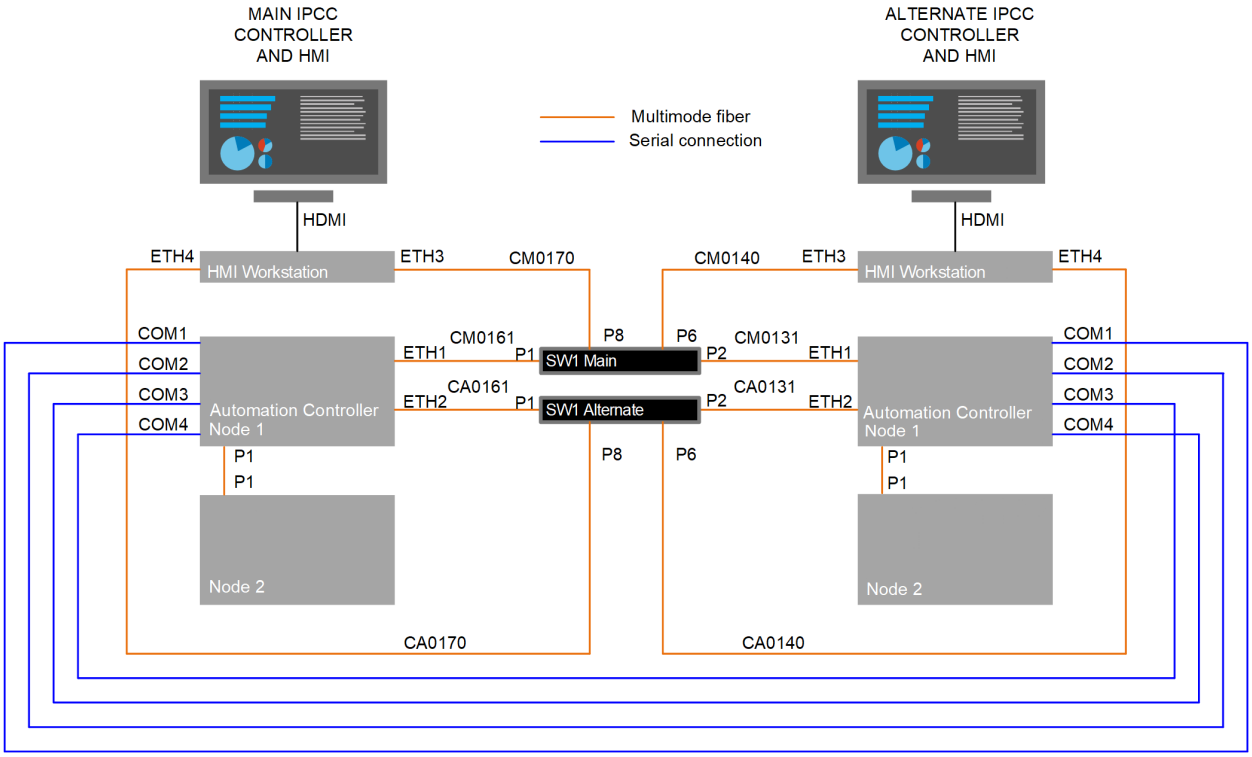

Fig. 6. Communications Architecture

4.1 Voltage Measurement

The calculations are done within the task cycle of 200 milliseconds. Logic has been created to calculate the percentage of positive-sequence and negative-sequence voltage in the controller, as shown in Equations (9) and (10).

$$V1[\%] = \frac{V1[kV]}{27.6\ kV} \cdot 100 \tag{12}$$

$$V2[\%] = \frac{V2[kV]}{V1[kV]} \cdot 100 \tag{13}$$

In all bus configurations, both IPCC controllers measure voltages from both sides. Under normal operating conditions (bus-tie breaker closed), the main IPCC and the alternate IPCC controller use their respective voltage transformers (VTs) for voltage measurement. Under normal conditions, a voltage discrepancy alarm is issued when the positive-sequence voltage measured by one VT deviates from that measured by the other VT by more than 10 percent for 2 seconds or more.

If there is a voltage discrepancy between measured voltages from both VTs on each controller, the controller uses the signals from the VT with positive-sequence voltage measurement that is closer to nominal. This functionality is an improvement over the legacy controller in which a voltage discrepancy alarm was asserted when there was a mismatch and an operator voltage discrepancy override command was required to switch over to the controller with the healthy voltage.

Under a split-bus condition (bus-tie breaker open), the controller designated as active processes the logic individually for each bus using VTs from the corresponding side. The voltage discrepancy alarm logic is not implemented for a split-bus condition, since the VTs are reading different voltages and cannot be compared against one another.

4.2 Active/Standby Configuration

The two controllers are labeled as main and alternate controllers. The control systems work in an active-standby configuration. One of the two controllers can be set as active via a local HMI or from SCADA. Consequently, the other controller is automatically assigned as standby.

The controller hardware failure alarm contacts are hardwired to a remote terminal unit (RTU). The indication of an alarm on one of the controllers is received by the other from the RTU via DNP3. A controller goes into an alarm state upon hardware or software failures or upon reboots. If the alarm is identified in the active controller, the standby controller is automatically assigned as active. If both controllers simultaneously restart (e.g., when there is a station direct current surge or fluctuation), the controller that initializes first starts as the active and the other controller becomes the standby.

Both main and alternate controllers have local HMIs (see Fig. 7), which can be accessed from the corresponding controller panel.

4.3 Automatic/Manual Mode

The active controller can be set in automatic or manual mode from either the local HMI or from SCADA (if the remote is enabled). The standby controller follows the active controller's mode.

In the automatic mode, the controller measures the negative-sequence voltage in real time and automatically provides asymmetrical compensation to compensate voltage unbalances by switching in/out the appropriate number of capacitors using the control strategy, as explained in Section 2. The controller waits for a user-specified delay duration before executing a switching operation. This delay should be coordinated with the substation transformer load tap changer so that switching transients are not introduced [3]. Symmetrical compensation must be executed by issuing user commands either locally or from SCADA (when the remote is enabled), and these user commands are accepted and executed only in automatic mode.

Individual capacitor branches can be controlled via local HMI only in manual mode. This is considered a brute-force execution and should be avoided except for testing, troubleshooting, or other rare circumstances. The controller switches itself to manual mode upon the:

- Simultaneous restart of both main and alternate controllers. If the active controller alone restarts, the standby becomes the active controller and continues in the same mode that the active previously was in.
- Hunting limit being reached.
- Voltage being out of range (90 to 112 percent of nominal voltage).

4.4 Capacitor Branch Tags Out

Whenever a capacitor branch is commanded to close/open and the controller does not receive feedback that a change of state occurred within 5 seconds, the branch is tagged out and an alarm is issued. The controller continues in automatic mode.

An operator can tag out a vacuum switch from the local HMI in both automatic and manual modes. However, the tag can be released, and the switch can be placed in service only in the manual mode. A tagged-out vacuum switch appears in yellow on the HMI.

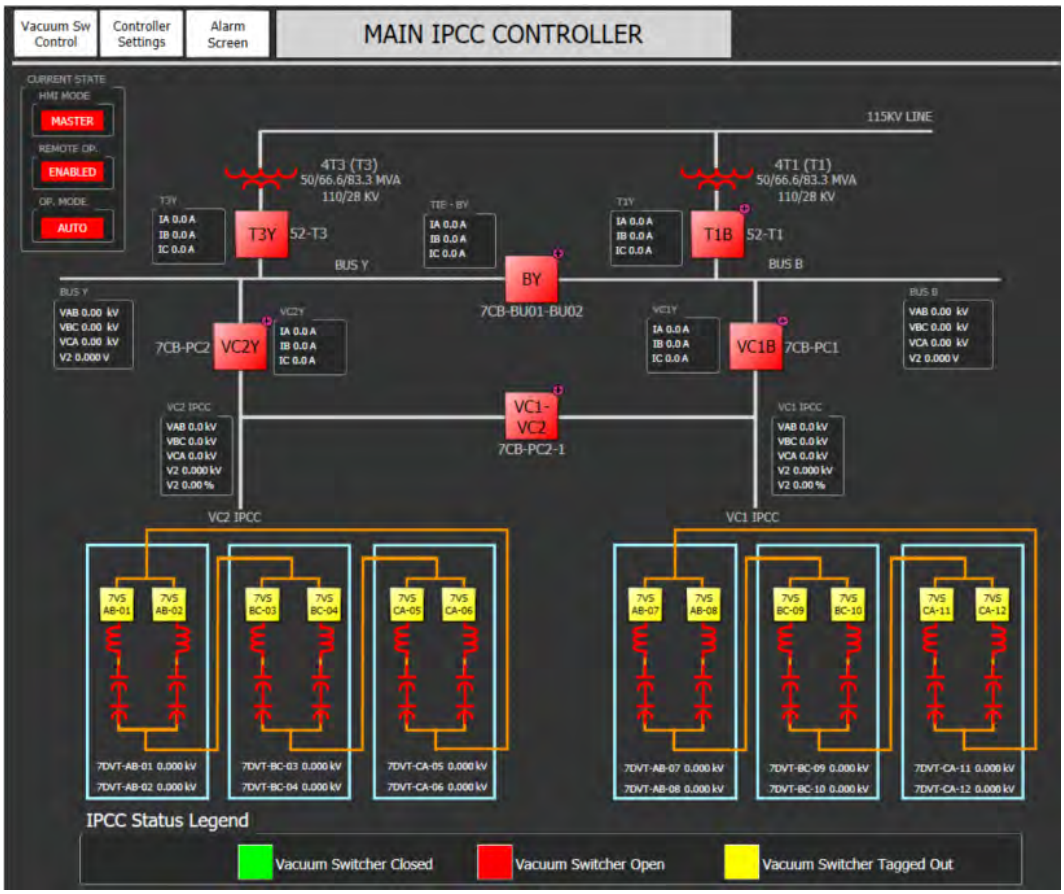

Fig. 7. One-Line Diagram on HMI Screen

4.5 Operations Counter Logic

Some capacitor branches are cycled more than the others over time if a predetermined order of switching is assigned. Therefore, a rolling switching algorithm based on an operations counter logic has been implemented so that capacitor branch operations can be distributed uniformly among all four stages in each phase. The branches are operated such that balance between capacitors on either of 27.6 kV bus is given higher priority than the operation counters. This is an improvement over the legacy controller.

4.6 Capacitor Bank Protection

IPCC controller provides voltage unbalance protection utilizing the single-phase DVT measurements across the individual capacitor branches. Under normal conditions, the DVTs should read 0 V across each capacitor branch. When internal capacitor fuses are blown, an unbalance is introduced, which is measured by the DVTs. The IPCC controller provides the following protection functions.

- Time-delayed unbalance trip: when the measured DVT voltage on a capacitor branch exceeds the trip set point for a time period, the corresponding 27.6 kV breaker is tripped. The trip set point and the time delay are user-configurable.
- Instantaneous unbalance trip: when the measured DVT voltage on a capacitor branch exceeds the instantaneous trip set point, the corresponding 27.6 kV breaker is tripped. The trip set point is user-configurable, and there is no intentional time delay.

Unlike the control algorithm, the protection logic is executed simultaneously in both the active and standby controllers, and the output contacts for issuing a trip are actuated in both controllers. See Fig. 8.

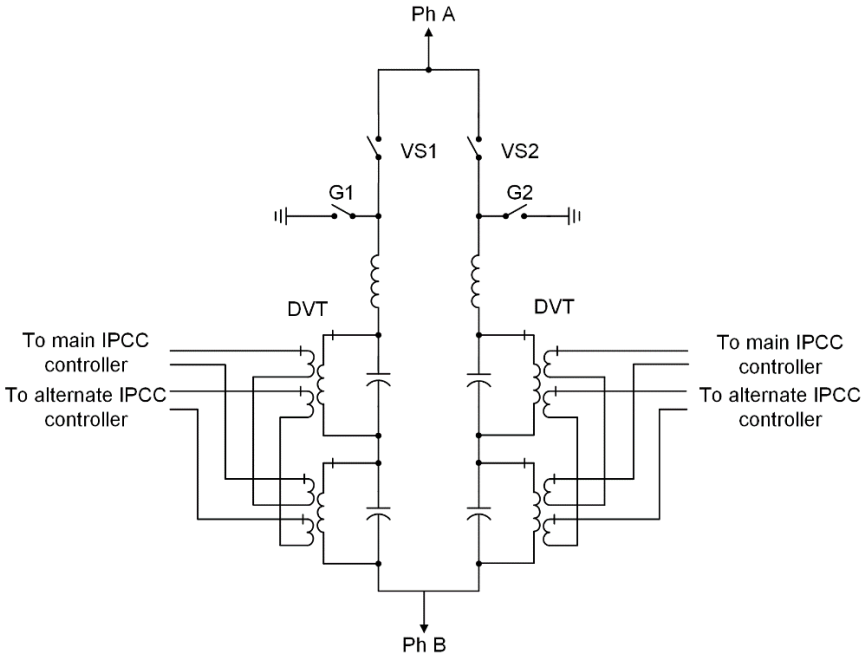

Fig. 8. Protection and Switching Device Details

4.7 Manual Transfer Scheme

A bus outage on either bus triggers a need for transfer of the IPCC branches to the available bus side by closing the IPCC tie breaker.

In case of bus outage, the IPCC controller assesses the system conditions and provides a hardwired close permissive for the IPCC tie breaker when it is safe to perform a transfer. The operators can then transfer the IPCC branches manually. The close permissive is issued when the following conditions are met.

- Station service associated with the bus is lost.
- All capacitor branches connected to the dead bus are opened.
- The bus to which transfer is being performed is healthy. A healthy bus is identified by having the incoming main breaker closed and a measured bus positive-sequence voltage greater than 90 percent of nominal.

4.8 Alarms and Checks

- Hunting: if the control logic causes any capacitor to switch in/out repeatedly more than a user-specified number of operations and under a specified time limit, then a hunting alarm is issued and the automatic mode on the controller is disabled.
- Capacitor switching unsuccessful: this alarm is issued when the control logic issues a close/trip command to a capacitor branch and a change of state is not recorded. The controller automatically tags that branch out and continues in automatic mode compensating using other branches.
- Compensation unsuccessful: the asymmetrical/symmetrical compensation unsuccessful alarm is issued when there is an attempt/command for either kind of compensation but there are not enough capacitor branches available to achieve the goal.

- Unbalance alarm: when the measured DVT voltage on a capacitor branch exceeds the alarm set point for 2 seconds, an alarm is issued. The 2-second time delay for the alarm is hard-coded.
- IPCC controller failure: the controller hardware failure alarm contacts from both main and alternate controllers are hardwired to an RTU. The indication of an alarm on one of the controllers is received by the other from the RTU via DNP3.

5 Testing and In-Service Performance

5.1 Onsite Testing

The solution described in the previous section was tested in the field prior to putting in service. This section describes the testing methodology and provides in-service performance results.

The testing was performed on a de-energized system. Voltage signals to the main and alternate controllers were injected using two synchronized secondary injection test sets. While the system was extensively tested in the lab, a subset of test scenarios was tested in the field, as shown in Table I. The test scenarios for the field were selected to represent all possible features of the algorithm—a split-bus operation, single-ended operation, combination of simultaneous symmetrical and asymmetrical compensation, and operation with tagged-out branches. The results of the field testing matched the expected sequence of operations, thereby instilling confidence for the team to put the system in service.

Table I
FIELD TESTING SCENARIOS

	System Configuration				
Scenario	**T3Y**	**T1B**	**Bus Tie**	**Symmetrical Compensation**	**Tagged-Out Branches**
1	Closed	Closed	Closed	None	None
2	Closed	Closed	Closed	One stage	None
3	Closed	Closed	Closed	None	One
4	Closed	Open	Closed	Two stages	None
5	Closed	Closed	Open	None	None
6	Closed	Closed	Open	One stage	None
7	Closed	Closed	Open	None	Two

5.2 In-Service Performance

The new controller has been in service for nearly a year. The in-service performance for the most recent month is shown in Fig. 9 and Fig. 10. Fig. 9 shows the SCADA data collected over a month. Fig. 10 shows a zoomed-in view of single switching operation.

The results confirm that the IPCC controller is performing as designed to reduce negative-sequence voltage and improve power quality. The control algorithm’s ability to dynamically adjust to real-time data is a key factor in its effectiveness. Future work will possibly focus on deploying the solution at other substations.

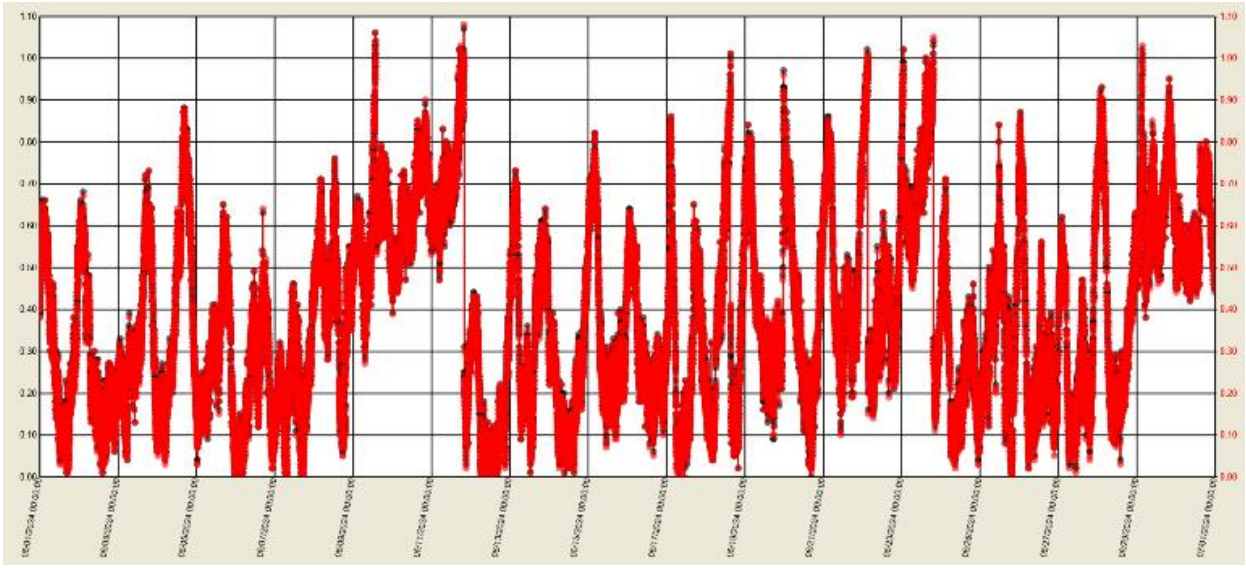

Fig. 9. In-Service Negative-Sequence (V2%) Measurement Over a Month

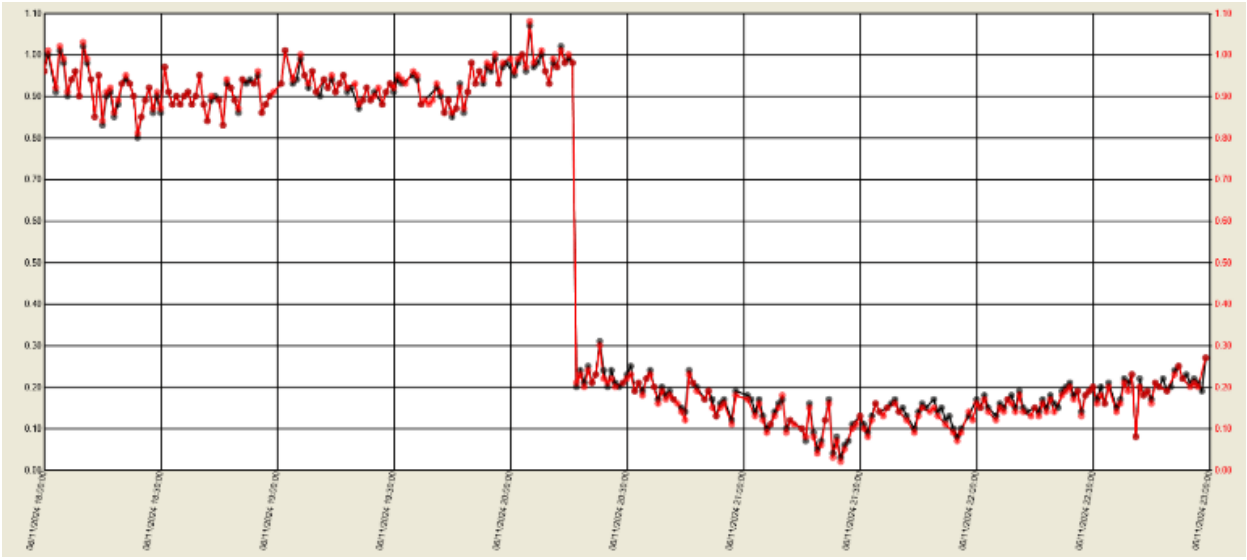

Fig. 10. V2% Change With One IPCC Switching

6 Conclusion

This paper describes the developing, modeling, and implementing of an IPCC system. The IPCC system introduces different capacitances in each phase of the power system, thereby canceling out negative-sequence voltage. The paper highlights improvements made over the legacy systems, such as a split-bus operating algorithm, switch based on operation counters, elimination of hunting by using a state- and space-based control system, design of a local HMI, and ability for the user to tag out a branch for maintenance, thereby improving the usability and increasing the longevity of the power system components.

7 Appendix: Test Values

In the test scenario described in this Appendix , the three-phase voltages, as shown in Table II, are the measured phase-to-phase voltages on the 27.6 kV bus. V_{2P} (user-set negative-sequence voltage threshold) is set as 0.80 percent. The system is operated in normal condition with the bus tie closed, and none of the capacitor branches on either bus are switched in or tagged out.

As seen in Table II, the negative-sequence voltage percentage (V2) is greater then the set point (V2P). Equation (3) is satisfied; therefore, it is concluded that a switching action is required.

As per the initial conditions, none of the capacitors are switched in or tagged out. Therefore, symmetrical and asymmetrical state transitions are: K equals zero and Kab, Kbc, and Kca equal zero. Using Equation (8), the initial state can be determined as Cab, Cbc, and Cac equal [0, 0, 0].

Table II
OBSERVED VOLTAGE BEFORE COMPENSATION

Vab		**Vbc**		**Vca**		**V2/V1**
Mag	Ang	Mag	Ang	Mag	Ang	
28,654.2	0	28,977.5	–119.283	29,120.3	119.78	0.97%

The controller calculates values for Dmax, Dmid, and Dmin using Equations (4) through (7). See Table III.

Table III
CALCULATED VOLTAGE DEVIATIONS IN EACH PHASE

Dmax	**Dmid**	**Dmin**
Dab = –0.0091	Dca = 0.007019	Dbc = 0.002081

The deviation of Phase AB is observed to be the highest. To compensate this deviation, two options for the state transition [Kab, Kbc, Kca] are possible:

- [1, 0, 0] – switching on a capacitor branch (AB).
- [0, –1, –1] – switching out two capacitor branches (BC, CA).

With the control strategy prioritizing minimum switching operations, the controller selects the first option, resulting in Nab, Nbc, and Nca equaling [1, 0, 0]. One branch is switched in for Phase AB, resulting in the reduction of negative-sequence voltage. See Table IV.

Table IV
OBSERVED VOLTAGE AFTER COMPENSATION

Vab	**Vbc**			**Vca**		**V2/V1**
Mag	Ang	Mag	Ang	Mag	Ang	
29,237.2	0	29,044.1	–119.557	29,351	120.556	0.60%

References

[1] M. O'Donovan, E. Cowhey, N. Barry, and J. Connell, "The Effects of Mutual Coupling Compensation on Distance Protection of Parallel Lines," proceedings of the 55th International Universities Power Engineering Conference (UPEC), Torino, Italy, September 2020.

[2] H. Schellekens, "Capacitor Bank Switching with Vacuum Circuit Breakers," proceedings of the China International Conference on Electricity Distribution, Guangzhou, China, 2008, pp. 1–7.

[3] N. Daratha, B. Das, and J. Sharma, "Coordination Between OLTC and SVC for Voltage Regulation in Unbalanced Distribution System Distributed Generation," *IEEE Transactions on Power Systems*, Vol. 29, No. 1, pp. 289–299, January 2014.

Biographies

Mudit Kumar, PE, received his Bachelor of Engineering in Electrical Engineering from Thapar University, Patiala, India, in 2015, and his Master of Science in Electrical Engineering from Michigan Technological University in 2019. He has over 6 years of experience in power engineering, specializing in substation automation, field testing, microgrid controls, distribution automation and controls, and project management. Since 2019, he has been serving as a project engineer at SEL Engineering Services, Inc., (SEL ES) in Plymouth, Michigan. He is a licensed PE in the state of Michigan.

Harish Chaluvadi, PE, received his Bachelor of Technology in Electrical and Electronics Engineering from the National Institute of Technology, Tiruchirappalli, India, in 2005 and his Master of Science in Electrical Engineering from Clemson University, South Carolina, in 2008. He has over 15 years of experience in power system engineering, including analytical studies, substation design, field testing, and project management. He joined SEL Engineering Services, Inc., (SEL ES) in 2012, and is currently serving in Hawthorn Woods, Illinois, as a project engineer. His interests are power system protection, power system planning, power quality, electromagnetic transients, renewable energy, and microgrids. He is a licensed PE in the states of California, Iowa, Wisconsin, Illinois, and Minnesota.

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Abstract—A utility-owned distribution substation with a 115 kV source and two step-down transformers was experiencing voltage unbalance on the 27.6 kV distribution buses. The 115 kV line is on the same tower as another 500 kV line, and the mutual coupling between the two lines manifests as voltage unbalance on the 115 kV line during high-power flow conditions on the 500 kV line. The unbalance is further magnified at the 27.6 kV substation buses and shows up as a high-standing negative-sequence voltage, degrading power quality for downstream end users. To address this challenge, the utility implemented an independent phase-controlled capacitor (IPCC) with multiple stages, capable of counteracting the negative-sequence voltage in the year 1991. The system operated with some gaps, such as the inability to operate in a split-bus condition, lack of control center visibility, and fixed switching sequence for capacitor branches. Legacy component failure necessitated an upgrade. This paper details the implementation of a new control algorithm to replace a legacy controller. It covers the algorithm's design, software simulation validation, controller development, testing, and in-service performance. The implementation successfully bridged the gaps in the legacy controller and demonstrated the effectiveness of a new control algorithm.

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