The Need for Simplicity in Arc-Flash Protection Design

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***Abstract*—Electrical switchboards ranging from low voltage to medium voltage have an inherent risk—arc flash. According to Industrial Safety & Hygiene News, approximately 30,000 arc-flash incidents occur each year. Of these incidents, 7,000 are burn injuries, 2,000 are hospitalizations, and 400 are fatal.**

Both historically and today, most installations have used an administrative and personal protective equipment (PPE) approach to reduce this risk. With advancements in technology, this risk can now be economically reduced by means of an engineering solution.

This paper explores the complexity of arc-flash protection systems due to their flexibility and why there is a need to simplify these designs. The consequence of the risk is based on the severity of the arc flash, and this severity is directly proportional to the duration, current magnitude, and system voltage. Out of these three variables, the duration is the only one that can be influenced by the protection system. The more complex the design, the longer the duration.

Arc-flash protection schemes have three main functions: light detection, current detection, and tripping. Having all three functions in a single protection device is the most time-efficient design. Due to the complexity of the power system, a single protection device may not be able to perform all three functions. To achieve this, a common application uses communications to link devices. This paper discusses the time impact that communications introduces.

Power system operators are beginning to request that discrimination be incorporated into arc-flash protection scheme designs. To achieve discrimination requires additional logic. With any protection system, discrimination inherently adds time. This paper provides a practical example where complexity due to flexibility caused a possible trip time to be slower than busbar protection.

This paper demonstrates the mathematical relationship between the three variables to show the impact that design considerations have on the arc-flash risk. Understanding the impact can lead to more economical designs when time is less critical and highlight the need for detailed design when time is more critical.

I. Introduction

Since the first arc-flash paper in 1982, which discussed the risks associated with arc flash in electrical switchboards, there has been a growing need to manage this electrical risk. Initially, the protection devices that were installed to detect and isolate these faults were most likely the electromechanical type that were not high speed and needed to be on an incomer, which meant they had to discriminate with downstream protection. The evolution of protection devices has also provided a means to improve protection system design using other detection methods, such as light detection.

A growing trend in arc-flash protection systems is to use communications to distribute protection system functions across multiple devices. Understanding the impact of using this method can help designers develop more efficient systems.

Along with secondary system evolution, the primary system has also changed. This change is regarding multiple sources in the network. The operation of electrical switchboards is growing in complexity with the need for varying operational configurations. This paper uses a recent project as an example to illustrate this evolution.

When developing an engineering solution to mitigate risk, it is important to understand how the end result is impacted. The National Fire Protection Association (NFPA) 70E *Standard, Standard for Electrical Safety in the Workplace*, is a well-established document that clearly defines methods for assessing the risk [1]. In particular, IEEE Std 1584, *IEEE Guide for Performing Arc Flash Hazard Calculations* [2], which defines a method for calculating the incident energy level, is used in the NFPA 70E standard. To demonstrate the impact of adding complexity to an arc-flash protection design, this paper presents an analysis of the impact that tripping time has on the incident energy level.

II. Source for Complexity

Arc-flash protection system design complexity is caused by the need for security and reliability. Security is needed because light is not a reliable source of information to determine that an arc-flash event has occurred. Light can be generated by sources other than an arc-flash event, which could cause a maloperation. The protection system utilizes a current check measurement to ensure the light was generated by an arc-flash event.

Prior to the development of dedicated arc-flash protection devices, protection systems used only current to determine that there was an arc-flash fault. It was not uncommon for the arc-flash ratings to use a timed overcurrent element as the detection element. These current-only protection schemes do not have the speed of new arc-flash protection.

Electric networks have evolved from simple, single-source systems to complex networks with multiple source configurations. An example of this is discussed later in the paper. The key requirement for modern arc-flash protection systems is the need to adapt to changing network arrangements to obtain the correct current check, and then isolate all current sources.

Complexity has also been driven by the need for a reliable network. System reliability is quantified by the system's availability. When there is a fault on the network, isolating only the impacted area improves the availability of the remaining network.

A common application for arc flash is medium-voltage switchboards, which can consist of multiple bus sections with many feeders. Discriminating the location of the fault and minimizing its impact adds complexity to the arc-flash protection design.

III. Arc-Flash Design Impacts

The two design impacts investigated as part of this paper are the introduction of communications and the use of standard logic. To understand the impacts, a test lab was set up. To develop a base level, 200 tests were conducted using a single relay. This device was responsible for switching both the current and light sources using a high-speed output contact. A typical timing diagram for this test is shown in Fig. 1.

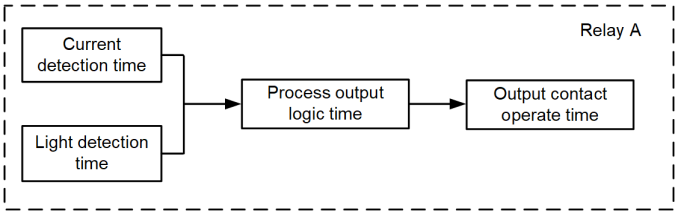

Fig. 1 Single relay timing diagram

Each test produced measured times using high-accuracy test equipment and the internal recording function of the protection device. These results are presented in Table I. When reviewing the test results, note that the internal time stamping has only a 1 ms resolution.

Table I Base Level Test Results

Test Results	Min. (ms)	Mean (ms)	Max. (ms)	Std. Dev. (ms)
Light Pickup – Internal	4	5	6	0.27
Current Pickup – Internal	2	3.63	7	1.51
Trip – Test Equipment	4.9	5.21	6.3	0.48

IV. Communications Impact

Arc-flash protection designs increase the utilization of communications systems within the design. The purpose of the communications system in the arc-flash protection design is to allow the distribution of light, current detection, and tripping between devices. A practical example of this is discussed later in the paper. The impact of incorporating communications into the design has not been well understood.

The use of communications has been easily adopted with the peer-to-peer protocol Generic Object-Oriented Substation Event (GOOSE) in the IEC 61850 standard. This standard allows for the binary status of the light pickup and current pickup to be mapped into a GOOSE message. The time variation from when either element picks up until the GOOSE message is sent depends on when the element pickup occurs within the processing cycle of the device. This is also true for the receiving of the GOOSE message at the receiving device.

The impact on the trip time has the possibility of variability because of the way a numerical relay processes information. Fig. 2 illustrates the component times that determine the trip time of a two-device arc-flash protection system.

The objective of the testing was to determine the time delay caused by the communications. To reduce the timing error caused by the analog system, the testing consisted of two tests: sending light pickup and sending current pickup via GOOSE.

Using 200 test results, the data have been analyzed to determine the minimum, mean, and maximum for each time measurement. The results are presented in Table II and Table III.

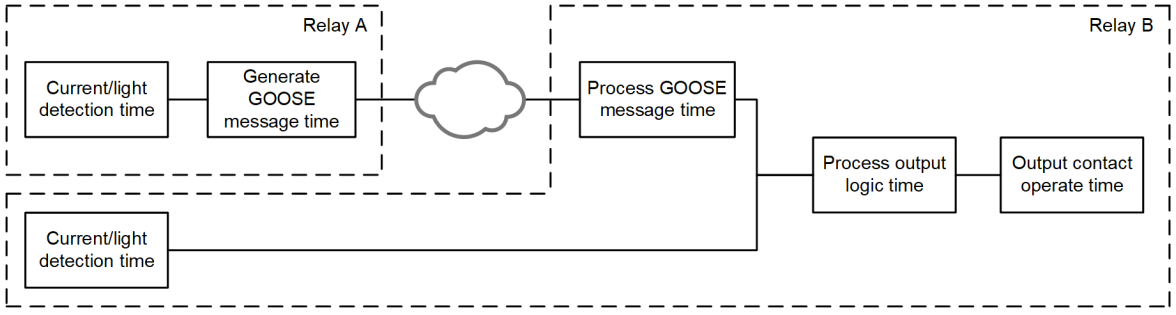

Fig. 2 Time components for arc-flash trip incorporating communications

TABLE II COMMUNICATIONS TEST RESULTS – LIGHT DETECTION GOOSE

Test Results	Min. (ms)	Mean (ms)	Max. (ms)	Std. Dev. (ms)
Light Pickup – Internal	4	5.02	6	0.26
Current Pickup – Internal	2	3.91	7	1.52
GOOSE Receive – Test Equipment	7.2	8.88	11.4	1.36
GOOSE Receive – Internal	7	11.53	16	2.21
Trip – Test Equipment	8.0	10.55	13.8	1.48

TABLE III COMMUNICATIONS TEST RESULTS – CURRENT DETECTION GOOSE

Test Results	Min. (ms)	Mean (ms)	Max. (ms)	Std. Dev. (ms)
Light Pickup – Internal	4	5.02	6	0.26
Current Pickup – Internal	2	3.91	7	1.52
GOOSE Receive – Test Equipment	4.4	8.01	13.1	2.04
GOOSE Receive – Internal	5	10.31	16	2.56
Trip – Test Equipment	6.2	9.66	13.8	2.08

V. LOGIC IMPACT

The complexity of the arc-flash design, which may result in the need for logic to implement the system requirements, can impact the trip time. The test devices used in this paper utilize two different processing rates. The protection processing in the device uses a 1/4-power-cycle processing time. The arc-flash elements use a 1/16-power-cycle processing, which includes the output logic.

Whether it is due to complexity or unfamiliarity with the device, certain end users are using standard logic in their designs. In this case, the design will have a mixture of elements being processed at different rates. Fig. 3 illustrates the component times that determine the trip time when the system includes components with different processing times. How different processing times impact the overall trip time has not been well-documented.

To simplify the testing, only Relay A and Relay C were used. The test results for assessing the impact of using standard logic are shown in Table IV.

TABLE IV STANDARD LOGIC TEST RESULTS

Test Results	Min. (ms)	Mean (ms)	Max. (ms)	Std. Dev. (ms)
Light Pickup – Internal	4	5	6	0.24
Current Pickup – Internal	2	3.91	7	1.52
GOOSE Receive – Test Equipment	4.5	7.95	13.2	2.12
Logic Processed – Internal	5	10.42	18	2.62
Trip – Test Equipment	7.5	13.03	20.1	2.63

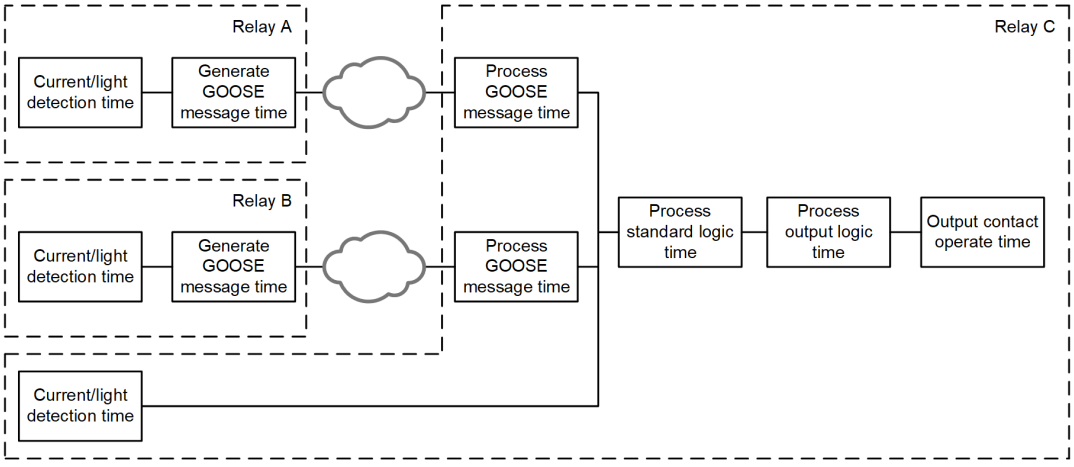

Fig. 3 Time components for arc-flash trip incorporating standard logic

VI. Design Summary

The solutions presented to address design complexity requirements had an impact on the trip time, which can be seen in Table V.

TABLE V Test Trip Time Summary

Test Results	Min. (ms)	Mean (ms)	Max. (ms)	Std. Dev. (ms)
Base Level Trip Time	4.9	5.21	6.3	0.48
Communication Trip Time	6.2	9.66	13.8	2.08
Logic and Communication				
Trip Time	7.5	13.03	20.1	2.63

VII. Complex System Design

A. Background

A Queensland power station recently completed a switchboard protection system upgrade. As part of the upgrade, the power station operator required the protection system to incorporate arc-flash protection. As shown in Fig. 4, this switchboard consists of three bus sections: A, B, and C.

The switchboard configurations mean that for an arc-flash event in either Bus Section A or C, current can be supplied by either the incomer connected to that bus section or via the respective bus tie. Bus Section B is more complicated, given that it has a backup generator and four interconnectors, all of which can supply fault current to an arc-flash event.

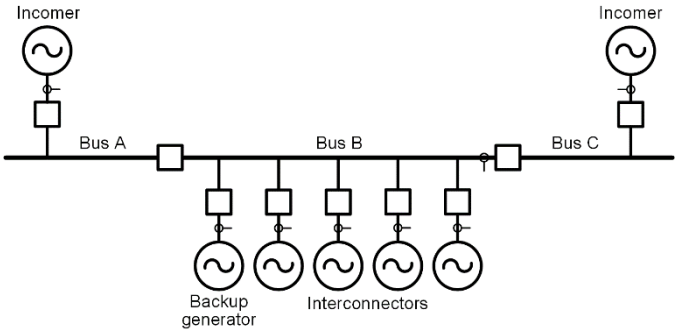

Fig. 4 Switchboard source connections

To make the maintenance easy on this switchboard and avoid any nuisance tripping, each bus section has its own arc-flash enable/disable switches. This means that Bus Sections A, B, and C can be in test modes independently. This adds to the complexity of the arc-flash protection as every trip decision has to check an extra enabled/disabled input. To add to the complexity, even if the arc flash is disabled, a test trip output is required to operate so that maintenance testing on arc-flash protection can be performed.

B. Arc-Flash Protection for Buses A and C

Both bus sections have a common complexity due to the two possibilities for the current check. The light sensors are connected to the relay located at the incomer. As part of the design and implementation, there was a change to the arc-flash functional design.

1) Initial Design

The arc-flash system was designed such that the incomer relay is responsible for:

a. Measuring the incomer circuit current.
b. Detecting all light in the associated bus section.
c. Tripping the incomer circuit breaker (CB).
d. Sending a trip signal to the bus-tie relay via GOOSE.

The bus-tie relay is responsible for:

a. Measuring the bus-tie circuit current.
b. Sending the bus-tie current check to the incomer relay via GOOSE.
c. Tripping the bus-tie CB.

The interaction between the two relays can be seen in Fig. 5.

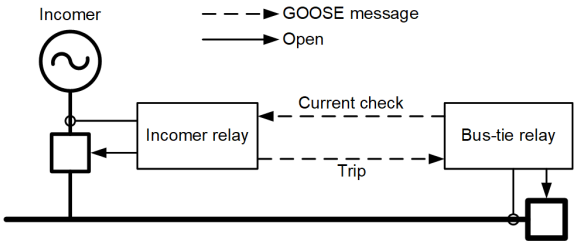

Fig. 5 Bus Section A and C signal diagram

There are two operating conditions: the bus section is supplied either by the incomer or via the bus tie. When the supply is via the incomer and there is an arc-flash event, then the incomer relay determines that there is both light and current and opens the incomer breaker and bus-tie breaker with two fast outputs. The relay then sends a GOOSE message to the bus-tie relay to open the bus-tie CB.

When the bus section is supplied by the bus tie and an arc-flash event occurs, the bus-tie relay sends the current check to the incomer relay. The incomer relay then determines that both light and current have been met. It then sends a GOOSE message to the bus-tie relay to open the bus-tie CB.

2) Design Modification

To decrease the trip time of the bus tie when light is detected by the incomer and current is detected by the bus-tie CB, a fast output of the incomer relay was configured for light detection and connected in series with a fast bus-tie relay output configured for phase or neutral current pickup, as shown in Fig. 6. This eliminates the reliance of tie breaker trip on GOOSE altogether and any time delays associated with GOOSE communications.

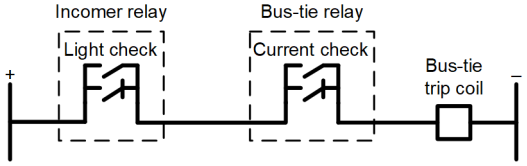

Fig. 6 Bus-tie arc-flash trip circuit

Simplifying the arc-flash design for this system configuration removes the time associated with the GOOSE messaging. The original system required two GOOSE transmissions. The final system has the same performance as a single relay application.

C. Arc-Flash Protection for Bus B

Bus B has the most complex design. The complexity is driven by seven possible fault current sources. Arc-flash protection needs to accommodate various switchboard configuration scenarios, considering 14 possible current pickup elements and many possible light detection elements.

The main complexity in the design has to do with incorporating the remote end relay for each interconnector into the arc-flash system. The final arc-flash design due to the remote relays requires the use of MIRRORED BITS protocol. The timing impact of this is not explored in this paper.

1) Initial Design

The overall arc-flash protection architecture includes a single relay not associated with any particular bay. This relay is the logic engine for all possible arrangements. The main relay receives all the current check and light information and determines if a trip is required. It then sends out the required trip signals.

The bus-tie bays have a relay, as discussed previously. Each interconnector and emergency generator panel has a relay. The relays associated with an interconnector incorporate both light and current detection. The interactions between each relay can be seen in Fig. 7. To simplify the drawing, only one interconnector is shown.

1) Design Modification

The worst-case scenario was identified when an arc-flash event occurred in the Bus B interconnector cable compartment. In this case, the local interconnector relay detected light, but current was not detected. The interconnector remote arc-flash relay picked up current and transmitted the current pickup element via MIRRORED BITS to the local interconnector relay, which transmitted this current pickup element via GOOSE to the master arc-flash relay. Then, the master arc-flash relay decided to trip since both current and light checks were high. The trip was transmitted to the interconnector local relay for it to then transmit it to the interconnector remote relay, which isolated the fault via the fast output.

To reduce this time, the arc-flash sensor from the CB compartment of interconnectors was moved to the cable compartment of interconnectors and a local zone between local and remote relays of the interconnector was created such that both local and remote relays send light detection and current pickup elements to each other via a MIRRORED BITS channel and a tripping decision is made in both the local and remote relays' interconnector. This achieves better tripping times.

VIII. Incident Energy Impact

The incident energy level is proportional to the protection operating time. Therefore, any impact that the design has on the tripping time has a direct impact on the incident energy level. The goal of arc-flash protection should be to detect the arc fault and isolate current in the most time-efficient manner.

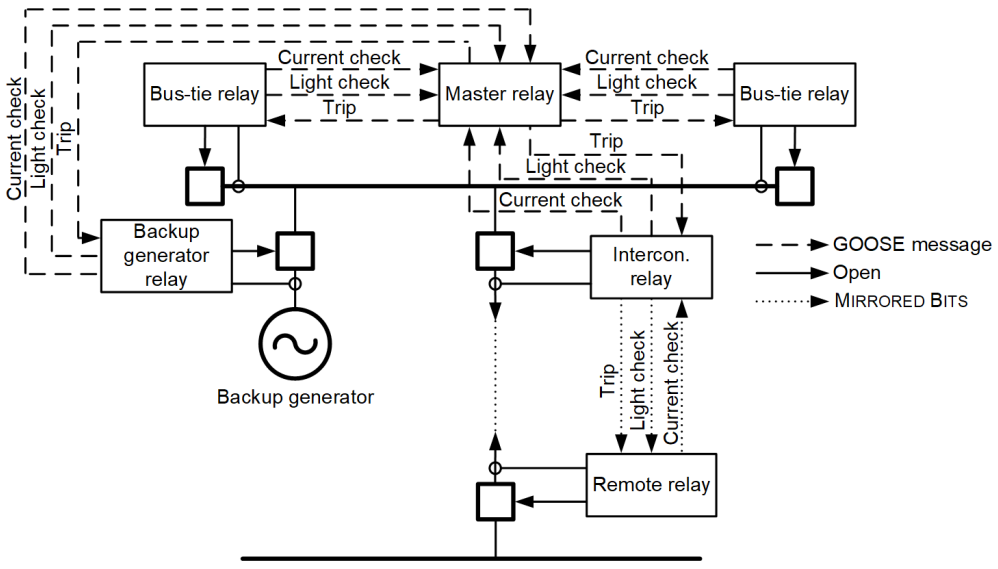

Fig. 7 Bus-tie arc-flash trip circuit

It is not always possible to reduce the complexity of the design. Understanding the impact that the design decisions have on the performance of the protection system is critical for arc flash, which this paper has discussed.

The arc-flash classification commonly adopted in the industry is based on Table 130.7(C) of NFPA 70E [1]. The incident energy level associated with each category has been summarized in Table VI. Typically, the design criterion is to achieve Category 2 or better.

NFPA 70E Annex D, Section D.4 references the equations in IEEE 1584 as the method to calculate the incident energy level [1]. The arc duration time used in these equations must include the relay operate time and the CB operate time. The other key consideration is that an arc can only be interrupted at a current zero crossing.

TABLE VI NFPA 70E ARC-FLASH PPE CATEGORIES

Category	Incident Energy Level
1	< 16.75 J/cm2
2	16.75 J/cm2 < 33.5 J/cm2
3	33.5 J/cm2 < 104.7 J/cm2
4	104.7 J/cm2 < 167.5 J/cm2

The calculation of the incident energy level has three main variables: fault current, system voltage level, and arc extinguishing time. The system voltage level was observed to have the most significant impact when the voltage level went from below 1 kV to above it. The greater the voltage, the larger the arc-fault resistance, which impacts arc-fault current. The impact on the incident energy level due to the system voltage level can be seen in the differences between the two plots in Fig. 8.

These plots have been developed using 10 ms time intervals, starting at 80 ms and going up to 260 ms. The fault current was incremented in steps of 500 A. The range of current for the plots varied to maximize the resolution to observe the impact that time has on the transition between Categories 1, 2, and 3.

As expected, the increase in fault current places more importance on the arc extinguishing time. Both plots indicate that a change in the arc extinguishing time by half a power cycle has the potential to change the category rating.

IX. CONCLUSION

In some cases, arc-flash design complexity is unavoidable, but simplicity should be a key design criterion. The practical example used for this paper demonstrates that a design can be simplified when extended trip times are identified. These simplifications have a significant impact on the operate time of the protection system.

The use of communications adds a variable delay to the relay trip time. However, the CB can only clear the fault at the zero crossing, and delay due to communications must be rounded to the next zero crossing. An additional communications delay of between 6 ms (minimum) and 13.4 ms (maximum) results in an additional fault clearance delay of between one-half to one full cycle.

The testing observed only a single transmission of data. The impact of a series of transmissions can have a greater impact on the trip time. In some cases, this cannot be avoided, as discussed for Bus Section B. Understanding the impact will result in more efficient designs and possibly drive a more simplistic approach.

Finally, designing an arc-flash protection system requires an understanding of the risks associated with incident energy. The analysis provided demonstrates that every half cycle has the potential to impact the category rating or, ultimately, to impact whether a person is exposed to an arc-flash event.

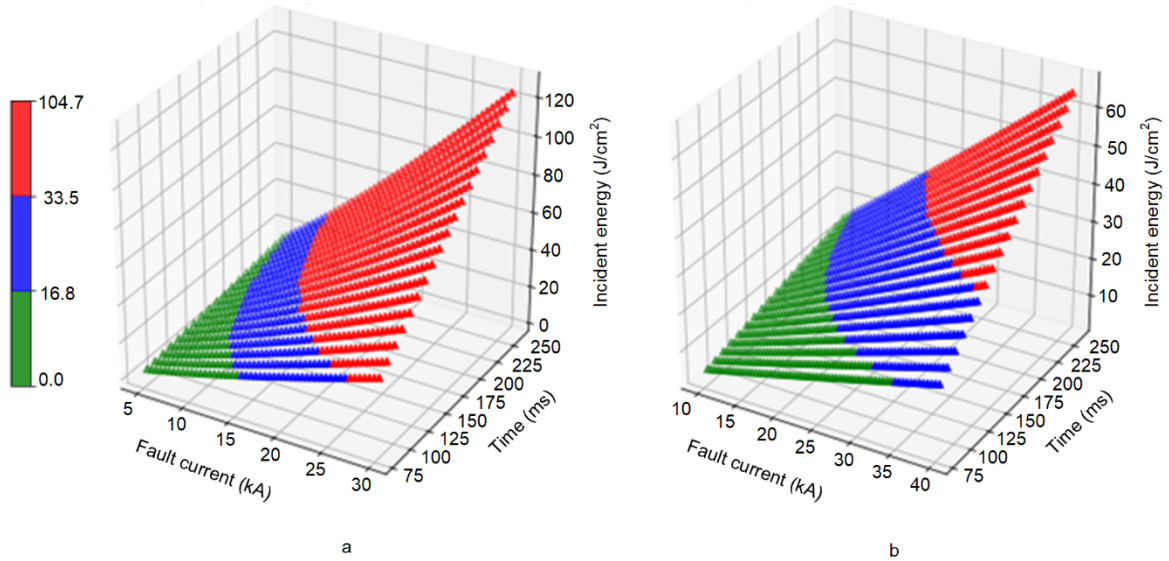

Fig. 8 Incident energy levels with system voltage less than 1 kV (a) and system voltage greater than 1 kV (b)

X. REFERENCES

[1] NFPA Standard 70E, *Standard for Electrical Safety in the Workplace®*. Available: nfpa.org.

[2] IEEE Std 1584-2002, *IEEE Guide for Performing Arc Flash Hazard Calculations*.

XI. BIOGRAPHIES

Luke Napier is a protection application engineer at Schweitzer Engineering Laboratories, Inc. (SEL). He is a chartered professional engineer (CPEng) with over 18 years of experience in the power industry. This experience included 15 years with Ergon Energy in a variety of roles, including 5 years as a protection engineer. His current role at SEL exposes Luke to protection applications in the mining and industrial electrical networks.

Qaisar Khan is an electrical engineer with passion for renewable energy resources and more than 14 years of experience in project engineering, power system design, application and technical support, technical sales, and the testing and commissioning of power generation, transmission, and distribution systems. He is currently a power system engineer at Eaton.