Effect of Stabilizing Resistance, CT Class, and MOV Maximum Clamping Voltage on High-Impedance Differential Scheme Performance

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Presented at the
50th Annual Western Protective Relay Conference
Spokane, Washington
October 10–12, 2023

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***Abstract*—High-impedance differential protection (87Z) schemes are widely used for bus protection and transformer restricted earth fault protection applications because of their security, sensitivity, and simplicity. The 87Z schemes consist of a dedicated set of current transformers (CTs) with all the secondary windings connected in parallel and terminated at a high-value stabilizing resistor. An overvoltage element measures the voltage across the stabilizing resistor. CT saturation during external faults causes lower voltage on the stabilizing resistor while internal faults cause higher voltage. It is often simple to find a voltage pickup setting between the values of the stabilizing resistor voltage during the maximum external fault and the minimum internal fault, which makes the 87Z scheme secure and dependable without sacrificing sensitivity. To limit the voltage that appears on the stabilizing resistor during internal faults, the 87Z schemes use metal-oxide varistors (MOVs) connected in parallel with the stabilizing resistor. This paper describes the design of a new 87Z relay and provides high-current test results for an 87Z scheme with different stabilizing resistance values, CT classes and ratios, and MOV clamping voltages. The test results explain the tradeoff involved in selecting the key components of the 87Z scheme, which include the stabilizing resistor, CTs, and an MOV. The paper also proposes a relay voltage pickup setting and provides a method for verifying if this setting is adequate for different applications.**

I. Introduction

High-impedance differential protection (87Z) schemes have been widely applied for decades. These schemes are preferred for their speed, security, and ease of setting and wiring, as well as the high number of breakers that can be included in the protection zone [1].

The 87Z schemes consist of a dedicated set of current transformers (CTs), one per terminal, with all the secondary windings connected in parallel and terminated at a high-value resistor, referred to as a stabilizing resistor. For external faults, the differential current provided by the parallel-connected CTs is zero if the CTs do not saturate. If CT saturation occurs for an external fault, the high impedance of the stabilizing resistor forces the current through the lower impedance path of the saturated CT. The voltage across the stabilizing resistor is very low. With this low (and easily quantifiable) voltage, the relay does not operate.

For internal faults, all the current flows through the stabilizing resistor. The resulting high voltage causes the relay to operate. This high voltage across the stabilizing resistor typically saturates all CTs. To limit the stabilizing resistor voltage for internal faults, 87Z schemes use metal-oxide varistors (MOVs) connected in parallel with the stabilizing resistor [2]. These MOVs clamp voltage for internal fault currents, and they must be considered in the design of these schemes. To prevent MOV and stabilizing resistor thermal overload, a bypass relay short-circuits the relay differential branch after the scheme trips for an internal fault.

While 87Z schemes are widely used and their principle of operation is well described in literature and understood by protection engineers, only a few publications describe the laboratory tests that evaluate the behavior of 87Z schemes for different implementation parameters.

Several 87Z application guidelines have been proposed based on theoretical analysis, test results, and field experience. In [3], the authors provide a review of 87Z protection. Reference [3] describes the performance of the CTs used in 87Z applications and shows CT and relay current waveforms captured in laboratory tests. The authors also investigate dependability for internal faults and security for external faults. Based on the test results, the authors propose guidelines for common and challenging applications. In [4], the authors discuss the potential misoperation of 87Z schemes when surge arresters are located within the relay protection zone. The relay interprets the current flowing through the surge arrester as internal fault current and may trip the bus. The authors recommend delaying the 87Z trip to allow the surge arrester to clear the overvoltage condition before tripping the bus. Adding this delay has two drawbacks: 1) the delay must be longer than the maximum surge arrester clearing time, which may be difficult to compute, and 2) the operation for internal faults is delayed for that time. In [5], the authors examine different methods for obtaining redundancy in bus 87Z schemes. Reference [5] focuses on methods of applying dual 87Z relays to an existing bus differential CT circuit. In [6], the authors present experimental results of a study about using mismatched ratio CTs in 87Z applications.

This paper describes the design of a new 87Z relay that includes phasor-based and time-domain elements to achieve high speed, security, and sensitivity. The paper also describes the high-current test results for an 87Z scheme with different stabilizing resistance values, CT classes and ratios, and MOV clamping voltages. Based on the test results, the paper provides a relay setting method. Section II describes the relay hardware design and protection algorithms. In Section III, we show the high-current test setup. In Section IV, we analyze the effect of

the stabilizing resistor value on the 87Z scheme performance. In Section V, we discuss the effect of the CT types used in the scheme. Section VI describes the effect of the MOV maximum clamping voltage. In Section VII, we propose a relay voltage pickup setting and provide a method for verifying if this setting is adequate for each particular application.

II. 87Z Relay Design

A. Relay Hardware

Fig. 1 shows a single-line diagram of the 87Z relay application to a bus with three feeders. The input signal to the relay is the differential current resulting from the parallel-connected CTs, which equals the sum of all the bus terminal currents. The relay introduces a high-value stabilizing resistor (2,000 Ω) in the differential branch of the circuit that reduces the current resulting from heavy CT saturation during external faults. An overvoltage (59) element measures a fraction of the voltage across the stabilizing resistor, which is comprised of resistors R1 and R2. It is common to have the stabilizing resistor in a voltage divider configuration to limit the voltage applied to the 59 element.

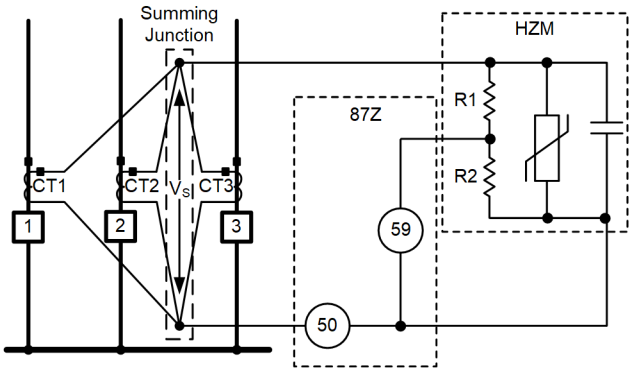

Fig. 1. Single-line diagram of the 87Z relay application to a bus with three feeders. The relay includes a high-impedance module (HZM) and a relay module (87Z).

The relay includes an MOV to limit the CT secondary circuit voltage to a safe value for internal faults. MOVs with maximum clamping voltages lower than 2 kV are typically used. The MOV used in this relay has a maximum clamping voltage of 800 V. To prevent MOV and stabilizing resistor thermal overload, the contact of a bypass relay short-circuits the stabilizing resistor and the MOV after the 87Z relay trips for an internal fault.

The relay also includes an instantaneous overcurrent (50) element, which sustains a breaker-failure initiation (BFI) signal when required [2]. When the 59 element operates and the bypass relay contact closes, the high-impedance path short-circuits and the 59 element drops out. The differential current continues to flow until all breakers successfully interrupt the fault, so the 50 element remains asserted and sustains the BFI signal. The 50 element can also improve scheme dependability by sustaining the trip condition if an MOV failure short-circuits the high-impedance path when high voltage is present. Note that while the MOV is not conducting and the bypass relay contact is open, the 59 and 50 elements operate on essentially the same quantity. We can apply equivalent pickup thresholds to both elements.

The relay comprises a high-impedance module (labeled HZM in Fig. 1) that hosts the stabilizing resistor, the MOV, and a bypass relay (not shown in the figure). A separate relay module (labeled 87Z in Fig. 1) includes the 59 and 50 elements. We use an output contact on the relay module to operate the bypass relay, which closes the contact shown in the HZM. Closing the bypass relay contact limits the energy absorbed by the stabilizing resistor and MOV by shunting current away from these components when the relay trips. The typical closing time of this contact is 2 cycles after fault inception.

B. Relay Protection Algorithms

For the protection functions, the 87Z relay uses a phasor-based algorithm and two types of time-domain algorithms. The phasor-based algorithm works on phasor quantities estimated by processing the signal samples in digital band-pass Fourier filters [7]. Time-domain algorithms work on raw signal samples. A brief description of these algorithms follows.

Algorithm 1 is the traditional phasor-based algorithm. The relay compares the magnitude of the voltage fundamental-frequency component obtained from the digital filter with a threshold value (V87Z) to determine if there is an internal fault. This approach has excellent performance when the 87Z scheme has adequately sized CTs. As shown in the test results section, when low-class CTs are used in the 87Z scheme, the band-pass filter underestimates the current magnitude, which desensitizes the 87Z relay.

Algorithm 2 uses the raw samples of the voltage signal to estimate its magnitude and compares this magnitude with a threshold value (V87Z) to determine if there is an internal fault. The signal magnitudes computed this way do not meet the general protection or metering requirements, but this method produces a better estimate of the actual signal magnitude compared to the method that uses filtered signals when low-class CTs are used.

The relay stores the voltage sampled values contained in the most recent full-cycle data window in a memory buffer and updates this information every time a new sample becomes available. The relay computes the magnitude, MAG_{RAW}, of the 87Z relay voltage by using (1) and compares it with the V87Z threshold. The main drawback of this method is that any noise in the input signal keeps the magnitude high for a full cycle until the samples are cleared from the buffer. To avoid security issues when using this method, a minimum delay of 1.25 cycle must be applied [8].

$$MAG_{RAW} = \left(\frac{Buffer_{MAX} - Buffer_{MIN}}{2\sqrt{2}} \right) \quad (1)$$

where:

$Buffer_{MAX}$ is the maximum positive sampled value contained in the data window.

$Buffer_{MIN}$ is the maximum negative sampled value contained in the data window.

Algorithm 3 is a waveshape recognition algorithm. Fig. 2 shows the logic of the waveshape recognition element. Inputs

to the logic are the raw voltage and current samples obtained from the A/D converters. The 87Z relay samples the signals at a rate of 2,400 Hz: 40 samples per cycle for 60 Hz power systems or 48 samples per cycle for 50 Hz systems. As shown in Fig. 2, the logic compares the current and voltage sampled values to corresponding positive and negative threshold values to ensure security. The binary signals resulting from these comparisons are processed through the AND and OR gates. The resulting binary quantities are stored in two 1-cycle memory buffers. The upper buffer in Fig. 2 stores a logical 1 every time the current and voltage sampled values exceed the thresholds. The bottom buffer stores a logical 1 every time the voltage sampled values exceed the thresholds. For the waveshape recognition element to issue a tripping signal, the logic requires that either both the voltage and current sampled values exceed the corresponding thresholds for a brief period of time (two entries in the top buffer in the latest cycle) or that just the voltage sampled values exceed the thresholds for twice as long (four entries in the bottom buffer). When either condition is true, the logic issues the 87ZT_TD bit. The reason for these two paths in the logic is that the voltage measurements are generally more dependable than the current measurements because the current measurements may be very low for the relay to accurately measure. For example, a V87Z threshold setting of 200 V in a scheme with a 2,000 Ω stabilizing resistor corresponds to 0.1 A, which is 2 percent of the typical 5 A relay nominal current. For this reason, we recommend using 1 A rated relays for 87Z applications even when CTs with 5 A secondary nominal current are used in the 87Z scheme.

As described in [4], surge arresters in the bus differential protection zone can potentially cause 87Z scheme misoperations. The traditional solution to avoid misoperations in these applications is to add a time delay to the tripping signal to allow the filter buffer to clear the samples from the arrester conduction. The new 87Z relay uses logic that can be enabled for in-zone arrester applications. Surge arrester conduction is a short-duration event that occurs during either the positive or negative semi-cycle of the voltage waveform. As a result, it produces unipolar current short-duration pulses (either positive or negative) in 1 cycle.

Fig. 3 shows a more comprehensive diagram of the waveshape recognition element logic including the in-zone arrester logic. The logic compares the voltage sampled values to the corresponding positive and negative threshold values. The binary signals resulting from these comparisons are stored in two 1-cycle memory buffers (one for the sampled values that exceed the positive threshold and the other for the sampled values that exceed the negative threshold). When both buffers contain at least one sampled value (indicating that the voltage pulses are bipolar), the logic issues an output bit (SATC). When the 87Z_TD bit and the SATC bit assert, the logic issues the 87ZT_WR bit. The delay introduced by waiting to verify that the differential signal is bipolar is typically around 0.5 cycle, which is much faster than using a fixed delay timer.

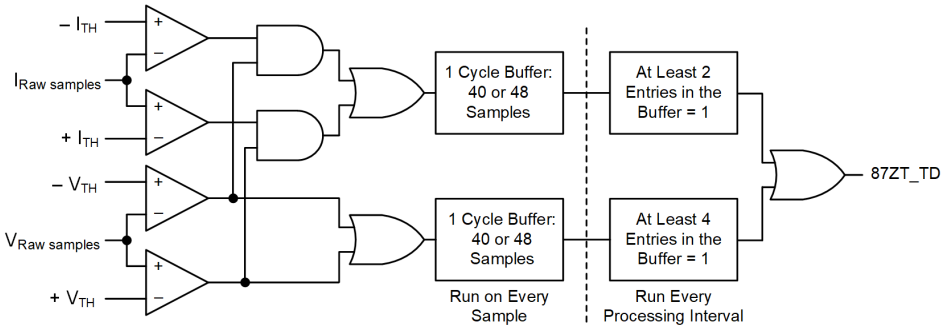

Fig. 2. Waveshape recognition element logic.

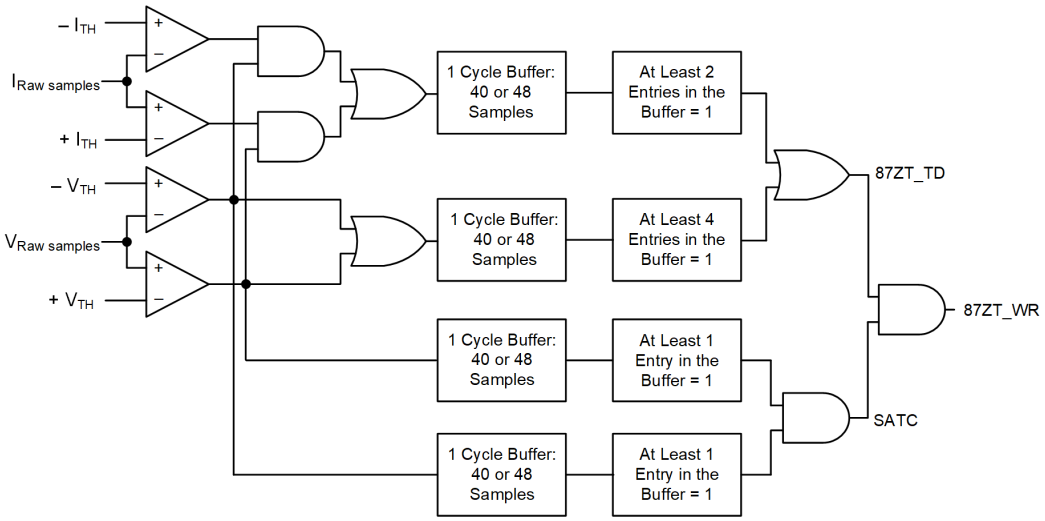

Fig. 3. The 87Z relay includes in-zone arrester logic that enables tripping when an arrester operation is not detected. This logic allows for fast 87Z tripping for internal faults while remaining secure during arrester conduction.

As shown in Fig. 4, the new 87Z relay includes three elements. One element processes band-pass filtered quantities (Algorithm 1). When this element operates, it outputs the 87ZT_F bit. The second element processes raw samples and applies Algorithm 2. When this element operates, it outputs the 87ZT_R bit. The third element processes raw samples and applies Algorithm 3 (Fig. 3). When this element operates, it outputs the 87ZT_WR bit. When any of the three elements operates, the 87Z relay logic outputs the 87ZT bit.

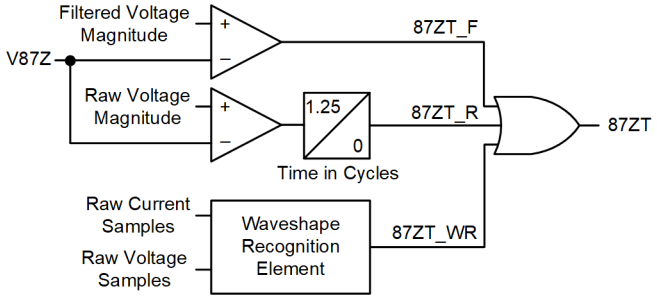

Fig. 4. The new 87Z relay includes three elements for best overall performance.

III. High-Current Tests

A. Test Setup

Fig. 5 shows the relay high-current test setup. To test the performance of an 87Z scheme for a range of stabilizing resistance values, CT classes and ratios, and MOV maximum clamping voltages, we used the test setup shown in Fig. 6, where we replaced the relay shown in Fig. 5 with externally connected stabilizing resistors and MOVs. In some of these tests, we also used the setup shown in Fig. 5. In all the tests (Fig. 5 and Fig. 6), we measured the stabilizing resistor voltage and the differential current. In the relay tests (Fig. 5), we also checked relay operation.

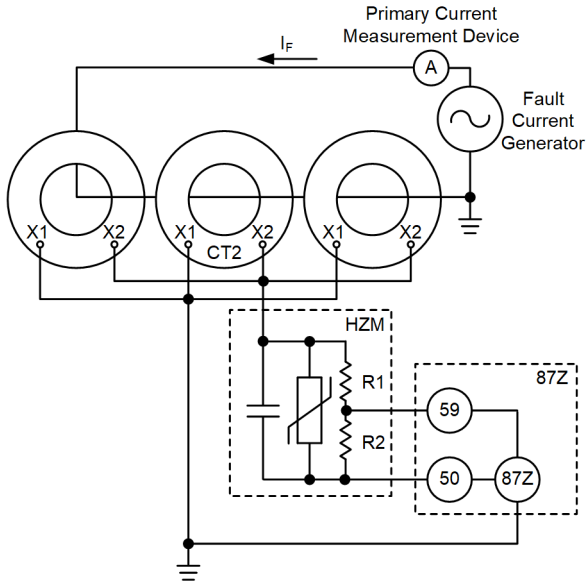

Fig. 5. Setup for testing the 87Z relay.

We connected three CTs as shown in Fig. 5 and Fig. 6 and used several types of high-current sources to inject primary currents that simulate faults. We used a 10 kVA source for low fault current tests and three parallel-connected 50 kVA sources for high fault current tests, including most of the MOV withstand capability tests. For very high fault currents, we used a test setup consisting of two parallel-connected 1 MVA, 13.2/0.48 kV transformers, connected on the high-voltage side to a 13.2 kV feeder. We applied faults on the transformer low-voltage side and connected inductors on the low-voltage side to limit the fault current.

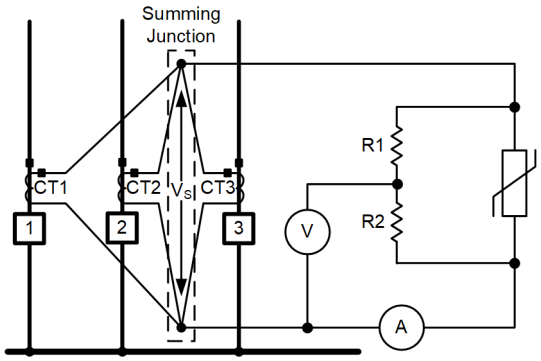

Fig. 6. Setup for testing an 87Z scheme for a range of stabilizing resistance values, CT classes and ratios, and MOV maximum clamping voltages.

B. Relay Signals for an Internal Fault

Fig. 7 depicts a relay test result for an internal fault. The top graph shows the primary fault current divided by the CT ratio (referred to as the ratio current) and the differential current measured by the 87Z relay. The bottom graph shows the voltage across the stabilizing resistor. The ratio current shows a large decaying exponential component in the primary current. We delayed closing the bypass relay contact for 4 cycles for this test. During these 4 cycles, a narrow pulse appears in the differential current after each zero crossing of the ratio current. The peak value of these pulses is 600 V. After 4 cycles, the bypass relay contact closes, diverting current away from the MOVs, and the CTs come out of saturation, as confirmed by the differential current approaching the ratio current and the stabilizing resistor voltage going to zero (the bypass relay contact closure prevents any voltage from developing across the stabilizing resistor). The result is a sequence of positive and negative voltage pulses. The fundamental-frequency component of this voltage signal is small, especially when the pulses are very narrow (in schemes that use CTs with low-accuracy class voltage, for example). As a result, relays that estimate the voltage magnitude by using band-pass digital filters may have sensitivity limitations when applied with low-accuracy class CTs.

Fig. 7 also shows that the decaying exponential current component causes the signal pulses to occur unevenly in time rather than happening every 0.5 cycle. This is because the pulses are associated with the current zero crossings, and the dc offset in the fault current shifts the zero crossings. This waveform with unevenly separated pulses further reduces the voltage magnitude estimated using band-pass digital filters.

Fig. 8 shows a zoomed-in view of one of the current and voltage pulses resulting from the internal fault applied to the 87Z scheme. The top figure shows the secondary currents of each of the CTs. The middle figure depicts the ratio and differential currents and also shows the components of the differential current flowing through the stabilizing resistor and the MOV. The bottom figure shows the voltage across the stabilizing resistor. Four regions can be identified in the figure:

- Region 1: Pre-fault condition.
- Region 2: Initial fault stage (less than 1 ms after the fault starts). The differential current flows through the stabilizing resistor, raising the voltage from 0 to about 600 V.
- Region 3: MOV conduction. The differential current flows through the parallel combination of the stabilizing resistor and the MOV. The MOV clamps the voltage. The current on the MOV keeps increasing until one of the CTs saturates.
- Region 4: CT saturation. The differential current and the stabilizing resistor voltage go to zero, where they remain until the next zero crossing of the ratio current.

As shown later in this paper, the width of the pulse is determined by the CT accuracy class voltage and the MOV clamping voltage. However, a higher differential current shortens the time when there is current flowing only through the stabilizing resistor (Region 2). In general, we can expect the duration of Region 2 to be much less than 0.5 ms.

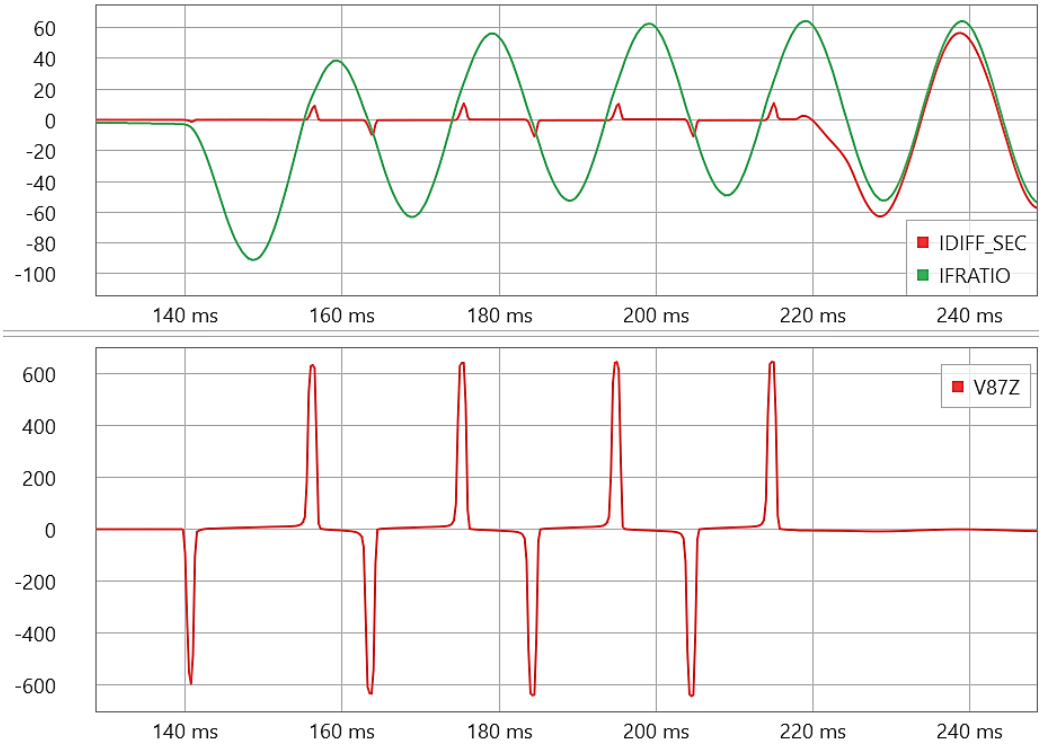

Fig. 7. Differential and ratio currents (top) and stabilizing resistor voltage (bottom) recorded by the 87Z relay during an internal fault test.

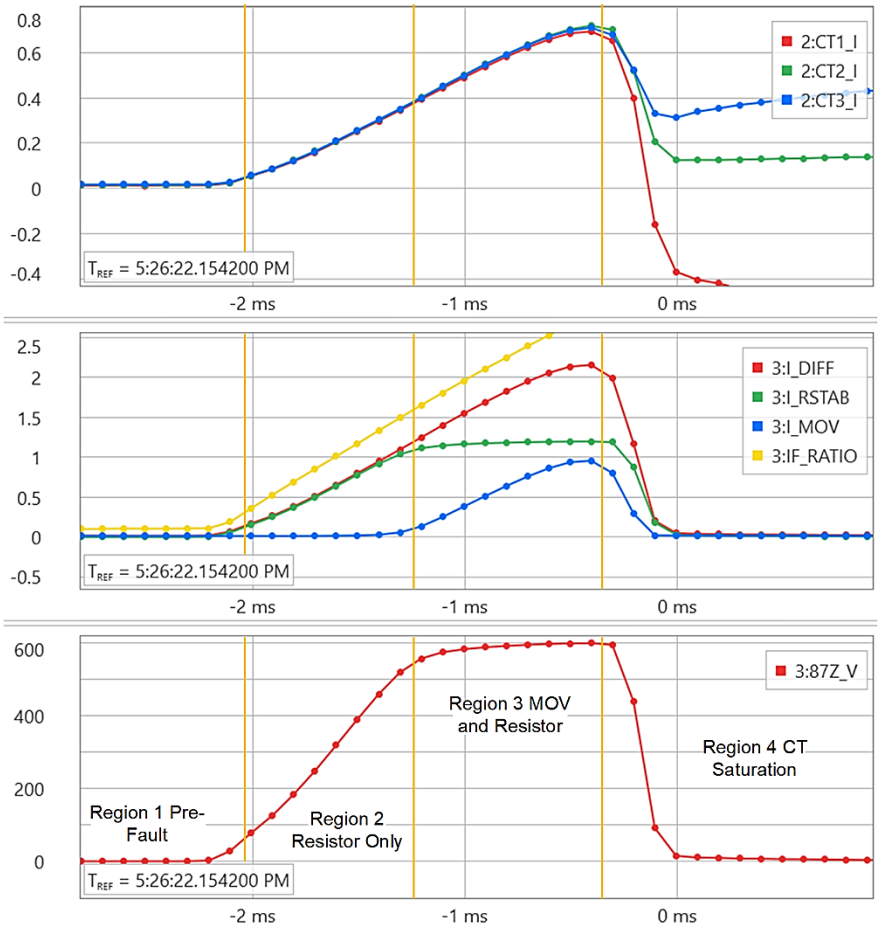

Fig. 8. Zoomed-in view of one of the current and voltage pulses recorded during an internal fault test.

IV. Effect of the Stabilizing Resistor Value

In this section, we study the effect of different stabilizing resistance values on the 87Z scheme performance. Let us consider an external fault occurring on Feeder 3 of the 87Z scheme shown in Fig. 6. In an 87Z scheme, the worst-case scenario for an external fault occurs when the CT on the faulted-branch circuit saturates completely, while the other CTs remain unsaturated. Fig. 9 illustrates this situation, where the magnetizing impedance of the fully saturated CT becomes a short circuit. The parallel connection of the unsaturated CTs delivers current equal to the total secondary fault current, I_{FS}, which divides into two components: the differential current, I_{DIFF}, which flows through the stabilizing resistor, and $I_{FS} - I_{DIFF}$, which flows through the saturated CT secondary circuit.

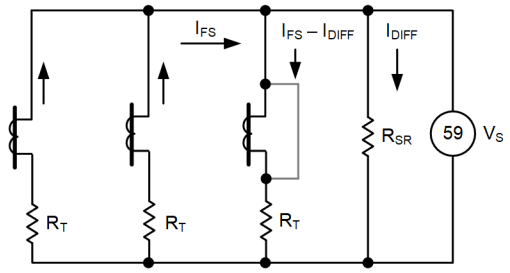

Fig. 9. Equivalent circuit of the 87Z scheme for the condition when one CT saturates completely and the other two CTs remain unsaturated.

The total resistance, R_T, of the saturated CT secondary branch is given by:

$$R_T = R_{CT} + 2R_L$$

where:

R_L is the resistance of each of the conductors connecting the summing junction with the most distant CT.

R_{CT} is the CT secondary resistance.

We calculate the differential current by applying the current divider rule:

$$I_{DIFF} = I_{FS} \frac{R_T}{R_T + R_{SR}} \quad (2)$$

where:

I_{DIFF} is the fault current in secondary amperes.

R_{SR} is the stabilizing resistance value.

Fig. 10 shows a plot of I_{DIFF} as a function of R_{SR} for different values of R_T (dashed traces) for an external fault current (I_{FS} = 100 A secondary). For the same R_T, I_{DIFF} is lower for a higher R_{SR} value, and for the same R_{SR}, I_{DIFF} is lower for a lower R_T value. Fig. 10 also shows a plot of I_{DIFF} as a function of R_{SR} for an internal fault causing a secondary fault current equal to 10 percent of a nominal CT current of 5 A (I_{DIFF} = 0.5 A). The horizontal solid line represents this I_{DIFF} value. The intersections of the I_{DIFF} internal fault line with the I_{DIFF} traces for the 100 A external fault indicate the minimum R_{SR} value needed for the internal fault current to be greater than the external fault current for a given R_T value.

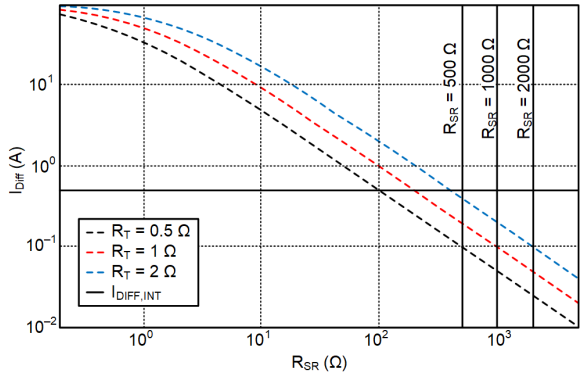

Fig. 10. Differential current as a function of the stabilizing resistance R_{SR} for an external fault current (I_{FS} = 100 A secondary) (dashed traces) and for an internal fault of 0.5 A secondary (horizontal solid line).

An overcurrent element can be set to discriminate between internal and external faults depending on the values of R_{SR} and R_T. For example, for a secondary external fault current of I_{FS} = 100 A, stabilizing resistor of R_{SR} = 1,000 Ω, and total CT branch resistance of R_T = 2 Ω, the differential current equals $I_{DIFF} \approx 0.2$ A (obtained from (2) or from Fig. 10). Therefore, setting the overcurrent element pickup greater than 0.2 A makes the scheme secure for external faults. Graphically, we can use the vertical lines corresponding to constant R_{SR} values to visually find the intervals of I_{DIFF} values below the horizontal I_{DIFF} internal fault line and above the I_{DIFF} external fault trace for a given R_T value. The overcurrent element pickup must be set to values within these current intervals.

We calculate the voltage across the stabilizing resistor, V_S, by using (3):

$$V_S = I_{DIFF} R_{SR} = I_{FS} \frac{R_T R_{SR}}{R_T + R_{SR}} \quad (3)$$

Thus, for $R_{SR} \gg R_V$, $V_S \cong I_{FS} R_T$.

Fig. 11 shows the variation of the stabilizing resistor voltage, V_S, as a function of the stabilizing resistance, R_{SR}, for an external fault current (I_{FS} = 100 A secondary) (dashed traces) and for an internal fault of 0.5 A secondary (solid trace). For example, for I_{FS} = 100 A and R_T = 0.5 Ω, V_S approaches 100 • 0.5 = 50 V as R_{SR} increases. Also, for the same R_{SR} value, V_S is higher for a higher R_T value.

In Fig. 11, the intersection of the V_S internal fault solid trace with the V_S traces for the 100 A external fault indicates the minimum R_{SR} values needed for the internal fault current to be greater than the external fault current for a given R_T value.

An overvoltage element can be set to discriminate between internal and external faults depending on the values of R_{SR} and R_T. For example, for a secondary external fault current where I_{FS} = 100 A, R_{SR} = 500 Ω, and R_T = 2 Ω, the stabilizing resistor voltage equals $V_S \approx 200$ V (obtained from (3) or from Fig. 11). Fig. 11 shows that, for the same resistance values, $V_S \approx 250$ V for the 0.5 A internal fault. Therefore, the overvoltage element pickup should be set greater than 200 V to ensure security for this external fault, and less than 250 V to ensure sensitivity to the 0.5 A internal fault. Graphically, we can use the vertical lines corresponding to constant R_{SR} values to visually find the interval of V_S values below the internal fault solid trace and above the external fault trace for a given R_T value. The overvoltage element pickup must be set to values within these voltage intervals.

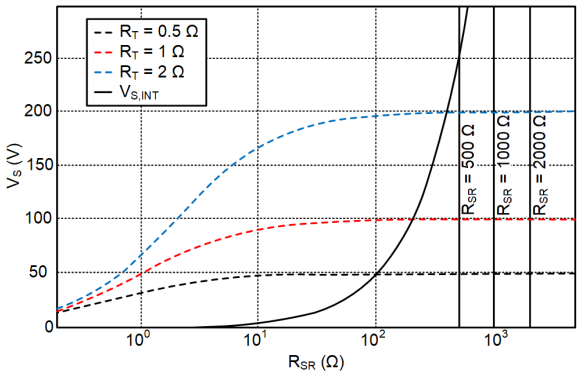

Fig. 11. Voltage across the stabilizing resistor, V_S, as a function of the stabilizing resistance, R_{SR}, for an external fault current (I_{FS} = 100 A secondary) (dashed traces) and for an internal fault of 0.5 A secondary (solid trace).

V. CT Class and Ratio Considerations

A key takeaway from testing 87Z schemes is that the CT voltage accuracy class and the MOV maximum clamping voltage strongly determine the signals measured by the relay. We conducted several high-current tests to study the effect of the CT accuracy class voltage on the 87Z scheme. We also studied the effect of using tapped CTs in the 87Z scheme.

A. Using Equal-Ratio Same Accuracy Class Voltage CTs

The common (and highly recommended) practice in 87Z schemes is to use equal-ratio same class CTs to get the best scheme performance. To study the effect of the CT accuracy class voltage on the 87Z scheme in this widely used arrangement, we conducted internal fault tests by using three sets of identical CTs. In Test Case 1, all CTs were C400. In Test Case 2, all CTs were C200. In Test Case 3, all CTs were C50. Fig. 12, Fig. 13, and Fig. 14 depict the stabilizing resistor voltages and the differential currents (in secondary amperes) measured in these tests. The measured voltage was scaled by the voltage divider ratio to get the full voltage across the stabilizing resistor.

The top graph in Fig. 12 shows the narrow, time-aligned voltage pulses resulting from heavy CT saturation; the voltage pulse peak values are equal (around 600 V) for all three CT classes. This voltage is determined by the relay MOV, which has a maximum clamping voltage of 800 V. This result shows that MOVs may start conducting at voltages less than the maximum clamping voltage [6]. On the other hand, Fig. 12 shows that the width (time duration) of the pulses depends on the CT accuracy class voltage: the higher the class, the wider the pulses (the pulse width is 6.5 ms for the C400 CTs, 3 ms for the C200 CTs, and 2 ms for the C50 CTs). The current waveforms in Fig. 12 (bottom graph) exhibit the typical CT saturation pattern: the level of saturation increases as the CT accuracy class voltage decreases.

Fig. 13 and Fig. 14 show the voltage and current magnitudes estimated using a Fourier digital filter that runs every 0.25 cycle (notice the stair-step traces). The relay underestimates the voltage and current magnitudes, which limits its sensitivity.

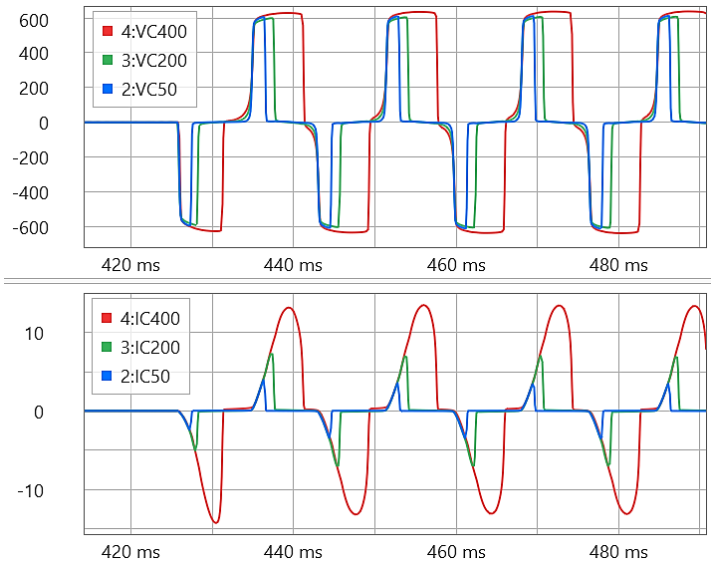

Fig. 12. Heavy CT saturation produces narrow voltage pulses and distorted current waveforms. For all three CT classes, the voltage pulses are clamped at a voltage determined by the MOV. The CT accuracy class voltage determines the width of the voltage pulses.

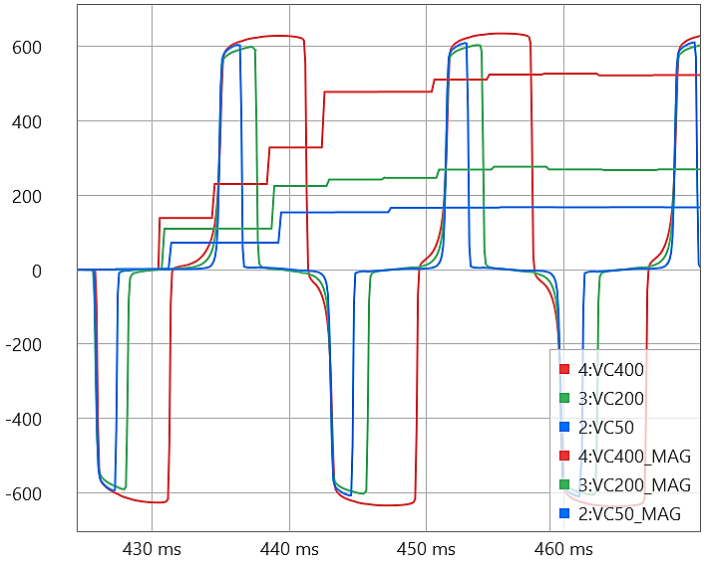

Fig. 13. The voltage magnitudes estimated by the relay digital filter are directly affected by the CT accuracy class voltage.

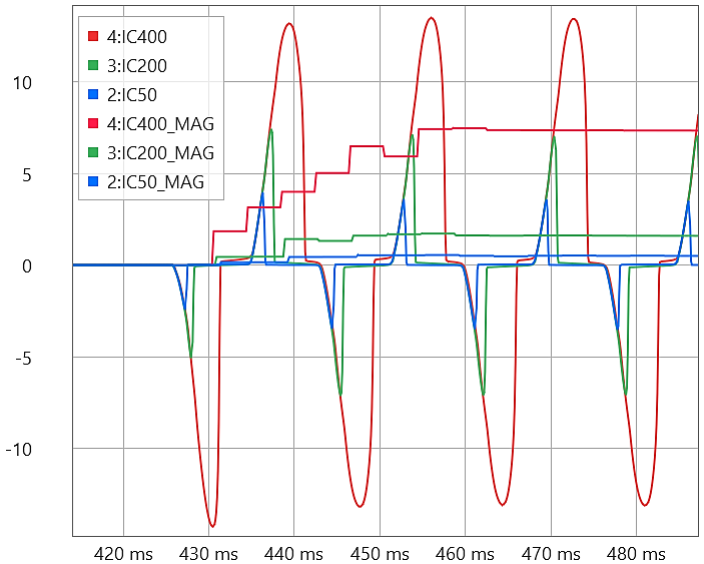

Fig. 14. The current magnitudes estimated by the relay digital filter are directly affected by the CT accuracy class voltage.

B. *Combining CTs of Different Accuracy Class Voltages and Equal Ratios in an 87Z Scheme*

Using CTs of different accuracy class voltages in a given 87Z scheme causes the voltage pulse width to reduce to that of the lowest class CT in the 87Z scheme. To confirm this concept, we conducted internal fault tests in the 87Z scheme by using three different mixes of equal-ratio C400, C200, and C50 CTs. Three tests were performed with 1,200:5 CTs. In Test Case 1, all CTs were C400. This case serves as a reference. In Test Case 2, one of the CTs was replaced by a C200 CT. In Test Case 3, one of the CTs was replaced with a C50 CT.

The top graph of Fig. 15 shows the measured differential currents and the ratio current in primary amperes. With all C400 CTs, saturation occurs after the CT current reaches the differential current peak. When C400 CTs are combined with lower accuracy class voltage CTs, saturation occurs faster (in less than 0.25 cycle). This is a high level of CT saturation.

The bottom graph of Fig. 15 shows the measured voltages across the stabilizing resistor. When lower class CTs are used in the scheme, the resulting fast CT saturation reduces the width of the voltage pulses as compared to the scheme with all C400 CTs (Fig. 12). The observed pulse widths are 6.2 ms with all C400 CTs, 2.3 ms with two C400 CTs and one C200 CT, and 1.7 ms with two C400 CTs and one C50 CT. In all test cases, the voltage pulse peak values are around 650 V.

In these tests, the pulse width reduction did not affect the sensitivity of the 87Z scheme, but these results should not be directly extrapolated to other installations.

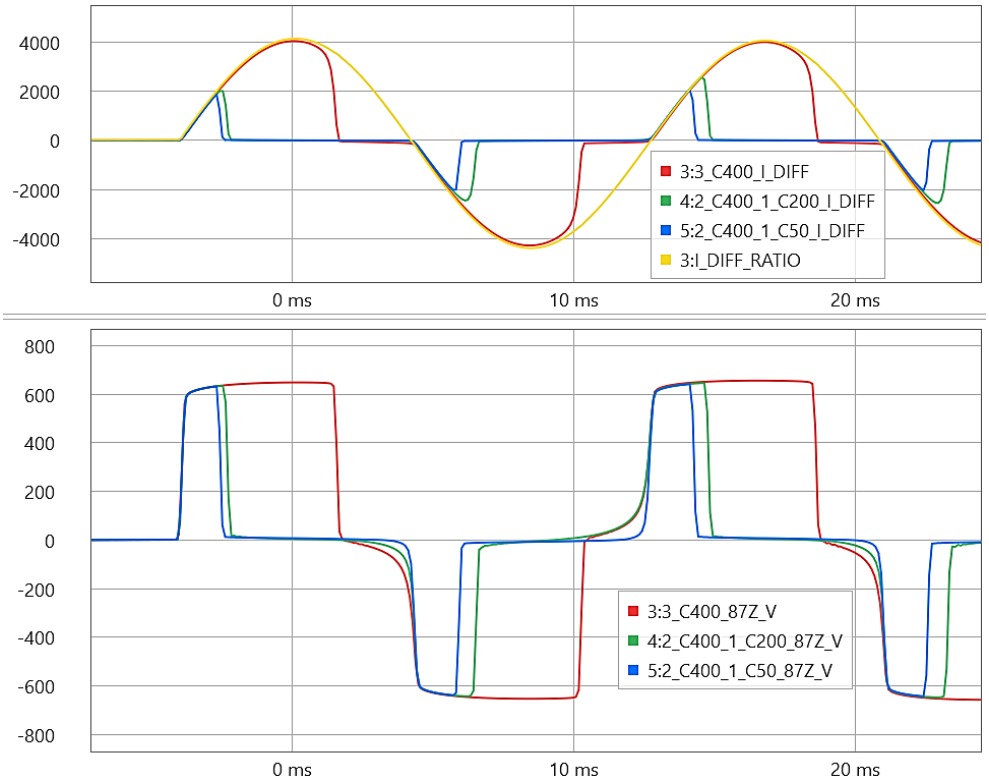

Fig. 15. Measured differential current and stabilizing resistor voltage for three 87Z schemes with equal-ratio different class CTs. The lowest class CT in the scheme determines the voltage pulse width.

C. *Paralleling Same-Class Multiratio CTs Using Equal Taps*

In multiratio CTs, the standard voltage rating applies only to the full winding. The voltage rating of a CT tap is directly proportional to the ratio between the CT ratio corresponding to the tap and the full CT ratio, provided the windings are fully distributed around the core. As an example, if a C800 3,000:5 CT is operated on a 1,200:5 tap, the accuracy rating at 1,200:5 is 320 V ([240 / 600] • 800 V = 320 V). This makes it equivalent to a C320 class CT.

To verify this concept, we performed two tests by using three identical C800 multiratio CTs. In Test Case 1, the relay HZM was connected across the 3,000:5 tap of all three CTs, as shown in Fig. 16. A current of 2,000 A was applied through each CT, which is equivalent to a primary internal fault current of 6,000 A. In Test Case 2, the HZM was connected across the 1,200:5 tap of all three CTs and the same primary fault current of 6,000 A was applied. Fig. 17 shows the differential currents (in primary amperes) and the stabilizing resistor voltages measured in these tests.

The top graph of Fig. 17 shows the measured differential currents and the ratio current in primary amperes. When we use the full range of the CT winding (3,000:5 tap), the measured differential current is very close to the ratio current after the first 0.5 cycle from the fault inception.

The bottom graph of Fig. 17 shows the measured voltages across the stabilizing resistor. When we use the 3,000:5 tap, the measured voltage is a pulse with 100 percent duty cycle. With both CTs connected at the lower tap of 1,200:5, saturation occurs and the measured differential current drops to zero after reaching a value close to the peak of the ratio current. Because of CT saturation, the pulse duration of the stabilizing resistor voltage waveform diminishes. The pulse duration is 8.2 ms for the 3,000:5 tap, and 4.7 ms for the 1,200:5 tap. In both test cases, the voltage pulse peak value was about 650 V.

Connecting the stabilizing resistor across a 1,200:5 tap of a C800 3,000:5 CT derated the CT accuracy class voltage, decreasing the voltage pulse width. This result is similar to that obtained when we studied the effect of the CT accuracy class voltage in three schemes, each having equal-class equal-ratio CTs.

Our tests also showed that the voltage pulse width for the paralleled C800 multiratio CTs that use the 1,200:5 tap is smaller than the pulse width for paralleled C400 1,200:5 fixed-ratio CTs. In our study, the measured voltage pulse width for this CT connection was about 6.2 ms.

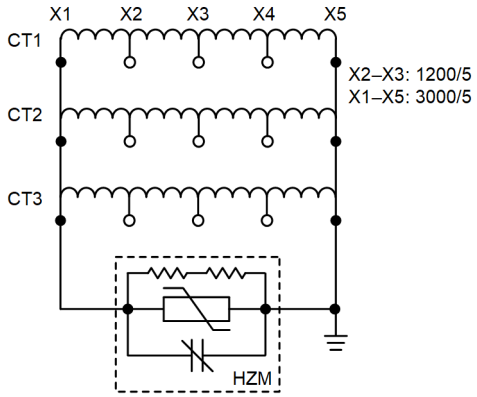

Fig. 16. Test setup to evaluate 87Z scheme performance for a scheme with same-class multiratio CTs that use equal taps.

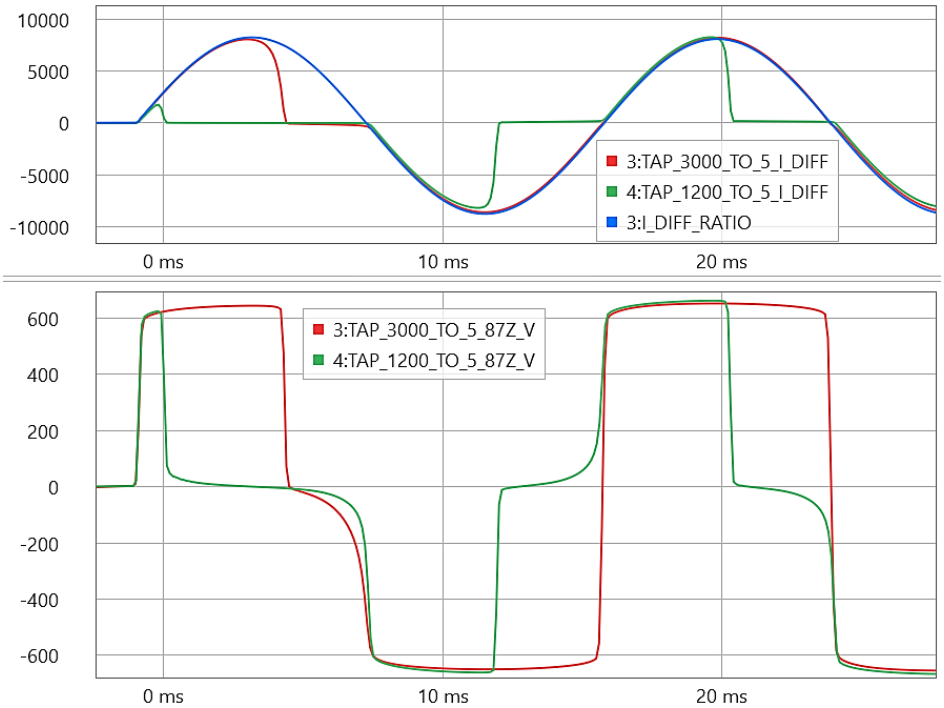

Fig. 17. Measured differential current and stabilizing resistor voltage for two 87Z schemes with multiratio CTs paralleled using the same taps. Using taps derates the CT accuracy class.

D. Combining Fixed-Ratio and Multiratio CTs

Because the 87Z scheme requires matched ratio CTs, using mismatched-ratio CTs implies using the taps of the higher-ratio CTs to match the ratios of the lower-ratio CTs. Fig. 18 depicts the setup of the tests that we performed to determine the effect of combining fixed-ratio and multiratio CTs in an 87Z scheme. In Test Case 1, we connected the relay HZM across the 1,200:5 tap of three C800 CTs. With reference to Fig. 18, CT1, CT2, and CT3 represent the 1,200:5 taps of the C800 CTs. This case serves as a reference. In Test Case 2, we replaced CT2 and CT3 with two C400 1,200:5 fixed-ratio CTs. In both tests, we applied a 6,000 A primary fault current.

Fig. 19 shows the stabilizing resistor voltages measured in the tests. When all three C800 CTs are paralleled using the 1,200:5 tap, the measured voltage pulse width is 4.7 ms. When two of the CTs are replaced with two C400 fixed-ratio CTs, the voltage pulse width diminishes to 3.4 ms. This pulse width is smaller than the 6.2 ms pulse width observed when we studied the parallel connection of three C400 equal-ratio CTs. The voltage pulse peak value was about 700 V. In these tests, we found that connecting the fixed-ratio CTs to the matching tap of a higher-ratio CT degrades 87Z performance more than paralleling equal taps of multiratio CTs or paralleling equal-ratio CTs.

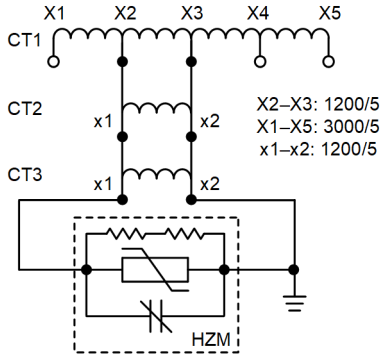

Fig. 18. Mismatched CT connection that uses the matching tap of the higher ratio CT.

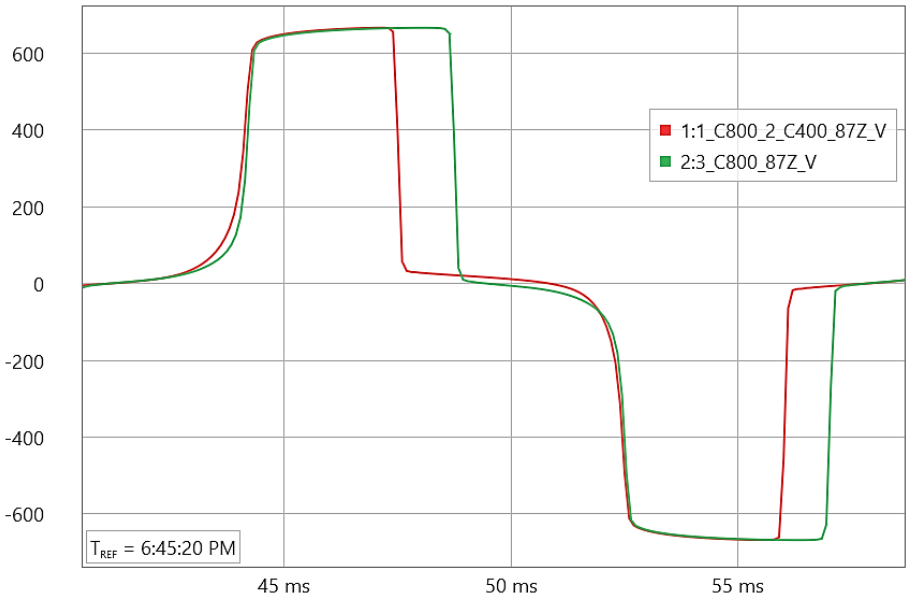

Fig. 19. Stabilizing resistor voltages measured in the tests. Connecting fixed-ratio CTs to the matching tap of a higher-ratio CT reduces the voltage pulse width.

VI. Effect of the MOV Maximum Clamping Voltage

The MOV function is to clamp the voltage to an acceptable level. Under fault conditions, large currents produce large voltages across stabilizing resistors. For this reason, MOVs are required in order to limit the secondary circuit voltage. As mentioned previously, the MOV used in the 87Z relay has a maximum clamping voltage of 800 V. In this section, we describe the tests that we performed to evaluate the effect of the MOV maximum clamping voltage on the 87Z scheme performance.

The MOV maximum clamping voltage significantly affects the voltage pulse peak value and width. Fig. 20 depicts the measured stabilizing resistor voltage in an 87Z scheme with three C400 equal-ratio CTs for two different MOV maximum clamping voltages: 800 V (MOV2) and 1,500 V (MOV1). The measured pulse peak values were 700 V for MOV2 and 1,400 V for MOV1. This result confirms that MOVs actually clamp the voltage at a lower value than the maximum clamping voltage. MOV specifications sheets typically provide for worst-case values under specific, very high-current laboratory conditions [6].

Fig. 20 shows that a lower MOV maximum clamping voltage results in a wider voltage pulse and, conversely, a higher maximum clamping voltage results in a narrower voltage pulse as required by the CT volt-time area concept [9]. Fig. 21 depicts a zoomed-in view of the measured voltage (top graph) and also the differential current waveforms (lower graph).

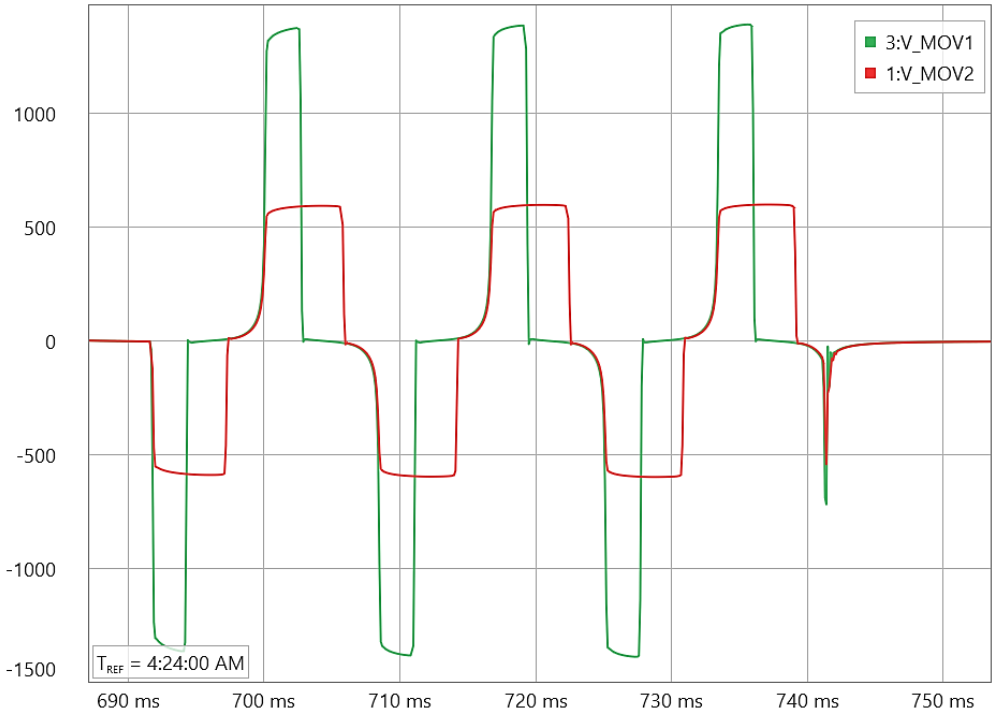

Fig. 20. Measured stabilizing resistor voltage in an 87Z scheme with three equal-ratio equal class CTs. The MOV maximum clamping voltage affects the voltage pulse peak value and width.

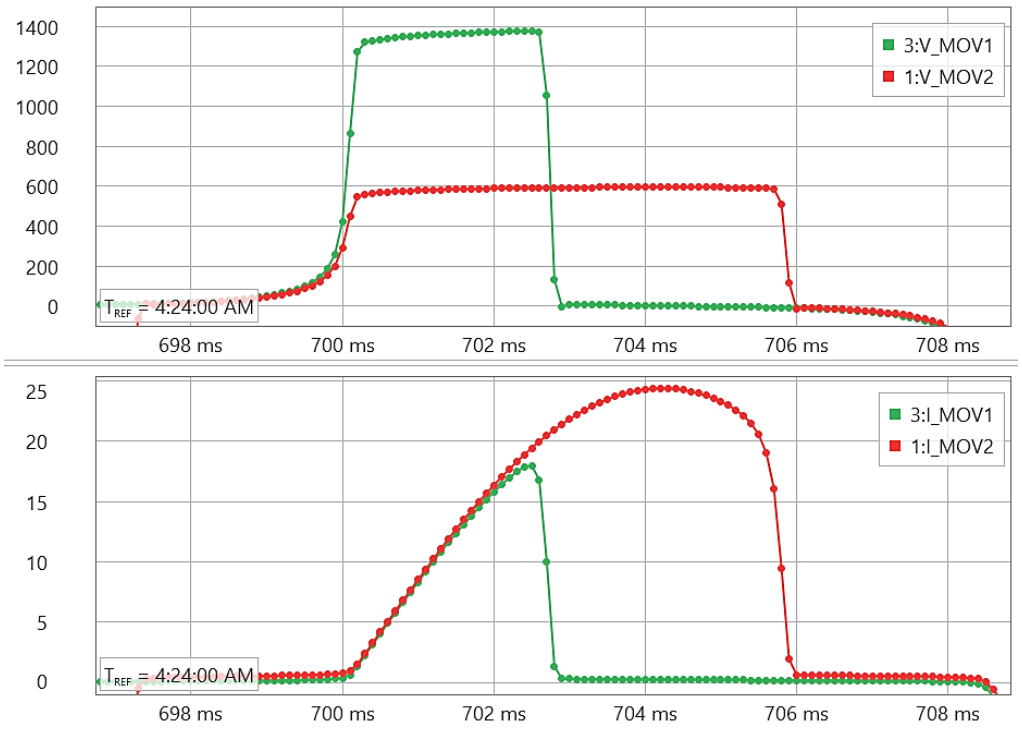

Fig. 21. Zoomed-in view of one of the Fig. 20 voltage pulses (top graph) and the corresponding differential current waveforms (lower graph).

VII. Relay Test Results and Settings

A. Relay Test Results

As explained in Section II, the new 87Z relay has a 2,000 Ω stabilizing resistor and an MOV with a maximum clamping voltage of 800 V. In the relay high-current tests, we found that a 200 V pickup setting (V87Z = 200 V) ensures satisfactory dependability for most CT accuracy classes and internal fault current levels.

B. Relay Setting Method

1. Set the relay voltage pickup to V87Z = 200 V (use the relay default setting).
2. Use (4) to verify the relay security for external faults.

$$I_{MAX} < \frac{0.8 \bullet V87Z \bullet CTR}{R_{CT} + 2 \bullet R_L} \quad (4)$$

where:

I_{MAX} is the maximum external fault current in primary amperes.

V87Z is the voltage pickup setting (V87Z = 200 V).

CTR is the CT ratio.

R_{CT} is the CT secondary resistance.

R_L is the resistance of one of the leads connecting the relay to the summing junction point.

3. Alternatively, in cases where high-class CTs (higher than C200) are used but (4) is not satisfied for V87Z = 200 V, use (5) to check security for external faults. For such cases, the CTs are expected to operate in their linear region and this condition does not result in a significant voltage across the relay stabilizing resistor for external faults.

$$I_{MAX} < \frac{V_{CT} \bullet CTR}{R_{CT} + 2 \bullet R_L} \quad (5)$$

where:

V_{CT} is 75 percent of the CT knee-point voltage.

Fig. 22 shows the maximum external fault current values for which the 87Z relay remains secure as a function of the total branch resistance R_T values for different CT classes.

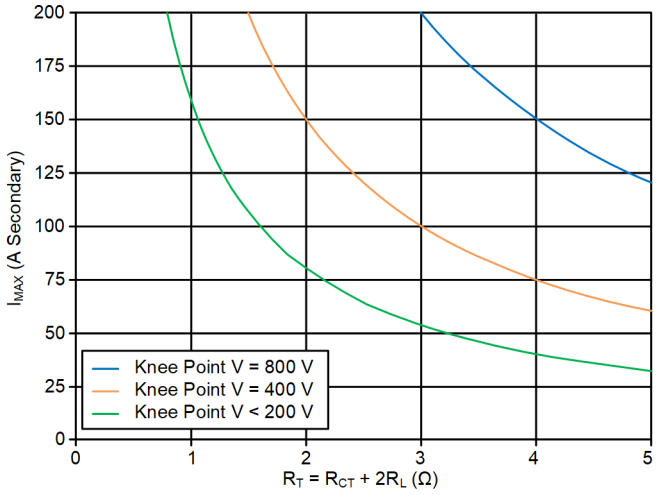

Fig. 22. Maximum external fault current for which the 87Z remains secure as a function of the total branch resistance for different CT classes.

4. Use (6) to determine the minimum fault current that is detected by the 87Z element. Equation (6) provides satisfactory results when the pickup threshold, V87Z, is set less than the knee voltage of the CTs (defined according to IEEE C37.110-2007 [10]). This is the

typical situation when the scheme CTs are C200 or better.

$$I_{MIN} = (N \bullet I_E + I_{SR} + I_{MOV}) \bullet CTR \quad (6)$$

where:

I_{MIN} is the minimum fault current in primary amperes for which the 87 element picks up.

N is the number of CTs per phase in the scheme.

I_E is the CT magnetizing current at the voltage setting V87Z.

I_{SR} is the current through the stabilizing resistor at the voltage setting (I_{SR} = V87Z / R_{SR} = 0.1 A).

I_{MOV} is the current through the MOV at the 200 V voltage setting (zero in the 87Z relay).

When the scheme CTs are of a class lower than C200, the V87Z value may be close to or higher than the knee-point voltage of the CT. In such cases, I_E cannot be reliably obtained from the CT data sheet and you should perform a primary current injection test of the CTs to obtain a more accurate estimate of the I_E value. Fig. 23 depicts an example test setup for an 87Z scheme with two CTs.

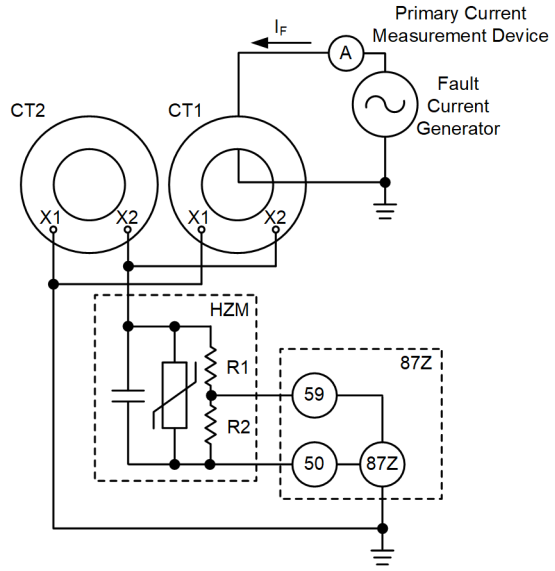

Fig. 23. Test setup to experimentally determine the magnetizing current of the CTs at the 87Z setpoint voltage.

Using this setup, you can experimentally determine the I_E value to use for applying (6). The procedure is the following:

1. Inject current through one CT and find the minimum primary current for which the 87Z element picks up. This is the I_{MIN} measured current, I_{MIN_M}. The current to inject should be equal to or lower than the minimum internal fault current expected in your 87Z scheme.
2. Use I_{MIN_M} in (7) to calculate the I_E value for a single CT. This is the calculated I_E value, I_{E_C}.
3. Use the calculated I_{E_C} value in (6) to find I_{MIN}.

If the relay does not pick up in this test, the relay will not be sensitive enough to detect the minimum internal fault expected in your 87Z scheme.

$$I_{E\_C} = \frac{1}{2}\left(\frac{I_{MIN\_M}}{CTR} - \frac{V87Z}{R_{SR}}\right) \quad (7)$$

For example, Fig. 24 depicts the magnetization characteristic of a C50 400:5 CT and shows a horizontal line representing the 200 V pickup setting. In this case, it is not possible to determine an I_E value by using the magnetizing characteristics of these CTs because there is no intersection between the V87Z horizontal line and the CT characteristic. This represents an I_E value greater than 10 A. With two C50 400:5 CTs in the circuit, as shown in Fig. 23, we found that for V87Z = 200 V, the 87Z relay tripped for an internal fault current of 76 A primary (I_{MIN_M} = 76 A). Using (7), we obtained an I_E value of 0.43 A (I_{E_C} = 0.43 A).

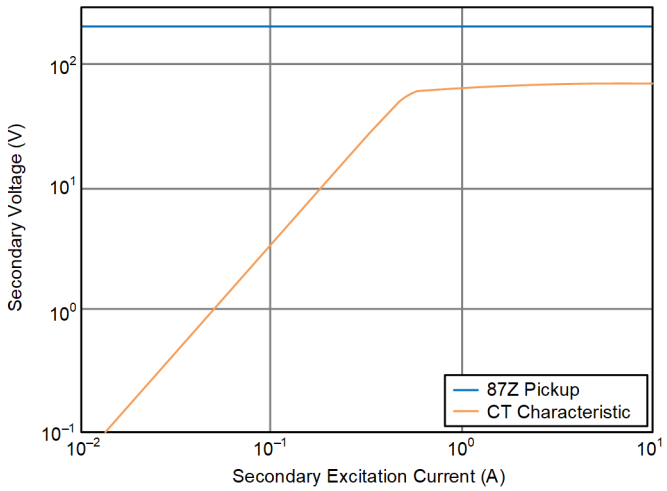

Fig. 24. Magnetization characteristic of a C50 400:5 CT and horizontal line representing the V87Z = 200 V relay pickup. The horizontal line does not intersect the CT characteristic.

To verify that the I_E value obtained from the test is accurate, we first used (6) to calculate the minimum internal fault current for a bus with seven feeders and I_{E_C} = 0.43 A. This calculation indicated that the 87Z relay should pick up for a minimum internal fault current of 250 A (I_{MIN} = 250 A). Then, we set up a seven-CT test and found that the 87Z relay dependably tripped for an internal fault current of 260 A, which closely aligns with the calculation.

The minimum internal fault current value obtained from the testing procedure explained previously is used mainly to gauge the sensitivity of the 87Z relay. In addition, this minimum internal fault current value provides the following application-specific benefits:

- Defines the maximum possible voltage pickup setting value for the open CT detection logic. The 87Z relay trips the bus if the load current on the feeder with the open CT becomes higher than the minimum internal fault current. The voltage pickup of the open CT detection logic should be set less than this minimum internal fault current multiplied by the stabilizing resistance.
- Defines the maximum allowed load current that a tapped load such as an auxiliary transformer can draw inside the bus differential zone.

- Defines the maximum primary current that will not cause an 87Z relay operation for a secondary fault on an auxiliary transformer or a VT secondary circuit inside the bus differential zone.

VIII. Conclusion

This paper describes the design of a new 87Z relay that includes a phasor-based element and two time-domain elements. The relay includes an in-zone arrester logic that improves the 87Z operation speed compared to using a fixed delay to ride through filter delays. The paper shows and discusses the results of high-current 87Z scheme testing for a range of stabilizing resistance values, CT classes and ratios, and MOV clamping voltages. The results of these tests explain the tradeoff involved in selecting these key components of an 87Z scheme.

The conclusions can be summarized as follows:

- The new 87Z relay has the following characteristics:
  - Includes a 2,000 Ω stabilizing resistor and an MOV with a maximum clamping voltage of 800 V.
  - Consists of three elements. One element compares the voltage magnitude obtained from a digital band-pass filter with a threshold value. The second element uses the raw samples of the voltage signal to estimate its magnitude and compares this magnitude with a threshold value. The third element uses the raw samples to apply a waveshape recognition algorithm. This element includes an in-zone arrester logic that improves the 87Z operation speed.
- In the 87Z relay high-current tests, we found that a 200 V pickup setting ensures satisfactory security and dependability for most CT accuracy classes and internal fault current levels. The paper provides a method for verifying if this setting is adequate for each particular application.
- In the 87Z scheme high-current tests, we found the following:
  - For high-current internal faults, the voltage across the stabilizing resistor consists of narrow pulses. The CT accuracy class voltage determines the time duration (width) of these pulses, and the MOV clamping voltage determines the pulse peak value and width.
  - Using CTs of different classes in a given 87Z scheme causes the voltage pulse width to reduce to that of the lowest class CT in the 87Z scheme.
  - Because the 87Z requires matched-ratio CTs, using mismatched-ratio CTs implies using taps of the higher-ratio CTs to match the ratios of the lower-ratio CTs. In our tests, we found that connecting fixed-ratio CTs to the matching tap of a higher-ratio CT degrades 87Z performance more than paralleling equal taps of multiratio CTs or paralleling equal-ratio CTs.

IX. References

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X. Biographies

Jay Hartshorn graduated from University of Idaho in 2013 with a B.S. in Electrical Engineering. He joined Schweitzer Engineering Laboratories, Inc. in 2016 and presently holds the title of lead power engineer in the Industrial and Rotating Machinery group. He holds several patents related to power system protection.

Josh LaBlanc received his B.S. of Electrical Engineering from the University of North Dakota in 2011. Upon graduating, he served two years as a power systems engineer for an oil and gas pipeline company, Enbridge Energy. The next four years, he worked as a relay and maintenance engineer at Minnesota Power. Josh joined Schweitzer Engineering Laboratories, Inc. in January 2018 as an application engineer. He is a registered professional engineer in the state of Minnesota.

Yusuf Zafer Korkmaz received his B.S. in electrical and electronics engineering from the Middle East Technical University, Ankara, Turkey, in 1995. He worked on protection and control schemes, substation automation and telemetry systems, and generator autosynchronization systems before he joined Schweitzer Engineering Laboratories, Inc. (SEL) in 2013.

Marcos Donolo (S 1999, M 2006, SM 2013) received his B.S.E.E. from Universidad Nacional de Río Cuarto, Argentina (2000), and received his MS degree in electrical engineering (2002), his M.S. degree in mathematics (2005), and his Ph.D in electrical engineering (2006) from the Virginia Polytechnic Institute and State University. Since 2006, he has been with Schweitzer Engineering Laboratories, Inc. (SEL), where he is presently a principal engineer. He holds several patents and has authored numerous papers related to power system protection.

Michael J. Thompson received his B.S., magna cum laude, from Bradley University in 1981 and an M.B.A. from Eastern Illinois University in 1991. Upon graduating, he served nearly 15 years at Central Illinois Public Service (now AMEREN). Prior to joining Schweitzer Engineering Laboratories, Inc. (SEL) in 2001, he worked at Basler Electric. He is presently a Distinguished Engineer at SEL Engineering Services, Inc. He is a senior member of the IEEE, Chair of the IEEE PES Power System Relaying and Control Committee, past chairman of the Substation Protection Subcommittee of the PSRC and received the Standards Medallion from the IEEE Standards Association in 2016. He is also a subject matter expert advising the System Protection and Control Working Group of the North American Electric Reliability Corporation. Michael is a registered professional engineer in six jurisdictions, was a contributor to the reference book, Modern Solutions for the Protection Control and Monitoring of Electric Power Systems, has published numerous technical papers and magazine articles, and holds three patents associated with power system protection and control.

Héctor J. Altuve Ferrer received his B.S.E.E. degree in 1969 from the Central University of Las Villas in Santa Clara, Cuba, and his Ph.D. degree in 1981 from Kiev Polytechnic Institute in Kiev, Ukraine. From 1969 until 1993, Dr. Altuve served on the faculty of the Electrical Engineering School at the Central University of Las Villas. From 1993 to 2000, he served as professor of the Graduate Doctoral Program in the Mechanical and Electrical Engineering School at the Autonomous University of Nuevo León in Monterrey, Mexico. In 1999 through 2000, he was the Schweitzer Visiting Professor in the Department of Electrical and Computer Engineering at Washington State University. Dr. Altuve joined Schweitzer Engineering Laboratories, Inc. (SEL) in January 2001, where he is currently a distinguished engineer and dean of SEL University. He has authored and coauthored more than 100 technical papers and several books and holds four patents. His main research interests are in power system protection, control, and monitoring. Dr. Altuve is an IEEE life fellow.

David Costello is the chief sales and services officer at Schweitzer Engineering Laboratories, Inc. (SEL), where he leads the engineering services, sales and customer service, and marketing divisions in supporting customers and addressing power industry challenges with SEL technologies and solutions. After graduating from Texas A&M University with a bachelor of science in electrical engineering, David worked as a system protection engineer for companies in Texas and Oklahoma. In 1996, David joined SEL as a field application engineer and has since held roles including technical support director, regional service manager, national sales and customer service director, and senior vice president of sales and customer service. He is the author of more than 30 technical papers and 25 application guides and has received numerous recognitions, including the 2008 Walter A. Elmore Best Paper Award from the Georgia Institute of Technology Protective Relaying Conference, the 2013 Outstanding Engineer Award from the Central Texas section of the IEEE Power and Energy Society, and the 2016 Best Overall Technical Presentation Award from the NETA PowerTest Conference. David completed the Utility Executive Course at the University of Idaho in 2017. He is a senior member of IEEE, a registered professional engineer in Texas and Michigan, and was a member of the planning committee for the Conference for Protective Relay Engineers at Texas A&M University for over 20 years.