Starting Large High-Inertia Synchronous Motors With Improved Field Application Relay Methods That Compensate for the Field Breaker Closing Time and Noisy Field Voltage Signals

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***Abstract*—To start a synchronous motor by using the induction starting method, direct current (DC) excitation must be applied to the field winding at an appropriate instant to synchronize the motor. This is done by closing the field breaker to connect the field winding to a DC source and simultaneously disconnecting a resistor connected across the field winding. Information about the ratio of rotation speed to synchronous speed (slip) and the orientation of the rotor with respect to the stator rotating magnetic field (rmf) is obtained by measuring the voltage across this resistor. These values are used to time the close command to the field breaker, so the rotor synchronizes with the stator rmf. Rotor synchronization can be affected by delays in field breaker closure and measurement noise in the voltage across the resistor. This paper describes a new microprocessor-based relay algorithm, used to determine the correct time to issue the field breaker close command, which takes the time needed for the breaker to close (breaker closing time) into account while rejecting noise in the field voltage measurement. Results from field tests that demonstrate the effectiveness of this new algorithm are presented.**

I. Introduction

Synchronous motors (SMs) do not develop starting torque like induction motors (IMs) do; they require special consideration and hardware to bring them up to rated speed and synchronize them to the electric grid [1]. A common procedure to start an SM is to treat it as an IM by connecting the stator terminals directly to the electric grid and the field winding to a discharge resistor, as shown in Fig. 1. Alternating currents (AC) in the stator generate a rotating magnetic field (rmf) that induces AC current in the field and damper windings in the rotor poles of the SM. The interaction between the rmf and the magnetic field generated by these two currents produces a torque, which, under normal conditions, accelerates the rotor from a standstill to near synchronous speed [2].

Once the SM reaches a preset synchronizing speed (typically, 95–98% of synchronous speed), the field breaker is closed, resulting in a direct current (DC) voltage being applied to the field winding and the discharge resistor being disconnected. The resulting DC current generates a strong magnetic field in the rotor, which, under normal conditions, brings the rotor up to synchronous speed by locking the rotor magnetic poles to those in the rmf generated by the stator currents. A Field Application Relay (FAR) is commonly used to control when the field breaker is closed. In the past, this relay was a stand-alone relay. More recently, the FAR functionality has been incorporated into existing motor protection microcontroller relays.

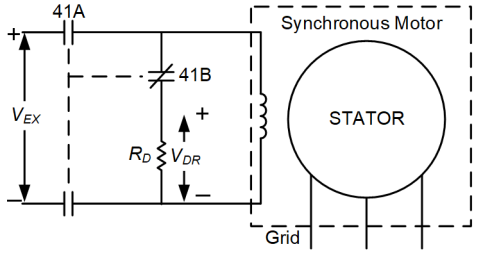

Fig. 1. Synchronous motor diagram.

An SM connected to loads with low rotating inertia (less than that of the SM) can often be started as an IM without any issue. The two main issues that arise when using this method to start SMs connected to high-inertia loads are long starting times and failure to synchronize upon closing the field breaker. Long starting times lead to longer periods of rotor heating, which can damage or reduce the life of the insulation. References [3]–[8] provide an overview of this problem and describe several ways of addressing it. In this paper, we focus on the second issue, that of failing to synchronize the rotor to the rmf.

We say the SM failed to synchronize when the rotor slips one or more magnetic poles after the DC voltage source is connected to the field winding. Slipping a pole implies that like poles (north-north and south-south) in the stator and the rotor pass in front of each other, generating a large, sudden change in the direction of the torque, which causes large forces to multiple parts of the SM.

To maximize the chances of successful synchronization, FARs aim to close the field breaker when magnetic poles of opposite polarity in the stator and rotor are aligned [9]. To this end, FARs monitor the voltage, V_{DR}, at the terminals of the discharge resistor, R_D, as shown in Fig. 1. The instantaneous value of the V_{DR} signal is related to the relative angle between the stator rmf and the rotor poles. Given the polarities in Fig. 1, the most appropriate time to energize the field winding to prevent synchronization failure is at a Positive-Going-Negative Zero Crossing (PNZC) of the V_{DR} signal.

In this paper, we show how noise in the V_{DR} signal and the time delay between the FAR close signal and actual field breaker closure caused an SM to fail to synchronize and propose methods to avoid this problem. The proposed methods lead to consistently successful motor starts and prevent damage to the equipment, which reduces repair or replacement costs.

II. Field Circuit of Synchronous Motors

In SMs, the field windings are connected to a discharge resistor, R_D, through a normally closed (41B) contact and to a DC source via a normally open (41A) contact, as shown in Fig. 1. A digital signal, 41CLOSE, issued by the FAR commands the field breaker to close, which closes the 41A contact and simultaneously opens the 41B contact (make-before-break contact).

Initially, 41CLOSE = 0 so that the field breaker is open (41A contact is open) and the field winding is connected to the field discharge resistor (41B contact is closed). When the SM is started, a voltage, V_{DR}, is developed across the discharge resistor, R_D. The FAR extracts information from the V_{DR} signal to determine the moment to apply DC excitation. The DC excitation, V_{EX}, is applied by closing the field breaker by setting 41CLOSE = 1. Thus, excitation is applied to lock the stator and field poles into synchronism and the discharge resistor is switched out of the field circuit.

Instead of directly measuring the V_{DR} signal indicated in Fig. 1, we use a resistive voltage divider to step the voltage down; this stepped-down voltage is provided as an input to the FAR, as shown in Fig. 2. Fig. 3 shows the V_{DR} signal during an SM start.

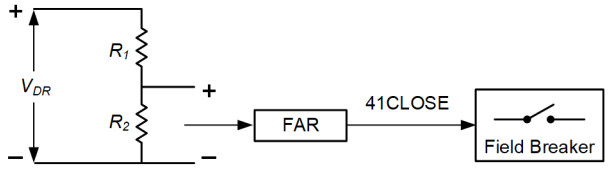

Fig. 2. Field application relay (FAR) input and output.

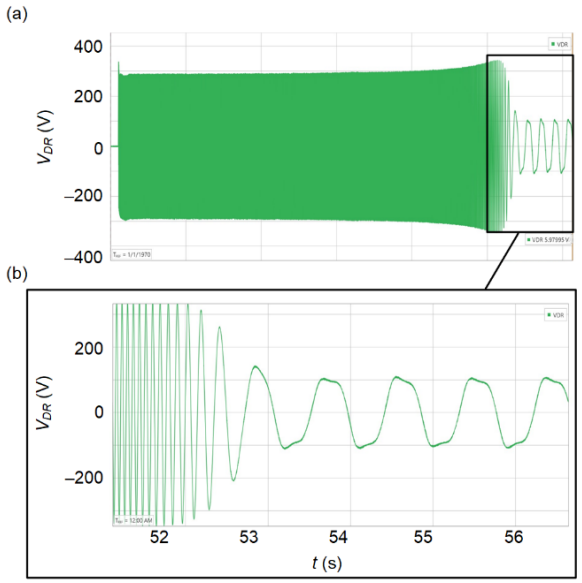

Fig. 3. V_{DR} signal during SM start (a) and a zoomed-in view of the final few seconds before application of DC excitation (b).

In Section III, we simulate an SM under various starting conditions to identify timing options when the field breaker may safely close and maximize the probability of a successful motor synchronization.

III. Region of Synchronization

We performed a series of simulations to identify the regions of synchronization of the SM with different loading conditions, field voltages, and load inertias. We considered the PNZC of the V_{DR} signal as the reference of the rotor angle. Once the rotor speed reaches the synchronizing speed and stabilizes, the field voltage is applied and the discharge resistor is disconnected simultaneously at different rotor angles. The region of synchronization is defined as the range of rotor angles for which the SM successfully synchronizes, i.e., pulls into step without slipping a pole.

In these simulations, we considered the base value for load inertia as the motor inertia (135860 kgm^2) and the base value for field voltage as 130 VDC, which is the field voltage that produces unity power factor at full load. The SM parameters are shown in Table I.

TABLE I.
Synchronous Motor Data

Parameter	Value	Parameter	Value
Nominal power	10.158 MVA	X_q	0.35 pu
Nominal voltage	13.8 kV	X'_d	0.26 pu
Nominal frequency	60 Hz	X'_q	0.35 pu
Motor inertia	135860 kgm^2	X''_d	0.178 pu
Discharge resistance	12.7 Ω	X''_q	0.18 pu
Rated speed	300 RPM	T'_{d0}	3.75 s
Load torque	323.344 kNm	T''_{d0}	0.03 s
X_d	0.51 pu	T''_{q0}	0.03 s

Regions of synchronization of the SM with different loading conditions are shown in Fig. 4 and Fig. 5. Examining the results for two different field voltages, 1 pu (Fig. 4) and 1.5 pu (Fig. 5) with a constant load inertia of 4 pu, we observe that when the load is light, the synchronization window is large and includes both the PNZC and the Negative-Going-Positive Zero Crossing (NPZC). However, when the load increases, the region shrinks to a small window encompassing the PNZC. Further, we observe that the SM fails to start successfully for loads above 1.03 pu when the field voltage is 1 pu and the SM fails to start for loads above 1.06 pu when the field voltage is 1.5 pu. This leads us to conclude that for a higher field voltage, the SM is able to synchronize without slipping a pole with higher starting loads. We can also conclude that the region of synchronization expands with light loading and higher field voltage.

Variations of the synchronization window with the field voltage are shown in Fig. 6. In these simulations, the load and load inertia with their respective bases were kept constant at 1 pu and 4 pu, respectively. These results show the region of synchronization growing as the field voltage increases.

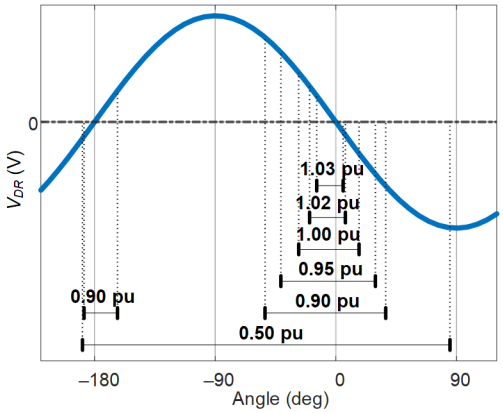

Fig. 4. Region of synchronization with different loads varied from 0.5 pu to 1.03 pu of nominal load (1 pu field voltage and 4 pu inertia).

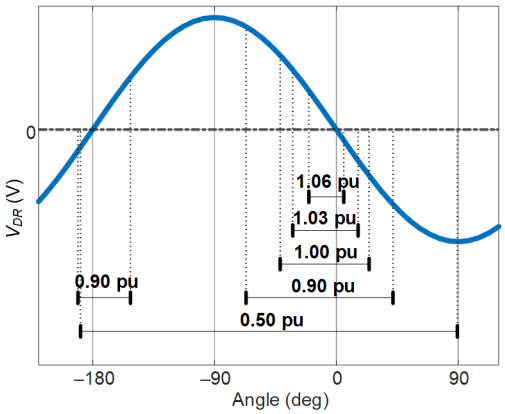

Fig. 5. Region of synchronization with different loads varied from 0.5 pu to 1.06 pu of nominal load (1.5 pu field voltage and 4 pu inertia).

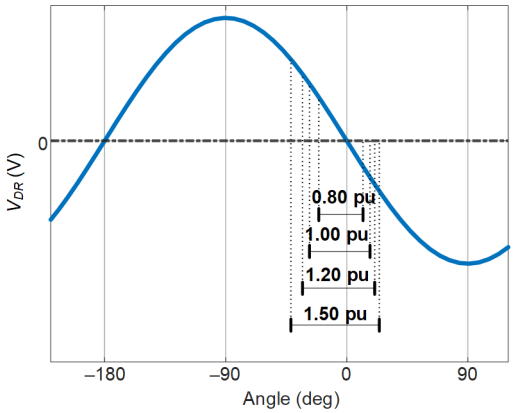

Fig. 6. Region of synchronization with different field voltages varied from 0.8 pu to 1.5 pu of nominal field voltage (1 pu load and 4 pu inertia).

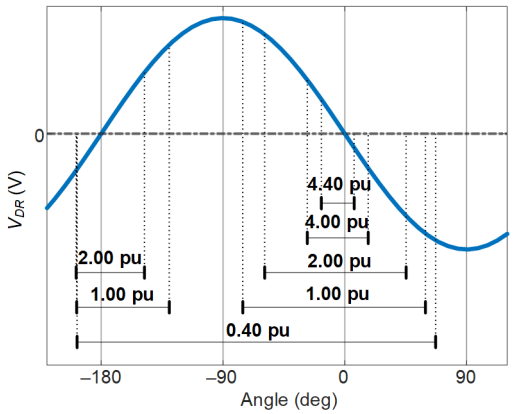

Fig. 7. Region of synchronization with different load inertias varied from 0.4 pu to 4.4 pu of motor inertia (1 pu load and 1 pu field voltage).

The effect of load inertia on the SM is shown in Fig. 7. The load and field voltage were kept constant at 1 pu with their respective bases. According to the results, the window of synchronization expands as the load inertia decreases. Further, at very low inertia, the region of synchronization includes both the PNZC and the NPZC.

From these observations, we conclude that the window of time near the PNZC is suitable for closing the field breaker, considering variations in the loading level, inertia, and applied field voltage. In Section IV, we propose an algorithm to ensure that the field breaker closes near the PNZC.

IV. Case Study

We consider an SM that drives a pump for water delivery. The parameters of the motor are shown in Table I, and the applied field voltage is 250 VDC. The FAR element in a multi-function motor protective relay controls when to close the field breaker during a motor start. The FAR element was programmed to send a close command (41CLOSE) to the field breaker at the PNZC of the V_{DR} signal after the rotor slip dropped below the synchronizing slip set to 2 percent. The SM takes approximately 60 s (starting from a standstill) to reach this slip condition. If the SM fails to synchronize within 70 s of starting, the FAR is programmed to trip the unit.

Our tests showed that the primary reason for unsuccessful synchronization was the time needed for the breaker to close (field breaker closing time): approximately 200 ms from the time 41CLOSE was set to when the 41A contact closed. In addition to the failed synchronization, the delayed closure occasionally caused excessive contact arcing (Fig. 8) when the 41B contact opening interrupted a negative field current through it.

To ensure that the breaker closes near the PNZC, the FAR should send the breaker close command in advance of the PNZC, accounting for the field breaker closing time. To implement this solution, initially a hardware solution was employed as follows: a capacitor was connected in series with the resistors in the voltage divider circuit (Fig. 9). This caused the phase of the stepped-down V_{DR} signal, which was sent to the FAR, to lead the phase of the actual V_{DR} signal by approximately 200 ms when the rotor slip reached 2 percent. Hence, the FAR sent a close command to the breaker at the PNZC of the input signal, which occurred approximately 200 ms earlier than the PNZC of the actual V_{DR} signal. This solution resulted in the breaker closing near the PNZC of the V_{DR} signal as intended.

In addition, during some motor starting tests, we observed that the SM failed to synchronize because the breaker closed prematurely as a result of the effect of noise coupling with the V_{DR} signal. An example of the noisy V_{DR} signal recorded during a motor starting test is shown in Fig. 10a. In the absence of noise, only one NPZC would have been observed at the

highlighted location and a PNZC would have occurred after another half cycle. However, the zoomed-in version in Fig. 10b shows multiple noise-induced zero crossings. Upon detecting a "false" PNZC, the FAR sent a premature close command, 41CLOSE = 1, as seen in Fig. 10a, and hence, the motor did not start successfully. Onsite personnel were able to reduce the periodic 60 Hz noise shown in the figure by better shielding the V_{DR} signal cable. However, smaller noise leading to spurious PNZCs persisted, as shown in the event report in Fig. 11a and its zoomed-in version, Fig. 11b.

Fig. 8. Contact arcing during a poorly timed field breaker closure.

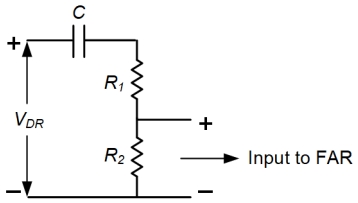

Fig. 9. Capacitor connected in the voltage divider circuit.

Using a motor protective relay allows us to pursue a software solution to control the timing of the close command and to eliminate the possibility of noise affecting the starting of the SM. A software solution is desirable because the hardware solution included additional components in the voltage divider circuit and the phase shift introduced by the hardware solution varied depending on the slip frequency. This frequency-dependent phase shift varied when the field breaker closed with respect to the PNZC of the field voltage signal. The motor was tolerant of this variation, but during some starts, large motor torque swings were noted, indicating the field breaker did not close at an optimum time.

In Section V, we set forth enhanced logic-based methods that can be used to address these issues.

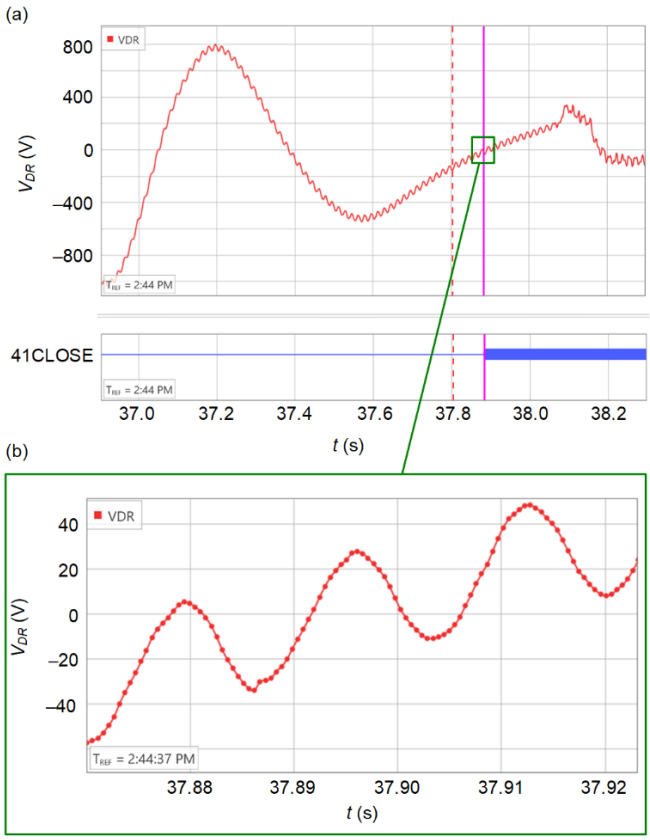

Fig. 10. Periodic 60 Hz noise in the V_{DR} signal that induces PNZCs that trigger a premature field breaker close command (a) and a zoomed-in view clearly showing the PNZCs (b).

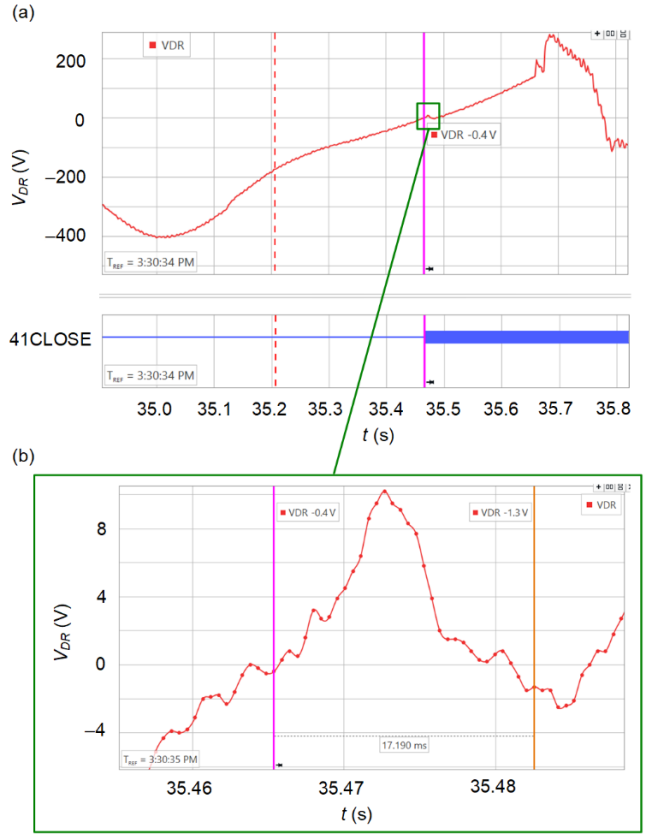

Fig. 11. Noise in the V_{DR} signal that induces PNZCs that trigger a premature field breaker closure (a) and a zoomed-in view clearly showing the PNZCs.

V. Enhanced Logic for FAR Operation

One key observation from Fig. 3 is that at the end of the induction start, the SM in this case study does not pull into synchronism but continues to slip at a near constant rate. Thus, the period of the V_{DR} signal settles over time to a constant value. We exploit this feature by having the FAR algorithm measure the period of the V_{DR} signal and predict the period of the next cycle (or the timing of the upcoming PNZC). Our objective is to issue the field breaker close command in advance of the PNZC such that the field breaker 41A contact closes near the next PNZC of the V_{DR} signal.

As shown in Fig. 12, the FAR algorithm pulses a bit, p, ($p = 1$) every time a PNZC is detected. The period is the time between consecutive pulses. Let the period of the latest complete cycle, cycle k, be T_k. The period of the previous cycle is T_{k-1}. When certain logic conditions, as described below, are satisfied, a bit, L41, pulses. The L41 pulse sets a latch, which sets its output, 41CLOSE, to 1. If the motor trips or stops, a bit, UL41, resets the latch, which forces 41CLOSE to 0.

Fig. 13 shows Logic A that tests three conditions. The condition c_1 determines if the two latest cycles have a similar period (within a tolerance defined by lower and upper preset thresholds $T_l > 0$ and $T_u > 0$). Condition c_2 determines whether the slip s has reached the preset synchronizing slip s_s. When both c_1 and c_2 are true, we conclude that the V_{DR} signal has entered the stage of near constant low frequency. Accordingly, we assume that the period of the following cycle, T_{k+1}, will be approximately equal to T_k. The final requirement to issue the L41 pulse is explained as follows.

At every PNZC, the timer is reset so $t = 0$. Thus, the next PNZC is expected to occur at time T_k. Let T_b be the breaker closing time. Then, at a time T_b before the next PNZC, i.e., at $t = T_k - T_b$, the c_3 bit should pulse, which pulses the L41 bit according to Fig. 13. For successful implementation, we had to ensure that a processing interval of the FAR algorithm falls within a time frame around $t = T_k - T_b$ and accordingly set parameters T_{d1} and T_{d2}. Condition c_3 compares the present time t to the target time frame defined by these parameters. The requirement that $T_k > T_b - T_{d2}$ also follows from this condition.

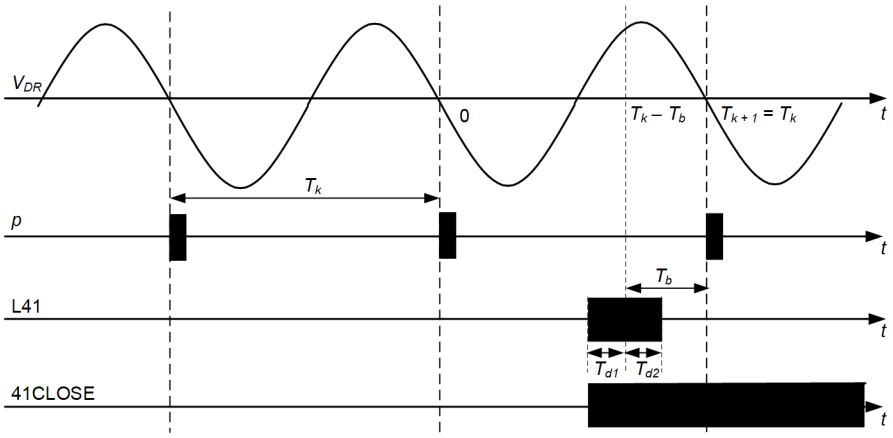

Fig. 12. 41CLOSE pulse timing.

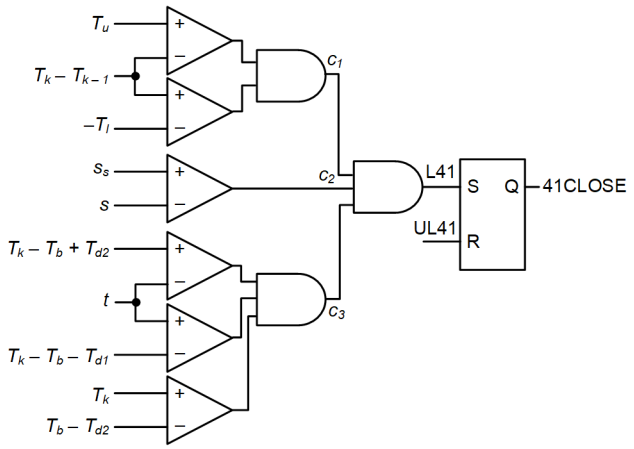

Fig. 13. Logic A in which three conditions (c_1 to c_3) are verified.

As explained in Section IV, because of noise in the V_{DR} signal, p may pulse at an NPZC when the slip is low. In such a case, the FAR measures approximately half of the actual period two consecutive times, which sets c_1 and causes the L41 pulse to be issued prematurely. To prevent such an undesirable operation, an additional condition, c_4, is included if an estimate or measured value of the final slip period of the V_{DR} signal is available from past event records. Let this estimate of the final slip period be T_{est}. We compare the measured cycle period with a threshold mT_{est} where m is a preset constant ($0.5 < m < 1$). If the period of a half cycle gets measured, it is discarded after checking that it does not exceed this threshold. Fig. 14 shows Logic B, which verifies that the conditions c_1 to c_4 are all true before issuing the close command at time t after the latest PNZC.

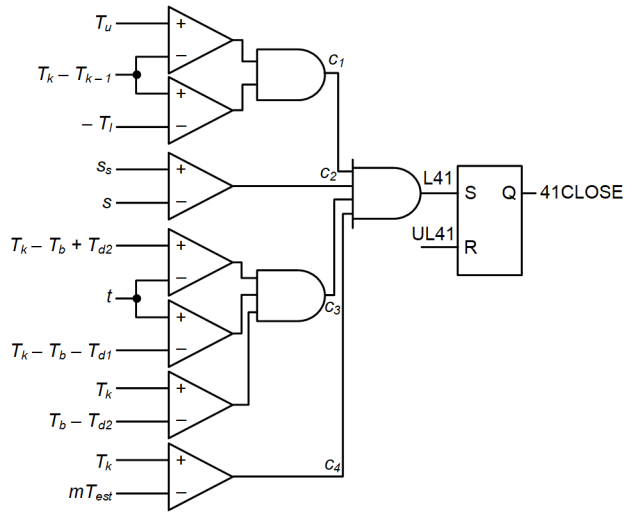

Fig. 14. Logic B in which four conditions (c_1 to c_4) are verified for noisy V_{DR} signal applications.

Note that the actual final period must be between mT_{est} and $2mT_{est}$ for proper operation. If it falls outside this range, improper operation of the FAR algorithm may occur, resulting in a failed motor start. Measuring this value prior to implementation of the algorithm may be necessary to obtain an accurate value. See the appendix for an explanation of this constraint.

VI. Results

The objective of the paper is to ensure a successful start of an SM. Before implementing either logic in the FAR connected to the onsite SM, it is important to verify the operation of the logic with realistic data.

To verify the operation of Logic A, we first implemented it in a FAR in the laboratory. We simulated an SM start to obtain an event report containing V_{DR} and stator currents and voltages. Then, we replayed the event report into the FAR and observed the output.

Similarly, we tested Logic B first by replaying the event report from the simulation. Following laboratory testing, Logic B was further tested in the onsite FAR with the SM connected. The breaker closing time, T_b, used in this case study was measured to be approximately 200 ms. For a 15 ms difference in the actual closing time and a processing delay of 25 ms, the breaker would close a maximum of 40 ms (approximately 8.5°) from the PNZC, which is acceptable for our application. The parameters of the onsite SM are in Table I.

A. Simulation Results With Logic A

We obtained an event report with a V_{DR} waveform similar to that generated by the SM in the field via simulation. We replayed this event report as an input to the FAR with the Logic A parameters as listed in Table II. The V_{DR} signal was noise-free.

Fig. 15 shows the V_{DR} signal, the slip calculated by the FAR, pulse p, the outputs of conditions c_1 to c_3, and the assertions of the L41 bit. We observe that the positive edge of L41 (left cursor) occurs approximately 191 ms before the upcoming PNZC (right cursor). Thus, a field breaker with a 200 ms closing time would close approximately 9 ms (approximately 2.7°) after the PNZC. This delay is acceptable for this installation, given our operating conditions.

Table II.
Logic A Parameters

Parameter	Value	Parameter	Value
T_l	50 ms	T_{d1}	0 ms
T_u	25 ms	T_{d2}	50 ms
s_s	2%		

B. Simulation Results With Logic B

Using records of past SM starting events, we measured T_{est} to be approximately 1.7 s. For this simulation, we set the parameter m to 0.6. The appendix describes one method for choosing the value of m. We first implemented Logic B in the FAR, setting the parameters as listed in Table III.

Table III.
Logic B Parameters

Parameter	Value	Parameter	Value
T_{est}	1.7 s	T_{d1}	0 ms
T_l	50 ms	T_{d2}	50 ms
T_u	50 ms	s_s	2%
m	0.6		

Next, we obtained another event report with a V_{DR} waveform similar to that generated by the SM in the field through a simulation, injecting a glitch (a PNZC) at the NPZC in one of the cycles after the slip reached s_s. We replayed this event report into the FAR programmed with Logic B. The result is shown in Fig. 16. We observe that c_4 resets when the FAR detects the spurious PNZC because the measured period is less than mT_{est} = 1.02 s. However, c_4 sets in the following cycle because no spurious PNZC is detected and the measured period is greater than mT_{est}. The positive edge of L41 (left cursor) occurs approximately 201 ms before the PNZC (right cursor).

C. *Field Test Results With Logic B*

Using the parameters listed in Table III, we tested the operation of Logic B five times in the field with the SM connected to the FAR. We found that between tests, the variation of when the breaker closed was small, less than 30 ms. Fig. 17 shows the measured V_{DR} signal, slip, outputs of the conditions c_1 to c_4, and the assertions of the L41 bit over the last few seconds of the motor starting in one of the test starts. A zoomed-in version of the last half cycle before the breaker is closed is shown in Fig. 18.

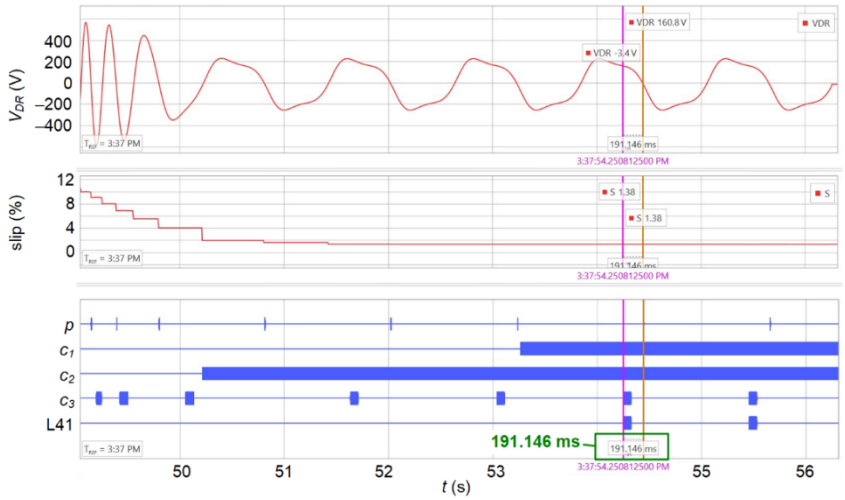

Fig. 15. Measured V_{DR} signal, slip, Logic A condition outputs (c_1 to c_3), and the close command (L41) bit assertions by the FAR with a simulated event input.

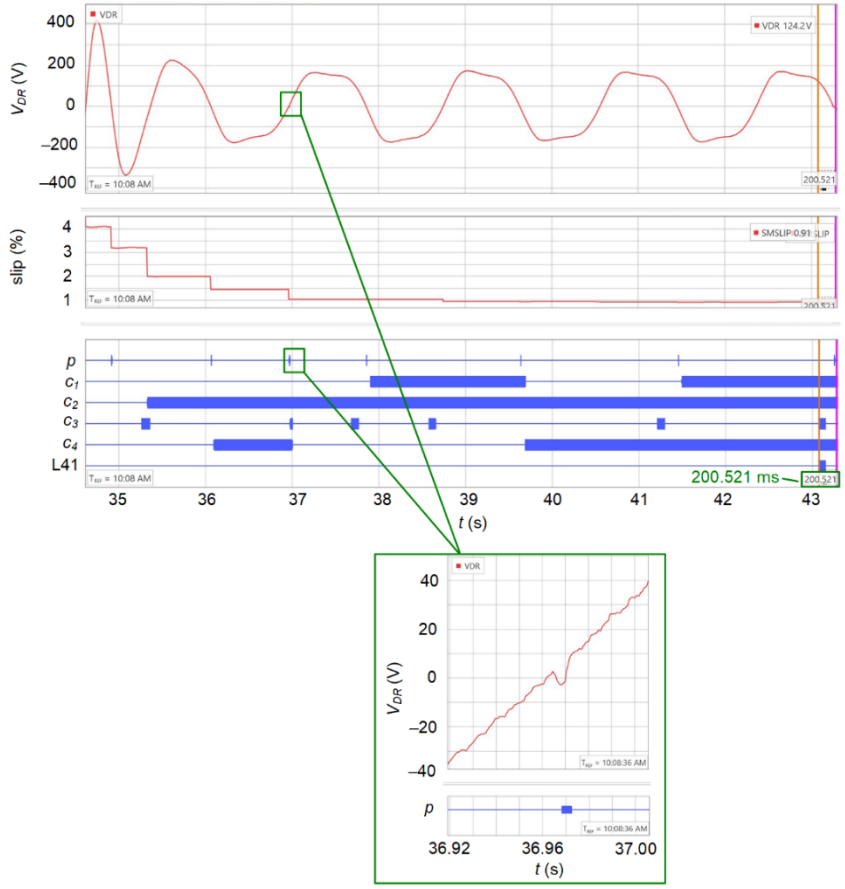

Fig. 16. Measured V_{DR} signal, slip, Logic B condition outputs (c_1 to c_4), and the close command (L41) bit assertions by the FAR with a simulated event input.

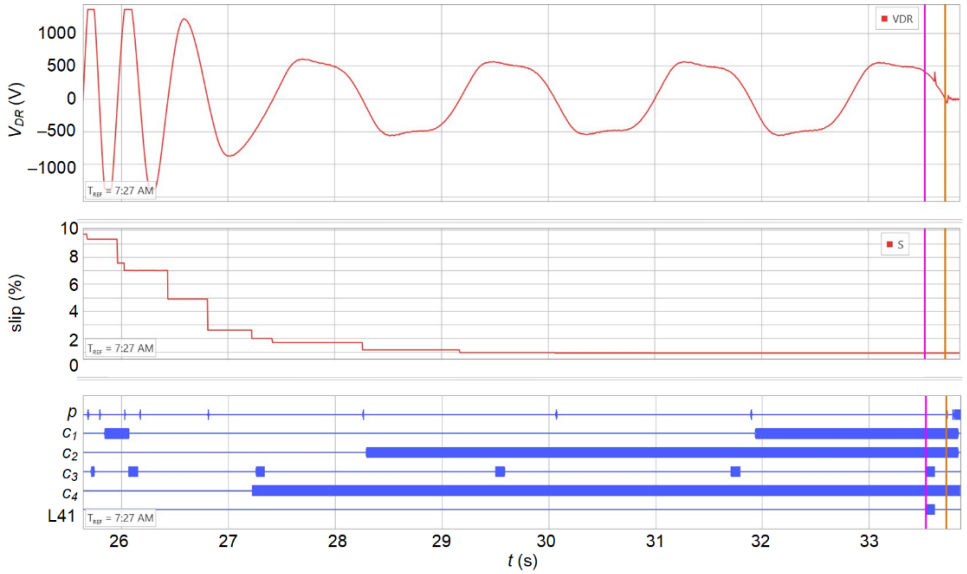

Fig. 17. Measured V_{DR} signal, slip, Logic B condition outputs (c_1 to c_4), and the close command (L41) bit assertions from a field test.

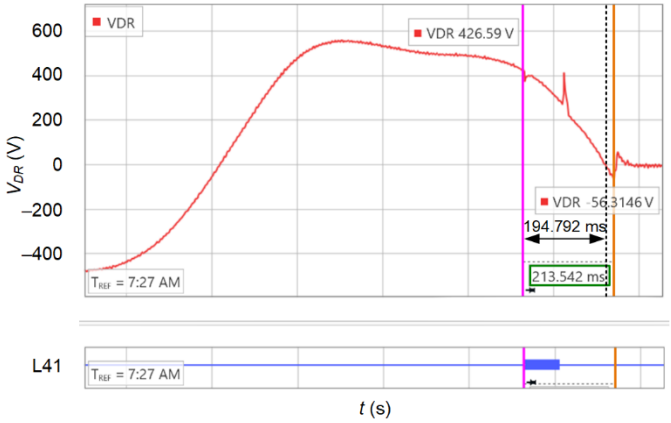

Fig. 18. FAR close command along the V_{DR} signal.

In Fig. 18, the left cursor indicates the time the L41 bit is triggered and the right cursor indicates the time the breaker closed. The time that elapsed between the rising edge of the L41 bit and closure of the field breaker is approximately 214 ms. Note that the rising edge of the L41 bit occurred approximately 195 ms before the PNZC (indicated by the dashed line) and the breaker closed 19 ms (approximately 3.9°) after the PNZC. This was suitable for this installation, given the operating conditions.

VII. Conclusion

Successful induction starting of large, high-inertia SMs hinges on when the field breaker closes and DC excitation is applied to the rotor field winding. This timing is controlled by the FAR. Our simulations demonstrated that the window of time along the V_{DR} signal that results in a successful synchronization varies depending on the field voltage applied, load inertia, and loading level. This region of synchronization shrinks to a small window that encompasses the PNZC for higher loads and load inertia and for lower field voltages. If the field breaker closes outside the region of synchronization, it can lead to contact arcing and failure to start.

To avoid such failures, we proposed an algorithm to determine the appropriate point-on-wave time to issue the field breaker close command, taking the breaker closing time into account. The algorithm uses the slip frequency and breaker closing time and dynamically measures the period of the V_{DR} signal to estimate the time of the next PNZC. Accordingly, the FAR sends the close command in advance to ensure that the closing of the field breaker contacts coincides with the PNZC of the V_{DR} signal. Further, we proposed an algorithm modification (which uses an estimate of the final stable period of the V_{DR} signal) to prevent electrical noise in the V_{DR} signal from leading to DC excitation of the field winding at the incorrect time.

With both simulation and field-testing results, we demonstrated the effectiveness of these solutions at ensuring successful SM starts. The new logic can be used for large, high-inertia machines to address starting issues related to field breaker closing times and poor signal quality present in some FAR applications, thereby improving the reliability of SM starting.

VIII. Appendix

For proper operation of Logic B (explained in Section V), the actual final period of the V_{DR} signal must be close to the estimated stable period, T_{est}. Specifically, the actual period should be between mT_{est} and $2mT_{est}$. Consider the example in Fig. 19 where the actual final period is less than mT_{est}. Condition c_4 will not be satisfied. Hence, 41CLOSE cannot be set even when $c_1 = c_2 = c_3 = 1$ because $c_4 = 0$.

On the other hand, if the period is greater than $2mT_{est}$, the time elapsed between a PNZC and the following NPZC may be greater than mT_{est}, as shown in Fig. 20. If a noise-induced PNZC is detected near the NPZC of the V_{DR} signal (as indicated by the pulse p), c_4 will be set. Assuming that the measured values, T_k and T_{k-1}, are approximately equal, c_1 will be set. Condition c_3 will be satisfied before the next NPZC, and assuming that c_2 is set, L41 will pulse along with c_3, leading to an untimely 41CLOSE command, as shown in Fig. 20.

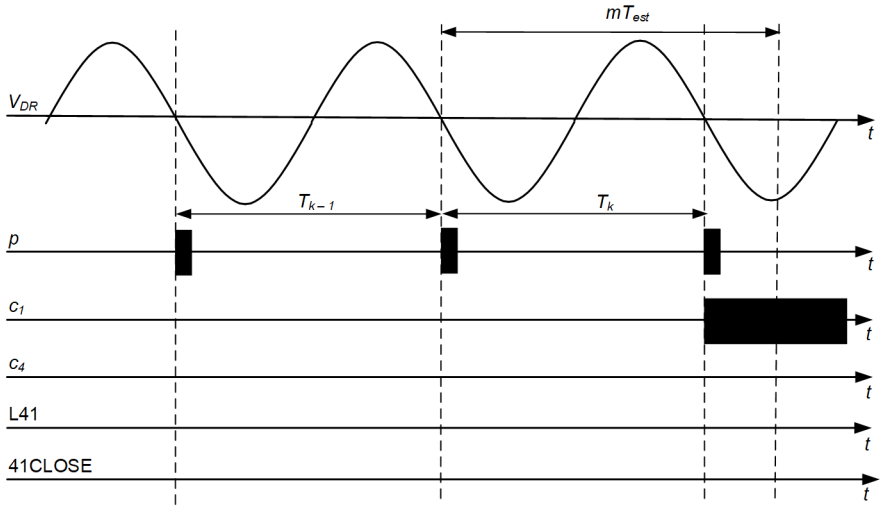

Fig. 19. Logic B operation when the actual period is less than mT_{est}.

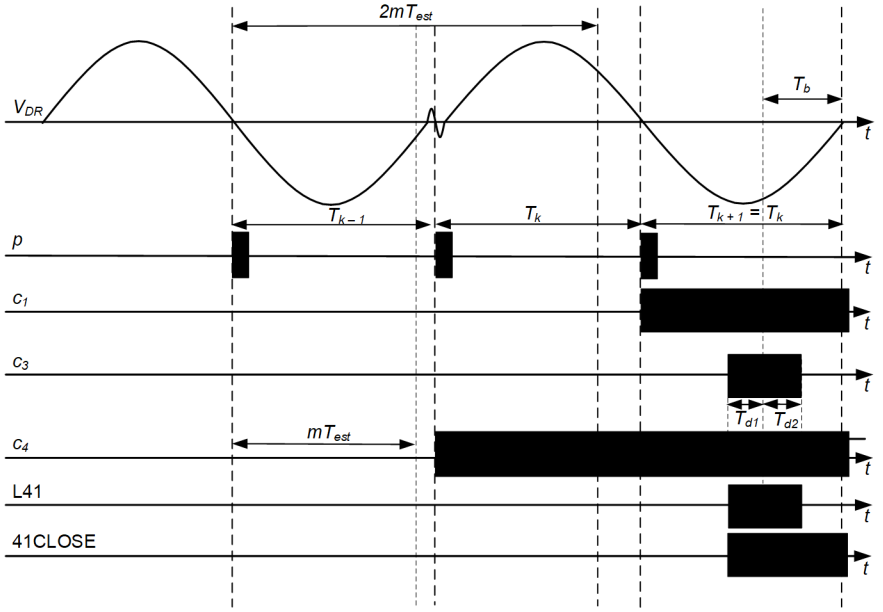

Fig. 20. Logic B operation when the actual period is greater than $2mT_{est}$.

The following describes one method for choosing m and T_{est}. First, set T_{est} by obtaining at least two records of past motor starting events. Let the minimum and maximum stable measured periods of the V_{DR} signal be T_{min} and T_{max}, respectively. Then, we express T_{est} as:

$$T_{est} = \frac{T_{min} + T_{max}}{2} \tag{1}$$

Let the actual period be within limits defined by an equal tolerance d outside T_{min} and T_{max}. These limits can then be equated as:

$$T_{min} - d = mT_{est} \tag{2}$$

$$T_{max} + d = 2mT_{est} \tag{3}$$

Solving the linear equations (1)–(3) simultaneously, we obtain $m = 2/3$. Alternatively, obtain T_{est} by simulating a model of the SM. If the actual period is expected to be within $T_{est} \pm d$, set $m = 2/3$.

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