SEL-487E-3, -4
Transformer Protection Relay

Instruction Manual

20201204

SEL SCHWEITZER ENGINEERING LABORATORIES

PM487E-02

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Preface

This manual provides information and instructions for installing and operating the relay. The manual is for use by power engineers and others experienced in protective relaying applications. Included are detailed technical descriptions of the relay and application examples. While this manual gives reasonable examples and illustrations of relay uses, you must exercise sound judgment at all times when applying the relay in a power system.

Manual Overview

The SEL-487E relay instruction manual consists of two volumes:

➤ SEL-487E Instruction Manual

➤ SEL-400 Series Relays Instruction Manual

SEL-487E Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction and Specifications. Introduces the relay features. Summarizes relay functions and applications. Lists relay specifications, type tests, and ratings.

Section 2: Installation. Discusses the ordering configurations and interface features (control inputs, control outputs, and analog inputs, for example). Provides information about how to design a new physical installation and secure the relay in a panel or rack. Details how to set relay board jumpers and make proper rear-panel connections (including wiring to CTs, PTs, and a GPS receiver). Explains basic connections for the relay communications ports.

Section 3: Testing. Describes techniques for testing the relay.

Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens that are unique to the SEL-487E.

Section 5: Protection Functions. Describes the function of various relay protection elements. Describes how the relay processes these elements. Gives detailed specifics on protection scheme logic for the differential elements. Provides trip logic diagrams, and current and voltage source selection details.

Section 6: Protection Application Examples. Provides examples of configuring the SEL-487E for some common applications.

Section 7: Metering, Monitoring, and Reporting. Describes SEL-487E specific metering, monitoring, and reporting features.

Section 8: Settings. Provides a list of all relay settings and defaults. The settings list is organized in the same order as in the relay and in the ACSELERATOR QuickSet SEL-5030 Software.

Section 9: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 10: Communications Interfaces. Describes the SEL-487E specific communications characteristics.

Section 11: Relay Word Bits. Contains a summary of Relay Word bits.

Section 12: Analog Quantities. Contains a summary of analog quantities.

Appendix A: Firmware, ICD File, and Manual Versions. Lists the current firmware and manual versions and details differences between the current and previous versions.

Appendix B: Converting Settings From SEL-487E-0, -2 to SEL-487E-3, -4. Describes differences in settings, Relay Word bits, analog quantities, and DNP3 mapping between these versions.

SEL-400 Series Relays Instruction Manual

Preface. Describes manual organization and conventions used to present information, as well as safety information.

Section 1: Introduction. Introduces SEL-400 Series Relay common features.

Section 2: PC Software. Explains how to use SEL Grid Configurator and ACSELERATOR QuickSet SEL-5030 Software.

Section 3: Basic Relay Operations. Describes how to perform fundamental operations such as applying power and communicating with the relay, setting and viewing passwords, checking relay status, viewing metering data, reading event reports and Sequential Events Recorder (SER) records, operating relay control outputs and control inputs, and using relay features to make relay commissioning easier.

Section 4: Front-Panel Operations. Describes the LCD display messages and menu screens. Shows you how to use front-panel pushbuttons and read targets. Provides information about local substation control and how to make relay settings via the front panel.

Section 5: Control. Describes various control features of the relay, including circuit breaker operation, disconnect operation, remote bits, and one-line diagrams.

Section 6: Autoreclosing. Explains how to operate the two-circuit breaker multishot recloser. Describes how to set the relay for single-pole reclosing, three-pole reclosing, or both. Shows selection of the lead and follow circuit breakers.

Section 7: Metering. Provides information on viewing current, voltage, power, and energy quantities. Describes how to view other common internal operating quantities.

Section 8: Monitoring. Describes how to use the circuit breaker monitors and the substation dc battery monitors.

Section 9: Reporting. Explains how to obtain and interpret high-resolution raw data oscillograms, filtered event reports, event summaries, history reports, and SER reports. Discusses how to enter SER trigger settings.

Section 10: Testing, Troubleshooting, and Maintenance. Describes techniques for testing, troubleshooting, and maintaining the relay. Includes the list of status notification messages and a troubleshooting chart.

Section 11: Time and Date Management. Explains timekeeping principles, synchronized phasor measurements, and estimation of power system states using the high-accuracy time-stamping capability. Presents real-time load flow/power flow application ideas.

Section 12: Settings. Provides a list of all common SEL-400 Series Relay settings and defaults.

Section 13: SELOGIC Control Equation Programming. Describes multiple setting groups and SELOGIC control equations and how to apply these equations. Discusses expanded SELOGIC control equation features such as PLC-style commands, math functions, counters, and conditioning timers. Provides a tutorial for converting older format SELOGIC control equations to new freeform equations.

Section 14: ASCII Command Reference. Provides an alphabetical listing of all ASCII commands with examples for each ASCII command option.

Section 15: Communications Interfaces. Explains the physical connection of the relay to various communications network topologies. Describes the various software protocols and how to apply these protocols to substation integration and automation. Includes details about Ethernet IP protocols, SEL ASCII, SEL Compressed ASCII, SEL Fast Meter, SEL Fast Operate, SEL Fast SER, and enhanced MIRRORED BITS communications.

Section 16: DNP3 Communication. Describes the DNP3 communications protocol and how to apply this protocol to substation integration and automation. Provides a Job Done example for implementing DNP3 in a substation.

Section 17: IEC 61850 Communication. Describes the IEC 61850 protocol and how to apply this protocol to substation automation and integration. Includes IEC 61850 protocol compliance statements.

Section 18: Synchrophasors. Describes the Phasor Measurement Unit (PMU) functions of the relay. Provides details on synchrophasor measurement and real-time control. Describes the IEEE C37.118 Synchrophasor Protocol settings. Describes the SEL Fast Message Synchrophasor Protocol settings.

Section 19: Digital Secondary Systems. Describes the basic concepts of digital secondary systems (DSS). This includes both the Time-Domain Link (TiDL) system and UCA 61850-9-2LE Sampled Values.

Appendix A: Manual Versions. Lists the current manual version and details differences between the current and previous versions.

Appendix B: Firmware Upgrade Instructions. Describes the procedure to update the firmware stored in Flash memory.

Appendix C: Cybersecurity Features. Describes the various features of the relay that impact cybersecurity.

Glossary. Defines various technical terms used in the SEL-400 series instruction manuals.

Safety Information

Dangers, Warnings, and Cautions

This manual uses three kinds of hazard statements, defined as follows:

⚠DANGER
Indicates an imminently hazardous situation that, if not avoided, **will** result in death or serious injury.

⚠WARNING
Indicates a potentially hazardous situation that, if not avoided, **could** result in death or serious injury.

⚠CAUTION
Indicates a potentially hazardous situation that, if not avoided, **may** result in minor or moderate injury or equipment damage.

Safety Symbols

The following symbols are often marked on SEL products.

	⚠CAUTION Refer to accompanying documents.	⚠ATTENTION Se reporter à la documentation.
Earth (ground)		Terre
Protective earth (ground)		Terre de protection
Direct current		Courant continu
Alternating current		Courant alternatif
Both direct and alternating current		Courant continu et alternatif
Instruction manual		Manuel d'instructions

Safety Marks

The following statements apply to this device.

General Safety Marks

⚠CAUTION	⚠ATTENTION
There is danger of explosion if the battery is incorrectly replaced. Replace only with Rayovac no. BR2335 or equivalent recommended by manufacturer. See Owner's Manual for safety instructions. The battery used in this device may present a fire or chemical burn hazard if mistreated. Do not recharge, disassemble, heat above 100°C or incinerate. Dispose of used batteries according to the manufacturer's instructions. Keep battery out of reach of children.	Une pile remplacée incorrectement pose des risques d'explosion. Remplacez seulement avec un Rayovac no BR2335 ou un produit équivalent recommandé par le fabricant. Voir le guide d'utilisateur pour les instructions de sécurité. La pile utilisée dans cet appareil peut présenter un risque d'incendie ou de brûlure chimique si vous en faites mauvais usage. Ne pas recharger, démonter, chauffer à plus de 100°C ou incinérer. Éliminez les vieilles piles suivant les instructions du fabricant. Gardez la pile hors de la portée des enfants.
⚠CAUTION	⚠ATTENTION
To ensure proper safety and operation, the equipment ratings, installation instructions, and operating instructions must be checked before commissioning or maintenance of the equipment. The integrity of any protective conductor connection must be checked before carrying out any other actions. It is the responsibility of the user to ensure that the equipment is installed, operated, and used for its intended function in the manner specified in this manual. If misused, any safety protection provided by the equipment may be impaired.	Pour assurer la sécurité et le bon fonctionnement, il faut vérifier les classements d'équipement ainsi que les instructions d'installation et d'opération avant la mise en service ou l'entretien de l'équipement. Il faut vérifier l'intégrité de toute connexion de conducteur de protection avant de réaliser d'autres actions. L'utilisateur est responsable d'assurer l'installation, l'opération et l'utilisation de l'équipement pour la fonction prévue et de la manière indiquée dans ce manuel. Une mauvaise utilisation pourrait diminuer toute protection de sécurité fournie par l'équipement.
For use in Pollution Degree 2 environment.	Pour l'utilisation dans un environnement de Degré de Pollution 2.

Other Safety Marks (Sheet 1 of 3)

⚠DANGER	⚠DANGER
Disconnect or de-energize all external connections before opening this device. Contact with hazardous voltages and currents inside this device can cause electrical shock resulting in injury or death.	Débrancher tous les raccordements externes avant d'ouvrir cet appareil. Tout contact avec des tensions ou courants internes à l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
⚠DANGER	⚠DANGER
Contact with instrument terminals can cause electrical shock that can result in injury or death.	Tout contact avec les bornes de l'appareil peut causer un choc électrique pouvant entraîner des blessures ou la mort.
⚠WARNING	⚠AVERTISSEMENT
Use of this equipment in a manner other than specified in this manual can impair operator safety safeguards provided by this equipment.	L'utilisation de cet appareil suivant des procédures différentes de celles indiquées dans ce manuel peut désarmer les dispositifs de protection d'opérateur normalement actifs sur cet équipement.
⚠WARNING	⚠AVERTISSEMENT
Have only qualified personnel service this equipment. If you are not qualified to service this equipment, you can injure yourself or others, or cause equipment damage.	Seules des personnes qualifiées peuvent travailler sur cet appareil. Si vous n'êtes pas qualifiés pour ce travail, vous pourriez vous blesser avec d'autres personnes ou endommager l'équipement.
⚠WARNING	⚠AVERTISSEMENT
This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.	Cet appareil est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accés non-autorisé á l'équipement peut être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accés non-autorisé.
⚠WARNING	⚠AVERTISSEMENT
Do not look into the fiber ports/connectors.	Ne pas regarder vers les ports ou connecteurs de fibres optiques.
⚠WARNING	⚠AVERTISSEMENT
Do not look into the end of an optical cable connected to an optical output.	Ne pas regarder vers l'extrémité d'un câble optique raccordé à une sortie optique.
⚠WARNING	⚠AVERTISSEMENT
Do not perform any procedures or adjustments that this instruction manual does not describe.	Ne pas appliquer une procédure ou un ajustement qui n'est pas décrit explicitement dans ce manuel d'instruction.
⚠WARNING	⚠AVERTISSEMENT
During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.	Durant l'installation, la maintenance ou le test des ports optiques, utilisez exclusivement des équipements de test homologués comme produits de type laser de Classe 1.

Other Safety Marks (Sheet 2 of 3)

⚠WARNING	⚠AVERTISSEMENT
Incorporated components, such as LEDs and transceivers are not user serviceable. Return units to SEL for repair or replacement.	Les composants internes tels que les leds (diodes électroluminescentes) et émetteurs-récepteurs ne peuvent pas être entretenus par l'usager. Retourner les unités à SEL pour réparation ou remplacement.
⚠CAUTION	⚠ATTENTION
Equipment components are sensitive to electrostatic discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.	Les composants de cet équipement sont sensibles aux décharges électrostatiques (DES). Des dommages permanents non-décelables peuvent résulter de l'absence de précautions contre les DES. Raccordez-vous correctement à la terre, ainsi que la surface de travail et l'appareil avant d'en retirer un panneau. Si vous n'êtes pas équipés pour travailler avec ce type de composants, contacter SEL afin de retourner l'appareil pour un service en usine.
⚠CAUTION	⚠ATTENTION
Equipment damage can result from connecting ac circuits to Hybrid (high-current interrupting) control outputs. Do not connect ac circuits to Hybrid control outputs. Use only dc circuits with Hybrid control outputs.	Des dommages à l'appareil pourraient survenir si un circuit CA était raccordé aux contacts de sortie à haut pouvoir de coupure de type "Hybrid." Ne pas raccorder de circuit CA aux contacts de sortie de type "Hybrid." Utiliser uniquement du CC avec les contacts de sortie de type "Hybrid."
⚠CAUTION	⚠ATTENTION
Substation battery systems that have either a high resistance to ground (greater than 10 kΩ) or are ungrounded when used in conjunction with many direct-coupled inputs can reflect a dc voltage offset between battery rails. Similar conditions can exist for battery monitoring systems that have high-resistance balancing circuits or floating grounds. For these applications, SEL provides optional ground-isolated (optoisolated) contact inputs. In addition, SEL has published an application advisory on this issue. Contact the factory for more information.	Les circuits de batterie de postes qui présentent une haute résistance à la terre (plus grande que 10 kΩ) ou sont isolés peuvent présenter un biais de tension CC entre les deux polarités de la batterie quand utilisés avec plusieurs entrées à couplage direct. Des conditions similaires peuvent exister pour des systèmes de surveillance de batterie qui utilisent des circuits d'équilibrage à haute résistance ou des masses flottantes. Pour ce type d'applications, SEL peut fournir en option des contacts d'entrée isolés (par couplage optoélectronique). De surcroît, SEL a publié des recommandations relativement à cette application. Contacter l'usine pour plus d'informations.
⚠CAUTION	⚠ATTENTION
If you are planning to install an INT4 I/O interface board in your relay, first check the firmware version of the relay. If the firmware version is R111 or lower, you must first upgrade the relay firmware to the newest version and verify that the firmware upgrade was successful before installing the new board. Failure to install the new firmware first will cause the I/O interface board to fail, and it may require factory service. Complete firmware upgrade instructions are provided when new firmware is ordered.	Si vous avez l'intention d'installer une Carte d'Interface INT4 I/O dans votre relais, vérifiez en premier la version du logiciel du relais. Si la version est R111 ou antérieure, vous devez mettre à jour le logiciel du relais avec la version la plus récente et vérifier que la mise à jour a été correctement installée sur la nouvelle carte. Les instructions complètes de mise à jour sont fournies quand le nouveau logiciel est commandé.
⚠CAUTION	⚠ATTENTION
Field replacement of I/O boards INT1, INT2, INT5, INT6, INT7, or INT8 with INT4 can cause I/O contact failure. The INT4 board has a pickup and dropout delay setting range of 0–1 cycle. For all other I/O boards, pickup and dropout delay settings (IN201PU–IN224PU, IN201DO–IN224DO, IN301PU–IN324PU, and IN301DO–IN324DO) have a range of 0–5 cycles. Upon replacing any I/O board with an INT4 board, manually confirm reset of pickup and dropout delays to within the expected range of 0–1 cycle.	Le remplacement en chantier des cartes d'entrées/sorties INT1, INT2, INT5, INT6, INT7 ou INT8 par une carte INT4 peut causer la défaillance du contact d'entrée/sortie. La carte INT4 présente un intervalle d'ajustement pour les délais de montée et de retombée de 0 à 1 cycle. Pour toutes les autres cartes, l'intervalle de réglage du délai de montée et retombée (IN201PU–IN224PU, IN201DO– IN224DO, IN301PU–IN324PU, et IN301DO–IN324DO) est de 0 à 5 cycles. Quand une carte d'entrées/sorties est remplacée par une carte INT4, vérifier manuellement que les délais de montée et retombée sont dans l'intervalle de 0 à 1 cycle.
⚠CAUTION	⚠ATTENTION
Do not install a jumper on positions A or D of the main board J21 header. Relay misoperation can result if you install jumpers on positions J21A and J21D.	Ne pas installer de cavalier sur les positions A ou D sur le connecteur J21 de la carte principale. Une opération intempestive du relais pourrait résulter suite à l'installation d'un cavalier entre les positions J21A et J21D.
⚠CAUTION	⚠ATTENTION
Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.	Un niveau d'isolation insuffisant peut entraîner une détérioration sous des conditions anormales et causer des dommages à l'équipement. Pour les circuits externes, utiliser des conducteurs avec une isolation suffisante de façon à éviter les claquages durant les conditions anormales d'opération.
⚠CAUTION	⚠ATTENTION
Relay misoperation can result from applying other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.	Une opération intempestive du relais peut résulter par le branchement de tensions et courants secondaires non conformes aux spécifications. Avant de brancher un circuit secondaire, vérifier la tension ou le courant nominal sur la plaque signalétique à l'arrière.

Other Safety Marks (Sheet 3 of 3)

⚠CAUTION	⚠ATTENTION
Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.	Des problèmes graves d'alimentation et de terre peuvent survenir sur les ports de communication de cet appareil si des câbles d'origine autre que SEL sont utilisés. Ne jamais utiliser de câble de modem nul avec cet équipement.
⚠CAUTION	⚠ATTENTION
Do not connect power to the relay until you have completed these procedures and receive instruction to apply power. Equipment damage can result otherwise.	Ne pas mettre le relais sous tension avant d'avoir complété ces procédures et d'avoir reçu l'instruction de brancher l'alimentation. Des dommages à l'équipement pourraient survenir autrement.
⚠CAUTION	⚠ATTENTION
Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.	L'utilisation de commandes ou de réglages, ou l'application de tests de fonctionnement différents de ceux décrits ci-après peuvent entraîner l'exposition à des radiations dangereuses.

General Information

The SEL-487E Instruction Manual uses certain conventions that identify particular terms and help you find information. To benefit fully from reading this manual, take a moment to familiarize yourself with these conventions.

Typographic Conventions

There are three ways to communicate with SEL-400 Series Relays:

➤ Using a command line interface on a PC terminal emulation window, such as Microsoft HyperTerminal

➤ Using the front-panel menus and pushbuttons

➤ Using ACSELERATOR QuickSet SEL-5030 Software

The instructions in this manual indicate these options with specific font and formatting attributes. The following table lists these conventions:

Example	Description
STATUS	Commands, command options, and command variables typed at a command line interface on a PC.
n **SUM *n***	Variables determined based on an application (in bold if part of a command).
<Enter>	Single keystroke on a PC keyboard.
<Ctrl+D>	Multiple/combination keystroke on a PC keyboard.
Start > Settings	PC software dialog boxes and menu selections. The > character indicates submenus.
ENABLE	Relay front- or rear-panel labels and pushbuttons.
`MAIN > METER`	Relay front-panel LCD menus and relay responses visible on the PC screen. The > character indicates submenus.

Logic Diagrams

Logic diagrams in this manual follow the conventions and definitions shown below.

NAME	SYMBOL	FUNCTION
COMPARATOR	A +, B − → C	Input A is compared to input B. Output C asserts if A is greater than B.
INPUT FLAG	A ▸	Input A comes from other logic.
OR	A, B → C	Either input A or input B asserted cause output C to assert.
EXCLUSIVE OR	A, B → C	If either A or B is asserted, output C is asserted. If A and B are of the same state, C is deasserted.
NOR	A, B → C	If neither A nor B asserts, output C asserts.
AND	A, B → C	Input A and input B must assert to assert output C.
AND W/ INVERTED INPUT	A, B → C	If input A is asserted and input B is deasserted, output C asserts. Inverter "O" inverts any input or output on any gate.
NAND	A, B → C	If A and/or B are deasserted, output C is asserted.
TIME DELAYED PICK UP AND/OR TIME DELAYED DROP OUT	A → [X/Y] → B	X is a time-delay-pickup value; Y is a time-delay-dropout value. B asserts time X after input A asserts; B will not assert if A does not remain asserted for time X. If X is zero, B will assert when A asserts. If Y is zero, B will deassert when A deasserts.
EDGE TRIGGER TIMER	A → [X/Y] → B	Rising edge of A starts timers. Output B will assert time X after the rising edge of A. B will remain asserted for time Y. If Y is zero, B will assert for a single processing interval. Input A is ignored while the timers are running.
SET RESET FLIP FLOP	S, R Q	Input S asserts output Q until input R asserts. Output Q deasserts or resets when R asserts.
FALLING EDGE	A ⌐ B	B asserts at the falling edge of input A.
RISING EDGE	A ⌐ B	B asserts at the rising edge of input A.
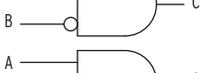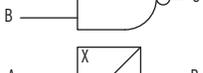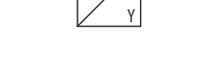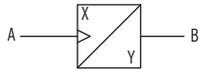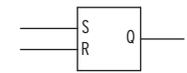
Trademarks

Trademarks appearing in this manual are shown in the following table.

ACSELERATOR Architect®	MIRRORED BITS®
ACSELERATOR QuickSet®	SELOGIC®
Best Choice Ground Directional Element®	

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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Introduction and Specifications

The SEL-487E relay, shown in *Figure 1.1*, provides a suite of current and voltage elements for the comprehensive protection of power transformers. In total, the relay consists of 24 analog channels, divided into three groups of analog inputs. The first group consists of 15 channels for phase current inputs that are divided into five groups of three-phase inputs. The second group consists of three channels for single-phase (neutral) current inputs, and the third group consists of six channels for two three-phase voltage inputs.

i4222c
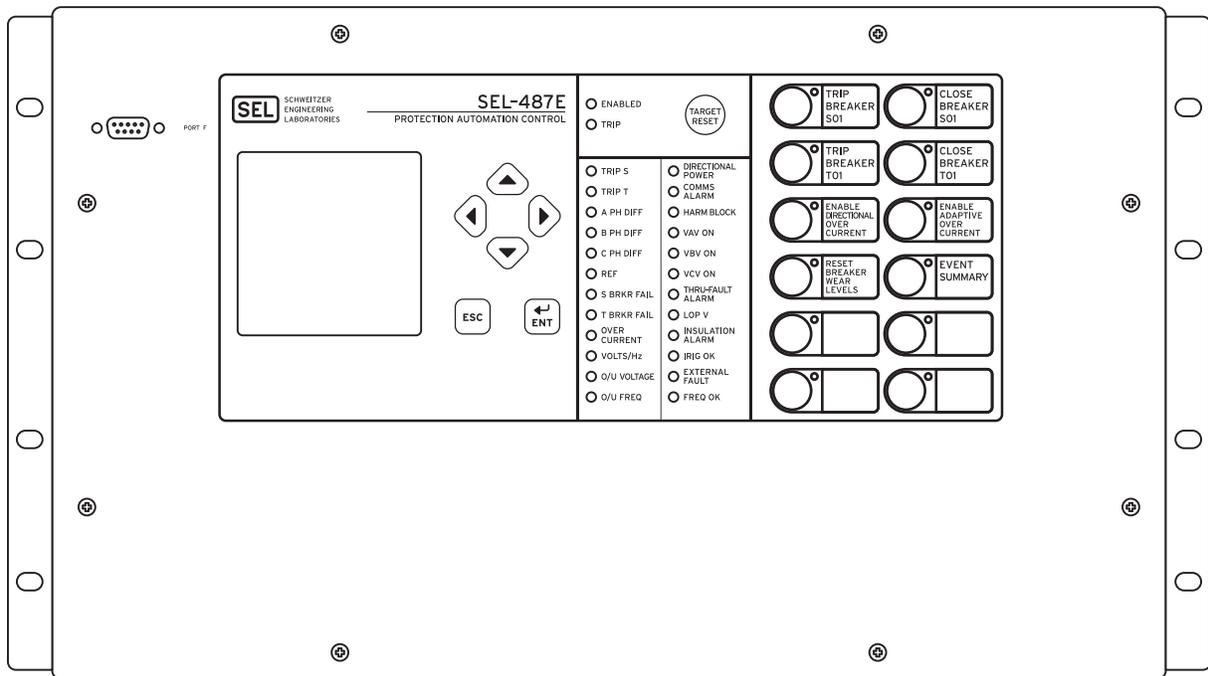
Figure 1.1 SEL-487E Current Differential Relay

In addition to transformer protection, the relay is suited for other current differential protection such as busbar protection for as many as five terminals with mismatched CT ratios as high as 35:1. When installed as busbar protection, use the relay as a PMU and a station-wide digital fault recorder to collect data from each of the five terminals.

As main protection for power transformers, current-operated protection includes an adaptive-slope phase percentage restraint differential element, an unrestraint differential element, a negative-sequence percentage restraint differential element, programmable restricted earth fault elements, breaker failure protection for each winding, and several voltage-polarized directional and nondirectional phase, negative-sequence and zero-sequence definite-time and inverse-time overcurrent elements.

Select secondary current inputs from a combination of 1 A and 5 A on a per-winding basis for the phase input windings (Winding S through Winding X), or a combination of 1 A and 5 A on a per-phase basis on the neutral windings (Winding Y).

Voltage-operated transformer protection includes under- and overfrequency elements, under- and overpower elements, several phase, positive-sequence, negative-sequence and zero-sequence voltage elements, and two levels of volts-per-hertz protection.

System measurement, monitoring, and reports include an IEEE C57.91-1995 thermal element, IEEE C37.118-2005-compliant synchrophasor measurements, an IEEE C57.109-1993 through-fault current monitor, breaker wear monitoring for each individual pole, battery voltage monitoring, sequential event reporting (SER), and 8 kHz COMTRADE event reports. Collect data from as many as 12 temperature measuring elements when used with the SEL-2600 RTD Module.

Select sampling rates for oscillography from 1 kHz, 2 kHz, 4 kHz, and 8 kHz. At a 1 kHz sampling rate, record as many as 24 seconds of event data.

For customized protection and automation functions, use the SELOGIC control equations with extensive programming capabilities. Because protection and automation programming require different execution times, the relay provides separate programming areas for protection and automation programming. You can organize automation SELOGIC control equation programming into 10 blocks of 100 program lines each for a total of 1000 lines of automation programming. Use as many as 250 lines in the separate protection programming area to program custom protection functions.

Communications interfaces include standard SEL ASCII and enhanced MIRRORED BITS communications protocols. Establish Ethernet connectivity with the optional Ethernet card to employ common industry communications tools including Telnet, FTP, DNP3 LAN/WAN, or IEC-61850 Protocol Option protocols.

The SEL-487E provides comprehensive protection, automation, and control for transformers.

The ACSELERATOR QuickSet SEL-5030 Software for the SEL-487E is available at no cost. Use QuickSet to assist you in setting, controlling, and acquiring data from the relays both locally and remotely. ACSELERATOR Architect SEL-5032 Software is included with purchase of the optional Ethernet card with IEC 61850 protocol support. Architect enables you to view and configure IEC 61850 settings, tightly integrated with QuickSet.

This section introduces the SEL-487E and provides information on the following topics:

➤ *Features on page 1.3*

➤ *Models and Options on page 1.6*

➤ *Applications on page 1.9*

➤ *Product Characteristics on page 1.12*

➤ *Specifications on page 1.14*

Features

The SEL-487E contains many protection, automation, and control features. *Figure 1.2* presents a simplified functional overview of the relay.
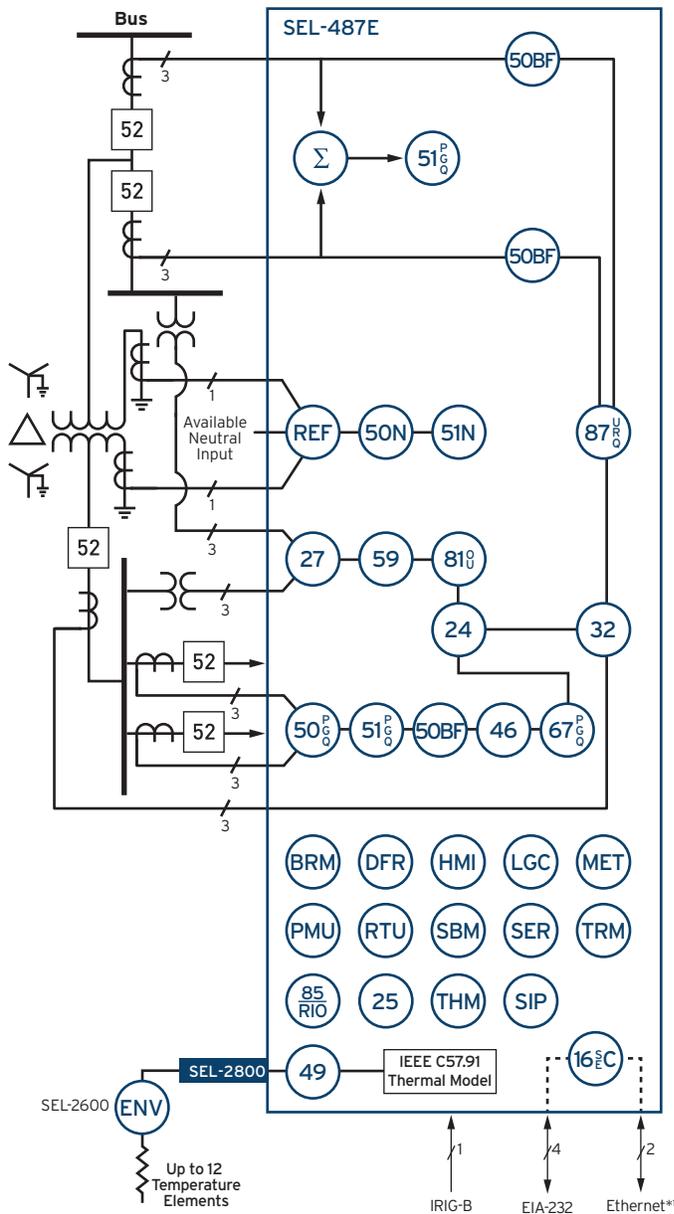
ANSI NUMBERS/ACRONYMS AND FUNCTIONS	
16 SEC	Access Security (Serial, Ethernet)
24	Volts/Hertz
25	Synchronism Check
27	Undervoltage
32	Directional Power
46	Current Unbalance
49	Thermal
50BF	Breaker Failure Overcurrent
50N	Neutral Overcurrent
50 (P, G, Q)	Overcurrent (Phase, Ground, Neg. Seq.)
51N	Neutral Time-Overcurrent
51 (P, G, Q)	Time-Overcurrent (Phase, Ground, Neg. Seq.)
59	Overvoltage
67 (P, G, Q)	Directional Overcurrent (Phase, Ground, Neg. Seq.)
81 (O, U)	Over- and Underfrequency
85 RIO	SEL MIRRORED BITS® Communications
87 (U, R, Q)	Transformer Differential (Unrestrained, Restrained, Neg. Seq.)
DFR	Event Reports
ENV	SEL-2600
HMI	Operator Interface
LGC	Expanded SELOGIC® Control Equations
MET	High-Accuracy Metering
PMU	Synchrophasors
REF	Restricted Earth Fault
RTU	Remote Terminal Unit
SER	Sequential Events Recorder

ADDITIONAL FUNCTIONS	
BRM	Breaker Wear Monitor
LDP	Load Data Profiling
SBM	Station Battery Monitor
SIP	Software-Invertible Polarities
THM	IEC 60255-Compliant Thermal Model
TiDL	Time-Domain Link Remote Data Acquisition
TRM	Transformer Monitor

[1] Copper or Fiber Optic   * Optional Feature

Figure 1.2   Functional Overview

The SEL-487E includes the following features:

Restraint Differential Element. Innovative algorithms switch the relay within 2 milliseconds to a high-security mode during through-fault conditions for maximum security. While in the high-security mode, the algorithm does not block the differential elements, thus avoiding unnecessary time delays for clearing faults evolving from external-to-internal faults.

CT Ratio Mismatch. Mismatched CTs of ratios as high as 35:1 can be installed. For example, one set of CTs in a breaker-and-a-half installation can have CT ratios of 4000/5 and the other set of CTs can have CT ratios of 120/5.

1 A/5 A CT Ratio Combination. Order each three-phase winding inputs with either 1 A or 5 A CT secondary current. For the restricted earth fault CTs, order each single-phase input with either 1 A or 5 A CT secondary current.

Unrestraint Differential Element. This element operates independent of the harmonic content of the differential current, providing fast, unrestraint tripping for high-current transformer faults, such as bushing faults. The unrestraint differential element compliments the phase differential elements, particularly during inrush conditions when harmonics in the differential current may cause the restraint differential elements to operate slower. Waveshape-based inrush detection addresses inrush conditions that contain low second- and fourth-harmonic content.

Negative-Sequence Differential Element. Use the negative-sequence differential element to provide greater sensitivity for turn-to-turn faults during heavy load conditions, when phase-current differential elements are less sensitive.

Restricted Earth Fault Element. Provides fast, sensitive protection for ground faults close to the neutral for grounded wye-transformer windings.

Breaker Failure Protection. The SEL-487E provides breaker failure protection for each of the five windings, initiated by either phase current, zero-sequence current, or a combination of phase current and zero-sequence current. To reduce breaker failure coordination time, advanced open-phase detection ensures current-element reset in less than one cycle.

Nondirectional Overcurrent Elements. Compliment the differential elements with a large number of instantaneous, definite-time, and adaptive inverse-time phase overcurrent elements; instantaneous, definite-time, and inverse-time residual (zero-sequence) overcurrent elements; instantaneous, definite-time, and inverse-time negative-sequence overcurrent elements, as well as combined overcurrent elements (inverse-time for phase and ground) for applications such as stations with breaker-and-a-half layouts.

Directional Overcurrent Elements. Convert any nondirectional overcurrent element to a directional overcurrent with a range of voltage-polarized directional elements.

Voltage Elements. The SEL-487E provides phase overvoltage and undervoltage elements, phase-to-phase overvoltage and undervoltage elements, as well as positive-sequence, negative-sequence, and zero-sequence voltage elements for each of the two sets of voltage inputs.

Synchronism Check. The SEL-487E includes synchronism-check elements for as many as five breakers. The synchronism-check function incorporates slip frequency, maximum angle difference, maximum voltage difference, breaker close time, and allows different sources of synchronizing voltage.

Frequency Elements. Any of the six levels of frequency elements can operate as either an underfrequency element, or as an overfrequency element. The frequency elements are suited for applications such as under-frequency load shedding and restoration control systems.

Volts-per-Hertz Elements. Combining the voltage elements with the frequency elements, the SEL-487E offers two levels of volts-per-hertz elements; one level for an unloaded transformer, and the other level for a loaded transformer.

Power Elements. Set the per-phase power elements to detect real and reactive power flow for applications such as reverse power protection/control and overpower and/or underpower protection/control.

Monitoring Elements. Use the SEL-487E to monitor a variety of items in the substation. To monitor the transformer insulation health, use the thermal element based on IEEE Std C57.91-1995, Guide for Loading Mineral-Oil-Immersed Power Transformer; monitor the ac ripple and battery ground faults with the built-in battery monitor; calculate the percentage breaker wear and record the number of operations to optimize breaker maintenance with the breaker wear monitor. Monitor the transformer through-fault current on a per-phase basis to determine the impact of through faults on the transformer windings.

Fault Identification Logic. Determines which phase(s) was involved in a fault for which the transformer tripped on a per-terminal basis. Faulted phase identification is based on current inputs from wye-connected CTs.

Synchrophasor. The relay provides C37.118-compliant synchrophasors for all 24 channels. The relay supports five independent synchrophasor data streams that can be channeled through both serial and Ethernet ports. The relay supports message rates as high as 60 messages per second and three different filters. The relay can record synchrophasor data for as many as 120 seconds. The relay can process synchrophasor data from a remote source for real-time control.

Parallel Redundancy Protocol (PRP). Provide seamless recovery from any single Ethernet network failure with this protocol, in accordance with IEC 62439-3. The Ethernet network and all traffic are fully duplicated with both copies operating in parallel.

Expanded SELOGIC Control Equations. Modify and set custom relay applications with PLC-style (programmable logic controller, IEC 61131-3) SELOGIC control equation programming that includes math and comparison functions. Use counters and multifunction timers for greater application flexibility, i.e., perform advanced PLC functions within the relay. The SEL-487E has separate protection and automation SELOGIC control equation programming areas. These programming areas provide ample protection programming capability and 10 blocks of 100-line automation programming capability (1000 lines).

Alias Settings. Use as many as 200 aliases to rename any digital or analog quantity in the relay. These aliases are then available for use in customized programming, making the initial programming and maintenance much easier.

Metering. View primary or secondary rms or fundamental metering information for phase currents and angles of all windings, phase voltages, and angles, as well as the per-unit operating and restraint values from all differential elements.

Control. Open and close breakers and disconnects from the front panel with the bay control function. Obtain custom-build screens to match your transformer layout.

Commissioning Assistant. Use the patented Commissioning Assistant to check CT polarities, cross-wired CTs, consistent CT ratio between phases, and to calculate the correct compensation matrices for all five windings.

Oscillography and Event Reporting. Record raw and/or filtered currents, voltages, and digital information (8 kHz, COMTRADE format) that you select. Investigate relay internal logic points and power system performance with event report phasor analysis.

Sequential Events Recorder (SER). Record 1000 system entries from 250 monitoring points, including settings changes, power ups, and Relay Word bit elements that you select. Set element names to easily understood aliases.

Digital Relay-to-Relay Communication. Use MIRRORED BITS communications to monitor internal element conditions between relays within a substation and between substations by using communication channels (SEL fiber-optic transceivers to send a direct transfer trip, for example).

Ethernet Communications Capability. Implement control and data gathering capabilities via substation LANs (local area networks) and company WANs (wide area networks) with the optional Ethernet card. Employ the FTP protocol for system data acquisition. Use Telnet for remote terminal interface. Use DNP3 and IEC 61850 for SCADA. Employ SNTP or PTP for time synchronization.

Computer Software and Settings Reduction. Use the rules-based settings editor, QuickSet, to develop settings offline. Internal relay programming shows only the settings for the functions and elements you have enabled.

Low-Energy Analog (LEA) Voltage Inputs (Ordering Option). Connect the low-level voltage outputs from less-costly power system voltage transducers to three-phase LEA voltage inputs on the SEL-487E.

Models and Options

NOTE: When used in TiDL applications, the relay is only available in the 4U chassis.

Depending on the number of interface boards, the SEL-487E is available in 5U (no interface boards), 6U (one interface board), or 7U sizes (two interface boards) (U is one rack unit in height—44.45 mm or 1.75 inches). Select I/O boards from a choice of four interface boards, each board designed to provide a wide range of input and output combinations to tailor the relay for your specific application. If your application requires more I/O, add contact I/O with the SEL-2505/SEL-2506 Remote I/O Module.

Firmware Options

The SEL-487E comes in two different ordering options: Transformer Protection Relay (SEL-487E-3) and Station Phasor Measurement Unit (SEL-487E-4). The only difference between the two options is the front overlay labeling. On the SEL-487E-3, the front overlay reads "Protection Automation Control." On the SEL-487E-4, the front overlay reads "Station Phasor Measurement Unit." All the relay functionality is the same in the two versions.

Current Channel Options

Select the CT secondary current for any one of the five windings (S, T, U, W, X) from 1 A or 5 A (all three phases 1 A or 5 A). For neutral windings (the three inputs of Winding Y), you can separately select the CT secondary current for each of the three inputs. For example, select 5 A secondary currents for the three phases of Winding S, 5 A secondary currents for the three phases of Winding T, 1 A secondary currents for the three phases of Winding U, 5 A secondary current for REF 1 (first neutral current input), and 1 A secondary current for REF 2 (second neutral current input).

Although each three-phase winding (S, T, U, W, and X) can be either 1 A or 5 A, and the Y-windings either 1 A or 5 A on a per-phase basis, the SEL-487E supports only the combinations shown in *Table 1.1*.

Table 1.1   Supported 1 A/5 A Windings Combinations

Windings S, T, U	Windings W, X, IY1, IY2, IY3
Winding S = 5 A Winding T = 5 A Winding U = 5 A	Winding W = 5 A Winding X = 5 A Winding IY1, IY2, IY3 = 5 A, 5 A, 5 A
Winding S = 5 A Winding T = 5 A Winding U = 1 A	Winding W = 5 A Winding X = 5 A Winding IY1, IY2, IY3 = 5 A, 5 A, 1 A
Winding S = 5 A Winding T = 1 A Winding U = 1 A	Winding W = 5 A Winding X = 5 A Winding IY1, IY2, IY3 = 5 A, 1 A, 1 A
Winding S = 1 A Winding T = 1 A Winding U = 1 A	Winding W = 5 A Winding X = 5 A Winding IY1, IY2, IY3 = 1 A, 1 A, 1 A Winding W = 1A Winding X = 1A Winding IY1, IY2, IY3 = 5 A, 5 A, 5 A Winding W = 1 A Winding X = 1 A Winding IY1, IY2, IY3 = 5 A, 5 A, 1 A Winding W = 1 A Winding X = 1 A Winding IY1, IY2, IY3 = 5 A, 1 A, 1 A Winding W = 1 A Winding X = 1 A Winding IY1, IY2, IY3 = 1 A, 1 A, 1 A

Voltage Channel Options

➤ 300 V phase-to-neutral wye configuration PT inputs

➤ Two three-phase, 8 Vac, C37.92-compliant LEA inputs

Connector Type

➤ Screw-terminal block inputs

➤ Connectorized

Conformal Coat

Conformal coating provides an additional barrier to harsh environments, such as high humidity and airborne contaminants. See selinc.com/conformalcoating/ for more information.

Interface Board (I/O) Options

Select from four interface boards to provide flexibility with the diverse I/O requirements when installing the SEL-487E at power plants, transmission and distribution networks. You can install the interface boards in any combination in the relay. *Table 1.2* provides I/O information about the main board and the four interface boards.

Table 1.2 Main Board and Interface Board Information

Board Name	Inputs	Description	Outputs	Description
Main	5	Optoisolated, independent, level-sensitive	3	High-current interrupting, Form A
	2	Optoisolated, common, level-sensitive	2	Standard Form A
			3	Standard Form C
INT2	8	Optoisolated, independent, level-sensitive	13	Standard Form A
			2	Standard Form C
INT4	18	Two sets of 9 common optoisolated, level-sensitive	6	High-speed, high-current interrupting, Form A
	6	Optoisolated, independent, level-sensitive	2	Standard Form A
INT7	8	Optoisolated, independent, level-sensitive	13	High-current interrupting, Form A
			2	Standard Form C
INT8	8	Optoisolated, independent, level-sensitive	8	High-speed, high-current interrupting, Form A

Voltage ranges for the inputs on the main board as well as for the inputs on the four interface boards are as follows:

➤ 24 Vdc
➤ 48 Vdc
➤ 110 Vdc
➤ 125 Vdc
➤ 220 Vdc
➤ 250 Vdc

Power Supply Options

➤ 24–48 Vdc
➤ 48–125 Vdc or 110–120 Vac
➤ 125–250 Vdc or 110–240 Vac

Ethernet Connection Options

Ethernet card with combinations of 10/100BASE-T and 100BASE-FX media connections on each of two ports.

Ethernet Communications Protocols

➤ Standard (FTP, Telnet, DNP3, PRP)
➤ Standard plus IEC 61850

Ordering Assistance

Contact the SEL factory or your local Technical Service Center for ordering information (see *Technical Support on page 3.43*). You can also view the latest ordering information on the SEL website at selinc.com.

Applications

Use the SEL-487E for as many as five restraint windings for transformers at power plants, transmission stations, distribution stations, and industrial plants. For information on connecting the relay, see *Section 2: Installation*. The figures in this section illustrate selected relay applications.

The SEL-487E supports remote data acquisition through use of the SEL-2240 Axion. The SEL Axion provides remote analog and digital data over an IEC 61158 EtherCAT TiDL network. This technology provides very low and deterministic latency over a point-to-point architecture. The SEL-487E can receive as many as eight fiber-optic links from as many as eight Axion remote data acquisition nodes. See *Section 2: Installation* for more details about TiDL applications.

Autotransformer

Figure 1.3 shows the SEL-487E applied to an autotransformer with both HV and LV busbars configured as breaker-and-a-half busbars. In this application, the relay accepts current transformer inputs from four phase current transformers, and one neutral current transformer, and PT inputs from both HV and LV busbars.

Figure 1.3 Autotransformer Application

By wiring the potential transformers into the relay, all protection elements requiring voltage inputs such as volts/hertz, under- and overpower elements, and directional elements become available. In addition to these protection functions, control functions, and data collection functions such as the frequency elements (underfrequency load shedding), synchrophasors (system data), and power metering data (real power, reactive power, energy, and power factor) also become available with the PT input.

Transformer With Grounding Bank

Figure 1.4 shows a wye-delta transformer with a grounding bank on the delta side. This installation calls for restricted earth fault protection (REF) on both the grounded wye winding and the grounding bank. Winding Y of the SEL-487E is dedicated to REF protection and includes three independent REF elements. In this application, the HV side has phase CT ratios of 800/1 and a neutral CT ratio of 800/5. On the LV side, the phase CT ratio is 2000/5 and the neutral CT of the grounding bank (NEC/R/T) is 100/1. Note that the ratio of the phase CT to the neutral CT on the LV side is 2000/100 = 20, well within the 35:1 CT mismatch capability of the relay.

Figure 1.4 Wye-Delta Transformer With Grounding Bank

Remote Breaker Application

Figure 1.5 shows an application where the transformer HV breaker is at a remote location. In this application, protect the power transformer with the SEL-487E, then use MIRRORED BITS communication to trip the remote HV breaker when the relay operates. After relay operation, the MIRRORED BITS trip information reaches the remote HV breaker in four milliseconds, ensuring fast clearance of the faulty transformer.
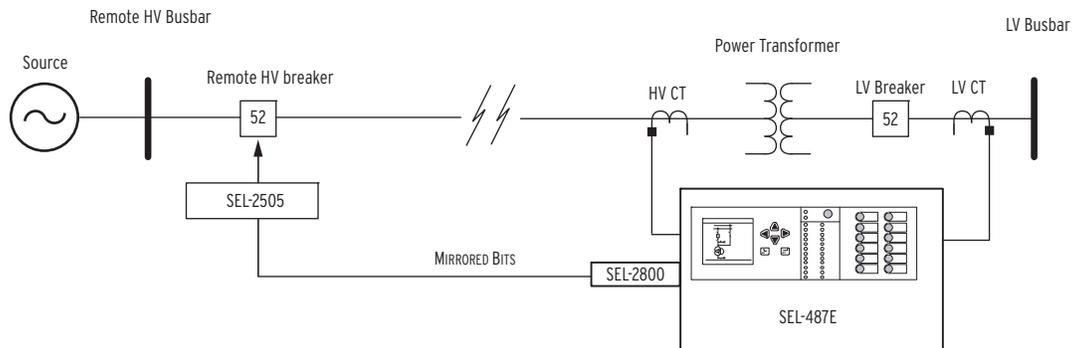
Figure 1.5 Installation With Remote HV Breaker

Application Highlights

Table 1.3 lists applications and key features of the relay.

Table 1.3 Application Highlights (Sheet 1 of 2)

Application	Key Features
Installation at power plants, transmission stations, and distribution stations	➤ Unique combination of protection including V/Hz), control, and monitoring makes the relay suitable for most transformer applications. ➤ Patented adaptive-slope differential characteristic provides fast tripping time.
Impedance-grounded systems	Three independent restricted earth fault elements provide sensitive ground fault protection.
Wye-delta transformers	The standard matrix settings compensate for all 30-degree transformer winding phase shifts.

Table 1.3   Application Highlights (Sheet 2 of 2)

Application	Key Features
Unit transformers, cogeneration	➤ Two separate V/Hz settings; one setting for a loaded transformer and one setting for an unloaded transformer. ➤ Use the built-in synchrophasors to synchronize the generator with the power system. ➤ Reverse power elements control power flow.
1 A CT secondary (HV REF) 5 A CT secondary (LV REF) or vice versa	Provides a choice of 1 A or 5 A CT secondary currents among the phases of Winding Y, or vice versa.
Large CT ratio mismatch among windings	The SEL-487E accepts a ratio mismatch of 35:1 among CTs; i.e., CT ratios of 3500/5 and 100/5.
Backup protection feeder overcurrent protection	Numerous voltage-polarized directional and nondirectional phase, negative-sequence, and zero-sequence 50 and 51 elements.
Optimize circuit breaker maintenance	Use the per-phase circuit breaker monitoring to calculate the circuit breaker contact wear.
Balance transformer insulation life aging with temporary overloading	Calculate the accelerated aging factor for the insulation with the IEEE C57.91-1995 transformer thermal model.
Collect through-fault data and the calculated damage on the transformer windings	Based on IEEE C57.109-1993, the through-fault monitor calculates mechanical and electrical damage to the transformer resulting from through faults.
Remote Data Acquisition[a]	The TiDL SEL-487E works with a time-domain link (TiDL) system.

[a] If the relay is using a remote data acquisition system, such as TiDL, the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Product Characteristics

Each SEL-400-series relay shares common features, but has unique characteristics. *Table 1.4* summarizes the unique characteristics for the SEL-487E.

Table 1.4   SEL-487E Relay Characteristics (Sheet 1 of 2)

Characteristic	Value
Standard Processing Rate	8 times per cycle
Battery Monitor	One
Autorecloser	None
MBG Protocol	Not supported
SELOGIC	
Protection Free-Form	250 lines
Automation Free-Form	10 blocks of 100 lines each
SELOGIC Variables	64 protection 256 automation
SELOGIC Math Variables	64 protection 256 automation
Conditioning Timers	32 protection 32 automation
Sequencing Timers	32 protection 32 automation
Counters	32 protection 32 automation
Latch Bits	32 protection 32 automation

Table 1.4   SEL-487E Relay Characteristics (Sheet 2 of 2)

Characteristic	Value
Control	
Remote Bits	32
Breakers	Five: S, T, U, W, X Three-pole only
Disconnects	20
Bay Control	Supported
Metering	
Maximum/Minimum Metering	Not supported
Energy Metering	Supported

Specifications

Note: If the relay is using a remote data acquisition system, such as TiDL, the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay. Element operate times will also have this small added delay.

Compliance

Designed and manufactured under an ISO 9001 certified quality management system

47 CFR 15B Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference in which case the user will be required to correct the interference at his own expense.

UL Listed to U.S. and Canadian safety standards
(File E212775; NRGU, NRGU7)

CE Mark

General

AC Analog Inputs

Sampling Rate:	8 kHz

AC Current Inputs (Secondary Circuits)

Note: Current transformers are Measurement Category II.

Input Current

5 A Nominal:	S, T, U, W, X, and Y terminals
1 A Nominal:	S. T, U, W, X, and Y terminals
1 A/5 A Nominal:	Y terminal only (REF)

Current Rating (With DC Offset at X/R = 10, 1.5 cycles)

5 A Nominal:	91.0 A
1 A Nominal:	18.2 A

Continuous Thermal Rating

5 A Nominal:	15 A 20 A (+55°C)
1 A Nominal:	3 A 4 A (+55°C)

Saturation Current (Linear) Rating

5 A Nominal:	100 A
1 A Nominal:	20 A

One-Second Thermal Rating

5 A Nominal:	500 A
1 A Nominal:	100 A

One-Cycle Thermal Rating

5 A Nominal:	1250 A-peak
1 A Nominal:	250 A-peak

Burden Rating

5 A Nominal:	≤0.5 VA at 5 A
1 A Nominal:	≤0.1 VA at 1 A

A/D Current Limit

Note: Signal clipping may occur beyond this limit.

5 A Nominal:	247.5 A
1 A Nominal:	49.5 A

AC Voltage Inputs

Three-phase, four-wire (wye) connections are supported.

Rated Voltage Range:	67–250 V_{LN}
Operational Voltage Range:	0–300 V_{LN}
Ten-Second Thermal Rating:	600 Vac
Burden:	≤0.1 VA @ 125 V

LEA Voltage Inputs

Rated Voltage Range:	4 V_{L-N}
Operational Voltage Range:	0–8 V_{L-N}
Ten-Second Thermal Rating:	300 Vac
Input Impedance:	1 MΩ

Frequency and Rotation

Rotation:	ABC ACB
Nominal Frequency Rating:	50 ±5 Hz 60 ±5 Hz
Frequency Tracking (Requires PTs):	Tracks between 40.0–65.0 Hz Below 40.0 Hz = 40.0 Hz Above 65.0 Hz = 65.0 Hz
Maximum Slew Rate:	15 Hz/s

Power Supply

24-48 Vdc

Rated Voltage:	24–48 Vdc
Operational Voltage Range:	18–60 Vdc
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	20 ms at 24 Vdc, 100 ms at 48 Vdc per IEC 60255-26:2013
Burden:	<35 W

48-125 Vdc or 110-120 Vac

Rated Voltage:	48–125 Vdc, 110–120 Vac
Operational Voltage Range:	38–140 Vdc 85–140 Vac
Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	14 ms @ 48 Vdc, 160 ms @ 125 Vdc per IEC 60255-26:2013
Burden:	<35 W, <90 VA

125-250 Vdc or 110-240 Vac

Rated Voltage:	125–250 Vdc, 110–240 Vac
Operational Voltage Range:	85–300 Vdc 85–264 Vac
Rated Frequency:	50/60 Hz
Operational Frequency Range:	30–120 Hz
Vdc Input Ripple:	15% per IEC 60255-26:2013
Interruption:	46 ms @ 125 Vdc, 250 ms @ 250 Vdc per IEC 60255-26:2013
Burden:	<35 W, <90 VA

Control Outputs

Standard

Make:	30 A
Carry:	6 A continuous carry at 70°C 4 A continuous carry at 85°C
1 s Rating:	50 A
MOV Protection (maximum voltage):	250 Vac, 330 Vdc
Pickup/Dropout Time:	≤6 ms, resistive load
Update Rate:	1/8 cycle

Breaking Capacity (10,000 Operations) per IEC 60255-23:1994

24 Vdc	0.75 A	L/R = 40 ms
48 Vdc	0.50 A	L/R = 40 ms
125 Vdc	0.30 A	L/R = 40 ms
250 Vdc	0.20 A	L/R = 20 ms

Cyclic Capacity (10,000 Operations) per IEC 60255-23:1994
Rate: 2.5 cycles/second for 4 seconds followed by 2 minutes idle for thermal dissipation

24 Vdc	0.75 A	L/R = 40 ms
48 Vdc	0.50 A	L/R = 40 ms
125 Vdc	0.30 A	L/R = 40 ms
250 Vdc	0.20 A	L/R = 20 ms

Hybrid (High-Current Interrupting)

Make:	30 A
Carry:	6 A continuous carry at 70°C 4 A continuous carry at 85°C
1 s Rating:	50 A
MOV Protection (Maximum Voltage):	330 Vdc
Pickup/Dropout Time:	≤6 ms, resistive load
Update Rate:	1/8 cycle

Breaking Capacity (10,000 Operations) per IEC 60255-23:1994

24 Vdc	10.0 A	L/R = 40 ms
48 Vdc	10.0 A	L/R = 40 ms
125 Vdc	10.0 A	L/R = 40 ms
250 Vdc	10.0 A	L/R = 20 ms

Cyclic Capacity (10,000 Operations) per IEC 60255-23:1994
Rate: 2.5 cycles/second for 4 seconds followed by 2 minutes idle for thermal dissipation

24 Vdc	10.0 A	L/R = 40 ms
48 Vdc	10.0 A	L/R = 40 ms
125 Vdc	10.0 A	L/R = 40 ms
250 Vdc	10.0 A	L/R = 20 ms

Note: Do not use hybrid control outputs to switch ac control signals. These outputs are polarity-dependent.

High-Speed, High-Current Interrupting

Make:	30 A
Carry:	6 A continuous carry at 70°C 4 A continuous carry at 85°C
1 s Rating:	50 A
MOV Protection (Maximum Voltage):	250 Vac/330 Vdc
Pickup Time:	≤10 µs, resistive load
Dropout Time:	≤8 ms, resistive load
Update Rate:	1/8 cycle

Breaking Capacity (10,000 Operations) per IEC 60255-23:1994

24 Vdc	10.0 A	L/R = 40 ms
48 Vdc	10.0 A	L/R = 40 ms
125 Vdc	10.0 A	L/R = 40 ms
250 Vdc	10.0 A	L/R = 20 ms

Cyclic Capacity (10,000 Operations) per IEC 60255-23:1994
Rate: 2.5 cycles/second for 4 seconds, followed by 2 minutes idle for thermal dissipation

24 Vdc	10.0 A	L/R = 40 ms
48 Vdc	10.0 A	L/R = 40 ms
125 Vdc	10.0 A	L/R = 40 ms
250 Vdc	10.0 A	L/R = 20 ms

Note: Make rating per IEEE C37.90-2005.
Note: Per IEC 61810-2:2005.

Control Inputs

Optoisolated (Use With AC or DC Signals)

Main Board:	5 inputs with no shared terminals 2 inputs with shared terminals
INT2, INT7, and INT8 Interface Boards:	8 inputs with no shared terminals

INT4 Interface Board:	6 inputs with no shared terminals
	18 inputs with shared terminals
	  (2 groups of 9 inputs with each group
	  sharing one terminal)

Voltage Options:	24, 48, 110, 125, 220, 250 V
Current Drawn:	<5 mA at nominal voltage <8 mA for 110 V option
Sampling Rate:	2 kHz

DC Thresholds (Dropout Thresholds Indicate Level-Sensitive Option)

24 Vdc:	Pickup 19.2–30.0 Vdc; Dropout <14.4 Vdc
48 Vdc:	Pickup 38.4–60.0 Vdc; Dropout <28.8 Vdc
110 Vdc:	Pickup 88.0–132.0 Vdc; Dropout <66.0 Vdc
125 Vdc:	Pickup 105–150 Vdc; Dropout <75 Vdc
220 Vdc:	Pickup 176–264 Vdc; Dropout <132 Vdc
250 Vdc:	Pickup 200–300 Vdc; Dropout <150 Vdc

AC Thresholds (Ratings Met Only When Recommended Control Input Settings Are Used—see *Table 2.1*.)

24 Vac:	Pickup 16.4–30.0 Vac rms; Dropout <10.1 Vac rms
48 Vac:	Pickup 32.8–60.0 Vac rms; Dropout <20.3 Vac rms
110 Vac:	Pickup 75.1–132.0 Vac rms; Dropout <46.6 Vac rms
125 Vac:	Pickup 89.6–150.0 Vac rms; Dropout <53.0 Vac rms
220 Vac:	Pickup 150.3–264 Vac rms; Dropout <93.2 Vac rms
250 Vac:	Pickup 170.6–300 Vac rms; Dropout <106 Vac rms

Communications Ports

EIA-232:	1 Front and 3 Rear
Serial Data Speed:	300–57600 bps

Communications Card Slot for Optional Ethernet Card

Ordering Options:	10/100BASE-T
Connector Type:	RJ45
Ordering Option:	100BASE-FX Fiber-Optic
Connector Type:	LC
Fiber Type:	Multimode
Wavelength:	1300 nm
Source:	LED

Min. TX Power:	–19 dBm
Max. TX Power:	–14 dBm
RX Sensitivity:	–32 dBm
Sys. Gain:	13 dB

Communications Ports for Optional TiDL Interface

EtherCAT Fiber-Optic

Ports:	8
Data Rate:	Automatic
Connector Type:	LC fiber
Protocols:	Dedicated EtherCAT

Class 1 LASER/LED

Wavelength:	1300 nm
Fiber Type:	Multimode
Link Budget:	11 dB
Min. TX Power:	–20 dBm
Min. RX Sensitivity:	–31 dBm
Fiber Size:	50–200 μm
Approximate Range:	2 km
Data Rate:	100 Mbps
Typical Fiber Attenuation:	–2 dB/km

Time Inputs

IRIG Time Input–Serial Port 1

Input:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc
Operational Voltage Range:	0–8 Vdc
Logic High Threshold:	≥2.8 Vdc
Logic Low Threshold:	≤0.8 Vdc
Input Impedance:	2.5 kΩ

IRIG-B Input–BNC Connector

Input:	Demodulated IRIG-B
Rated I/O Voltage:	5 Vdc
Operational Voltage Range:	0–8 Vdc
Logic High Threshold:	≥2.2 Vdc
Logic Low Threshold:	≤0.8 Vdc
Input Impedance:	>1 kΩ
Dielectric Test Voltage:	0.5 kVac

PTP–Ethernet Port 5A, 5B

Input:	IEEE 1588 PTPv2
Profiles:	Default, C37.238-2011 (Power Profile)
Synchronization Accuracy:	±100 ns @ 1-second synchronization intervals when communicating directly with master clock

Operating Temperature

–40° to +85°C (–40° to +185°F)

Note: LCD contrast impaired for temperatures below –20° and above +70°C

Humidity

5% to 95% without condensation

Weight (Maximum)

4U Rack Unit (TiDL only):	6.4 kg (14.1 lb)
5U Rack Unit:	13.2 kg (29.2 lb)
6U Rack Unit:	15.1 kg (33.3 lb)
7U Rack Unit:	16.4 kg (36.2 lb)

Terminal Connections

Rear Screw-Terminal Tightening Torque, #8 Ring Lug

Minimum:	1.0 Nm (9 in-lb)
Maximum:	2.0 Nm (18 in-lb)

User terminals and stranded copper wire should have a minimum temperature rating of 105°C. Ring terminals are recommended.

Wire Sizes and Insulation

Wire sizes for grounding (earthing), current, voltage, and contact connections are dictated by the terminal blocks and expected load currents. You can use the following table as a guide in selecting wire sizes. The grounding conductor should be as short as possible and sized equal to or greater than any other conductor connected to the device, unless otherwise required by local or national wiring regulations.

Connection Type	Min. Wire Size	Max. Wire Size
Grounding (Earthing) Connection	14 AWG (2.5 mm^2)	N/A
Current Connection	16 AWG (1.5 mm^2)	10 AWG (5.3 mm^2)
Potential (Voltage) Connection	18 AWG (0.8 mm^2)	14 AWG (2.5 mm^2)
Contact I/O	18 AWG (0.8 mm^2)	10 AWG (5.3 mm^2)
Other Connection	18 AWG (0.8 mm^2)	10 AWG (5.3 mm^2)

Type Tests

Installation Requirements

Overvoltage Category:	3
Pollution Degree:	2

Safety

Product Standards	IEC 60255-27:2013 IEEE C37.90-2005 21 CFR 1040.10
Dielectric Strength:	IEC 60255-27:2013, Section 10.6.4.3 2.5 kVac, 50/60 Hz for 1 min: Analog Inputs, Contact Outputs, Digital Inputs 3.6 kVdc for 1 min: Power Supply, Battery Monitors 2.2 kVdc for 1 min: IRIG-B 1.1 kVdc for 1 min: Ethernet
Impulse Withstand:	IEC 60255-27:2013, Section 10.6.4.2 IEEE C37.90-2005 Common Mode: ±1.0 kV: Ethernet ±2.5 kV: IRIG-B ±5.0 kV: All other ports Differential Mode: 0 kV: Analog Inputs, Ethernet, IRIG-B, Digital Inputs ±5.0 kV: Standard Contact Outputs, Power Supply Battery Monitors +5.0 kV: Hybrid Contact Outputs
Insulation Resistance:	IEC 60255-27:2013, Section 10.6.4.4 >100 MΩ @ 500 Vdc
Protective Bonding:	IEC 60255-27:2013, Section 10.6.4.5.2 <0.1 Ω @ 12 Vdc, 30 A for 1 min
Object Penetration:	IEC 60529:2001 + CRGD:2003 Protection Class: IP30
Max Temperature of Parts and Materials:	IEC 60255-27:2013, Section 7.3
Flammability of Insulating Materials:	IEC 60255-27:2013, Section 7.6 Compliant

Electromagnetic (EMC) Immunity

Product Standards:	IEC 60255-26:2013
	IEC 60255-27:2013
	IEEE C37.90-2005
Surge Withstand Capability (SWC):	IEC 61000-4-18:2006 + A:2010
	IEEE C37.90.1-2012
	Slow Damped Oscillatory, Common and Differential Mode:
	±1.0 kV
	±2.5 kV
	Fast Transient, Common and Differential Mode:
	±4.0 kV
Electrostatic Discharge (ESD):	IEC 61000-4-2:2008
	IEEE C37.90.3-2001
	Contact:
	±8 kV
	Air Discharge:
	±15 kV
Radiated RF Immunity:	IEEE C37.90.2-2004
	IEC 61000-4-3:2006 + A1:2007 + A2:2010
	20 V/m (>35 V/m, 80% AM, 1 kHz)
	Sweep: 80 MHz to 1 GHz
	Spot: 80, 160, 450, 900 MHz
	10 V/m (>15 V/m, 80% AM, 1 kHz)
	Sweep: 80 MHz to 1 GHz
	Sweep: 1.4 GHz to 2.7 GHz
	Spot: 80, 160, 380, 450, 900, 1850, 2150 MHz
Electrical Fast Transient Burst (EFTB):	IEC 61000-4-4:2012
	Zone A:
	±2 kV: Communication ports
	±4 kV: All other ports
Surge Immunity:	IEC 61000-4-5:2005
	Zone A:
	±2 kV$_{L-L}$
	±4 kV$_{L-E}$
	±4 kV: communication ports (Ethernet)
	Note: Cables connected to EIA-422, G.703, EIA-232, and IRIG-B communications ports shall be less than 10 m in length for Zone A compliance.
	Zone B:
	±1 kV$_{L-L}$: 24–48 Vdc power supply
	±2 kV$_{L-E}$: 24–48 Vdc power supply
	±2 kV: communication ports (except Ethernet)
	Note: Cables connected to EIA-232 communications ports shall be less than 10 m in length for Zone B compliance.
Conducted Immunity:	IEC 61000-4-6:2013
	20 V/m; (>35 V/m, 80% AM, 1 kHz)
	Sweep: 150 kHz–80 MHz
	Spot: 27, 68 MHz
Power Frequency Immunity (DC Inputs):	IEC 61000-4-16:2015
	Zone A:
	Differential: 150 V$_{RMS}$
	Common Mode: 300 V$_{RMS}$
Power Frequency Magnetic Field:	IEC 61000-4-8:2009
	Level 5:
	100 A/m; ≥60 Seconds; 50/60 Hz
	1000 A/m 1 to 3 Seconds; 50/60 Hz
	Note: 50G1P ≥0.05 (ESS = N, 1, 2)
	50G1P ≥0.1 (ESS = 3, 4)

Power Supply Immunity:	IEC 61000-4-11:2004
	IEC 61000-4-17:1999/A1:2001/A2:2008
	IEC 61000-4-29:2000
	AC Dips & Interruptions
	Ripple on DC Power Input
	DC Dips & Interruptions
	Gradual Shutdown/Startup (DC only)
	Discharge of Capacitors
	Slow Ramp Down/Up
	Reverse Polarity (DC only)
Damped Oscillatory Magnetic Field:	IEC 61000-4-10:2016
	Level 5:
	100 A/m

EMC Compatibility

Product Standards:	IEC 60255-26:2013
	47 CFR
	ICES-003
Emissions:	IEC 60255-26:2013, Section 7.1
	47 CFR Part 15.109
	47 CFR Part 15.107
	ICES-003, Issue 6
	Radiated:
	Class A
	Conducted:
	Class A

Environmental

Product Standards:	IEC 60255-27:2013
Cold, Operational:	IEC 60068-2-1:2007
	Test Ad: 16 hours at –40°C
Cold, Storage:	IEC 60068-2-1:2007
	Test Ad: 16 hours at –40°C
Dry Heat, Operational:	IEC 60068-2-2:2007
	Test Bd: 16 hours at +85°C
Dry Heat, Storage:	IEC 60068-2-2:2007
	Test Bd: 16 hours at +85°C
Damp Heat, Cyclic:	IEC 60068-2-30:2005
	Test Db: +25 °C to +55°C, 6 cycles (12 + 12-hour cycle), 95% RH
Damp Heat, Steady State:	IEC 60068-2-78:2013
	Severity: 93% RH, +40°C, 10 days
Cyclic Temperature:	IEC 60068-2-14:2009
	Test Nb: –40°C to +80°C, 5 cycles
Vibration Resistance:	IEC 60255-21-1:1988
	Class 2 Endurance, Class 2 Response
Shock Resistance:	IEC 60255-21-2:1988
	Class 1 Shock Withstand, Class 1 Bump Withstand, Class 2 Shock Response
Seismic:	IEC 60255-21-3:1993
	Class 2 Quake Response

Reporting Functions

High-Resolution Data

Rate:	8000 samples/second
	4000 samples/second
	2000 samples/second
	1000 samples/second
Output Format:	Binary COMTRADE

Note: Per IEEE C37.111-1999 and IEEE C37.111-2013, *Common Format for Transient Data Exchange (COMTRADE) for Power Systems*.

Event Reports

Length:	0.25–24 seconds (based on LER and SRATE settings)
Volatile Memory:	3 s of back-to-back event reports sampled at 8 kHz
Nonvolatile Memory:	At least 4 event reports of a 3 s duration sampled at 8 kHz
Resolution:	4 and 8 samples/cycle

Event Summary

Storage:	100 summaries

Breaker History

Storage:	128 histories

Sequential Events Recorder

Storage:	1000 entries
Trigger Elements:	250 relay elements
Resolution:	0.5 ms for contact inputs
Resolution:	1/8 cycle for all elements

Processing Specifications

AC Voltage and Current Inputs

8000 samples per second, 3 dB low-pass analog filter cut-off frequency at 2.8 kHz, ±5%
Digital filtering
Full-cycle cosine after low-pass analog filtering

Protection and Control Processing

8 times per power system cycle

Control Points

32 remote bits
32 local control bits
32 latch bits in protection logic
32 latch bits in automation logic

Relay Element Pickup Ranges and Accuracies

Differential Elements (General)

Number of Zones:	1 (A, B, and C elements)
Number of Windings:	5
TAP Pickup:	$(0.1–32.0) \cdot I_{NOM}$ A secondary
TAP Range:	$TAP_{MAX}/TAP_{MIN} \leq 35$
Time-Delay Accuracy:	±0.1% plus ±0.125 cycle

Differential Elements (Restraint)

Pickup Range:	0.1–4.0 per unit
Pickup Accuracy:	1 A nominal: ±5% ±0.02 A 5 A nominal: ±5% ±0.10 A
Pickup Time (If E87UNB = N):	1.25 minimum cycle 1.38 typical cycle 1.5 maximum cycle
Pickup Time (If E87UNB = Y):	0.5 minimum cycle 0.75 typical cycle 1.5 maximum cycle
Slope 1	
Setting Range:	5%–100%
Slope 2	
Setting Range:	5%–100%

Differential Elements (Unrestraint)

Pickup Range:	$(1.0–20.0) \cdot TAP$
Pickup Accuracy:	±5% of user setting, $±0.02 \cdot I_{NOM}$ A

Pickup Time (Filtered Unrestraint):	0.7 minimum cycle 0.85 typical cycle 1.2 maximum cycle
Pickup Time (Raw Unrestraint):	0.25 minimum cycle 0.5 typical cycle 1.0 maximum cycle

Note: The raw unrestraint pickup is set to $U87P \cdot \sqrt{2} \cdot 2$

Harmonic Elements (2nd, 4th, 5th)

Pickup Range:	OFF, 5–100% of fundamental
Pickup Accuracy:	1 A nominal ±5% ±0.02 A 5 A nominal ±5% ±0.10 A
Time-Delay Accuracy:	±0.1% plus ±0.125 cycle

Negative-Sequence Differential Element

Pickup Range:	0.05–1 per unit
Slope Range:	5–100%
Pickup Accuracy:	±5% of user setting, $±0.02 \cdot I_{NOM}$ A
Maximum Pickup/Dropout Time:	4 cycles
Winding Coverage:	2%

Incremental Restraint and Operating Threshold Current Supervision

Setting Range:	0.1–10.0 per unit
Accuracy:	$±5% ±0.02 \cdot I_{NOM}$

Open-Phase Detection Logic

3 elements per winding (S, T, U, W, X)

Pickup Range	
1 A Nominal:	0.04–1.00 A
5 A Nominal:	0.2–5.00 A
Maximum Pickup/Dropout Time:	0.625 cycle

Restricted Earth Fault (REF)

Elements

Three Independent Elements:	REF1, REF2, REF3

REF1F, REF1R (Element 1, forward and reverse)
REF2F, REF2R (Element 2, forward and reverse)
REF3F, REF3R (Element 3, forward and reverse)

Operating Quantity

Select:	IY1, IY2, IY3

Restraint Quantity

Select:	3I0S, 3I0T, 3I0U, 3I0W, and 3I0X
Pickup Range:	0.05–5 per unit 0.02–0.05 positive-sequence ratio factor (I0/I1)
Pickup Accuracy	
1 A Nominal:	0.01 A
5 A Nominal:	0.05 A
Maximum Pickup/Dropout Time:	1.75 cycles

Instantaneous/Definite-Time Overcurrent Elements (50)

Phase- and Negative-Sequence, Ground-Residual Elements

Pickup Range	
5 A Nominal:	0.25–100.00 A secondary, 0.01-A steps
1 A Nominal:	0.05–20.00 A secondary, 0.01-A steps

Accuracy (Steady State)

5 A Nominal:	±0.05 A plus ±3% of setting
1 A Nominal:	±0.01 A plus ±3% of setting

Transient Overreach (Phase and Ground Residual)

5 A Nominal:	±5% of setting, ±0.10 A
1 A Nominal:	±5% of setting, ±0.02 A

Transient Overreach (Negative Sequence)

5 A Nominal:	±6% of setting, ±0.10 A
1 A Nominal:	±6% of setting, ±0.02 A
Time-Delay Range:	0.00–16000.00 cycles, 0.125 cycle steps
Timer Accuracy:	±0.25 cycle plus ±0.1% of setting
Maximum Pickup/Dropout Time:	1.5 cycles

Adaptive Time-Overcurrent Elements (51)

Pickup Range (Adaptive Within the Range)

5 A Nominal:	0.25–16.00 A secondary, 0.01 A steps
1 A Nominal:	0.05–3.20 A secondary, 0.01 A steps

Accuracy (Steady State)

5 A Nominal:	±0.05 A plus ±3% of setting
1 A Nominal:	±0.01 A plus ±3% of setting

Transient Overreach

5 A Nominal:	±5% of setting, ±0.10 A
1 A Nominal:	±5% of setting, ±0.10 A

Time Dial Range (Adaptive Within the Range)

U.S.:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps
Curve Timing Accuracy:	±1.50 cycles plus ±4% of curve time (for current between 2 and 30 multiples of pickup)

Curves operate on definite time for current greater than 30 multiples of pickup.

Reset:	1 power cycle or Electromechanical Reset Emulation time

Combined Time-Overcurrent Elements (51)

Pickup Range

5 A Nominal:	0.25–16.00 A secondary, 0.01 A steps
1 A Nominal:	0.05–3.20 A secondary, 0.01 A steps

Accuracy (Steady State)

5 A Nominal:	±0.05 A plus ±3% of setting
1 A Nominal:	±0.01 A plus ±3% of setting

Transient Overreach

5 A Nominal:	±5% of setting, ±0.10 A
1 A Nominal:	±5% of setting, ±0.20 A

Time Dial Range

U.S.:	0.50–15.00, 0.01 steps
IEC:	0.05–1.00, 0.01 steps
Curve Timing Accuracy:	±1.50 cycles plus ±4% of curve time (for current between 2 and 30 multiples of pickup)

Curves operate on definite time for current greater than 30 multiples of pickup.

Reset:	1 power cycle or electromechanical reset emulation time

Phase Directional Elements (67)

Number:	5 (1 each for S, T, U, W, X)
Polarization:	Positive-sequence memory voltage Negative-sequence voltage
Time-Delay Range:	0.000–16,000 cycles, 0.125 cycle increment
Time-Delay Accuracy:	±0.1% of setting ±0.25 cycle

Phase-to-Phase Directional Elements

Number:	5 (1 each for S, T, U, W, X)
Polarization Quantity:	Negative-sequence voltage
Operate Quantity:	Negative-sequence current ($3I_2$)
Sensitivity:	$0.05 \cdot I_{NOM}$ A of secondary $3I_2$
Accuracy:	±0.05 Ω secondary
Transient Overreach:	+5% of set reach
Max. Delay:	1.75 cycles
Time-Delay Range:	0.000–16,000 cycles, 0.125-cycle increment
Time-Delay Accuracy:	±0.1% of setting ±0.25 cycle

Ground Directional Elements

Number:	5 (1 each for S, T, U, W, X)
Outputs:	Forward and Reverse
Polarization Quantity:	Zero-sequence voltage
Operate Quantity:	Zero-sequence current 3I0, where 3I0 = IA + IB + IC
Sensitivity:	$0.05 \cdot I_{NOM}$ of secondary 3I0
Accuracy:	±0.05 Ω secondary
Transient Overreach:	+5% of set reach
Max. Delay:	1.75 cycles

Undervoltage and Overvoltage Elements

Pickup Ranges

300 V Maximum Inputs

Phase Elements:	2–300 V_{LN} in 0.01-V steps
Phase-to-Phase Elements:	4–520 V_{LL} in 0.01-V steps
Sequence Elements:	2–300 V_{LN} in 0.01-V steps

8 V LEA Maximum Inputs (see *Potential Transformer (PT) Ratio Settings With LEA Inputs on page 5.2* for information on setting voltage elements when using LEA inputs.)

Phase Elements:	0.05–8.00 V
Phase-to-Phase Elements:	0.10–13.87 V
Sequence Elements:	0.05–8.00 V

Pickup Accuracy (Steady State)

Phase Elements:	±3% of setting, ±0.5 V
Phase-to-Phase Elements (Wye):	±3% of setting, ±0.5 V
Phase-to-Phase Elements (Delta):	±3% of setting, ±1 V
Sequence Elements:	±5% of setting, ±1 V

Pickup Accuracy (Transient Overreach)

Phase Elements:	±5%
Phase-to-Phase Elements (Wye):	±5%
Phase-to-Phase Elements (Delta):	±5%
Sequence Elements:	±5%

Maximum Pickup/Dropout Time

Phase Elements:	1.5 cycles
Phase-to-Phase Elements (Wye):	1.5 cycles
Sequence Elements:	1.5 cycles

Under- and Overfrequency Elements

Pickup Range:	40.01–69.99 Hz, 0.01-Hz steps
Accuracy, Steady State Plus Transient:	±0.005 Hz for frequencies between 40.00 and 70.00 Hz
Maximum Pickup/Dropout Time:	3.0 cycles
Time-Delay Range:	0.04–300.00 s, 0.001-s increment
Time-Delay Accuracy:	±0.1% ±0.0042 s
Pickup Range, Undervoltage Blocking:	20.00–200.00 V_{LN} (Wye) or V_{LL} (Open-Delta)
Pickup Accuracy, Undervoltage Blocking:	±2% ±0.5 V

Volts/Hertz Elements (24)

Definite-Time Element

Pickup Range:	100–200% steady state
Pickup Accuracy, Steady-State:	±1% of set point
Maximum Pickup/Dropout Time:	1.5 cycles
Time-Delay Range:	0.0–400.00 s
Time-Delay Accuracy:	±0.1% ±4.2 ms @ 60 Hz
Reset Time-Delay Range:	0.00–400.00 s

User-Definable Curve Element

Pickup Range:	100–200%
Pickup Accuracy:	±1% of set point
Reset Time-Delay Range:	0.00–400.00 s

Breaker-Failure Instantaneous Overcurrent

Setting Range

5 A Nominal:	0.50–50 A, 0.01-A steps
1 A Nominal:	0.10–10.0 A, 0.01-A steps

Accuracy

5 A Nominal:	±0.05 A, ±3% of setting
1 A Nominal:	±0.01 A, ±3% of setting

Transient Overreach

5 A Nominal:	±5%, ±0.10 A
1 A Nominal:	±5%, ±0.02 A
Maximum Pickup Time:	1.5 cycles
Maximum Dropout Time:	less than 1 cycle
Maximum Reset Time:	less than 1 cycle

Timers

Setting Range:	0–6000 cycles, 0.125-cycle steps
Time-Delay Accuracy:	±0.1% of setting ±0.125 cycle

Directional Overpower/Underpower Element

Operating Quantities:	OFF, 3PmF, 3QmF, 3PqpF, 3QqpF (m = S, T, U, W, X qp = ST, TU, UW, WX)
Pickup Range:	–20000.00 VA (secondary) to 20000.00 VA (secondary, 0.01 steps) Pickup range cannot fall within ±I_{NOM}
Pickup Accuracy:	±3% of setting and ±5 VA, power factor >±0.5 at nominal frequency

Time-Delay Range:	0.000–16,000 cycles, 0.25-cycle increment
Time-Delay Accuracy:	±0.1% of setting ±0.25 cycle

Bay Control

Breakers:	5 maximum
Disconnects (Isolators):	20 maximum

Timers

Setting Range:	1–99999 cycles, 1-cycle steps
Time-Delay Accuracy:	±0.1% of setting ±0.25 cycle

Station DC Battery System Monitor Specifications

Rated Voltage:	24–250 Vdc
Operational Voltage Range:	0–350 Vdc
Input Sampling Rate:	2 kHz
Processing Rate:	1/8 cycle
Operating Time:	≤1.5 seconds (element dc ripple) 1.5 cycles (all elements but dc ripple)

Setting Range

DC Settings:	1 Vdc Steps (OFF, 15–300 Vdc)
AC Ripple Setting:	1 Vac Steps (1–300 Vac)
Pickup Accuracy:	±10% ±2 Vdc (dc ripple) ±3% ±2 Vdc (all elements but dc ripple)

Metering Accuracy

All metering accuracies are based on an ambient temperature of 20°C and nominal frequency.

Absolute Phase-Angle Accuracy

IA, IB, and IC per Terminal:	±0.5° (both 1 and 5 A)
VA, VB, and VC Per Terminal:	±0.125°

Currents

Phase Current Magnitude

5 A Model:	±0.2% plus ±4 mA (2.5–15 A sec)
1 A Model:	±0.2% plus ±0.8 mA (0.5–3.0 A sec)

Phase Current Angle

All Models:	±0.2° in the current range (0.5–3.0) • I_{NOM}

Sequence Current Magnitude

5 A Model:	±0.3% plus ±4 mA (0.5–100 A s)
1 A Model:	±0.3% plus ±0.8 mA (0.1–20 A s)

Sequence Current Angle

All Models:	±0.3°

Voltages

300 V Maximum Inputs

Phase and Phase-to-Phase Voltage Magnitude:	±2.5% ±1 V (5–33.5 V) ±0.1% (33.5–300 V)
Phase and Phase-to-Phase Angle:	±1.0° (5–33.5 V) ±0.5° (33.5–300 V)
Sequence Voltage Magnitude (V1, V2, 3V0):	±2.5%, ±1 V (5–33.5 V) ±0.1% (33.5–300 V)
Sequence Voltage Angle (V1, V2, 3V0):	±1.0° (5–33.5 V) ±0.5° (33.5–300 V)

8 V LEA Maximum Inputs

Phase and Phase-to-Phase Voltage Magnitude:	±0.3% (0.2–0.6 V) ±0.1% (0.6–8.0 V)
Phase and Phase-to-Phase Angle:	±0.5° (0.2–8.00 V)

Sequence Voltage Magnitude (V1, V2, 3V0):	±0.3%, (0.2–0.6 V) ±0.1% (0.6–8.0 V)
Sequence Voltage Angle (V1, V2, 3V0):	±0.5° (0.2–8.00 V)

Power

MW (P), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

±1% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)
±0.7% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

MVAr (Q), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

±1% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 0, 0.5 lead, lag (1φ)
±0.7% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 0, 0.5 lead, lag (3φ)

MVA (S), Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

±1% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)
±0.7% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

PF, Per Phase (Wye), 3φ (Wye or Delta) Per Terminal

±1% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)
±0.7% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

Energy

MWh (P), Per Phase (Wye), 3φ (Wye or Delta)

±1% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 1, 0.5 lead, lag (1φ)
±0.7% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 1, 0.5 lead, lag (3φ)

MVARh (Q), Per Phase (Wye), 3φ (Wye or Delta)

±1% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 0, 0.5 lead, lag (1φ)
±0.7% (0.1–1.2) • I_{NOM}, 33.5–300 Vac, PF = 0, 0.5 lead, lag (3φ)

Demand/Peak Demand Metering

Time Constants:	5, 10, 15, 30, and 60 minutes
IA, IB, and IC per Terminal:	±0.2% ±0.0008 • I_{NOM}, (0.1–1.2) • I_{NOM}
3I2 per Terminal 3I0 (IG) per Terminal (Wye-Connected Only):	±0.3% ±0.0008 • I_{NOM}, (0.1–20) • I_{NOM}

Optional RTD Elements
(Models Compatible With SEL-2600 Series RTD Module)

12 RTD inputs via SEL-2600 Series RTD Module and SEL-2800 Fiber-Optic Transceiver

Monitor Ambient or Other Temperatures

PT 100, NI 100, NI 120, and CU 10 RTD-Types Supported, Field Selectable

As long as 500 m Fiber-Optic Cable to SEL-2600 Series RTD Module

Synchrophasor

Number of Synchrophasor Data Streams:	5

Number of Synchrophasors for Each Stream:
24 Phase Synchrophasors (6 Voltage and 18 Currents)
8 Positive-Sequence Synchrophasors (2 Voltage and 6 currents)

Number of User Analogs for Each Stream:	16
Number of User Digitals for Each Stream:	64
Synchrophasor Protocol:	IEEE C37.118-2005, SEL Fast Message (Legacy)
Synchrophasor Data Rate:	As many as 60 messages per second

Synchrophasor Accuracy

Voltage Accuracy:	±1% Total Vector Error (TVE) Range 30–150 V, f_{NOM} ±5 Hz
Current Accuracy:	±1% Total Vector Error (TVE) Range (0.1–2.0) • I_{NOM} A, f_{NOM} ±5 Hz
Synchrophasor Data Recording:	Records as much as 120 s IEEE C37.232-2011, File Naming Convention

Breaker Monitoring

Running Total of Interrupted Current (kA) per Pole:	±5% ±0.02 • I_{NOM}
Percent kA Interrupted for Trip Operations:	±5%
Percent Breaker Wear per Pole:	±5%
Compressor/Motor Start and Run Time:	±1 s
Time Since Last Operation:	±1 day

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Installation

The first steps in applying the SEL-487E relay are installing and connecting the relay. This section describes installation requirements for the physical configurations of the SEL-487E.

To install and connect the relay safely and effectively, you must be familiar with relay configuration features and options and relay jumper configuration. You should carefully plan relay placement, cable connections, and relay communication. This section also contains drawings of typical ac and dc connections to the SEL-487E (see *AC/DC Connection Diagrams on page 2.43*). Use these drawings as a starting point for planning your particular relay application. Consider the following when installing the SEL-487E.

It is also very important to limit access to the SEL-487E settings and control functions by using passwords. For information on relay access levels and passwords, see *Changing the Default Passwords in the Terminal on page 3.10 in the SEL-400 Series Relays Instruction Manual*.

For more introductory information on using the relay, see *Section 2: PC Software* and *Section 3: Basic Relay Operations in the SEL-400 Series Relays Instruction Manual*.

Shared Configuration Attributes

There are common or shared attributes among the many possible configurations of the SEL-487E. This section discusses the main shared features of the relay.

Relay Sizes

NOTE: When used in TiDL applications, the relay is only available in the 4U chassis.

SEL produces the 5U relay in horizontal and vertical rack-mount versions and horizontal and vertical panel-mount versions. The 6U and 7U versions are available in horizontal orientation only. Note that the 6U size is available with or without an additional I/O board. The 7U version has provision for two additional I/O boards. Relay sizes correspond to height in rack units, U, where U is approximately 44.45 mm (1.75 in). The relay is available in 4U, 5U, and 6U sizes.

Front-Panel Templates

Horizontal front-panel templates and vertical front-panel templates are the same for all sizes of the relay. *Figure 2.1* and *Figure 2.2* illustrate examples of horizontal and vertical front-panel templates. The front panel has three pockets for slide-in labels: one pocket for the target LED labels, and two pockets for the operator control labels. *Figure 2.1* and *Figure 2.2* show the front-panel pocket areas and openings for typical horizontal and vertical relay orientations; dashed lines denote the pocket areas. Refer to the instructions included in the Configurable Label kit for information on reconfiguring front-panel LED and pushbutton labels.
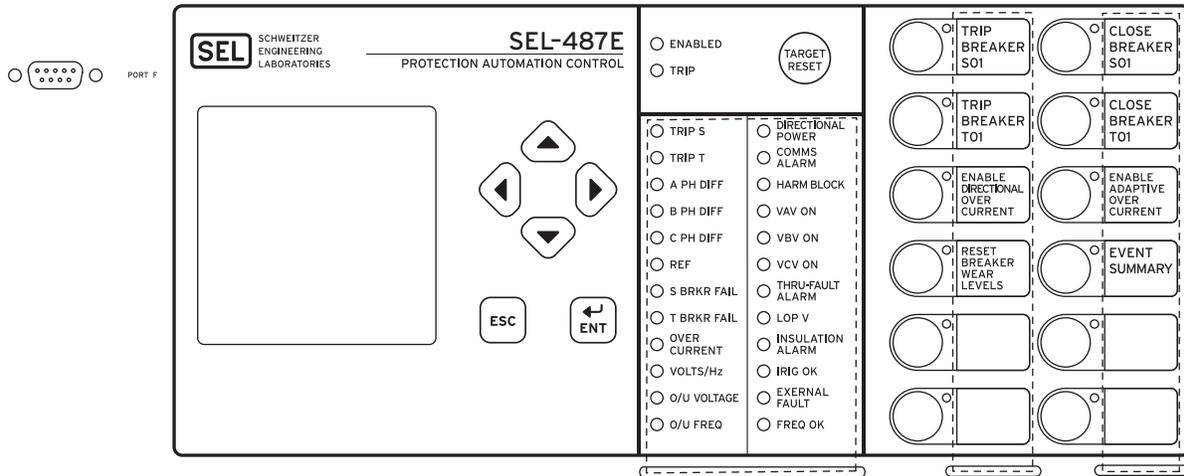
Figure 2.1   SEL-487E Horizontal Front Panel
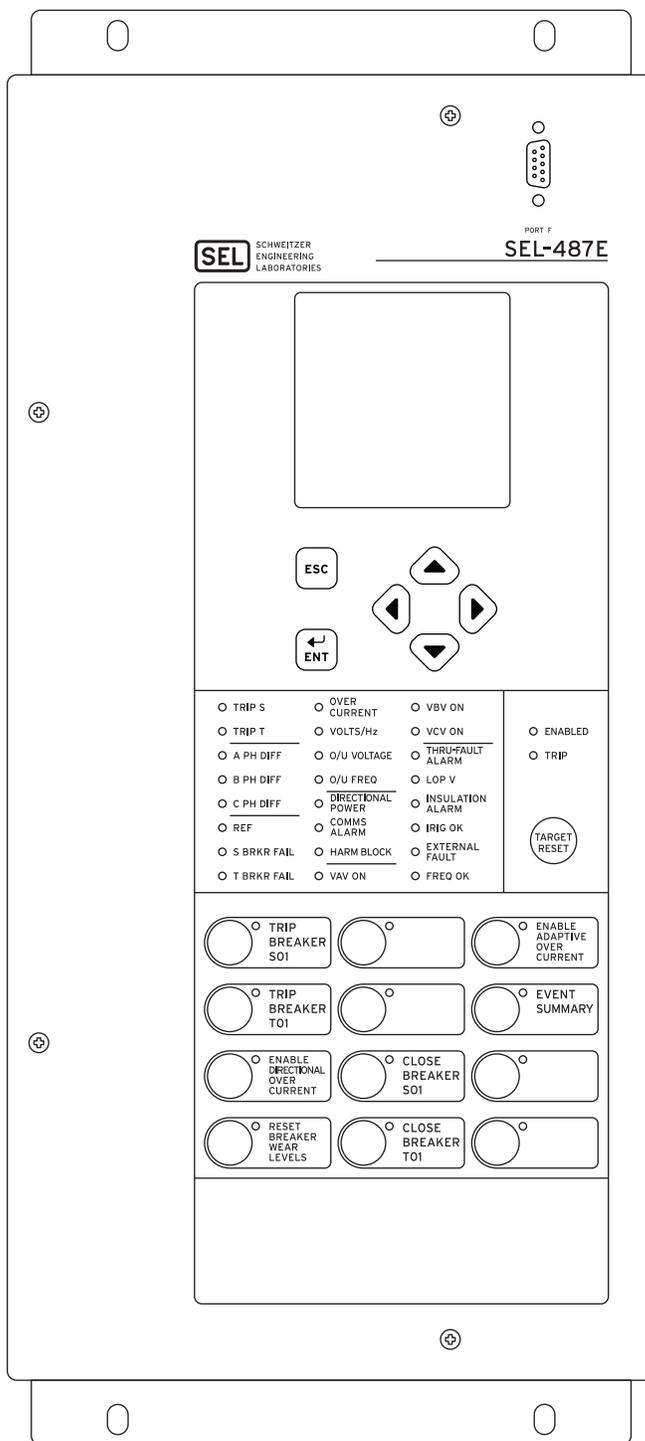
Figure 2.2   SEL-487E Vertical Front Panel

Rear Panels

Figure 2.3 shows the 7U rear panel with fixed terminal block analog inputs. *Figure 2.4* shows the 6U rear panel with Connectorized inputs. For clarity, these figures do not show a communications card installed in **PORT 5**. *Figure 2.5* shows the 5U rear panel.

Connector Types

Screw-Terminal Connectors—I/O and Battery Monitor/Power

Connection to the relay I/O and Monitor/Power terminals on the rear panel is through screw-terminal connectors. You can remove the entire screw-terminal connector from the back of the relay to disconnect relay I/O, dc battery monitor, and power without removing each wire connection. The screw-terminal connectors are each uniquely keyed (see *Figure 2.22*) and will only fit into one slot on the rear panel. In addition, the receptacle key prevents you from inverting the screw-terminal connector. This feature makes relay removal and replacement easier.

Secondary Circuit Connectors

Fixed Terminal Blocks

Connect CT and PT inputs to the fixed terminal blocks in the bottom two rows of the relay rear panel. You cannot remove these terminal blocks from the relay rear panel. These terminals offer a secure high-reliability connection for CT and PT secondaries.

Connectorized

The Connectorized SEL-487E features receptacles that accept plug-in/plug-out connectors for terminating CT and PT inputs. This requires ordering a Connectorized wiring harness kit (SEL-WA0487E) with mating plugs and wire leads. *Figure 2.4* shows the relay with Connectorized CT and PT analog inputs (see *Connectorized on page 2.27* for more information).

Time-Domain Link (TiDL)

The TiDL SEL-487E features eight fiber-optic EtherCAT connections instead of the standard CT and PT analog inputs (see *TiDL Connections on page 2.30* for more information).
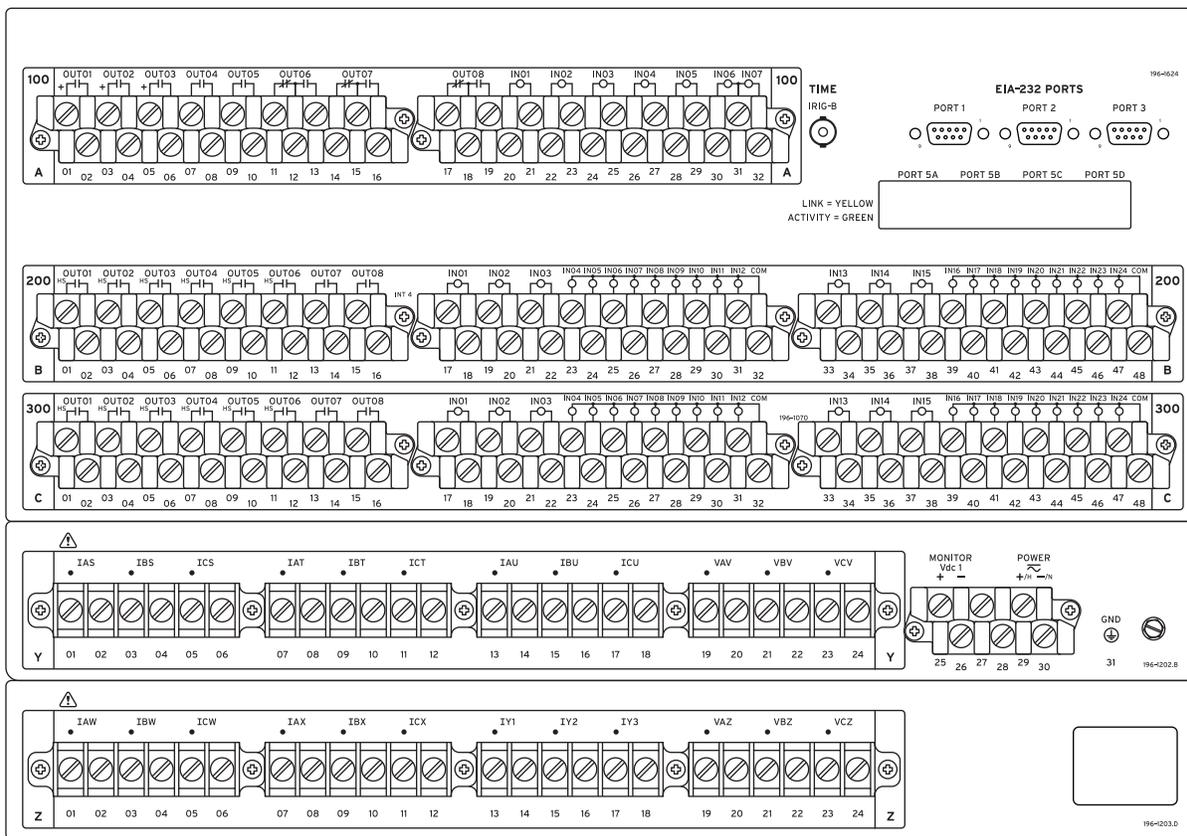
Figure 2.3   Rear Panel With Fixed Terminal Blocks (7U) With INT4 I/O Board
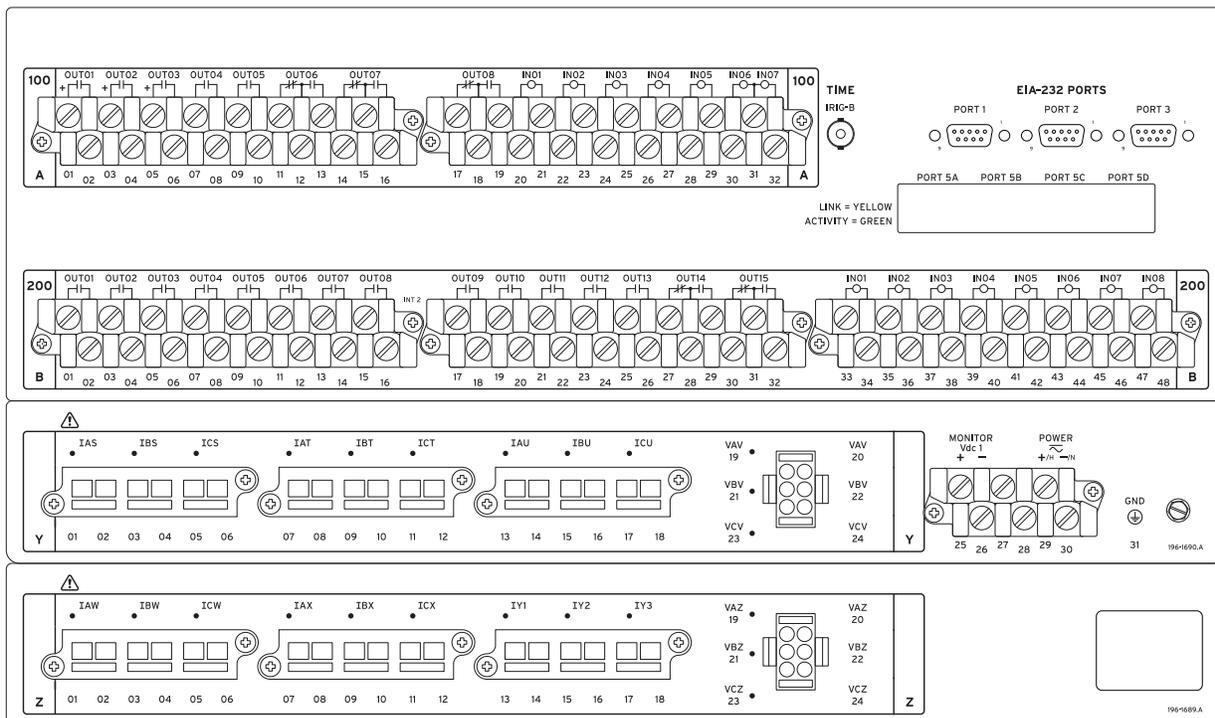
Figure 2.4   Rear Panel Connectorized (6U)
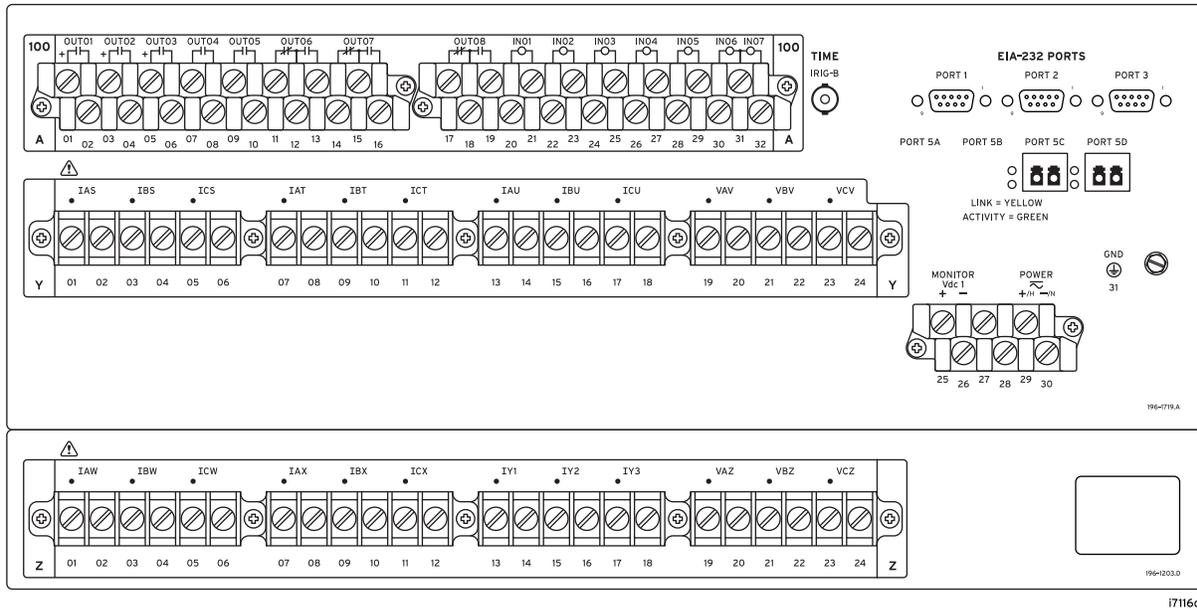
Figure 2.5 Rear Panel With Fixed Terminal Blocks (5U)

Secondary Circuits

The SEL-487E presents a low burden load on the CT secondaries and PT secondaries. The relay accepts the following five sets of three-phase CT inputs:

➤ IAS, IBS, and ICS

➤ IAT, IBT, and ICT

➤ IAU, IBU, and ICU

➤ IAW, IBW, and ICW

➤ IAX, IBX, and ICX

⚠**WARNING**

Before working on a CT circuit, first apply a short to the secondary winding of the CT.

The relay also accepts the following three single-phase CT inputs, primarily for restricted earth fault protection: IY1, IY2, and IY3.

For 5 A relays, the rated nominal input current, I_{NOM}, is 5 A. For 1 A relays, the rated nominal input current, I_{NOM}, is 1 A. Continuous input current for both relay types is 3 • I_{NOM} (or 4 • I_{NOM} as high as 55°C). See *AC Current Inputs (Secondary Circuits) on page 1.14* for complete CT input specifications.

The relay also accepts the following two sets of three-phase potentials from power system PT or CCVT (capacitor-coupled voltage transformer) secondaries.

➤ VAV, VBV, and VCV

➤ VAZ, VBZ, and VCZ

The nominal line-to-neutral input voltage for the PT inputs is 67 volts with a range of 0–300 volts, and a burden of less than 0.1 VA at 125 volts, L-N. PT connections can be four-wire (wye) or open-delta connections.

Relays that use the TiDL system do not contain secondary circuits on the relay. The secondary circuit uses a remote SEL-2240 Axion to supply the voltages and currents through a direct fiber link; however, the nominal current must be selected to appropriately apply scaling through various protection functions. The relay, by default, assumes 5 A as the nominal current selection, so for 1 A scaling, use the **CFG CTNOM** command to change this (see *Table 14.28 in the SEL-400 Series Relays Instruction Manual* for more information). The

SEL-2245-42 AC Analog Input Module also sets its internal calculations based on this command. The relay internally transmits these data to the Axion modules and adjusts the appropriate scaling in the Axion module when this command is used.

In addition to the CT nominal values, TiDL relays also require you to set the nominal frequency by issuing the **CFG NFREQ** command. At Access Level 2, issue a **CFG NFREQ 60** command to set the relay to 60 Hz nominal or issue a **CFG NFREQ 50** command to set the relay to 50 Hz nominal. This command changes the NFREQ setting and restarts the relay, and it is only available in TiDL relays. The relay defaults to 60 Hz, so only use this command if you want to switch to 50 Hz nominal. Issue this command after the **CFG CTNOM** command but before sending settings to the relay.

Control Inputs

The SEL-487E main board inputs and the inputs on the optional I/O interface boards (INT2, INT4, INT7, or INT8 I/O boards) are fixed pickup threshold, optoisolated, control inputs. Specify the pickup voltage level for each board when you order the relay. Use these inputs for monitoring change-of-state conditions of power system equipment.

Inputs can be independent or common. Independent inputs have two separate ground-isolated connections, with no internal connections among inputs. Common inputs share one input leg in common; all input legs of common inputs are ground-isolated. Each group of common inputs is isolated from all other groups.

Nominal current drawn by these inputs is 8 mA or less with six voltage options covering a wide range of voltages, as listed below *Interface Board (I/O) Options on page 1.8*. You can debounce the control input pickup delay and dropout delay separately for each input, or you can use a single debounce setting that applies to all the contact input pickup and dropout times (see *Global Settings on page 8.2*).

AC Control Signals

Optoisolated control inputs can be used with ac control signals, within the ratings shown in *Interface Board (I/O) Options on page 1.8*. *Table 2.1* shows the specific pickup and dropout time-delay settings necessary when applying ac to the inputs.

Table 2.1   Required Settings for Use With AC Control Signals[a]

Global Settings	Description	Entry[b]	Relay Recognition Time for AC Control Signal State Change
IN*nmm*PU[c]	Pickup Delay	2.0 ms at 60 Hz 2.5 ms at 50 Hz (approximately 1/8 cycle)	0.6250 cycles maximum (assertion)
IN*nmm*DO[c]	Dropout Delay	16.5 ms at 60 Hz 20.0 ms at 50 Hz (approximately 1 cycle)	1.1875 cycles maximum (deassertion)

[a] First set Global setting EICIS := Y to gain access to the individual input pickup and dropout timer settings.

[b] These are the only setting values that SEL recommends for detecting ac control signals. Other values may result in inconsistent operation.

[c] Where *n* is 1 for Main Board, 2 for Interface Board 1, and 3 for Interface Board 2; *mm* is number of available contact inputs depending on the type of board.

Furthermore, you can mix ac and dc control signals on the same interface board with optoisolated contact inputs, provided that the two signal types are not present on the same set of combined inputs. Use standard debounce time settings (usually the same value in both the pickup and dropout settings) for the inputs being used with dc control voltages.

The recognition times listed in *Table 2.1* are only valid when all of the following are true:

➤ The ac signal applied is at the same frequency as the power system.

➤ The signal is within the ac threshold pickup ranges defined in Optoisolated (use with ac or dc signals).

➤ The signal contains no dc offset.

The SEL-487E samples the optoisolated inputs at 2 kHz.

Control Outputs

I/O control outputs from the relay include standard outputs, hybrid (high-current interrupting) outputs, and high-speed high-current interrupting outputs. Form A (normally open) output contacts are individually isolated, and Form C outputs share a common connection between the NC (normally closed) and NO (normally open) contacts.

The relay updates control outputs eight times per cycle. Updating of relay control outputs does not occur when the relay is disabled. When the relay is reenabled, the control outputs assume the state that reflects the protection processing at that instant.

Standard Control Outputs

NOTE: You can use ac or dc circuits with standard control outputs.

The standard control outputs are dry Form A (NO) contacts rated for tripping duty. Ratings for Standard outputs are 30 A make, 6 A continuous, and 0.75 A or less break (depending on circuit voltage). Standard contact outputs have a maximum voltage rating of 250 Vac/330 Vdc. Maximum break time is 6 ms with a resistive load. The maximum pickup time for the standard control outputs is 6 ms. *Figure 2.6* shows a representative connection for a Form A standard control output on the main board I/O terminals.

OUT04

O7
O8
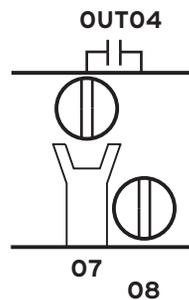
Figure 2.6   Standard Control Output Connection

See *Control Outputs on page 2.8* for complete standard control output specifications.

Hybrid (High-Current Interrupting) Control Outputs

⚠**CAUTION**

Equipment damage can result from connecting ac circuits to hybrid (high-current interrupting) control outputs. Do not connect ac circuits to hybrid control outputs. Use only dc circuits with hybrid control outputs.

The hybrid (high-current interrupting) control outputs are polarity-dependent and are capable of interrupting high-current, inductive loads. Hybrid control outputs use an insulated gate bipolar junction transistor (IGBT) in parallel with a mechanical contact to interrupt (break) highly inductive dc currents. The contacts can carry continuous current while eliminating the need for heat sinking and providing security against voltage transients.

With any hybrid output, break time varies according to the L/R (circuit inductive/ resistive) ratio. As the L/R ratio increases, the time needed to interrupt the circuit fully increases also. The reason for this increased interruption delay is that circuit current continues to flow through the output MOV after the output deasserts until all of the inductive energy dissipates. Maximum dropout (break) time is 6 ms with a resistive load, the same as for the standard control outputs. The other ratings of these control outputs are similar to the standard control outputs, except that the hybrid outputs can break current as great as 10 A. Hybrid contact outputs have a maximum voltage rating of 330 Vdc.

The maximum contact closing time for the hybrid control outputs is 6 ms. *Figure 2.7* shows a representative connection for a Form A hybrid control output on the main board I/O terminals.
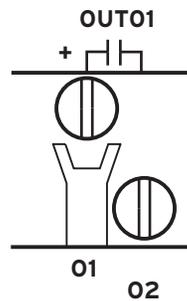
Figure 2.7   Hybrid Control Output Connection

See *Control Outputs on page 2.8* for complete hybrid control output specifications.

High-Speed, High-Current Interrupting Control Outputs

In addition to the standard control outputs and the hybrid control outputs, the INT4 and INT8 I/O interface boards offer high-speed high-current interrupting control outputs. A metal-oxide varistor (MOV) protects against excess voltage transients for each contact. These control outputs have a resistive load contact closing time of 10 ms, which is much faster than the 6 ms contact closing time of the standard and hybrid control outputs. The high-speed contact outputs open at a maximum time of 8 ms. The maximum voltage rating is 250 Vac/330 Vdc. See *Control Outputs on page 2.8* for more information.

Figure 2.8 shows a representative connection for a Form A high-speed contact output on the INT4 I/O interface terminals. The HS marks are included to indicate that this is a high-speed control output.
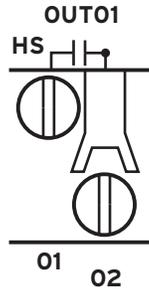
Figure 2.8 INT4 High-Speed Control Output Connection (Three Terminals)

Figure 2.9 shows a representative connection for a Form A fast hybrid control output on the INT8 I/O interface terminals.

The INT8 high-speed contact output uses three terminal positions, while the INT4 high-speed contact output uses two. The third terminal of each INT8 high-speed control output is connected to precharge resistors that can be used to mitigate transient inrush current conditions, as explained below. A similar technique can be used with INT4 board high-speed control outputs using external resistors. Short transient inrush current can flow at the closing of an external switch in series with open high-speed contacts. This transient will not energize the circuits in typical relay-coil control applications (trip coils and close coils), and standard auxiliary relays will not pick up. However, an extremely sensitive digital input or light-duty, high-speed auxiliary relay can pick up for this condition. This false pickup transient occurs when the capacitance of the high-speed output circuitry charges (creating a momentary short circuit that a fast, sensitive device sees as a contact closure). A third terminal (03 in *Figure 2.9*) provides an internal path for precharging the high-speed output circuit capacitance when the circuit is open.
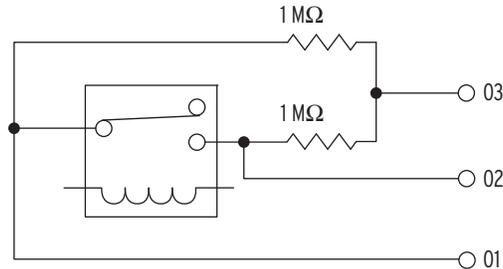
Figure 2.9 High-Speed Control Output Typical Terminals, INT8

Figure 2.10 shows some possible connections for this third terminal that will eliminate the false pickup transients when closing an external switch. In general, you must connect the third terminal to the dc rail (positive or negative) that is on the same side as the open external switch condition. If an open switch exists on either side of the output contact, then you can accommodate only one condition because two open switches (one on each side of the contact) defeat the precharge circuit.
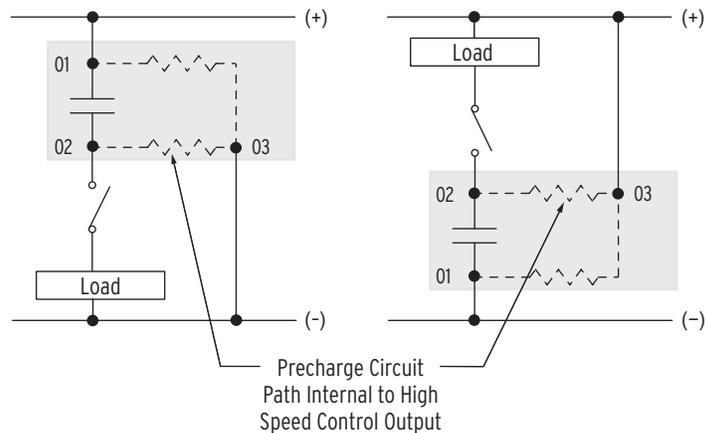
Figure 2.10 Precharging Internal Capacitance of High-Speed Output Contacts, INT8

For wiring convenience, on the INT8 I/O Interface Board, the precharge resistors shown in *Figure 2.10* are built into the I/O board, and connected to a third terminal. On the INT4 I/O Interface Board, there are no built-in precharge resistors, and each high-speed control output has only two terminal connections.

Main Board I/O

Every SEL-487E configuration includes the main board I/O and features the following connections:

➤   Two standard Form A outputs

➤   Three hybrid (high-current interrupting) Form A outputs

➤   Three standard Form C outputs

➤   Seven level-sensitive optoisolated control inputs (five independent and two common)

IRIG-B Inputs

The SEL-487E has a regular IRIG-B timekeeping mode, and a high-accuracy IRIG-B timekeeping mode. The IRIG-B serial data format consists of a 1-second frame containing 100 pulses divided into fields, from which the relay decodes the second, minute, hour, and day fields and sets the internal time clock upon detecting valid time data in the IRIG time mode. There is one IRIG-B input on the SEL-487E rear panel, capable of supporting the HIRIG mode.

IRIG-B Pins of Serial Port 1

This IRIG-B input is capable of regular IRIG mode timekeeping only. Timing accuracy for the IRIG time mode is 500 μs.

IRIG-B BNC Connector

This IRIG-B input is capable of both modes of timekeeping. If the connected timekeeping source is qualified as high-accuracy, the relay enters the HIRIG mode, which has a timing accuracy of 1 μs. If both inputs are connected, the SEL-487E will use the IRIG-B BNC connector signal if a signal is detected.

Battery-Backed Clock

If relay input power is lost or removed, a lithium battery powers the relay clock, providing date and time backup. The battery is a 3 V lithium coin cell, Rayovac no. BR2335 or equivalent. If power is lost or disconnected, the battery discharges to power the clock. At room temperature (25°C), the battery will operate for approximately 10 years at rated load.

When the SEL-487E is operating with power from an external source, the self-discharge rate of the battery is very small. Thus, battery life can extend well beyond the nominal 10-year period because the battery rarely discharges after the relay is installed. The battery cannot be recharged.

If the relay does not maintain the date and time after power loss, replace the battery (see *Replacing the Lithium Battery on page 10.27 in the SEL-400 Series Relays Instruction Manual*).

Communications Interfaces

The SEL-487E has several communications interfaces you can use to communicate with other intelligent electronic devices (IEDs) via EIA-232 ports: **PORT 1**, **PORT 2**, **PORT 3**, and **PORT F**. See *Section 10: Communications Interfaces* for more information and options for connecting your relay to the communications interfaces.

An optional Ethernet card provides Ethernet capability for the SEL-487E. An Ethernet card gives the relay access to popular Ethernet networking standards including TCP/IP, FTP, Telnet, DNP3, IEEE C37.118 Synchrophasors, and IEC 61850 over local area and wide area networks (the Ethernet card with IEC 61850 support is available at purchase as a factory-installed option). For information on DNP3 applications, see *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. For more information on IEC 61850 applications, see *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Plug-In Boards

The SEL-487E is available in 5U (no interface boards), 6U (option of one interface board), or 7U (option of two interface boards).

An optional Ethernet plug-in communications card allows you to use TCP/IP, FTP, Telnet, DNP3, LAN/WAN, and IEC 61850 applications on an Ethernet network. This card is only available at the time of purchase of a new SEL-487E as a factory-installed option or as a factory-installed conversion to an existing relay.

I/O Interface Boards

In addition to the main board I/O, you can choose among four input/output interface boards (INT2, INT4, INT7, and INT8) for additional I/O. *Figure 2.11–Figure 2.14* show the rear screw-terminal connectors of these interface boards.
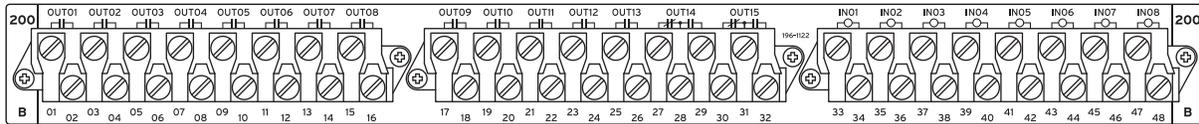
Figure 2.11   I/O Interface Board INT2
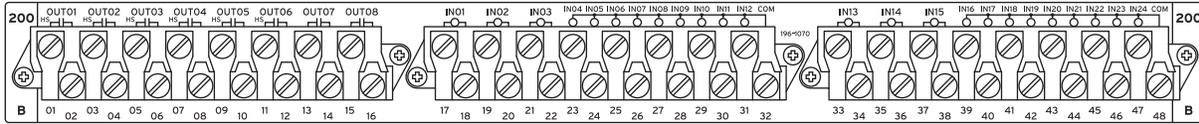
Figure 2.12   I/O Interface Board INT4
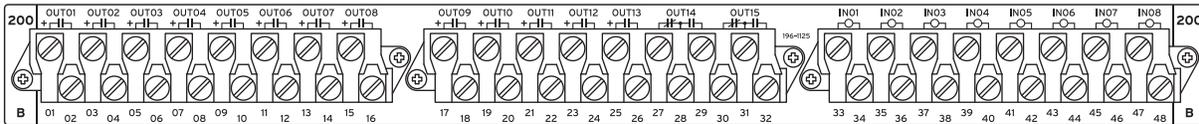
Figure 2.13   I/O Interface Board INT7
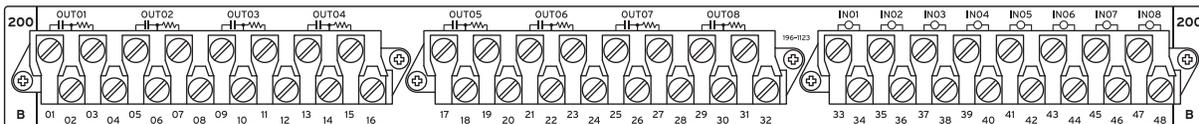
Figure 2.14   I/O Interface Board INT8

I/O of the main board and interface boards vary by the type and amount of output capabilities. *Table 2.2* lists the inputs of the main board and additional I/O interface boards, and *Table 2.3* lists the outputs of the main board and additional I/O interface boards.

Table 2.2   Control Inputs

Board	Independent Contact Pairs	Common Contacts
INT2, INT7, and INT8	8	
INT4	6	Two sets of 9
Main Board	5	2

Table 2.3   Control Outputs

| Board | Standard | | Fast Hybrid[a] | Hybrid[b] |
	Form A	Form C	Form A	Form A
INT2	13	2		
INT4	2		6	
INT7		2		13
INT8			8	
Main Board	2	3		3

[a] High-speed/high-current interrupting.

[b] High-current interrupting.

Ethernet Card

You can add Ethernet communications protocols to the SEL-487E by purchasing the Ethernet card option. Factory-installed in the rear relay Port 5, the Ethernet card provides Ethernet ports for industrial applications that process data traffic between the SEL-487E and a local area network (LAN).

Jumpers

The SEL-487E contains jumpers that configure the relay for specific operating modes. These jumpers are located on the main board (the top board) and the I/O interface boards (one or two boards located immediately below the main board).

Main Board Jumpers

The jumpers on the main board of the SEL-487E perform the following functions:

➤ Temporary/emergency password disable

➤ Circuit breaker control enable

➤ Rear serial port +5 Vdc source enable

The main board jumpers are in two locations. The password disable jumper and circuit breaker control jumper are at the front of the main board. The serial port jumpers are near the rear-panel serial ports; each serial port jumper is directly in front of the serial port that it controls.

Password and Circuit Breaker Jumpers

You can access the password disable jumper and circuit breaker control jumper without removing the main board from the relay cabinet. Remove the SEL-487E front cover to view these jumpers (use appropriate ESD precautions). The password and circuit breaker jumpers (position number J18) are located on the front of the main board, immediately left of the power connector (see *Figure 2.15*).

⚠**CAUTION**
Do not install a jumper on Positions A or D of the main board J18 header. Relay misoperation can result if you install jumpers on positions J18A or J18D.

There are four jumpers denoted D, BREAKER, PASSWORD, and A from left to right (position D is on the left). Position PASSWORD is the password disable jumper; position BREAKER is the circuit breaker control enable jumper. Positions D and A are for SEL use. *Figure 2.15* shows the jumper header with the circuit breaker/control jumper in the ON position and the password jumper in the OFF position; these are the normal jumper positions for an in-service relay. *Table 2.4* lists the jumper positions and functions.
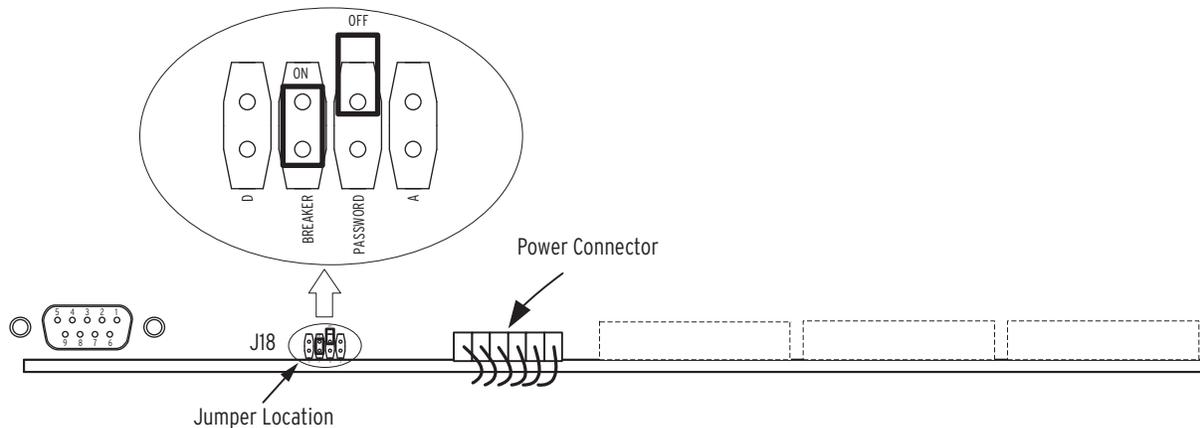
Figure 2.15   Jumper Location on the Main Board

Table 2.4   Main Board Jumpers[a]

Jumper	Jumper Location	Jumper Position	Function
A	Front	OFF	For SEL use only
PASSWORD	Front	OFF	Enable password protection (normal and shipped position)
		ON	Disable password protection (temporary or emergency only)
BREAKER	Front	OFF	Disable circuit breaker commands (**OPEN** and **CLOSE**) and output **PULSE** commands[b] (shipped position)
		ON	Enable circuit breaker command (**OPEN** and **CLOSE**) and output **PULSE** commands[b]
D	Front	OFF	For SEL use only

[a] ON is the jumper shorting both pins of the jumper location. Place the jumper over one pin only for OFF.

[b] Also affects the availability of SCADA Control Messages and the front-panel LOCAL CONTROL > BREAKER CONTROL and LOCAL CONTROL > OUTPUT TESTING screens.

The password disable jumper, PASSWORD, is for temporary or emergency suspension of the relay password protection mechanisms. Under no circumstance should you install PASSWORD on a long-term basis. The SEL-487E ships with password disable jumper PASSWORD OFF (passwords enabled).

The circuit breaker control enable jumper, BREAKER, supervises the **CLOSE** *n* command, the **OPEN** *n* command, the **PULSE OUT***nnn* command, and front-panel local bit control. To use these functions, you must install Jumper BREAKER. The relay checks the status of the circuit breaker control jumper when you issue **CLOSE** *n*, **OPEN** *n*, **PULSE OUT***nnn*, and when you use the front panel to close or open circuit breakers, control a local bit, or pulse an output. The SEL-487E ships with circuit breaker Jumper BREAKER OFF. For commissioning and testing of the SEL-487E contact outputs, it may be convenient to set BREAKER ON, so that the **PULSE OUT***nnn* commands can be used to check output wiring. BREAKER must also be set ON if SCADA (DNP, Fast Operate, IEC 61850) control of the circuit breaker is required or if the LOCAL CONTROL > BREAKER CONTROL screens are going to be used.

Serial Port Jumpers

Place jumpers on the main board to connect +5 Vdc to Pin 1 of each of the three rear-panel EIA-232 serial ports. The maximum current (sum of all three ports) available from the Pin 1 source is 0.5 A. The Pin 1 source is useful for powering an external modem. *Table 2.5* describes the JMP2, JMP3, and JMP4 positions. The SEL-487E ships with JMP2, JMP3, and JMP4 in the OFF position (no +5 Vdc on Pin 1).

Table 2.5   Main Board Serial Port Jumpers (JMP2, JMP3, and JMP4)

Jumper	Jumper Location	Jumper Position	Function
JMP2	Rear	OFF	Serial Port 3, Pin 1 = not connected
		ON	Serial Port 3, Pin 1 = +5 Vdc
JMP3	Rear	OFF	Serial Port 2, Pin 1 = not connected
		ON	Serial Port 2, Pin 1 = +5 Vdc
JMP4	Rear	OFF	Serial Port 1, Pin 1 = not connected
		ON	Serial Port 1, Pin 1 = +5 Vdc
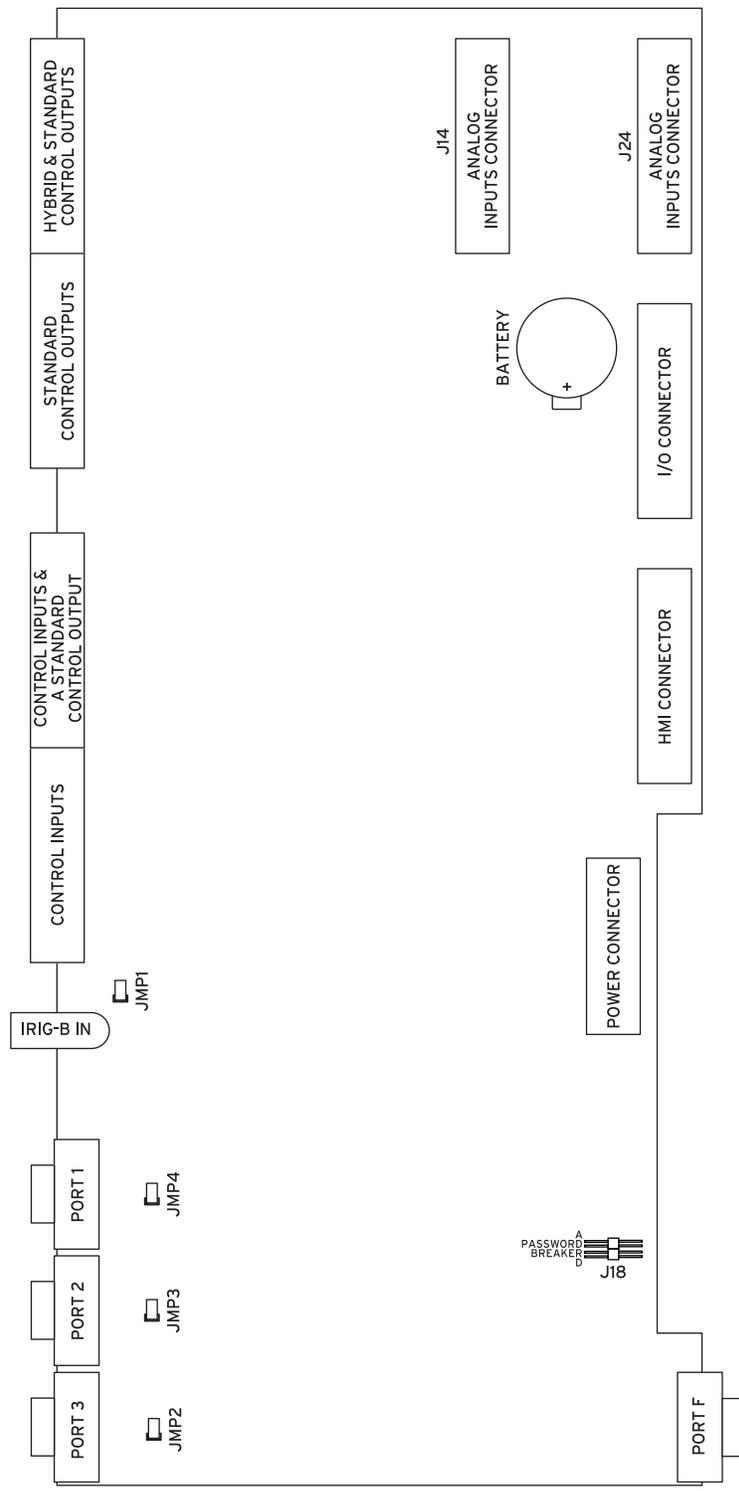
Figure 2.16   Major Component Locations on the SEL-487E Main Board

Changing Serial Port Jumpers

You must remove the main board to access the serial port jumpers. Perform the following steps to change the JMP2, JMP3, and JMP4 jumpers in an SEL-487E.

Step 1.   Follow your company standard to remove the relay from service.

Step 2.   Disconnect power from the SEL-487E.

Step 3. Retain the **GND** connection, if possible, and ground the equipment to an ESD mat.

Step 4. Remove the communications cable connected to the front-panel serial port, if applicable.

Step 5. Remove the rear-panel **EIA-232 PORTS** mating connectors.

Unscrew the keeper screws and disconnect any serial cables connected to the Port 1, Port 2, and Port 3 rear-panel receptacles, as well as the BNC and Ethernet connectors.

Step 6. Remove all Ethernet and IRIG-B connections.

Step 7. Loosen the four front-panel screws (they remain attached to the front panel), and remove the relay front panel.

Step 8. Remove the 34-pin ribbon cable from the front panel by pushing the extraction ears away from the connector.

Step 9. Disconnect the power, interface board, and analog input board cables from the main board.

Step 10. Carefully pull out the drawout assembly containing the main board.

Step 11. Locate the jumper you want to change.

Jumpers JMP2, JMP3, and JMP4 are located at the rear of the main board, directly in front of Port 3, Port 2, and Port 1, respectively (see *Figure 2.16*).

Step 12. Install or remove the jumper as needed (see *Table 2.5* for jumper position descriptions).

Step 13. Reinstall the SEL-487E main board and reconnect the power, interface board, and analog input board cables.

Step 14. Reconnect the cable removed in *Step 7* and reinstall the relay front-panel cover.

Step 15. Reattach the rear-panel connections.

Step 16. Reconnect any serial, BNC, or Ethernet cables that you removed from the relay in the disassembly process.

Step 17. Follow your company standard procedure to return the relay to service.

I/O Interface Board Jumpers

Jumpers on the I/O interface boards identify the particular I/O board configuration and I/O board control address. Four I/O interface boards are available: INT2, INT4, INT7, and INT8. The jumpers on these I/O interface boards are at the front of each board, as shown in *Figure 2.17*.

CONTROL INPUTS | CONTROL INPUTS | STANDARD CONTROL OUTPUTS | STANDARD CONTROL OUTPUTS | STANDARD CONTROL OUTPUTS | STANDARD CONTROL OUTPUTS

JUMPER CONFIGURATION

VER	2xx	3xx
JMP1A	OFF	ON
JMP1B	OFF	OFF
JMP2A	OFF	ON
JMP2B	OFF	OFF

A B
JMP2

A B
JMP1

CONNECTOR

SEL-487E INT 2 BOARD

CONTROL INPUTS | CONTROL INPUTS | CONTROL INPUTS | CONTROL INPUTS | STANDARD & HIGH-SPEED HIGH-CURRENT INTERRUPTING CONTROL OUTPUTS | HIGH-SPEED HIGH-CURRENT INTERRUPTING CONTROL OUTPUTS

JUMPER CONFIGURATION

	200	300	400	500
JMP49A	OFF	ON	OFF	ON
JMP49B	OFF	OFF	ON	ON
JMP50A	OFF	ON	OFF	ON
JMP50B	OFF	OFF	ON	ON

A B
JMP49

A B
JMP50

CONNECTOR

SEL-487E INT 4 BOARD

CONTROL INPUTS | CONTROL INPUTS | STANDARD & HYBRID CONTROL OUTPUTS | HYBRID CONTROL OUTPUTS | HYBRID CONTROL OUTPUTS | HYBRID CONTROL OUTPUTS

JUMPER CONFIGURATION

VER	2xx	3xx
JMP1A	OFF	ON
JMP1B	OFF	OFF
JMP2A	OFF	ON
JMP2B	OFF	OFF

A B
JMP2

A B
JMP1

CONNECTOR

SEL-487E INT 7 BOARD

CONTROL INPUTS | CONTROL INPUTS | HIGH-SPEED HIGH-CURRENT INTERRUPTING CONTROL OUTPUTS | HIGH-SPEED HIGH-CURRENT INTERRUPTING CONTROL OUTPUTS | HIGH-SPEED HIGH-CURRENT INTERRUPTING CONTROL OUTPUTS | HIGH-SPEED HIGH-CURRENT INTERRUPTING CONTROL OUTPUTS

JUMPER CONFIGURATION

VER	2xx	3xx
JMP1A	OFF	ON
JMP1B	OFF	OFF
JMP2A	OFF	ON
JMP2B	OFF	OFF

A B
JMP2

A B
JMP1

CONNECTOR

SEL-487E INT 8 BOARD

Figure 2.17 Top to Bottom: INT2, INT4, INT7, and INT8 With Jumper Locations Indicated

To confirm the positions of your I/O board jumpers, remove the front panel and visually inspect the jumper placements. *Table 2.6* lists the four jumper positions for I/O interface boards. Refer to *Figure 2.17* for the locations of these jumpers.

The I/O board control address has a hundreds-series prefix attached to the control inputs and control outputs for that particular I/O board chassis slot. A 6U chassis has a 200-addresses slot for inputs IN201, IN202, etc., and outputs OUT201, OUT202, etc. A 7U chassis has a 200-addresses slot and a 300-addresses slot. The drawout tray on which each I/O board is mounted is keyed. See *Installing Optional I/O Interface Boards on page 10.29 in the SEL-400 Series Relays Instruction Manual* for information on the key positions for the 200-addresses slot trays and the 300-addresses slot trays.

Table 2.6   I/O Board Jumpers

I/O Board Control Address	JMP1A/ JMP49A[a]	JMP1B/ JMP49B[a]	JMP2A/ JMP50A[a]	JMP2B/ JMP50B[a]
2XX	OFF	OFF	OFF	OFF
3XX	ON	OFF	ON	OFF

[a] INT4 I/O interface board jumper numbering.

Relay Placement

Proper placement of the SEL-487E helps make certain that you receive years of trouble-free power system protection. Use the following guidelines for proper physical installation of the SEL-487E.

Physical Location

You can mount the SEL-487E in a sheltered indoor environment (a building or an enclosed cabinet) that does not exceed the temperature and humidity ratings for the relay.

The relay is rated at Installation/Overvoltage Category II and Pollution Degree 2. This rating allows mounting the relay indoors or in an outdoor (extended) enclosure where the relay is protected against exposure to direct sunlight, precipitation, and full wind pressure, but neither temperature nor humidity are controlled.

You can place the relay in extreme temperature and humidity locations. The temperature range over which the relay operates is –40° to +185°F (–40° to +85°C, see *Operating Temperature on page 1.16*). The relay operates in a humidity range from 5 percent to 95 percent, no condensation, and is rated for installation at a maximum altitude of 2000 m (6560 ft) above mean sea level.

Rack Mounting

When mounting the SEL-487E in a rack, use the reversible front flanges to either semiflush-mount or projection-mount the relay.

The semiflush mount results in a small panel protrusion from the relay rack rails of approximately 27.9 mm (1.1 inches). The projection mount places the front panel approximately 88.9 mm (3.5 inches) in front of the relay rack rails.

See *Figure 2.18* for exact mounting dimensions for both the horizontal and vertical rack-mount relays. Use four screws of the appropriate size for your rack.

RACK-MOUNT CHASSIS

PANEL-MOUNT CHASSIS

8.50
(215.9)

TOP

1.12
(28.4)

8.50
(215.9)

TOP

#10-32
STUD

1.12
(28.4)

19.00
(482.6)

A

FRONT

E

B

18.31
(465.1)

19.80
(502.9)

C

FRONT

SIDE

17.63
(447.8)

Ø1/4
(Ø6.4)

D

PANEL CUTOUT

E

B

18.31
(465.1)

LEGEND

in
(mm)
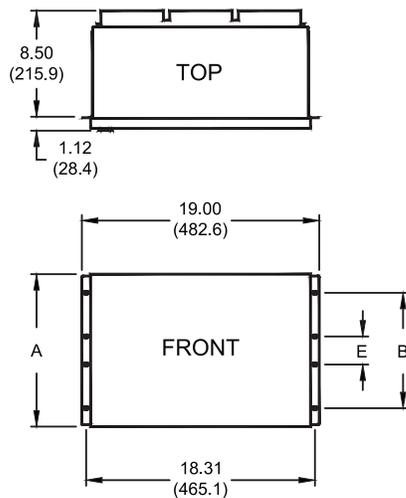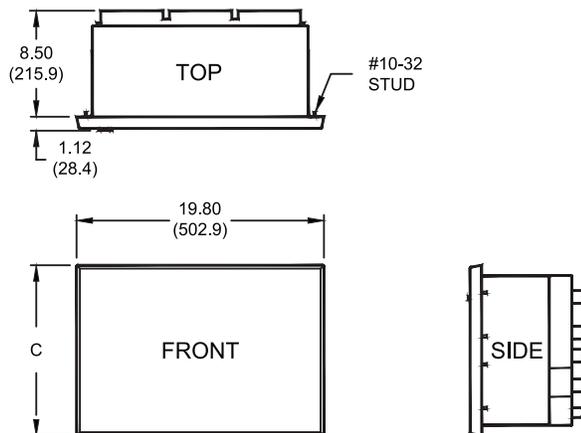
DIMENSION	NO I/O BOARD (5U)	ONE I/O BOARD (6U)	TWO I/O BOARD (7U)
A	8.72 (221.5)	10.47 (265.9)	12.22 (310.4)
B	5.75 (146.1)	7.50 (190.5)	9.25 (235.0)
C	10.15 (257.8)	12.10 (307.3)	13.65 (346.7)
D	8.6 (218.4)	10.55 (268.0)	12.10 (307.3)
E	N/A	3.00 (76.2)	2.25 (57.2)
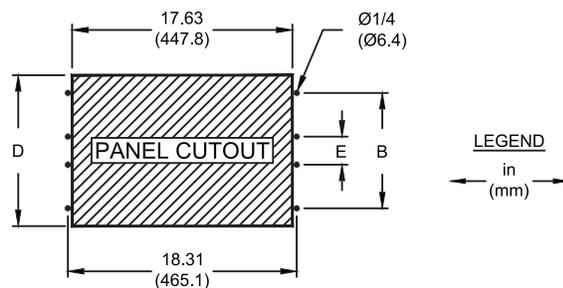
*ADD 0.30 (7.6) FOR CONNECTORIZED RELAYS

i9309c

Figure 2.18   SEL-487E Chassis Dimensions

Panel Mounting

Place the panel-mount versions of the SEL-487E in a switchboard panel. See the drawings in *Figure 2.18* for panel cut and drill dimensions (these dimensions apply to both the horizontal and vertical panel-mount relay versions). Use the supplied mounting hardware to attach the relay.

Connection

⚠CAUTION
Insufficiently rated insulation can deteriorate under abnormal operating conditions and cause equipment damage. For external circuits, use wiring of sufficiently rated insulation that will not break down under abnormal operating conditions.

The SEL-487E is available in many different configurations, depending on the number and type of control inputs, control outputs, and analog input termination you specified at ordering. This section presents a representative sample of relay rear-panel configurations and the connections to these rear panels. Only horizontal chassis are shown; rear panels of the 5U vertical chassis are identical to horizontal chassis rear panels for the 5U size.

When connecting the SEL-487E, refer to your company plan for wire routing and wire management. Be sure to use wire that is appropriate for your installation with an insulation rating of at least 90°C.

Rear-Panel Layout

Figure 2.3–Figure 2.5 and *Figure 2.19–Figure 2.20* show some of the available SEL-487E rear panels.

All relay versions have screw-terminal connectors for I/O, power, and battery monitor. You can order the relay with fixed terminal blocks for the CT and PT connections, or you can order SEL Connectorized rear-panel configurations that feature plug-in/plug-out PT connectors and shorting CT connectors for relay analog inputs.

The screw-terminal connections for the INT2 and the INT7 I/O interface boards are the same. The INT8 I/O interface board has control output terminals grouped in threes, with the fourth terminal as a blank additional separator (Terminals 4, 8, 12, 16, 20, 24, 28, and 32). The INT4 and INT8 I/O interface boards both contain fast hybrid control outputs, but use a different terminal layout—see *Control Outputs on page 2.8* for details.

For more information on the main board control inputs and control outputs, see *Main Board I/O on page 2.11*. For more information on the I/O interface board control inputs and control outputs, see *I/O Interface Board Jumpers on page 2.18*.
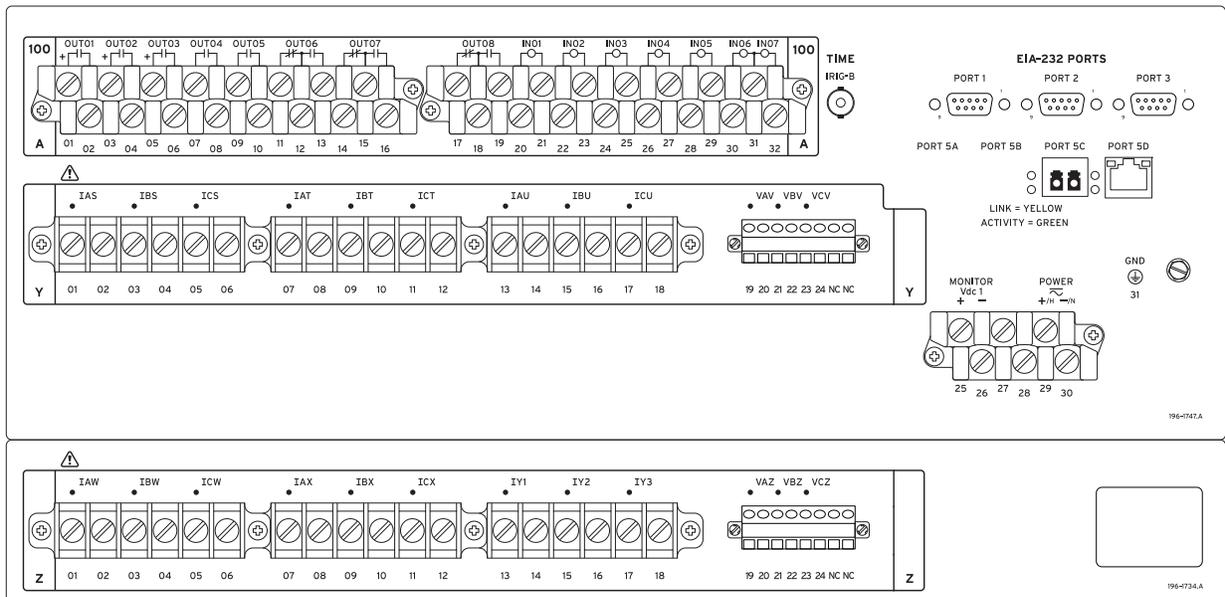
Figure 2.19   5U Rear Panel With Low-Energy Analog (LEA) Voltage Inputs
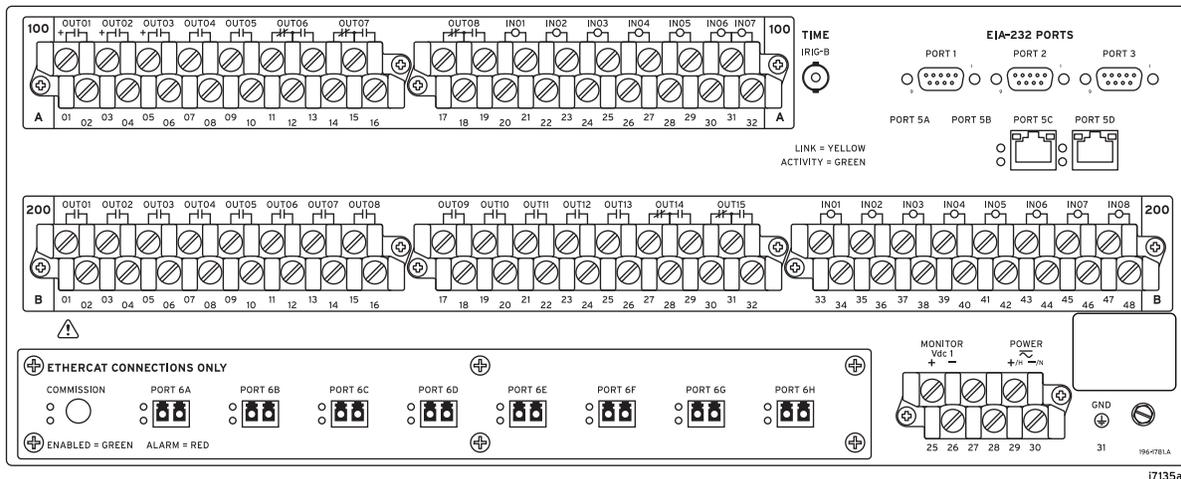
Figure 2.20   EtherCAT Board for TiDL

Rear-Panel Symbols

There are important safety symbols on the rear of the SEL-487E (see *Figure 2.21*). Observe proper safety precautions when you connect the relay at terminals marked by these symbols. In particular, the danger symbol located on the rear panel corresponds to the following: *Contact with instrument terminals can cause electrical shock that can result in injury or death*. Be careful to limit access to these terminals.
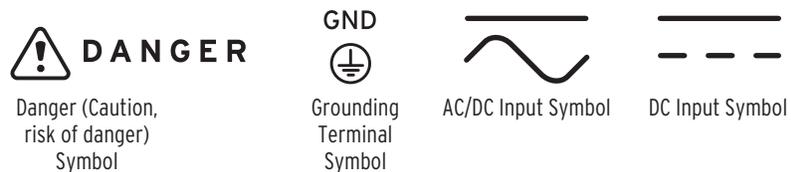
Figure 2.21   Rear-Panel Symbols

Screw-Terminal Connectors

Terminate connections to the SEL-487E screw-terminal connectors with ring-type crimp lugs. Use a #8 ring lug with a maximum width of 9.1 mm (0.360 in). The screws in the rear-panel screw-terminal connectors are #8-32 binding-head, slotted, nickel-plated brass screws. Tightening torque for the terminal connector screws is 1.0 Nm to 2.0 Nm (9 in-lb to 18 in-lb).

You can remove the screw-terminal connectors from the rear of the SEL-487E by unscrewing the screws at each end of the connector block. Perform the following steps to remove a screw-terminal connector.

Step 1.   Remove the connector by pulling the connector block straight out. Note that the receptacle on the relay circuit board is keyed; you can insert each screw-terminal connector in only one location on the rear panel.

Step 2.   To replace the screw-terminal connector, confirm that you have the correct connector and push the connector firmly onto the circuit board receptacle.

Step 3.   Reattach the two screws at each end of the block.

Changing Screw-Terminal Connector Keying

You can rotate a screw-terminal connector so that the connector wire dress position is the reverse of the factory-installed position (for example, wires entering the relay panel from below instead of from above). In addition, you can move similar function screw-terminal connectors to other locations on the rear panel. To move these connectors to other locations, you must change the screw-terminal connector keying. Inserts in the circuit board receptacles key the receptacles for only one screw-terminal connector in one orientation. Each screw-terminal connector has a missing web into which the key fits (see *Figure 2.22*). If you want to move a screw-terminal connector to another circuit board receptacle or reverse the connector orientation, you must rearrange the receptacle keys to match the screw-terminal connector block. Use long-nosed pliers to move the keys. *Figure 2.23* shows the factory-default key positions.
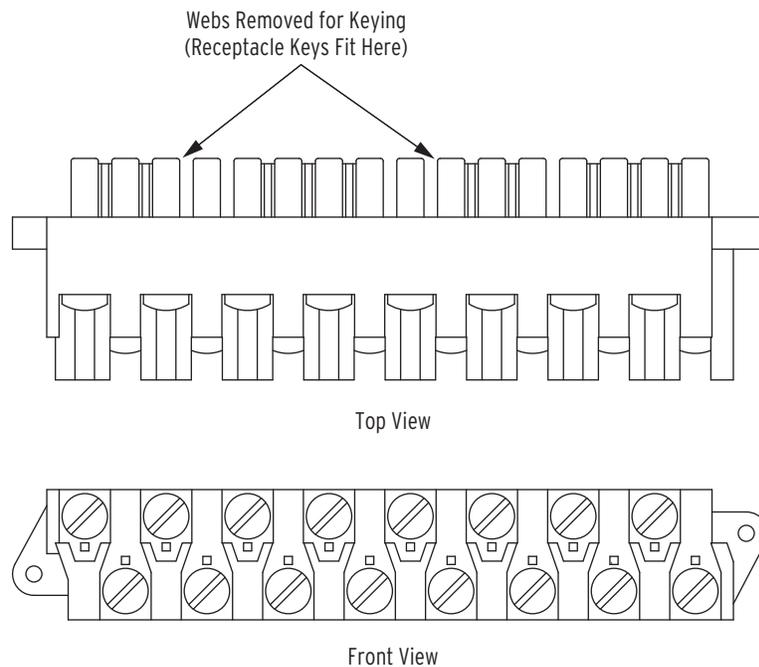
Figure 2.22   Screw-Terminal Connector Keying
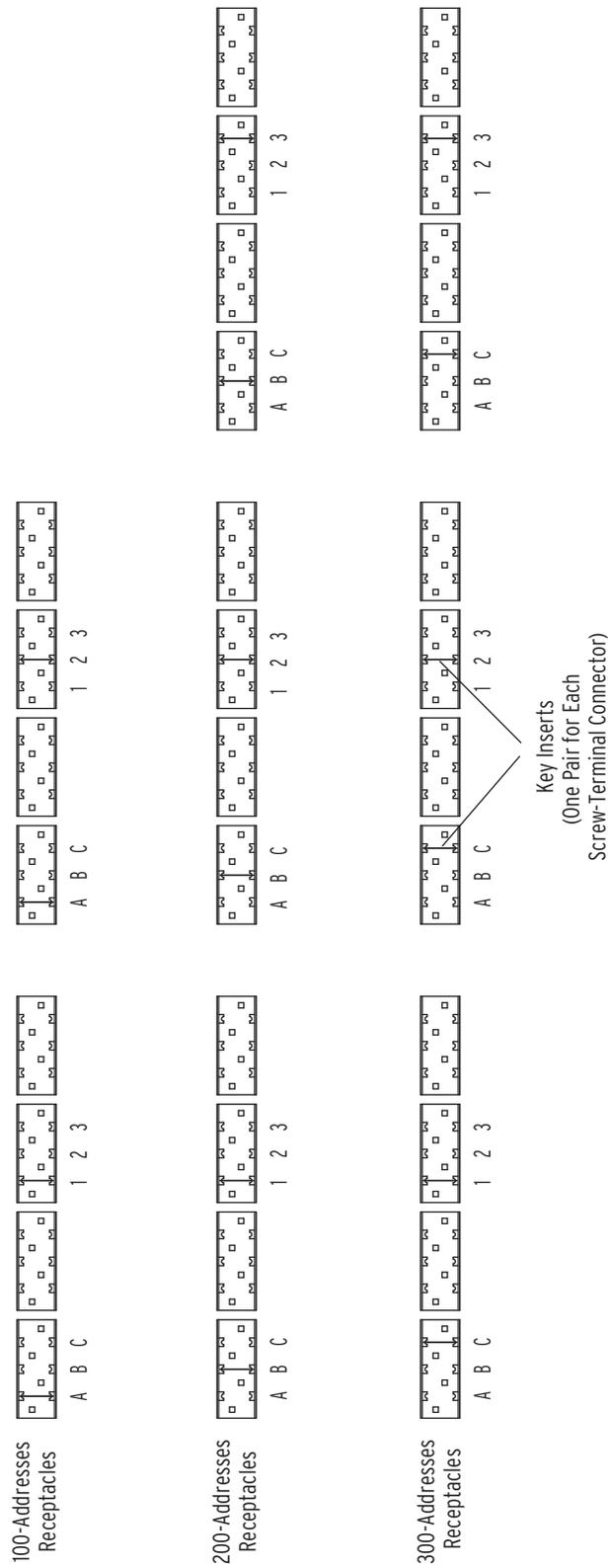
Figure 2.23   Rear-Panel Receptacle Keying

Grounding

Connect the grounding terminal (#**Y31**) labeled **GND** on the rear panel to a rack frame ground or main station ground for proper safety and performance. This protective earthing terminal is in the lower right side of the relay panel. The symbol that indicates the grounding terminal is shown in *Safety Symbols on page xviii in the Preface*. Use 2.5 mm^2 (14 AWG) or larger wire less than 2 m (6.6 ft) in length for this connection. This terminal connects directly to the internal chassis ground of the SEL-487E.

Power Connections

The terminals labeled **POWER** on the rear panel (#**Y29** and #**Y30**) must connect to a power source that matches the power supply characteristics that your SEL-487E specifies on the rear-panel serial number label (see *Power Supply on page 1.14*, for complete power input specifications). For the relay models that accept dc input, the serial number label specifies dc with the symbol shown in *Figure 2.21*.
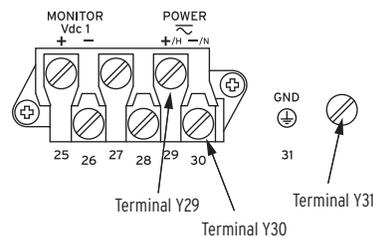
Figure 2.24   Power Connection Area of the Rear Panel

NOTE: The combined voltages applied to the **POWER** and **MONITOR** terminals must not exceed 600 V (rms or dc).

The **POWER** terminals are isolated from chassis ground. Use 0.8 mm^2 (18 AWG) or larger wire to connect to the **POWER** terminals. Connection to external power must comply with IEC 60947-1 and IEC 60947-3 and must be identified as the disconnect device for the equipment. Place an external disconnect device, switch/ fuse combination, or circuit breaker in the **POWER** leads for the SEL-487E; this device must interrupt both the hot (**H/+**) and neutral (**N/−**) power leads. The current rating for the power disconnect circuit breaker or fuse must be 20 A maximum.

Operational power is internally fused by power supply Fuse F1. *Table 2.7* lists the SEL-487E power supply fuse requirements. Be sure to use fuses that comply with IEC 127-2.

You can order the SEL-487E with one of three operational power input ranges listed in *Table 2.7*. Each of the three supply voltage ranges represents a power supply ordering option. As noted in *Table 2.7*, model numbers for the relay with these power supplies begin 0487E3X*n* (or 487E4X*n*), where *n* is 2, 4, or 6, to indicate low, medium, and high voltage input power supplies, respectively. Note that each power supply range covers two widely used nominal input voltages. The SEL-487E power supply operates from 30 Hz to 120 Hz when ac power is used for the **POWER** input.

Table 2.7   Fuse Requirements for the Power Supply

Rated Voltage	Operational Voltage Range	Fuse F1	Fuse Description	Model Number
24–48 Vdc	18–60 Vdc	T5.0AH250V	5x20 mm, time-lag, 5.0 A, high break capacity, 250 V	0487E3X2 or 0487E4X2
48–125 Vdc or 110–120 Vac	38–140 Vdc or 85–140 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V	0487E3X4 or 0487E4X4
125–250 Vdc or 110–240 Vac	85–300 Vdc or 85–264 Vac (30–120 Hz)	T3.15AH250V	5x20 mm, time-lag, 3.15 A, high break capacity, 250 V	0487E3X6 or 0487E4X6

The SEL-487E accepts dc power input for all power supply models. The 48–125 Vdc supply also accepts 110–120 Vac; the 125–250 Vdc supply also accepts 110–240 Vac. When connecting a dc power source, you must connect the source with the proper polarity, as indicated by the **+** (Terminal #**Y29**) and **–** (Terminal #**Y30**) symbols on the power terminals. When connecting to an ac power source, the **+** Terminal #**Y29** is hot (**H**), and the **–** Terminal #**Y30** is neutral (**N**). Each model of the SEL-487E internal power supply exhibits low power consumption and a wide input voltage tolerance. For more information on the power supplies, see *Power Supply on page 1.14*.

Monitor Connections (DC Battery)

The SEL-487E monitors one dc battery system. For information on the battery monitoring function, see *Station DC Battery System Monitor on page 7.14*. Connect the positive lead of the battery system to Terminal #**Y25** and the negative lead to Terminal #**Y26**. (Usually the battery system is also connected to the rear-panel **POWER** input terminals.)

Secondary Circuit Connections

⚠CAUTION
Relay misoperation can result from applying anything other than specified secondary voltages and currents. Before making any secondary circuit connections, check the nominal voltage and nominal current specified on the rear-panel nameplate.

⚠DANGER
Contact with instrument terminals can cause electrical shock that can result in injury or death.

The SEL-487E has five sets of three-phase current inputs, three single-phase current inputs, and two sets of three-phase voltage inputs. *Shared Configuration Attributes on page 2.1* describes these inputs in detail. The alert symbol and the word **DANGER** on the rear panel indicate that you should use all safety precautions when connecting secondary circuits to these terminals.

To verify these connections, use SEL-487E metering (see *Metering on page 7.1*). You can also review metering data in an event report that results when you issue the **TRIGGER** command (see *Triggering Data Captures and Event Reports on page 9.6 in the SEL-400 Series Relays Instruction Manual*).

Fixed Terminal Blocks

Connect the secondary circuits to the **Y** and **Z** terminal blocks on the relay rear panel. Note the polarity dots above the odd-numbered terminals for CT inputs. Similar polarity dots are above the odd-numbered terminals for PT inputs.

Connectorized

For the Connectorized SEL-487E, order the wiring harness kit, SEL-WA0487E. The wiring harness contains eight prewired connectors for the relay current and voltage inputs.

You can order the wiring harness with various wire sizes and lengths. Contact your local Technical Service Center or the SEL factory for ordering information.

Perform the following steps to install the wiring harness:

Step 1. Plug the CT shorting connectors into terminals #Y01 through #Y18 and #Z01 through #Z18 as appropriate.

Odd-numbered terminals are the polarity terminals.

Step 2. Secure the connector to the relay chassis with the two screws located on each end of the connector.

When you remove the CT shorting connector, pull straight away from the relay rear panel.

As you remove the connector, internal mechanisms within the connector separately short each power system current transformer.

You can install these connectors in only one orientation.

Step 3. Plug the PT voltage connectors into terminals #Y19 to #Y24 for the W inputs, and #Z19 to #Z24 for the VZ inputs, as appropriate.

Odd-numbered terminals are the polarity terminals. You can install these connectors in only one orientation.

Control Circuit Connections

You can configure the SEL-487E with many combinations of control inputs and control outputs. See *Main Board I/O on page 2.11* and *I/O Interface Boards on page 2.12* for information about I/O configurations. This section provides details about connecting these control inputs and outputs. Refer to *Figure 2.3–Figure 2.6* for representative rear-panel screw-terminal connector locations.

Control Inputs

No control input on the relay is polarity sensitive, which means you cannot damage these inputs with a reverse polarity connection. Note that the main board I/O control inputs have one set of two inputs that share a common input leg. These inputs are IN106 and IN107 found on Terminals A30, A31, and A32. To assign the functions of the control inputs, see *Operating the Relay Inputs and Outputs on page 3.53 in the SEL-400 Series Relays Instruction Manual*, or the **SET G** command in *SET on page 9.6* for more details. You can also use QuickSet to set and verify operation of the inputs.

Control Outputs

The SEL-487E has the following three types of outputs:

➤ Standard outputs (for example: main board OUT104)

➤ Hybrid (high-current interrupting) outputs (for example: main board OUT101)

➤ High-speed, high-current interrupting (for example: INT4 board OUT01). See *Control Outputs on page 2.8* for more information.

You can connect the standard outputs and the high-speed, high-current interrupting outputs in either ac or dc circuits. Connect the high-current interrupting outputs to dc circuits only. The screw-terminal connector legends alert you about these requirements by showing polarity marks on the hybrid (high-current interrupting) contacts and HS marks on the high-speed, high-current interrupting contacts. Two pairs of Form C contacts are on the main board.

Alarm Output

The SEL-487E monitors internal processes and hardware in continual self-tests. If the relay senses an out-of-tolerance condition, the relay declares a Status Warning or a Status Failure. The relay signals a Status Warning by pulsing the HALARM Relay Word bit (hardware alarm) to a logical 1 for five seconds. For a Status Failure, the relay latches the HALARM Relay Word bit at logical 1. To provide remote alarm status indication, connect the b contact of OUT108 to your control system remote alarm input. *Figure 2.25* shows the configuration of the a and b contacts of control output OUT108.
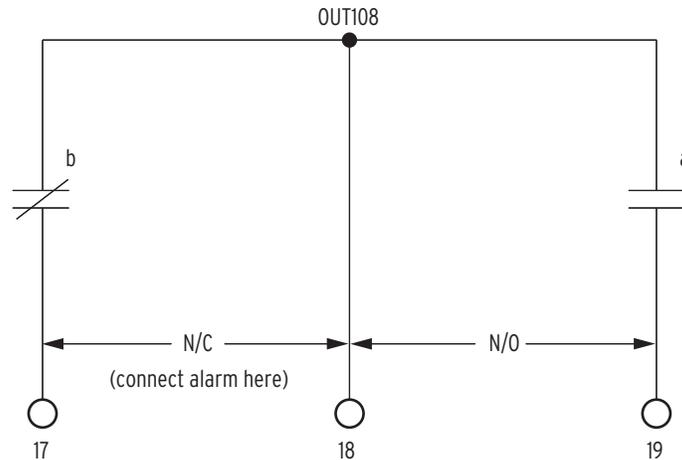
Figure 2.25   Control Output OUT108

Program OUT108 to respond to NOT HALARM by entering the following SELOGIC control equation with a communications terminal or QuickSet:

OUT108 := **NOT HALARM**

When the relay is operating normally, the NOT HALARM signal is at logical 1 and the b contacts of control output OUT108 are open. When a Status Warning condition occurs, the relay pulses the NOT HALARM signal to logical 0 and the b contacts of OUT108 close momentarily to indicate an alarm condition. For a Status Failure, the relay disables all control outputs and the OUT108 b contacts close to trigger an alarm. Also, when relay power is off, the OUT108 b contacts close to generate a power-off alarm. See *Relay Self-Tests on page 10.19 in the SEL-400 Series Relays Instruction Manual* for information on relay self-tests. The relay pulses the SALARM Relay Word bit for software programmed conditions; these conditions include settings changes, access level changes, alarming after three unsuccessful password entry attempts, and Ethernet firmware upgrade attempts.

You can add the software alarm SALARM to the alarm output by entering the following SELOGIC control equation:

OUT108 := **NOT (HALARM OR SALARM)**

Tripping and Closing Outputs

To assign the control outputs for tripping, see *Setting Outputs for Tripping and Closing on page 3.59 in the SEL-400 Series Relays Instruction Manual*. In addition, you can use the **SET O** command; see *SET on page 9.6* for more details.

TiDL Connections

SEL-487E-3, -4 Relays that support TiDL have a 4U chassis. The SEL-487E supports I/O on the main board as well as one additional I/O board. The main board and additional I/O board map to the 100- and 200-level inputs and outputs. The Axion remote modules provide additional I/O for the 300, 400, and 500 levels and analog channels.

The protection functions remain unchanged from the standard SEL-487E-3, -4 Relay.

Axion Remote Modules

The SEL-2240 Axion is a fully integrated analog and digital I/O control solution that is suitable for remote data acquisition. An Axion node consists of a 10-slot, 4-slot, or dual 4-slot chassis that is configurable to contain a power module and combinations of CT/PT, digital input (DI), or digital output (DO) modules.
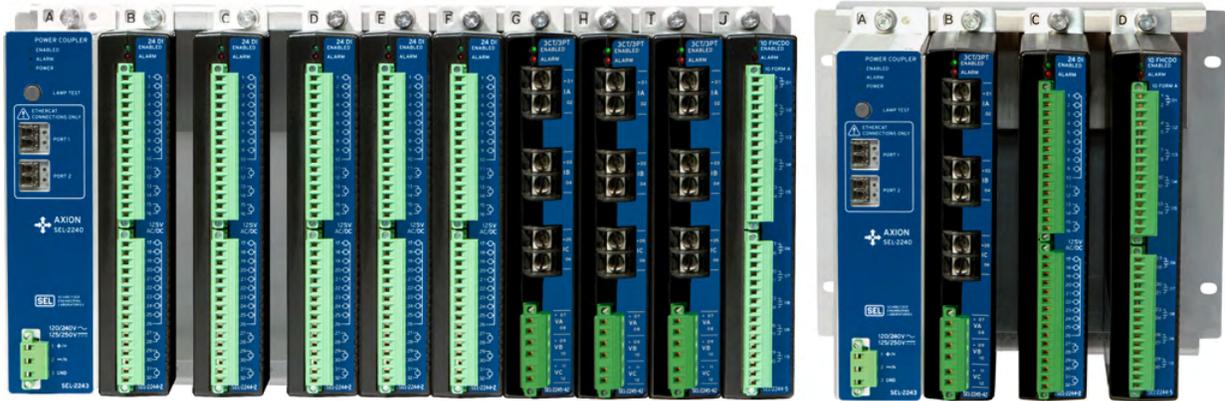
Figure 2.26   Axion Chassis

SEL-2243 Power Coupler

Each chassis requires an SEL-2243 Power Coupler (see *Figure 2.27*). This module supplies power to the rest of the node and transmits the data to the relay through fiber-optic communication. Although the power coupler has two fiber-optic ports, only **PORT 1** is currently used for TiDL.

Figure 2.27   SEL-2243 Power Coupler

The SEL-2243 has sufficient power capacity to accommodate an entire Axion node. The terminal strip at the bottom of the unit (shown in *Figure 2.27*) is the connection point for incoming power. All Axion modules have a 55-position IEC C-style connector that provides a communications and power interface to the backplane. See the *SEL-2240 Axion Instruction Manual* for more information.

SEL-2244-2 Digital Input Module

The SEL-2244-2 Digital Input Module (see *Figure 2.28*) consists of 24 optoisolated inputs that are not polarity-dependent. These inputs can be configured to respond to ac or dc control signals. The TiDL system maps as many as 72 DI points to the relay in the 300, 400, and 500 I/O board levels, based on the modules that occur in the network. Only the first 12 of 24 inputs are used in each module to help distribute the I/O around the network more efficiently. The inputs are mapped to the relay inputs based on the order in which the DI module occurs in the TiDL network.

There can be multiple DI modules in an Axion node, and the order of the DI modules will proceed from left to right in the node to determine the mapping of the inputs.

The first DI module that exists in the system, for example, on **PORT 6A**, will map to **IN301**–**IN312**, and if a second module is available on **PORT 6A**, it will map to **IN313**–**IN324**. If a second module does not exist on **PORT 6A**, **IN313**–**IN324** will be mapped from the next module appearing in the TiDL system. Mapping order determination starts with **PORT 6A** and ends with the last port, **PORT 6H**.

First SEL-2244-2 DI Module	**IN301**–**IN312**
Second SEL-2244-2 DI Module	**IN313**–**IN324**
Third SEL-2244-2 DI Module	**IN401**–**IN412**
Fourth SEL-2244-2 DI Module	**IN413**–**IN424**

Fifth SEL-2244-2 DI Module   **IN501–IN512**

Sixth SEL-2244-2 DI Module   **IN513–IN524**
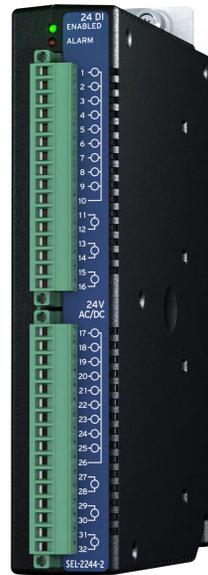
Figure 2.28   SEL-2244-2 Digital Input Module

SEL-2244-5 Fast High-Current Digital Output Module

The SEL-2244-5 Fast High-Current Digital Output Module consists of 10 fast, high-current output contacts. The outputs use the first 8 of the 10 outputs and map as follows:

First SEL-2244-5 DO Module   **OUT301–OUT308**

Second SEL-2244-5 DO Module   **OUT309–OUT316**

Third SEL-2244-5 DO Module   **OUT401–OUT408**

Fourth SEL-2244-5 DO Module   **OUT409–OUT416**

Fifth SEL-2244-5 DO Module   **OUT501–OUT508**

Sixth SEL-2244-5 DO Module   **OUT509–OUT516**
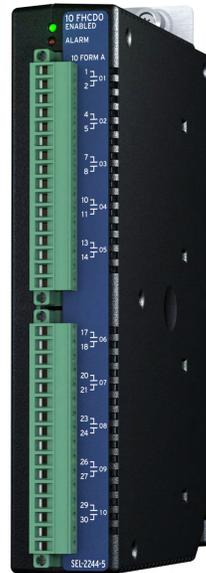
Figure 2.29   SEL-2244-5 Fast High-Current Digital Output Module

For both the DI and DO modules, use 24–12 AWG (0.2–3.31 mm^2) wire of suffi-
cient current capacity to connect to the digital input and output terminals for your
application.

The order of mapping for DO modules is the same as that for DI modules.

SEL-2245-42 AC Analog Input Module

The SEL-2245-42 AC Analog Input Module (see *Figure 2.30*) provides protec-
tion-class ac analog input (CT/PT) and can accept three voltage and three current
inputs. The module samples at 24 kHz and is 1 A or 5 A software-selectable.
Depending on the supported fixed topology, multiple CT/PT input modules can
function in each node. Some topologies only support one CT/PT module per
node. See *Topologies on page 2.34* for more information on supported relay
topologies and their connections.

Figure 2.30   SEL-2245-42 AC Analog Input Module

Topologies

The SEL-487E-3, -4 Relay has a set of fixed topologies. These topologies map the voltages and currents internally in the relay to maintain existing settings and functionality. When the TiDL system is commissioned (see *Commissioning on page 2.36*), the firmware validates the connected Axion nodes and identifies if the installed CT/PT modules in the system match one of the supported topologies for the SEL-487E.

Ports listed as optional in the following topology diagrams do not require a CT/PT module to be connected to them. All other ports require a CT/PT module connected for the relay to verify the topology.

Port	Analogs
6A	IAS, IBS, ICS, VAV, VBV, VCV
	IAT, IBT, ICT
	IAU, IBU, ICU (optional)
	IAW, IBW, ICW (optional)
	IAX, IBX, ICX (optional)
	IY1, IY2, IY3 (optional)
6B	VAZ, VBZ, VCZ
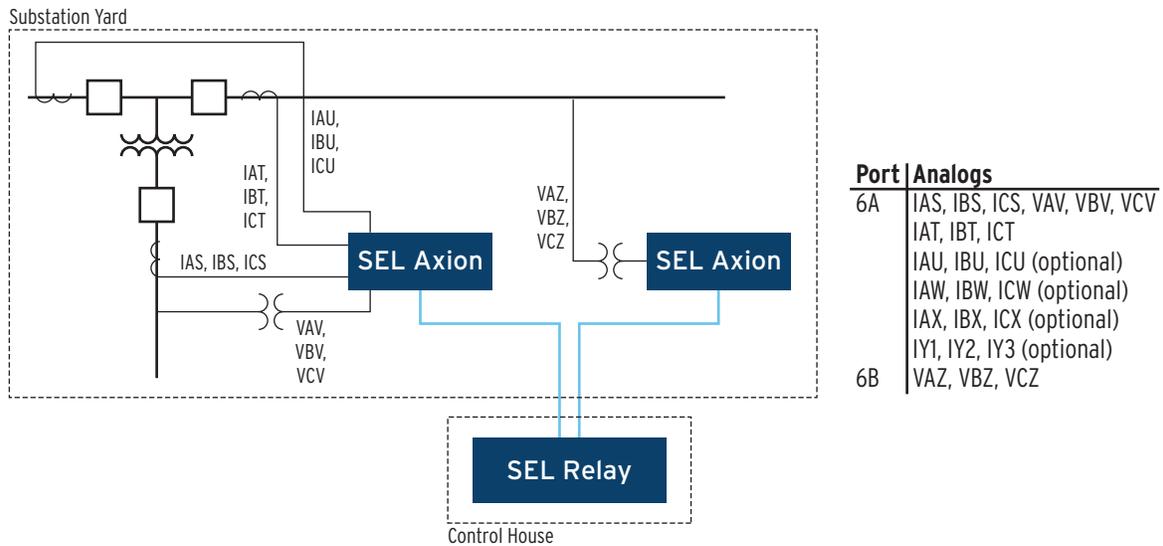
This topology uses three to seven CT/PT modules installed in one Axion node. The first module maps to the S currents and V voltages, the second module maps to the T currents, the third maps to the U currents, etc.

Figure 2.31   Topology 1

Port	Analogs
6A	IAS, IBS, ICS, VAV, VBV, VCV
6B	IAT, IBT, ICT (optional)
6C	IAU, IBU, ICU, VAZ, VBZ, VCZ
6D	IAW, IBW, ICW (optional)
6E	IAX, IBX, ICX (optional)
6F	IY1, IY2, IY3 (optional)
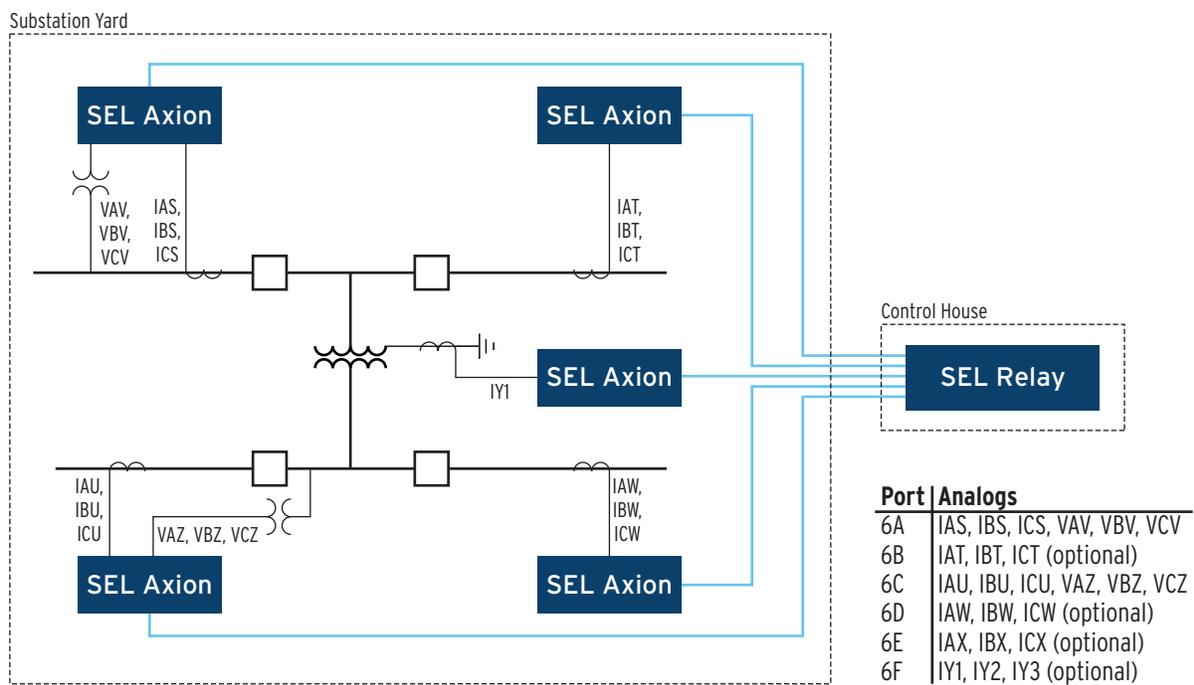
Figure 2.32   Topology 2
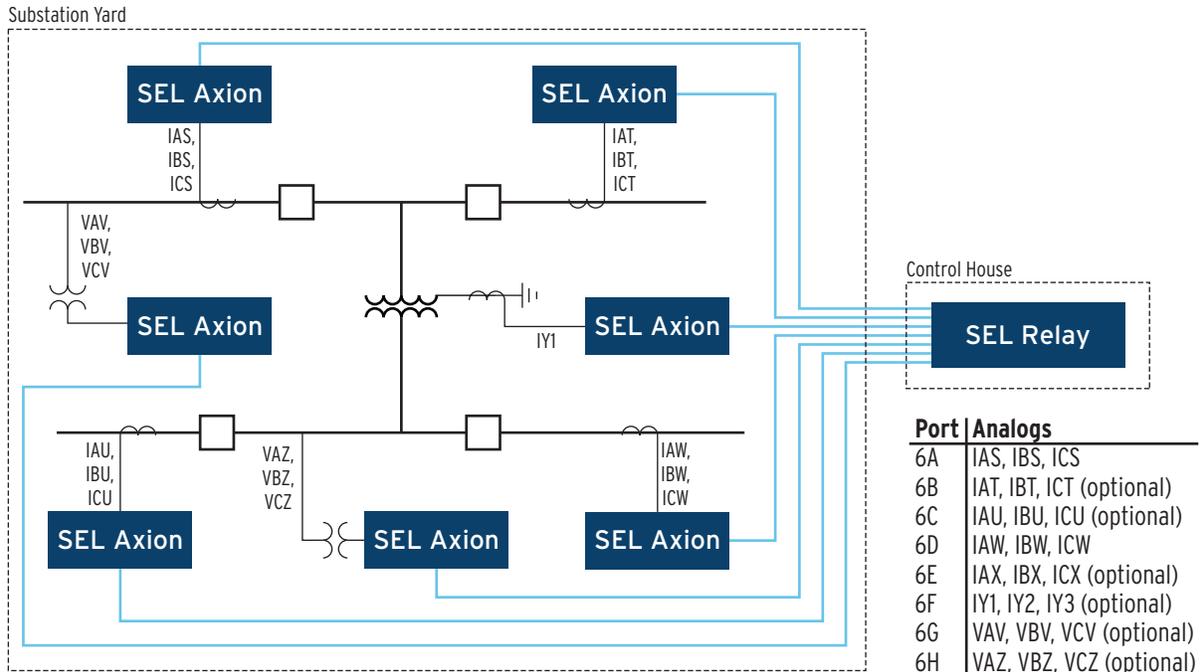
Figure 2.33   Topology 3
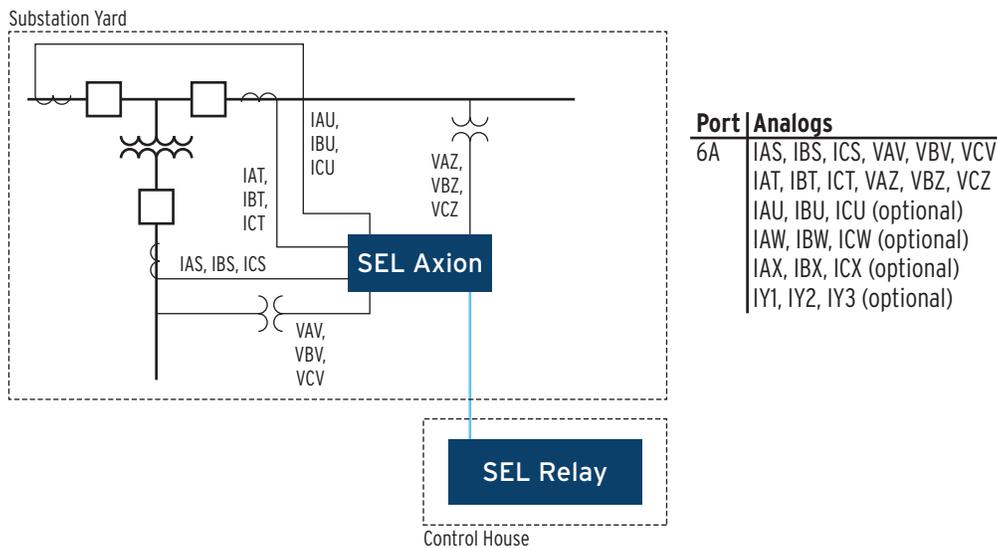
This topology uses two to six CT/PT modules installed in one Axion node. The first module maps to the S currents and V voltages, the second module maps to the T currents and Z voltages, the third maps to the U currents, etc.

Figure 2.34   Topology 4

Commissioning

In TiDL applications, the relay receives currents from a remote module. You must set the nominal current input of the relay to either 1 A or 5 A. Many settings and ranges of settings depend on the nominal current. Use the **CFG CTNOM** command to set the nominal current value. At Access Level 2, issue the **CFG CTNOM** i j command to modify the nominal currents. See *Table 2.8* and *Table 2.9* for the available options for the command parameters. This command is only available in relays that support TiDL technology. Note that after issuing this command, the relay settings are forced to their default values and the relay turns

off and back on again to reinitialize the settings. The relay defaults to 5 A nominal, so only use this command if you are switching to a 1 A setting (see *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual* for more information). The SEL-2245-42 AC Analog Input Module also sets its internal calculations based on this command. The relay internally transmits these data to the Axion modules and adjusts the scaling appropriate in the Axion module when this command is used.

Table 2.8   CFG CTNOM *i* Parameter Options

Parameter *i*	Terminal S	Terminal T	Terminal U
1	5 A	5 A	5 A
2	5 A	5 A	1 A
3	5 A	1 A	1 A
4	1 A	1 A	1 A

Table 2.9   CFG CTNOM *j* Parameter Options

Parameter *j*	Terminal W	Terminal X	Terminal Y1	Terminal Y2	Terminal Y3
1	5 A	5 A	5 A	5 A	5 A
2	5 A	5 A	5 A	5 A	1 A
3	5 A	5 A	5 A	1 A	1 A
4	5 A	5 A	1 A	1 A	1 A
5	1 A	1 A	5 A	5 A	5 A
6	1 A	1 A	5 A	5 A	1 A
7	1 A	1 A	5 A	1 A	1 A
8	1 A	1 A	1 A	1 A	1 A

In addition to the CT nominal values, TiDL relays also require that the nominal frequency be set by issuing the **CFG NFREQ** command. At Access Level 2, issue a **CFG NFREQ 60** command to set the relay to 60 Hz nominal or issue a **CFG NFREQ 50** command to set the relay to 50 Hz nominal. This command changes the NFREQ setting and restarts the relay, and it is only available in TiDL relays. The relay defaults to 60 Hz. This command should be issued after the **CFG CTNOM** command but before settings are sent to the relay.

The TiDL system uses a commissioning feature to identify that the connected remote Axion nodes meet the requirements of the supported topologies for the applied relay. These topologies are a balance between copper reduction and number of nodes. The nodes must be connected in one of the supported topologies so that the relay will map the voltages and currents accordingly.

The SEL-487E has a new interface on its back panel that replaces the original CT and PT input connections. These standard inputs are replaced with a remote module interface that supports eight fiber ports, labeled PORT 6A–PORT 6H (see *Figure 2.35*).
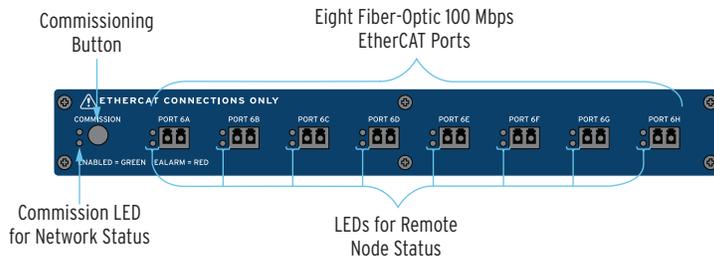
Figure 2.35   Remote Module Interface

Once all the remote Axion nodes are connected to the relay, press the **COMMISSION** pushbutton on the Remote Module Interface. This process verifies that the connected ports and Axion nodes are installed according to one of the supported topologies. Once the process is complete, the topology is stored in memory. At each additional startup of the relay, the firmware validates that the connected modules match those of the stored configuration. It recognizes whether any of the CT/PT modules within the node have changed. If the topology needs to be changed (e.g., modules are added or replaced), the system will need to be recommissioned by pressing the **COMMISSION** pushbutton.

When the commissioning and validation of the topology is complete, the voltages and currents map according to the topology assignments (see *Topologies on page 2.34*). Secondary injection testing takes place at each Axion node. Test sources must inject voltages and currents to the Axion node to verify correct installation and mapping. Monitoring of the voltages and currents remains in the control house with the relay.

LED Status

As shown in *Figure 2.35*, the TiDL relay provides LED status indication about the network and configuration. Once the system is connected, and the **COMMISSION** pushbutton is pressed, the LEDs will provide the status of the commissioning process. *Table 2.10* shows the status of the rear-panel LEDs for each commissioning state.

Table 2.10   TiDL LED Status (Sheet 1 of 2)

State	Description	LED Status	
Initial State	Determining if topology exists	Green **COMMISSION** LED	OFF
		Red **COMMISSION** LED	ON
		Green LED: **PORT 6A–PORT 6H**	OFF
		Red LED: **PORT 6A–PORT 6H**	ON
Verify Topology	Determining if topology is supported	Green **COMMISSION** LED	Blinking
		Red **COMMISSION** LED	ON
		Green LED: **PORT 6A–PORT 6H**	Blinking
		Red LED: **PORT 6A–PORT 6H**	ON

Table 2.10   TiDL LED Status (Sheet 2 of 2)

State	Description	LED Status	
Topology Mismatch	Connection does not match supported topology	Green **COMMISSION** LED	Blinking
		Red **COMMISSION** LED	ON
		Green LED: **PORT 6A**–**PORT 6H**	OFF—mismatched/unused
			ON—matched
		Red LED: **PORT 6A**–**PORT 6H**	Blinking—mismatched
			ON—matched
			OFF—ports unused
Topology Matched	Connection matches topology	Green **COMMISSION** LED	ON
		Red **COMMISSION** LED	OFF
		Green LED: **PORT 6A**–**PORT 6H**	ON
		Red LED: **PORT 6A**–**PORT 6H**	OFF
N/A	A commissioned port experiences an error	Green **COMMISSION** LED	ON
		Red **COMMISSION** LED	OFF
		Green LED: **PORT 6A**–**PORT 6H**	ON
		Red LED: **PORT 6A**–**PORT 6H**	Blinking—failed port

IRIG-B Input Connections

The SEL-487E accepts a demodulated IRIG-B signal through two types of rear-panel connectors. These IRIG-B inputs are the BNC connector labeled **IRIG-B** and Pin 4 (+) and Pin 6 (–) of the DB-9 rear-panel serial port labeled **PORT 1**. When you use the **PORT 1** input, ensure that you connect Pins 4 and 6 with the proper polarity. See *Communications Ports Connections on page 2.40* for other DB-9 connector pinouts and additional details.

These inputs accept the dc shift time-code generator output (demodulated) IRIG-B signal with positive edge on the time mark. See *Section 11: Time and Date Management in the SEL-400 Series Relays Instruction Manual* for more information on IRIG-B inputs.

The **PORT 1** IRIG-B input connects to a 2.5 kΩ grounded resistor and goes through a single logic signal buffer. The **PORT 1** IRIG-B is equipped with robust ESD and overvoltage protection but is not optically isolated. When you are using the **PORT 1** input, ensure that you connect Pin 4 (+) and Pin 6 (–) with the proper polarity.

The IRIG network should be properly terminated with an external termination resistor (SEL 240-1802, BNC Tee, and SEL 240-1800, BNC terminator, 50 ohm) placed on the unit that is farthest from the source. This termination provides impedance matching of the cable for the best possible signal-to-noise ratio.

Where distance between the SEL-487E and the IRIG-B sending device exceeds the cable length recommended for conventional EIA-232 metallic conductor cables, you can use transceivers to provide isolation and to establish communication to remote locations.

Conventional fiber-optic and telephone modems do not support IRIG-B signal transmission. The SEL-2810 Fiber-Optic Transceiver/Modem includes a channel for the IRIG-B time code. These transceivers enable you to synchronize time precisely from IRIG-B time-code generators (such as the SEL-2032 Communications Processor) over a fiber-optic communications link.

For ease of connection or for runs as long as 91.44 m (300 ft) between the IRIG-B generator and the SEL-487E, use the BNC IRIG-B input to connect the IRIG-B input of the SEL-487E to the IRIG-B generation equipment. Make this connection with a 50-ohm coaxial cable assembly.

Communications Ports Connections

The SEL-487E has three rear-panel EIA-232 serial communications ports labeled **PORT 1**, **PORT 2**, and **PORT 3** and one front-panel port, **PORT F** (see *Section 10: Communications Interfaces*). In addition, the rear panel features **PORT 5** for an optional factory-installed Ethernet communications card. For additional information about communications topologies and standard protocols that are available in the SEL-487E, see *Section 10: Communications Interfaces*, *DNP3 Communication on page 10.9*, and *IEC 61850 Communication on page 10.35*.

Serial Ports

The SEL-487E serial communications ports use EIA-232 standard signal levels in a DB-9 connector. To establish communication between the relay and a DTE device (a computer terminal, for example) with a DB-9 connector, use an SEL-C234A cable. Alternatively, you can use an SEL-C662 cable to connect to a USB port.

Figure 2.23 shows the configuration of an SEL-C234A cable that you can use for basic ASCII and binary communication with the relay. A properly configured ASCII terminal, terminal emulation program, or QuickSet along with the SEL-C234A cable provide communication with the relay in most cases.

SEL-487E Relay				9-Pin DTE Device	
Pin Func.	Pin #			Pin #	Pin Func.
RXD	2	————————		3	TXD
TXD	3	————————		2	RXD
GND	5	————————		5	GND
CTS	8	————————		8	CTS
				7	RTS
				1	DCD
				4	DTR
				6	DSR
SHELL		———— SHIELD ————		NO CONNECTION	
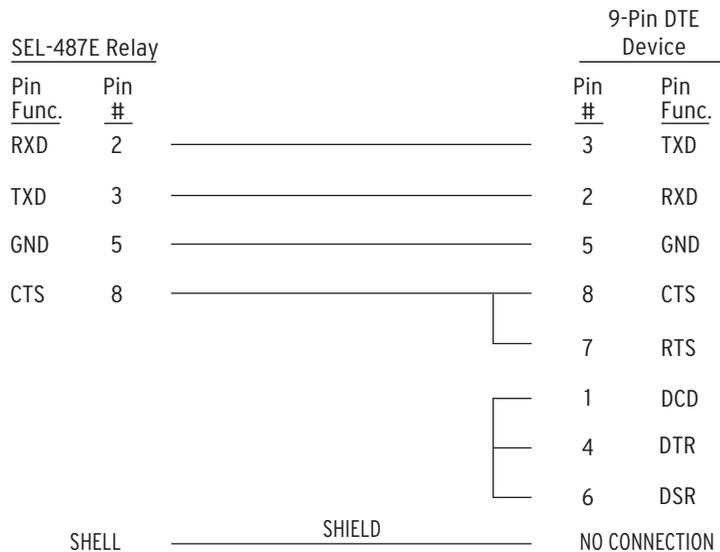
Figure 2.36   SEL-487E to Computer DB-9 Connector Diagram

Serial Cables

⚠ **CAUTION**
Severe power and ground problems can occur on the communications ports of this equipment as a result of using non-SEL cables. Never use standard null-modem cables with this equipment.

Using an improper cable can cause numerous problems or failure to operate, so you must be sure to specify the proper cable for application of your SEL-487E. Several standard SEL communications cables are available for use with the relay.

The following list provides additional rules and practices you should follow for successful communication using EIA-232 serial communications devices and cables.

➤ Route communications cables well away from power and control circuits. Switching spikes and surges in power and control circuits can cause noise in the communications circuits if power and control circuits are not adequately separated from communications cables.

➤ Keep the length of the communications cables as short as possible to minimize communications circuit interference and also to minimize the magnitude of hazardous ground potential differences that can develop during abnormal power system conditions.

➤ Ensure that EIA-232 communications cable lengths never exceed 15.25 m (50 ft), and always use shielded cables for communications circuit lengths greater than 13.05 m (10 ft).

➤ Modems provide communication over long distances and give isolation from ground potential differences that are present between device locations (examples are the SEL-2800 series transceivers).

➤ Lower data speed communication is less susceptible to interference and will transmit greater distances over the same medium than higher data speeds. Use the lowest data speed that provides an adequate data transfer rate.

Ethernet Network Connections

The optional Ethernet card for the SEL-487E comes with two ports, either A and B or C and D. You can use either installed port. These ports can work together to provide a primary and backup interface. Other operating modes (FIXED and SWITCHED) are also available. The following list describes the Ethernet card port options.

➤ 10/100BASE-T. 10 Mbps or 100 Mbps communications using Cat 5 cable (category 5 twisted-pair) and an RJ45 connector

➤ 100BASE-FX. 100 Mbps communications over multimode fiber-optic cable using an LC connector

Ethernet Card Rear-Panel Layout

⚠**CAUTION**
Use of controls or adjustments, or performance of procedures other than those specified herein, may result in hazardous radiation exposure.

⚠**WARNING**
Do not look into the end of an optical cable connected to an optical output.

⚠**WARNING**
Do not perform any procedures or adjustments that this instruction manual does not describe.

⚠**WARNING**
During installation, maintenance, or testing of the optical ports, use only test equipment qualified for Class 1 laser products.

Rear-panel layouts for the three Ethernet card port configurations are shown in *Figure 2.37–Figure 2.42*.

Figure 2.37   Two 100BASE-FX Port Configuration on Ports 5A and 5B
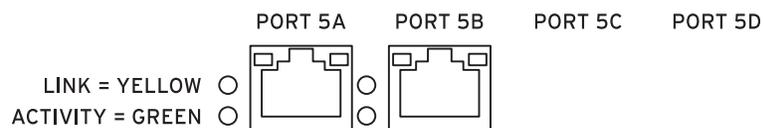
Figure 2.38   Two 10/100BASE-T Port Configuration on Ports 5A and 5B

PORT 5A   PORT 5B   PORT 5C   PORT 5D

LINK = YELLOW
ACTIVITY = GREEN

Figure 2.39   100BASE-FX and 10/100BASE-T Port Configurations on Ports 5A and 5B

PORT 5A   PORT 5B   PORT 5C   PORT 5D

LINK = YELLOW
ACTIVITY = GREEN

Figure 2.40   Two 10/100BASE-T Port Configuration on Ports 5C and 5D

PORT 5A   PORT 5B   PORT 5C   PORT 5D

LINK = YELLOW
ACTIVITY = GREEN

Figure 2.41   100BASE-FX and 10/100BASE-T Port Configuration on Ports 5C and 5D

PORT 5A   PORT 5B   PORT 5C   PORT 5D

LINK = YELLOW
ACTIVITY = GREEN

Figure 2.42   Two 100BASE-FX Port Configuration on Ports 5C and 5D

Twisted-Pair Networks

While Unshielded Twisted Pair (UTP) cables dominate office Ethernet networks, Shielded Twisted Pair (STP) cables are often used in industrial applications. The SEL-487E Ethernet card is compatible with standard UTP cables for Ethernet networks as well as STP cables for Ethernet networks.

NOTE: Use caution with UTP cables as these cables do not provide adequate immunity to interference in electrically noisy environments unless additional shielding measures are employed.

Typically UTP cables are installed in relatively low-noise environments including offices, homes, and schools. Where noise levels are high, you must either use STP cable or shield UTP using grounded ferrous raceways such as steel conduit.

Several types of STP bulk cable and patch cables are available for use in Ethernet networks. If noise in your environment is severe, you should consider using fiber-optic cables. We strongly advise against using twisted-pair cables for segments that leave or enter the control house.

If you use twisted-pair cables, you should use care to isolate these cables from sources of noise to the maximum extent possible. Do not install twisted-pair cables in trenches, raceways, or wireways with unshielded power, instrumentation, or control cables. Do not install twisted-pair cables in parallel with power, instrumentation, or control wiring within panels; rather, make them perpendicular to the other wiring.

You must use a cable and connector rated as Category 5 (Cat 5) to operate the twisted-pair interface (10/100BASE-T) at 100 Mbps. Because lower categories are becoming rare and because you may upgrade a 10 Mbps network to 100 Mbps, we recommend using all Cat 5 components.

Some industrial Ethernet network devices use 9-pin connectors for STP cables. The Ethernet card RJ45 connectors are grounded so you can ground the shielded cable using a standard, externally shielded jack with cables terminating at the Ethernet card.

AC/DC Connection Diagrams

You can apply the SEL-487E in many power system protection schemes. *Figure 2.43* shows an autotransformer with both HV and LV sides configured as breaker-and-a-half. This figure does not show any PT or dc connections. For more applications examples, see *Applications on page 1.9.*

Figure 2.44 shows typical dc connections for the SEL-487E. Because the application has Bay Control for both the HV and LV side (only HV disconnect connections shown), this example includes an INT4 interface board.
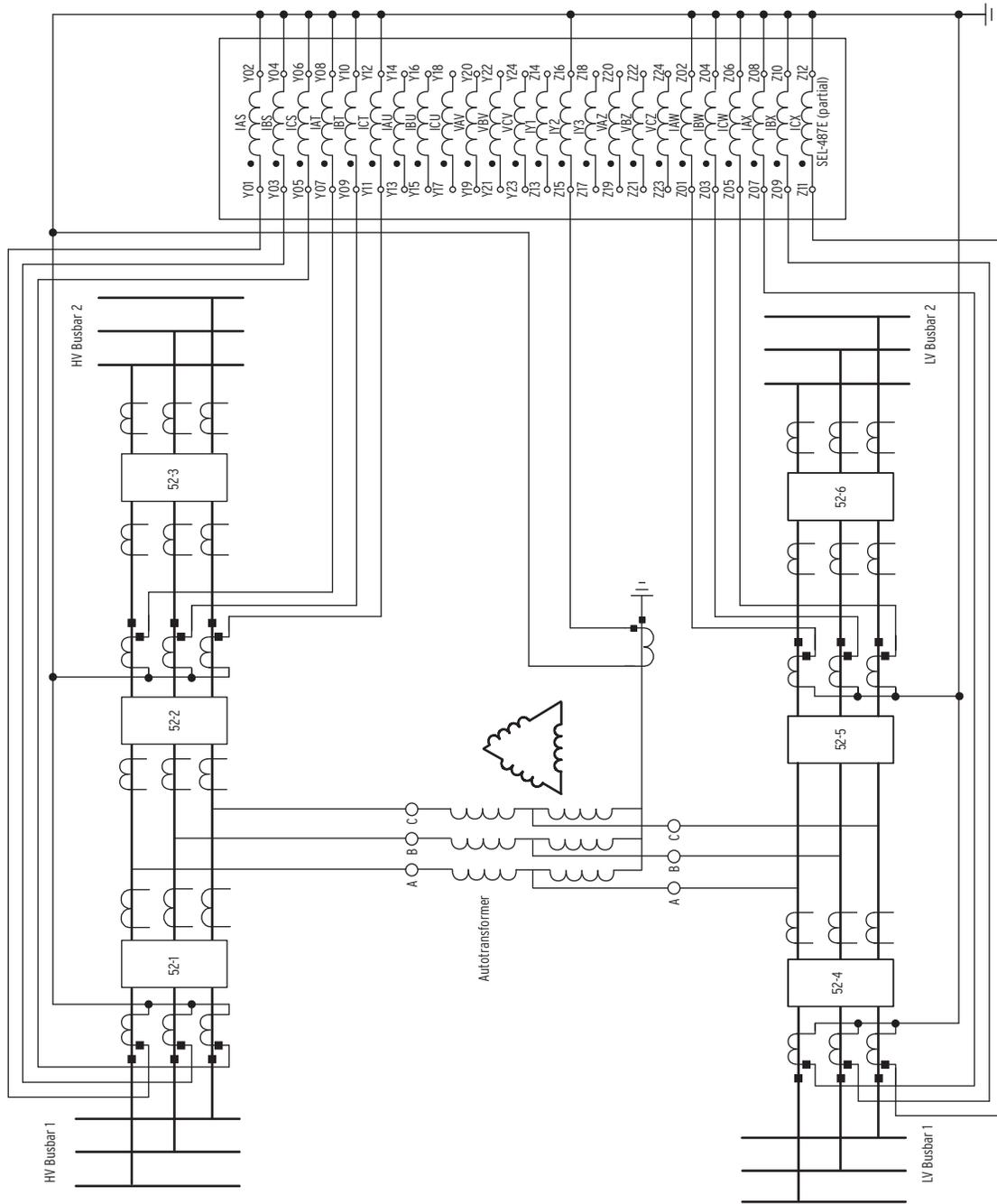
Figure 2.43 Autotransformer Application
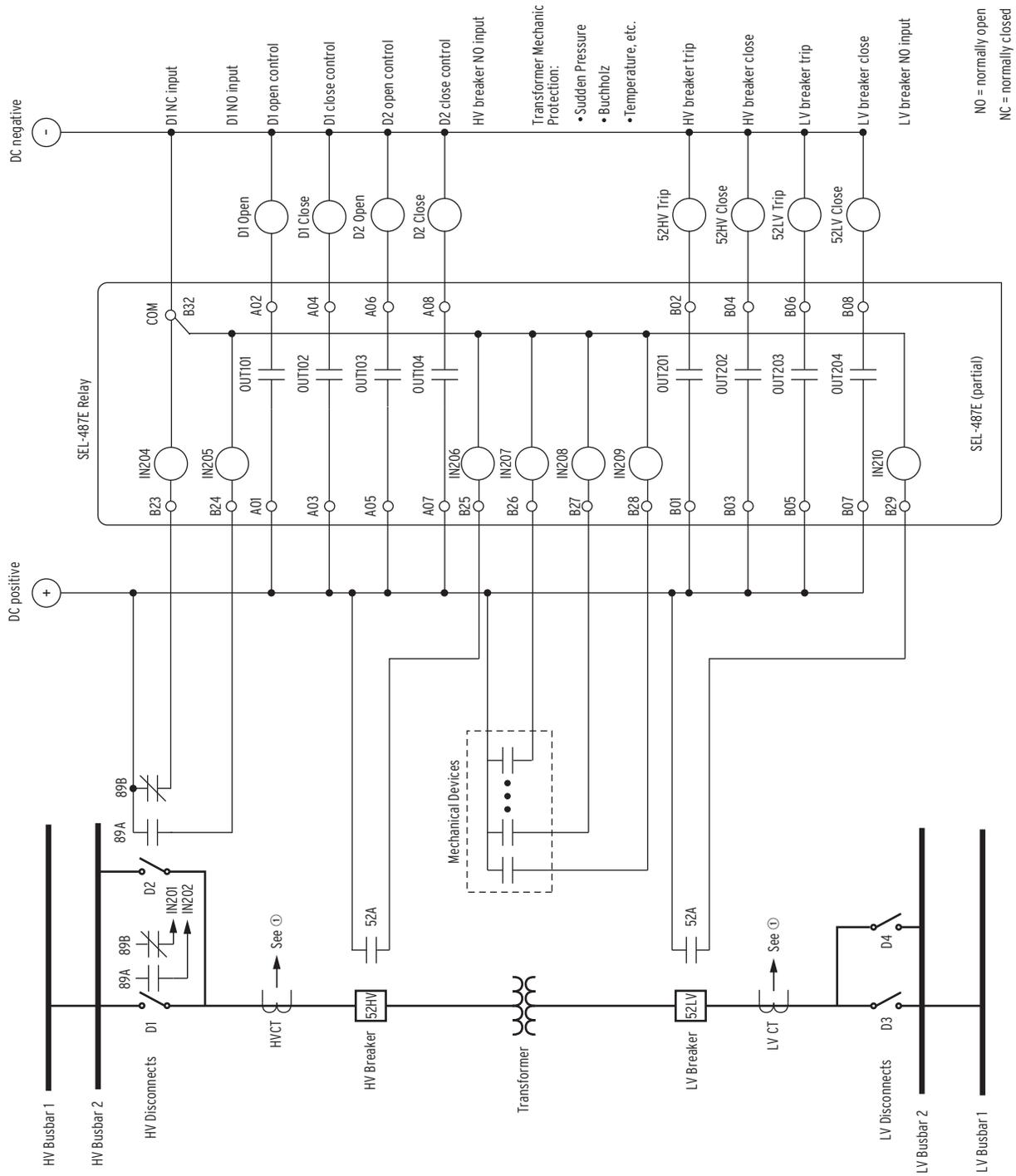
① *Figure 2.43.*

Figure 2.44   Typical External DC Connections

Figure 2.45 shows the connections for an open-delta connected PT when wired to the V-PT inputs. Connect the A-Phase and C-Phase polarity wires from the PT secondary to the SEL-487E A-Phase (**Y19**) and C-Phase (**Y23**) terminals with polarity marks. Connect the common point from the PT to the SEL-487E B-phase (**Y21**) terminal with polarity mark. Connect jumpers between terminals **Y20**, **Y22**, and **Y24**, and also connect this wire to **Y21**. *Figure 2.45* shows the

ground connection on the common point; be sure to follow the wiring standards of your company when grounding the PTs. However, be sure to apply only one ground to the PTs.
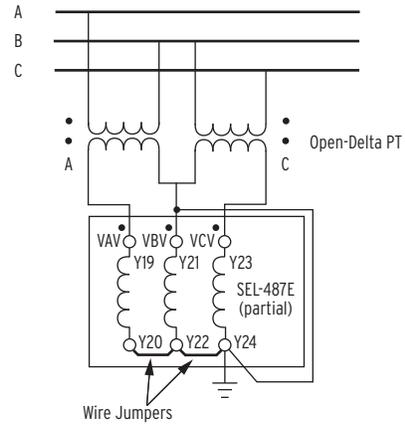
Figure 2.45   Wiring Connections for Open-Delta Connected PTs

Testing

This section provides guidelines for determining and establishing test routines for the SEL-487E relay. Follow the standard practices of your company in choosing testing philosophies, methods, and tools. *Section 10: Testing, Troubleshooting, and Maintenance in the SEL-400 Series Relays Instruction Manual* provides additional information related to testing.

Topics presented in this section include the following:

➤ *Low-Level Test Interface on page 3.1*

➤ *Relay Test Connections on page 3.4*

➤ *Selected Element Tests on page 3.4*

➤ *Commissioning Testing on page 3.30*

➤ *Technical Support on page 3.43*

➤ *SEL-487E Relay Commissioning Test Worksheet on page 3.44*

The SEL-487E is factory calibrated; this section contains no calibration information. If you suspect that the relay is out of calibration, contact your Technical Service Center or the SEL factory.

Low-Level Test Interface

⚠**CAUTION**
The relay contains devices sensitive to Electrostatic Discharge (ESD). Undetectable permanent damage can result if you do not use proper ESD procedures. Ground yourself, your work surface, and this equipment before removing any cover from this equipment. If your facility is not equipped to work with these components, contact SEL about returning this device and related SEL equipment for service.

You can test the relay in two ways: by using secondary injection testing or by applying low-magnitude ac voltage signals to the low-level test interface. This section describes the low-level test interface between the calibrated input module and the separately calibrated processing module.

Access the test interface by removing the relay front panel. At the right side of the relay main board is the processing module. Inputs to the processing module are multipin connectors J14 and J24, the analog or low-level test interface connections. Receptacle J24 is on the right side of the main board, with J14 located 5 cm (2 in) behind J24; see *Figure 2.16* for a locating diagram.

Figure 3.1 shows the J24 low-level interface connections and signal scaling factors. The J14 interface has the same scaling factors as the front interface, but with the channel allocation shown in *Figure 3.2*. Remove the ribbon cable between the two modules to access the outputs of the input module and the inputs to the processing module (relay main board). You can test the relay processing module using signals from a low-level test source, such as the SEL-RTS Low-Level Relay Test System. Never apply voltage signals greater than 6.6 V peak-to-peak to the low-level test interface.
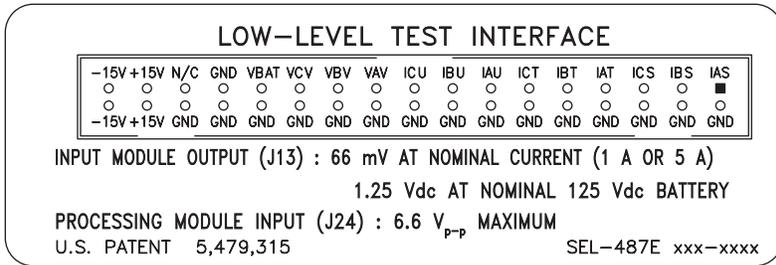
Figure 3.1   Low-Level Test Interface J24
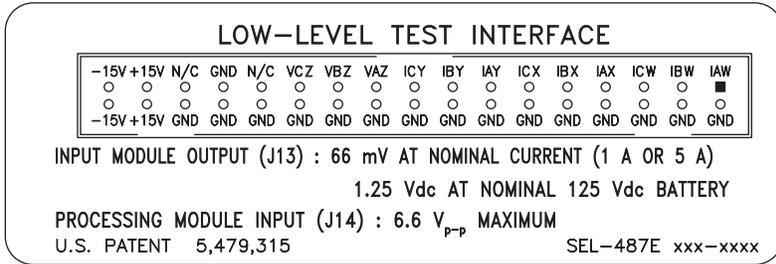
Figure 3.2   Low-Level Test Interface J14

Use signals from the Low-Level Relay Test System to test the relay processing module. These signals simulate power system conditions, taking into account PT ratio and CT ratio scaling. Use relay metering to determine whether the applied test voltages and currents produce correct relay operating quantities. The UUT Database entries for the SEL-487E in the SEL-5401 Relay Test System Software are shown in *Table 3.1–Table 3.4*.

Table 3.1   UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Y)–5 A Relay

Channel	Label	Scale Factor	Unit
1	IAS	75	A
2	IBS	75	A
3	ICS	75	A
4	IAT	75	A
5	IBT	75	A
6	ICT	75	A
7	IAU	75	A
8	IBU	75	A
9	ICU	75	A
10	VAV	150	V
11	VBV	150	V
12	VCV	150	V

Table 3.2   UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Z)–5 A Relay (Sheet 1 of 2)

Channel	Label	Scale Factor	Unit
1	IAW	75	A
2	IBW	75	A
3	ICW	75	A

Table 3.2 UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Z)–5 A Relay (Sheet 2 of 2)

Channel	Label	Scale Factor	Unit
4	IAX	75	A
5	IBX	75	A
6	ICX	75	A
7	IY1	75	A
8	IY2	75	A
9	IY3	75	A
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

Table 3.3 UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Y)–1 A Relay

Channel	Label	Scale Factor	Unit
1	IAS	15	A
2	IBS	15	A
3	ICS	15	A
4	IAT	15	A
5	IBT	15	A
6	ICT	15	A
7	IAU	15	A
8	IBU	15	A
9	ICU	15	A
10	VAV	150	V
11	VBV	150	V
12	VCV	150	V

Table 3.4 UUT Database Entries for SEL-5401 Relay Test System Software (Analog Input Board Z)–1 A Relay

Channel	Label	Scale Factor	Unit
1	IAW	15	A
2	IBW	15	A
3	ICW	15	A
4	IAX	15	A
5	IBX	15	A
6	ICX	15	A
7	IY1	15	A
8	IY2	15	A
9	IY3	15	A
10	VAZ	150	V
11	VBZ	150	V
12	VCZ	150	V

Relay Test Connections

Figure 3.3 shows the test set and relay connections for three-phase current injection.
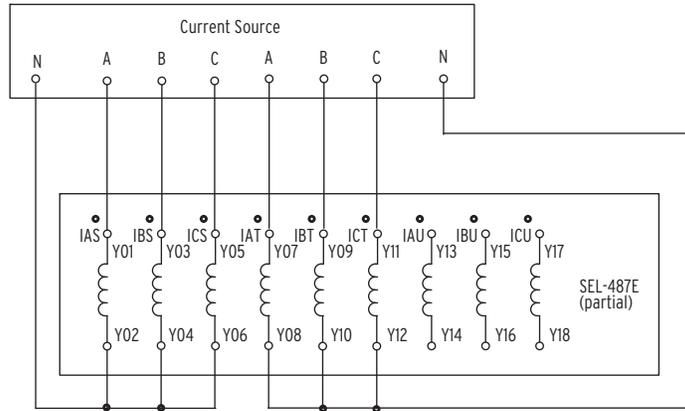
Figure 3.3   Test Connections for Balanced Load With Three-Phase Current Sources

Figure 3.4 shows the test set and relay connections for three-phase voltage injection.
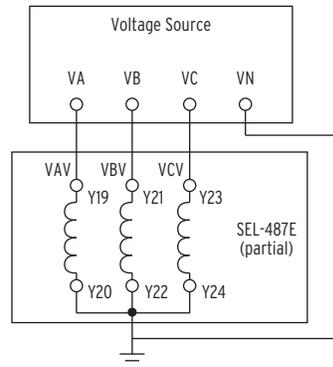
Figure 3.4   Voltage Test Connections

Selected Element Tests

This section discusses tests of selected functions in the SEL-487E. These tests are designed to show a method of testing a function in an easy way while at the same time familiarizing you with other functions such as programming logic functions, SER and the front panel. Each test starts with the default settings to avoid unexpected results from previous programming when testing other functions. This section provides tests for the following relay elements:

➤ Volts/Hertz Elements

➤ TOC (IDMT) Overcurrent Elements

➤ REF Elements

➤ Unrestrained-Phase Differential Element

➤ Restrained-Phase Differential Elements

➤ Negative-Sequence Differential Elements

➤ Negative-Sequence Directional Elements—Phase Elements

The paragraphs below describe when each type of test is performed, the goals of testing at that time, and the relay functions that you need to test at each point. This information is intended as a guideline for testing SEL relays.

Volts/Hertz

Although the V/Hz element offers definite-time and user-defined elements, this test shows how to test the user-defined function. For this test, you program a SELOGIC variable to assert LEDs on the front panel to indicate the status of the V/Hz element. You also program the SER to record the status of the V/Hz element, and then use these recorded values to calculate the element operating time(s).

Figure 3.5(a) shows a curve with four points defined, and *Figure 3.5(b)* shows an intermediate point Pt (107,?) between Point 24U101 and Point 24U102.
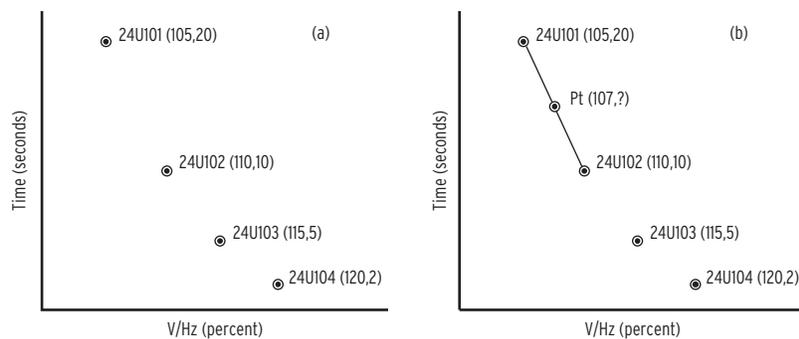
Figure 3.5   User-Defined V/Hz Curve 1

Because the relay linearly interpolates these data points, use *Equation 3.1* to calculate the operating time for a V/Hz value of 107 percent.

$$t = \left[\frac{t1 - t2}{P1 - P2}\right] \bullet Pt + \left[\frac{t1 \bullet P2 - t2 \bullet P1}{P2 - P1}\right]$$

Equation 3.1

where:

$\quad$ t1 = the operate time value of 24U101 (20)

$\quad$ P1 = the percentage V/Hz value of 24U101 (105)

$\quad$ t2 = the operate time value of 24U102 (10)

$\quad$ P2 = the percentage V/Hz value of 24U102 (110)

$\quad$ Pt = the percentage V/Hz value of 107 percent

$$t = \left[\frac{20 - 10}{105 - 110}\right] \bullet 107 + \left[\frac{20 \bullet 110 - 10 \bullet 105}{110 - 105}\right]$$

$$t = 16 \text{ seconds}$$

Equation 3.2

Table 3.5   Settings to Test the V/Hz Elements

Setting	Setting Category	Comments
EPTTERM = V	Group (SET)	Enable PT V; makes E24 settings available
E24 = Y	Group	Enable the V/Hz elements
24TC = 0	Group	Disable the definite-time V/Hz elements
24CCS = UI	Group	Select User-defined curve
24U1TC = 1	Group	Enable the logic for user-defined curves
24U1NP = 4	Group	Specify a curve with 4 points
24U101 = 105,20	Group	Coordinates for Point 1
24U102 = 110,10	Group	Coordinates for Point 2
24U103 = 115,5	Group	Coordinates for Point 3
24U104 = 120,2	Group	Coordinates for Point 4
PSV01 = 24RPU > 105	Protection Logic (SET L)	PSV01 asserts when V/Hz exceeds 105 percent
PSV02 = 24RPU > 107	Protection Logic	PSV02 asserts when V/Hz exceeds 107 percent
PB1_LED = PSV01	Front panel (SET F)	Pushbutton LED 1 reports the status of PSV01
PB1_COL = AG	Front panel	LED is amber when PSV01 asserts, and green when PSV01 deasserts
PB2_LED = PSV02	Front panel	Pushbutton LED 2 reports the status of PSV02
PB2_COL = AG	Front panel	LED is amber when PSV02 asserts, and green when PSV02 deasserts
PSV01,"V/Hz picked up"	Report (SER) (SET R)	Reports and time-stamps when PSV01 asserts
24U1T,"V/Hz timed out"	Report (SER)	Reports and time-stamps when V/Hz elements times out

Figure 3.6 shows the group settings (Group 1) for this test.

```
=>>SET <Enter>
Group 1

Relay Configuration

Enable Current Terminals (OFF or combo of S,T,U,W,X)
ECTTERM := "S,T"   ? <Enter>
Enable Voltage Terminals (OFF or combo of V,Z)       EPTTERM := OFF    ?V <Enter>
Enable Diff Elem. Prot. Terms (OFF or combo of S,T)
E87     := OFF    ? <Enter>
Enable Restricted Earth Fault Element (N,1-3)        EREF    := N     ? <Enter>
Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50     := OFF    ? <Enter>
Enable Inverse Time Overcurrent Elements (N, 1-10)   E51     := N     ? <Enter>
Enable Current Unb. Elements (OFF or combo of S,T)   E46     := OFF   ? <Enter>
Enable Over Voltage Elements (N,1-5)                 E59     := N     ? <Enter>
Enable Under Voltage Elements (N,1-5)                E27     := N     ? <Enter>
Enable Frequency Elements (N,1-6)                    E81     := N     ? <Enter>
Enable Volts per Hertz Element (Y,N)                 E24     := N     ?Y <Enter>
Enable Synch. Check (OFF or combo of S,T)            E25     := OFF   ? <Enter>
Enable Bkr Fail. Prot. (OFF or combo of S,T)         EBFL    := OFF   ? <Enter>
Enable Power Calc. Term (OFF or combo of S,T)        EPCAL   := OFF   ? <Enter>
Enable Demand Metering (N, 1-10)                     EDEM    := N     ? <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)            CTRS    := 100   ?> <Enter>

Potential Transformer Data

Potential Trans. Ratio Terminal V (1.0-10000.0)      PTRV   := 2000.0   ?> <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)            CTRS    := 100   ?> <Enter>

Potential Transformer Data

Potential Trans. Ratio Terminal V (1.0-10000.0)      PTRV   := 2000.0   ?> <Enter>

Voltage Reference Terminal Selection

Voltage Reference For Terminal S (OFF,V)             VREFS   := OFF   ?> <Enter>

Volts per Hertz Element

Level 1 Volts/Hertz P/U (100-200%)                   24D1P   := 110   ? <Enter>
Level 1 Time Delay (0.04 - 400 sec)                  24D1D   := 10.00 ? <Enter>
Volts/Hertz Torque control (SELogic Eqn)
24TC := 1
? 0 <Enter>
Level 2 composite Curve (OFF,DD,U1,U2)               24CCS   := OFF   ?U1 <Enter>

Volts per Hertz Level 2, User Defined Curve 1

User Defined Curve 1 Torque Control (SELogic Eqn)
24U1TC := 1 <Enter>
?
Number of Point on User 1 Curve (3-20)               24U1NP  := 3     ?4 <Enter>
User Def. Curve 1, Point 1 (100 - 200%, 0.04 - 400 sec)
24U101 := 200, 400.00
? 105,20 <Enter>
User Def. Curve 1, Point 2 (100 - 200%, 0.04 - 400 sec)
24U102 := 200, 400.00
? 110,10 <Enter>
User Def. Curve 1, Point 3 (100 - 200%, 0.04 - 400 sec)
24U103 := 200, 400.00
? 115,5 <Enter>
User Def. Curve 1, Point 4 (100 - 200%, 0.04 - 400 sec)
24U104 := 200, 400.00
? 120,2 <Enter>
User Def. Curve 1 Reset Time (0.01 - 400 sec)        24U1CR  := 0.01   ? <Enter>


Trip Logic

Trip Transformer (SELogic Eqn)
TRXFMR := 87R OR REFF1
? END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait..........
Settings Saved

=>>
```

Figure 3.6   Group Settings for the V/Hz Test

Figure 3.7 shows the Protection Logic setting for the test. Protection SELOGIC variable PSV01 asserts when the analog output (24RPU, see *Volts/Hertz Settings on page 5.95*) exceeds 105 percent, and PSV02 asserts when 24RPU exceeds 107 percent. Protection math variables PMV01 and PMV02 are included for easy monitoring of the values 24RPU and VPMAXVF.

```
=>>SET L TE <Enter>
Protection 1

1: # BREAKER S OPEN AND CLOSE CMD
?  >
21:
?  PSV01:=24RPU > 105 <Enter>
22:
?  PSV02:=24RPU > 107 <Enter>
23:
?  PMV01:=24RPU <Enter>
24:
?  PMV02:=VPMAXVF <Enter>
25:
?  END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait..........
Settings Saved

=>>
```

Figure 3.7   Logic Settings for the V/Hz Test

Program the front-panel pushbutton LEDs to indicate the status of PSV01 and PSV02. Set the LED to show amber when PSV01 (PB1_LED) and PSV02 (PB2_LED) are asserted, and to show green when PSV01 and PSV02 are deasserted. *Figure 3.8* shows the front-panel LED programming.

```
=>>SET F TE <Enter>
Front Panel

Front Panel Settings

Front Panel Display Time-Out (OFF,1-60 mins)      FP_TO   := 15     ?
Enable LED Asserted Color (R,G)                   EN_LEDC := G      ?
Trip LED Asserted Color (R,G)                     TR_LEDC := R      ?
Pushbutton LED 1 (SELogic Equation)
PB1_LED := NA
?  PSV01 <Enter>
PB1_LED Assert & Deassert Color (Enter 2: R,G,A,O)  PB1_COL := AO    ?AG <Enter>
Pushbutton LED 2 (SELogic Equation)
PB2_LED := NA
?  PSV02 <Enter>
PB2_LED Assert & Deassert Color (Enter 2: R,G,A,O)  PB2_COL := AO    ?AG <Enter>
Pushbutton LED 3 (SELogic Equation)
PB3_LED := NA
?  END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait..........
Settings Saved

=>>
```

Figure 3.8   Front-Panel Settings for the V/Hz Test

Use the sequential event recorder (SER) to record the exact time when PSV01 and PSV02 assert, and when the output from the V/Hz element (24U1T) asserts. Calculate the operating time of the V/Hz element by finding the difference between these two times. *Figure 3.9* shows the SER programming.

```
=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)    ESERDEL := N    ? <Enter>

SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
? PSV01,"V/Hz picked up 105" <Enter>
2:
? PSV02,"V/Hz picked up 107" <Enter>
3:
?  24U1T,"V/Hz timed out" <Enter>
4:
? END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait..........
Settings Saved

=>>
```

Figure 3.9   SER Settings for the V/Hz Test

This concludes the settings and programming. At this point, pushbutton PB1_LED and PB2_LED must both show green. Refer to *Figure 5.90* to see the logic that determines 24RPU. Notice that it compares the maximum phase-to-phase voltage with the nominal phase-to-phase voltage. To monitor 24RPU and VPMAXVF, perform a **MET PMV** command while running the test conditions below.

Step 1.   Connect an injection set as shown in *Figure 3.4* to the PT V terminals.

Step 2.   Calculate the line-to-line voltage for the nominal line-to-neutral voltage of 63.5 V (63.5 • ($\sqrt{3}$) = 110). Next, calculate 105% and 107% of 110 V to determine the magnitude of VPMAXVF that will cause PSV01 and PSV02 to assert. Start off by injecting the voltage values shown in the Initial Voltage (105%) column in *Table 3.6*.

Step 3.   Slowly increase the A-Phase voltage until PB1_LED changes from green to amber. Record this voltage value in *Table 3.6*. Perform a **MET PMV** command and record the values of PMV01 and PMV02 in the table.

Step 4.   Turn off the injection set.

Step 5.   Clear the SER by typing **SER C <Enter>**. Enter **Y <Enter>** at the prompt: Are you sure (Y/N)?

Table 3.6   Voltage Values

Initial Voltage (105%)	Recorded Voltage	Initial Voltage (107%)	Recorded Voltage
VA = 68 ∠0°	VA = PMV01 = % PMV02 = V	VA = 71∠0°	VA = PMV01 = % PMV02 = V
VB = 63.5∠–120°	VB = 63.5∠–120°	VB = 63.5∠–120°	VB = 63.5∠–120°
VC = 63.5∠120°	VC = 63.5∠120°	VC = 63.5∠120°	VC = 63.5∠120°

Step 6.   Inject the relay with the recorded voltages for at least 22 seconds (verify that PB1_LED is amber, and PB2_LED is green).

Step 7.   Stop the injection and turn the test set off. Type **SER <Enter>** to see the element assert and operate times, as shown in *Figure 3.10*.

```
=>>SER <Enter>

Relay 1                                  Date: 06/03/2015  Time: 04:40:38.976
Station A                                Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#    DATE        TIME          ELEMENT           STATE
2    06/03/2015  04:40:36.8201  V/Hz picked up 105   Asserted
1    06/03/2015  04:40:56.7316  V/Hz timed out       Asserted

=>>
```

Figure 3.10   Element Assert and Operate Times (105%)

Because we are testing point (105,20), we expect the V/Hz element to assert after 20 seconds. Calculate the trip time as follows:

Trip time = 56.7316 – 36.8201 = 19.91 seconds.

This result is within the tolerance range of the V/Hz element.

Step 8.   With the test set connected, repeat *Step 1* through *Step 5*, noting the voltage when PB2_LED changes from green to amber in *Step 3* (PB1_LED also changes from green to amber).

Step 9.   Inject the relay with the recorded voltages for at least 18 seconds (verify that both PB1_LED and PB2_LED are amber).

Step 10. Stop the injection and turn the test set off. Type **SER <Enter>** to see the element assert and operate times, as shown in *Figure 3.11*.

```
=>>SER <Enter>

Relay 1                                  Date: 06/03/2015  Time: 12:01:00.135
Station A                                Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#    DATE        TIME          ELEMENT           STATE
3    06/03/2015  12:00:42.3249  V/Hz picked up 105   Asserted
2    06/03/2015  12:00:42.3334  V/Hz picked up 107   Asserted
1    06/03/2015  12:00:58.2694  V/Hz timed out       Asserted

=>>
```

Figure 3.11   Element Assert and Operate Times (107%)

Because we are testing point (107,16), we expect the V/Hz element to assert after 16 seconds. Calculate the trip time as follows:

Trip time = 12:00:58.2694 – 12:00:42.3334 = 15.936 seconds

This result is within the tolerance range of the V/Hz element. This concludes the V/Hz tests for this example; use similar tests to test more points on the curve.

Adaptive Inverse-Time Overcurrent

This example tests the Element 01 set to the C1 curve (see *Figure 3.12*), using the A-Phase current from Terminal S. Use the same procedure to test all inverse-time overcurrent elements for each winding.

IEC Class A Curve (Standard Inverse): C1
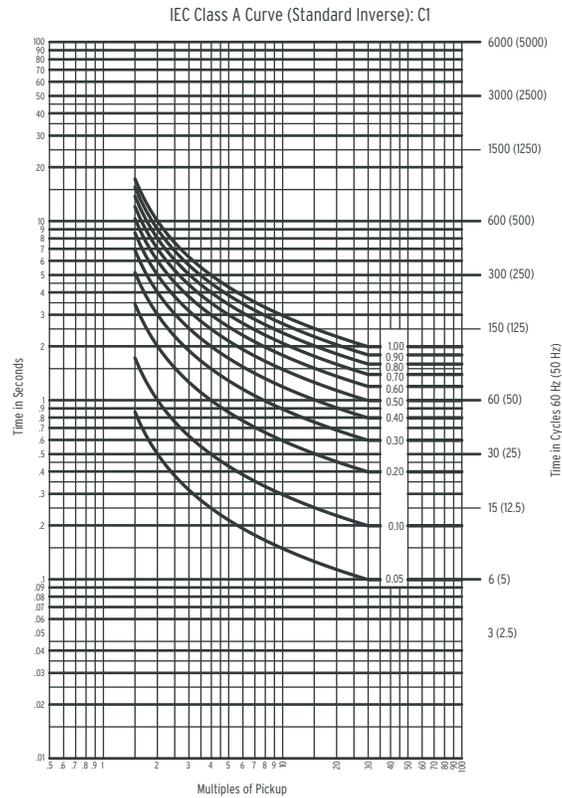
Figure 3.12   C1 Curve

For this test, you use remote bits to dynamically change the relay time dial setting. You also program the SER to record the status of the 51 element, and then use these recorded values to calculate the element operating time.

Be sure to enable each overcurrent element in two places: the ECTTERM and E51 settings. Enable the winding by including the particular winding in the ECTTERM setting, then select the number of 51 elements with the E51 setting.

Because the inverse-time overcurrent elements are adaptive, test three time-dial values, select arbitrary values of TD = 0.3 and TD = 0.6, and a third value of TD = 1.4. Setting TD = 1.4 exceeds the limit of the time dial range, causing the relay to clamp the time dial setting to the upper limit of the range. Use two remote bits (RB01 and RB02) to change the time setting from the default value of 0.3 to 0.6 and to 1.4.

Step 1.   Use *Equation 3.3* to determine the expected operate time of the overcurrent element. *Table 3.7* shows the pickup and time dial settings for the three tests.

$$T_p = TD \bullet \left[\frac{0.14}{M^{0.02} - 1} \right]$$

Equation 3.3

In all cases, inject a current of 10 A into the relay. With a pickup setting of 1.5 and current of 10 A, M = 6.667 (M = IMAXSF/51P01).

Table 3.7   Time Overcurrent Element Settings

Setting	Setting Category	Comment
E51 = 1	Group	Enable one 51 element
51P01 = 1.5	Group	Pickup (plug) setting
51TD01 = 0.3 + (RB01 • 0.3) + (RB02 • 0.8)	Group	Time-dial (multiplier) setting, resulting in trip times of 1.086, 2.172, and 3.620 seconds, respectively

> Step 2. Use the Group setting **SET** command to enable one 51 element, and apply the pickup and time dial settings as shown in *Table 3.7*. Save the settings, as shown in *Figure 3.13*.

```
=>>SET <Enter>
Group 1

Relay Configuration

Enable Current Terminals (OFF or combo of S,T,U,W,X)
ECTTERM := "S,T"  ? <Enter>
Enable Voltage Terminals (OFF or combo of V,Z)        EPTTERM := OFF    ? <Enter>
Enable Diff Elem. Prot. Terms (OFF or combo of S,T)
E87     := OFF    ?
Enable Restricted Earth Fault Element (N,1-3)         EREF    := N     ? <Enter>
Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50     := OFF    ?
Enable Inverse Time Overcurrent Elements (N, 1-10)  E51    := N     ?1 <Enter>
Enable Current Unb. Elements (OFF or combo of S,T)  E46    := OFF   ? <Enter>
Enable Bkr Fail. Prot. (OFF or combo of S,T)        EBFL   := OFF   ? <Enter>
Enable Demand Metering (N, 1-10)                    EDEM   := N     ? <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)           CTRS   := 100   ?> <Enter>

Inverse Time Overcurrent Element 01

Inv.Time O/C 1 Operate Quantity                     51O01   := IMAXSF ? <Enter>
Inv.Time O/C 1 Pickup Value (SEL Math Eqn.)
51P01 := 1.000000
?  1.5 <Enter>
Inv.Time O/C 1 Curve Selection (U1-U5, C1-C5)       51C01   := U1     ?C1 <Enter>
Inv.Time O/C 1 Time Dial (SEL Math Eqn)
51TD01 := 1.000000
?  0.3+(RB01*0.3)+(RB02*0.8) <Enter>
Inv.Time O/C 1 EM Reset (Y, N)                      51RS01  := N      ?
Inv.Time O/C 1 Torque control (SELogic Eqn)
51TC01 := 1
? <Enter>

Trip Logic

Trip Transformer (SELogic Eqn)
TRXFMR := 87R OR REFF1
?  END <Enter>
Group 1

.
.
.

CFD      := 4.00
Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait...........
Settings Saved

=>>
```

Figure 3.13   Group Settings for the 51 Tests

> Step 3. Set the SER to check the operate time of the element, as shown in *Figure 3.14*. When using the TERSE option (**SET TE**), there is no read back, so that the setting change is much faster.

```
=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)      ESERDEL := N      ? <Enter>

SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
?  51SO1 "51 Asserted"<Enter>
2:
?  51TO1 "51 Timed out"<Enter>
3:
?  END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait...........
Settings Saved

=>>
```

Figure 3.14   Setting the SER

Step 4. Use the **SER C** command to clear the SER before starting the test, as shown in *Figure 3.15*.

```
=>>SER C <Enter>

Clear the sequential events recorder for this port.
Are you sure (Y/N)?Y <Enter>

SER records for this port are cleared
```

Figure 3.15   Clearing the SER

Step 5. Inject 10 A into the relay for at least two seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.16*. Use the bold SER entries to calculate the operating time: 39.4516 – 38.3598 = 1.092 seconds. This value compares favorably with the expected value of 1.086 seconds.

```
=>>SER <Enter>

Relay 1                                 Date: 01/07/2015  Time: 04:52:44.740
Station A                               Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#    DATE        TIME          ELEMENT            STATE
4    01/07/2015  04:52:38.3598  51 ASSERTED       Asserted
3    01/07/2015  04:52:39.4516  51 TIMED OUT      Asserted
2    01/07/2015  04:52:41.7520  51 TIMED OUT      Deasserted
1    01/07/2015  04:52:41.7520  51 ASSERTED       Deasserted

=>>
```

Figure 3.16   SER Results

Step 6. To dynamically change the time dial (time multiplier) setting from 0.3 to 0.6, assert RB01. *Figure 3.17* shows how to assert RB01 by means of the **CON** (control) command.

```
=>>CON 01 S <Enter>
Remote Bit Operated
```

Figure 3.17   RBO1 Asserted

Step 7. Inject 10 A into the relay for at least three seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.18*. Use the bold SER entries to calculate the operating time: 35.0417 – 32.8581 = 2.184 seconds. This value compares favorably with the expected value of 2.172 seconds.

```
=>>SER <Enter>

Relay 1                                  Date: 01/07/2015 Time: 04:56:30.007
Station A                                Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#     DATE        TIME          ELEMENT           STATE
8     01/07/2015  04:52:38.3598  51 ASSERTED      Asserted
7     01/07/2015  04:52:39.4516  51 TIMED OUT     Asserted
6     01/07/2015  04:52:41.7520  51 TIMED OUT     Deasserted
5     01/07/2015  04:52:41.7520  51 ASSERTED      Deasserted
4     01/07/2015  04:55:32.8581  51 ASSERTED      Asserted
3     01/07/2015  04:55:35.0417  51 TIMED OUT     Asserted
2     01/07/2015  04:55:37.3755  51 TIMED OUT     Deasserted
1     01/07/2015  04:55:37.3755  51 ASSERTED      Deasserted

=>>
```

Figure 3.18   Test 2 SER Results

Step 8. To dynamically change the time-dial (time multiplier) settings from 0.6 to 1.4, assert RB02, as shown in *Figure 3.19*.

```
=>>CON O2 S <Enter>
Remote Bit Operated
```

Figure 3.19   RB02 Asserted

Step 9. Inject 10 A into the relay for at least five seconds, then stop the injection and turn the injection set off. Issue the **SER** command to see the results of the test, as shown in *Figure 3.20*. Use the bold SER entries to calculate the operating time: 6.8780 – 3.2357 = 3.642 seconds. This value compares favorably with the expected value of 3.62 seconds.

```
=>>SER <Enter>

Relay 1                                  Date: 01/07/2015 Time: 04:58:20.106
Station A                                Serial Number: 1151000001

FID=SEL-487E-3-R310-V0-Z104101-D20140515

#     DATE        TIME          ELEMENT           STATE
12    01/07/2015  04:52:38.3598  51 ASSERTED      Asserted
11    01/07/2015  04:52:39.4516  51 TIMED OUT     Asserted
10    01/07/2015  04:52:41.7520  51 TIMED OUT     Deasserted
9     01/07/2015  04:52:41.7520  51 ASSERTED      Deasserted
8     01/07/2015  04:55:32.8581  51 ASSERTED      Asserted
7     01/07/2015  04:55:35.0417  51 TIMED OUT     Asserted
6     01/07/2015  04:55:37.3755  51 TIMED OUT     Deasserted
5     01/07/2015  04:55:37.3755  51 ASSERTED      Deasserted
4     01/07/2015  04:58:03.2357  51 ASSERTED      Asserted
3     01/07/2015  04:58:06.8780  51 TIMED OUT     Asserted
2     01/07/2015  04:58:09.1242  51 TIMED OUT     Deasserted
1     01/07/2015  04:58:09.1242  51 ASSERTED      Deasserted

=>>
```

Figure 3.20   Test 3 SER Results

Restricted Earth Fault (REF) Test

The REF is a directional element, comparing the angle between the neutral current and the residual current from one or more windings. *Figure 3.21(a)* shows the element characteristic, an internal fault being the shaded area.

(a) REF Characteristic   (b) REF Test Setup
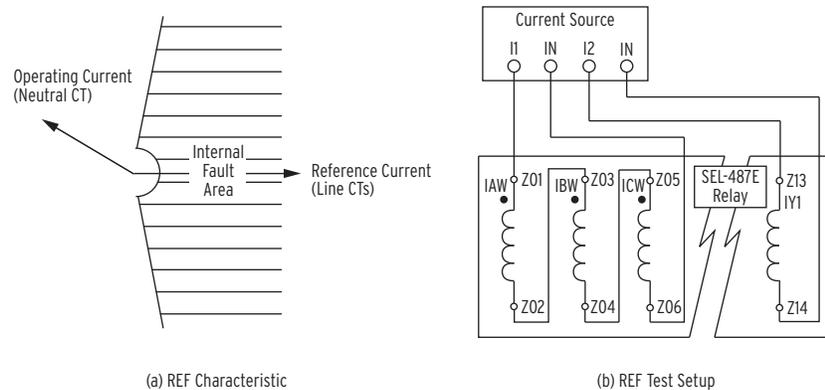
Figure 3.21   REF Characteristic and Test Setup

Figure 3.21(b) shows the test setup for the REF test. For this example, we test one REF element, configured between the W-Terminal currents and the IY1 neutral current.

Step 1.   Apply the following settings.

> SET
>
> ECTTERM = W
>
> EREF = 1
>
> REFRF1 = W
>
> REF50G1 = 0.05
>
> TCREF1 = 1
>
> CTRW = 100
>
> CTRY1 = 50
>
> CTCONW = Y

Step 2.   Wire the relay as shown in *Figure 3.21*, i.e., connect the three elements of the W-Terminal in series, and connect to a current source. Connect the Y-Terminal to a separate phase of the current source (or a different current source).

Inject the following signals:

> $I1 = 1.0 \angle 0°$
>
> $I2 = 1.5 \angle 180°$

Because the two currents are opposite in phase, the element should not operate. To verify this, enter the **TAR REFF1** command. Both Relay Word bits REFF1 and REFR1 are in this row. With the currents applied as above, the element should calculate a reverse fault, asserting Relay Word bit REFR1.

Change the angle of I2 to any value within ±75 degrees of I1 ($I2 = 1.5 \angle 60°$, for example) to move the fault to within the internal fault area, causing the REF element to operate. To verify this, again enter the **TAR REFF1** command. This time, Relay Word bit REFF1 (forward fault) must be asserted and Relay Word bit REFR1 deasserted.

U87P Unrestrained Phase-Differential Element

In this test, you test the filtered unrestrained differential element operation by injecting current in Winding S. *Table 3.8* shows the setting for this test.

Table 3.8   Unrestrained Phase-Differential Element Settings

Setting	Setting Category	Comment
E87U = F	Group	Enable unrestrained differential element
E87 = S, T	Group	Enable Windings S and T in the differential calculations
CTRS = 100	Group	Winding S CT ratio (default setting)
CTRT = 100	Group	Winding T CT ratio (default setting)
E87TS = 1	Group	Include Terminal S in the Differential Element (default setting)
E87TT = 1	Group	Include Terminal T in the Differential Element (default setting)
MVA = 100	Group	Transformer MVA rating
VTERMS = 275	Group	Winding S rated voltage (default setting)
VTERMT = 132	Group	Winding T rated voltage
U87P = 4	Group	Unrestrained Element Current pickup

Figure 3.22 shows the setting change in the Group category, using the **TE**(ERSE) option.

```
=>>SET U87P TE <Enter>
Group 1

Differential Element Configuration and Data

Unrestrained Element Current PU (1.00-20)        U87P    := 8.00   ?4 <Enter>
Incr. Operate Current Threshold p.u. (0.10-10)   DIOPR   := 1.20   ?END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait...........
Settings Saved

=>>
```

Figure 3.22   Group Settings

Use the **TAR 87U 999** (the 999 repeats the display 999 times on the screen) command to view the line in the relay that shows the status of the elements, as shown below.

```
=>>TAR 87U 999 <Enter>

87UA      87UB      87UC      87U       87T_SF    87T_SFA   87T_SFB   87T_SFC
0         0         0         0         0         0         0         0
0         0         0         0         0         0         0         0
0         0         0         0         0         0         0         0
0         0         0         0         0         0         0         0
```

Step 1.   Calculate the required current to pick up the unrestrained differential element (setting 4 per unit).

$$IAS = 4 \bullet TAPS$$

Equation 3.4

$$IAS = 4 \bullet 2.1 \, pu$$

Equation 3.5

$$IAS = 8.4A$$

Equation 3.6

Step 2. Start by injecting 7 A three-phase current, and enter **TAR 87U 999**. Slowly increase the current until the unrestrained differential elements assert, as shown below.

87UA	87UB	87UC	87U	87T_SF	87T_SFA	87T_SFB	87T_SFC
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

87RA, 87RB, and 87RC Restrained Differential Elements

This section provides tests to show the operation of the restraint differential element under the following system conditions (for ease of testing consider only two windings [Winding S and Winding T]):

➤ Internal fault

➤ External fault with heavy CT saturation

➤ Evolving fault, causing the relay to trip on Slope 2

In general, the relay uses *Equation 3.7* and *Equation 3.8* to calculate the operational operating current (IOP$_{OP}$) and the restraint current (IRT).

$$IOP_{OP} = \left| \overrightarrow{IAS} + \overrightarrow{IAT} \right|$$

Equation 3.7

$$IRT = |IAS| + |IAT|$$

Equation 3.8

Equation 3.7 calculates the absolute value of the vector sum of $\overrightarrow{IAS}$ and $\overrightarrow{IAT}$, and *Equation 3.8* calculates the sum of the absolute values of $\overrightarrow{IAS}$ and $\overrightarrow{IAT}$.

Equation 3.9 is the third equation that the differential element uses to make a trip/no trip decision.

$$IOP(IRT) = \frac{SLP}{100} \bullet IRT$$

Equation 3.9

Equation 3.9 provides the reference value (from the slope setting) for various restraint values, as shown in *Figure 3.23*.
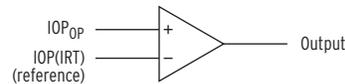
Figure 3.23   Differential Element Comparator

Each processing interval, the relay calculates IRT (*Equation 3.8*), uses this calculated IRT value to calculate IOP(IRT) (*Equation 3.9*), and compares this calculated IOP(IRT) value with the result of *Equation 3.7* (IOP$_{OP}$).

Figure 3.24 shows the characteristic of the differential element, together with IOP_{OP}. In *Figure 3.24*, the shaded area (area below the SLP line) is the non-oper-ating or restraint area, and the area above the SLP line is the operating or tripping area.
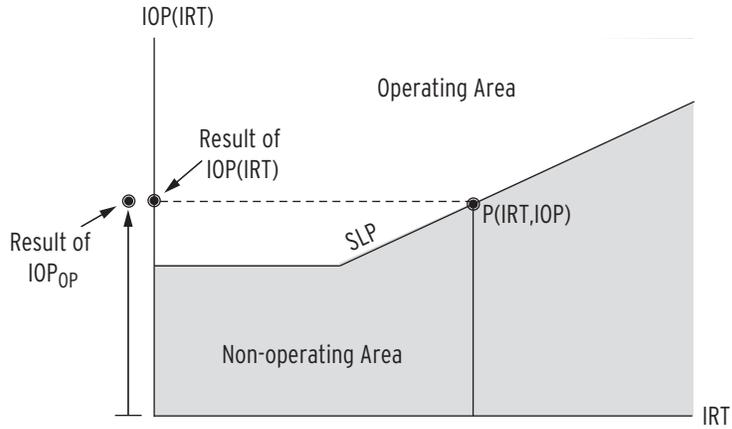
Figure 3.24   Differential Element Characteristic

To simplify *Equation 3.7*, consider a fixed angular relationship of 180 degrees between $\overline{IAS}$ and $\overline{IAT}$, i.e., $\overline{IAS} = IAS\angle 0°$ and $\overline{IAT} = IAT\angle 180°$. With this rela-tionship, both IAS and IAT are real numbers, and *Equation 3.7* becomes:

$$IOP_{OP} = IAS - IAT$$

Equation 3.10

or

$$IAS = IOP_{OP} + IAT$$

Equation 3.11

Also, from *Equation 3.8*,

$$IAS = IRT - IAT$$

Equation 3.12

Combine *Equation 3.11* and *Equation 3.12* to solve for IAT as follows:

$$IAT = \frac{IRT - IOP_{OP}}{2}$$

Equation 3.13

With this value, use *Equation 3.12* to calculate IAS as follows:

$$IAS = \frac{IRT + IOP_{OP}}{2}$$

Equation 3.14

Testing

Connect a three-phase test set to the SEL-487E as shown in *Figure 3.3*. Change the following settings, as shown in *Table 3.9* and *Figure 3.25*.

Table 3.9   Differential Element Settings

Setting	Setting Category	Comment
VTERMT = 132	Group	Rated line-to-line voltage for Winding S
E87 = S,T	Group	Include Windings S and T for the differential element
E87TS = 1	Group	Winding S is permanently included in the differential element
E87TT = 1	Group	Winding T is permanently included in the differential element
O87P = 0.3	Group	Restraint differential element pickup
SLP1 = 30	Group	Set Slope 1 to 30 percent
SLP2 = 60	Group	Set Slope 2 to 60 percent
MVA = 100	Group	Transformer maximum capacity

```
=>>SET TE <Enter>
Group 1

Relay Configuration

Enable Current Terminals (OFF or combo of S,T,U,W,X)
ECTTERM := "S,T"  ? <Enter>
Enable Voltage Terminals (OFF or combo of V,Z)       EPTTERM := OFF    ? <Enter>
Enable Diff Elem. Prot. Terms (OFF or combo of S,T)
E87     := OFF    ?S, T <Enter>
Enable Restricted Earth Fault Element (N,1-3)        EREF    := N      ? <Enter>
Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50     := OFF    ? <Enter>
Enable Inverse Time Overcurrent Elements (N, 1-10)   E51     := N      ? <Enter>
Enable Current Unb. Elements (OFF or combo of S,T)   E46     := OFF    ? <Enter>
Enable Bkr Fail. Prot. (OFF or combo of S,T)         EBFL    := OFF    ? <Enter>
Enable Demand Metering (N, 1-10)                     EDEM    := N      ? <Enter>


Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)            CTRS    := 100    ? <Enter>
Current Trans. Connection Terminal S (Y,D)           CTCONS  := Y      ? <Enter>
Current Trans. Ratio Terminal T (1-50000)            CTRT    := 100    ? <Enter>
Current Trans. Connection Terminal T (Y,D)           CTCONT  := Y      ? <Enter>


Differential Element Configuration and Data

Term S included in 87 Element (SELOGIC Eqn)
E87TS := 0
?  1 <Enter>
Term T included in 87 Element (SELOGIC Eqn)
E87TT := 0
?  1 <Enter>
Internal CT Conn. Compensation Enabled (Y,N)         ICOM    := Y      ? <Enter>
Terminal S CT Conn. Compensation (0 - 12)            TSCTC   := 12     ? <Enter>
Terminal T CT Conn. Compensation (0 - 12)            TTCTC   := 12     ? <Enter>
Transformer Max. Power Capacity (OFF, 1 - 5000MVA)   MVA     := OFF    ?100 <Enter>
Terminal S Line-to-Line Voltage  (1.00-1000 kV)      VTERMS  := 275.00 ? <Enter>
Terminal T Line-to-Line Voltage  (1.00-1000 kV)      VTERMT  := 275.00 ?132 <Enter>
Terminal S Current Tap  (0.50-175 A,sec)             TAPS    := 2.10   ? <Enter>
Terminal T Current Tap  (0.50-175 A,sec)             TAPT    := 4.37   ? <Enter>
Differential Element Oper. Current PU (0.10-4)       O87P    := 1.00   ?0.3 <Enter>
Slope 1 Percentage (5.00-100%)                       SLP1    := 35.00  ?30 <Enter>
Slope 2 Percentage (5.00-100%)                       SLP2    := 75.00  ?60 <Enter>
Unrestrained Element Current PU (1.00-20)            U87P    := 8.00   ? <Enter>
Incr. Operate Current Threshold p.u. (0.10-10)       DIOPR   := 1.20   ? <Enter>
Incr. Restraint Current Threshold p.u. (0.10-10)     DIRTR   := 1.20   ? <Enter>
Enable Harmonic Blocking Diff. Element (Y,N)         E87HB   := N      ? <Enter>
Enable Harmonic Restraint Diff. Element (Y,N)        E87HR   := Y      ? <Enter>
Second-Harmonic Percentage (OFF, 5-100%)             PCT2    := 15     ? <Enter>
Fourth-Harmonic Percentage (OFF, 5-100%)             PCT4    := 15     ? <Enter>
Fifth-Harmonic Percentage (OFF, 5-100%)              PCT5    := 35     ? <Enter>
Fifth-Harmonic Alarm Threshold p.u. (OFF, 0.2-3.2)   TH5P    := OFF    ? <Enter>
Enable Wave-Shape Blocking Diff. Element (Y,N)       E87T_WS := N      ? <Enter>
Neg. Seq. Differential Op current (0.05-1)           87QP    := 0.30   ? <Enter>
Neg. Seq. Differential Slope (5 - 100%)              SLPQ1   := 25     ?END <Enter>


Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait..........
Settings Saved

=>>
```

Figure 3.25   Group Settings for the Differential Test

Step 1.   With arbitrary values IRT = 3 per unit, SLP1 = 30, and
SLP2 = 60 percent, use *Equation 3.9* to calculate IOP(IRT) values
for Slope 1 and Slope 2:

$$IOP(IRT) = \frac{30}{100} \bullet 3 = 0.9\,pu \text{ (Slope 1)}$$

Equation 3.15

$$IOP(IRT) = \frac{60}{100} \bullet 3 = 1.8\,pu \text{ (Slope 2)}$$

Equation 3.16

Case 1: Internal Fault

Select an IOP_{OP} value greater than 1.8 to ensure that the relay will operate, such as 3 per unit. *Figure 3.26* shows the selected point P(3,3), which is well within the tripping area (shaded area).
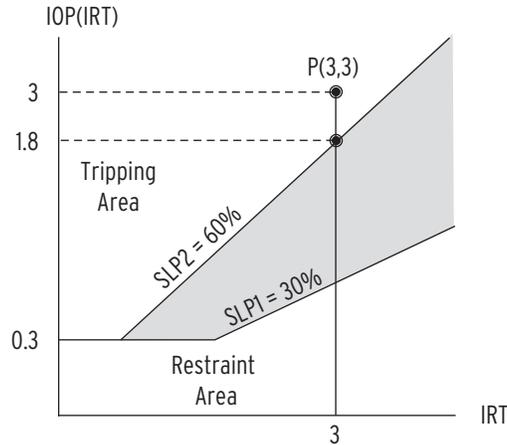
Figure 3.26   Values for Case 1

For this test, you need to inject current into Winding S only, i.e., InT (n = A, B, C) = 0, and InS = 3 per unit. Convert per-unit values (pu) to ampere values, by multiplying the per-unit values with the TAPS value (2.1), as shown in *Table 3.10*.

Table 3.10   Calculate the Current Values in Amperes (Case 1)

Current (per unit)	Current (Amperes)
IAS = 3∠0°pu • 2.1	IAS = 6.3∠0°A
IBS = 3∠–120°pu • 2.1	IBS = 6.3∠–120°A
ICS = 3∠120°pu • 2.1	ICS = 6.3∠120°A

Step 1.   Inject balanced 6.3 A into Winding S for 100 ms, then stop.

Step 2.   Verify that LEDs 3, 4, and 5 are illuminated.

Step 3.   Press the **TARGET RESET** button to reset the LEDs.

Case 2: External Fault With Heavy CT Saturation

This test simulates an external fault that eventually results in extreme CT saturation that would have caused the relay to trip if the relay were still operating on Slope 1. However, because the relay switched to Slope 2, the relay does not operate for this fault for less than one second. This test will be run in two stages, the first stage simulating an external fault without CT saturation and the second stage introducing heavy CT saturation.

Step 1. For Stage 1, select a large IRT value that will simulate an external fault without CT saturation (IOP_{OP} is zero); a good value for IRT is 3 pu. *Figure 3.27* shows the selected point P1(3,0).
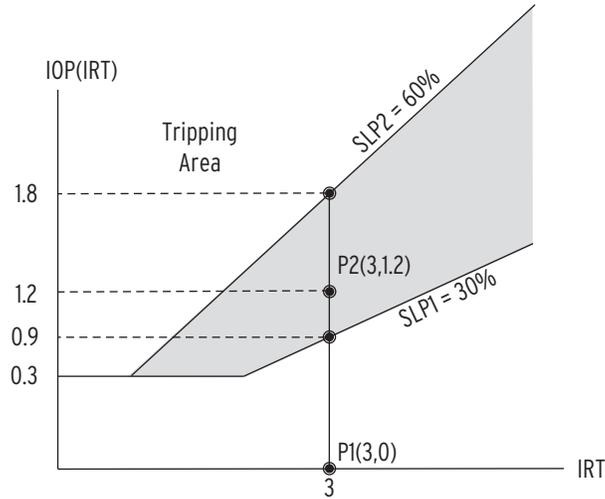
Figure 3.27   Values for Case 2

Step 2. Calculate IAS and IAT for the point P1(3,0):

$$\text{IAS} = \frac{\text{IRT} + \text{IOP}_{\text{OP}}}{2} = \frac{3+0}{2} = 1.5$$

Equation 3.17

$$\text{IAT} = \frac{\text{IRT} - \text{IOP}_{\text{OP}}}{2} = \frac{3-0}{2} = 1.5$$

Equation 3.18

Convert per-unit values (pu) to ampere values by multiplying the per-unit values with the TAP values, as shown in *Table 3.11*.

Table 3.11   Calculate the Current Values in Amperes (Case 2, Stage 1)

Current (per unit)	Current (Amperes)
IAS = 1.5∠0°pu • 2.1	IAS = 3.15∠0°A
IBS = 1.5∠–120°pu • 2.1	IBS = 3.15∠–120°A
ICS = 1.5∠120°pu • 2.1	ICS = 3.15∠120°A
IAT = 1.5∠180°pu • 4.37	IAT = 6.56∠180°A
IBT = 1.5∠60°pu • 4.37	IBT = 6.56∠60°A
ICT = 1.5∠–60°pu • 4.37	ICT = 6.56∠–60°A

Step 3. For Stage 2, select an IOP_{OP} value between 0.9 pu and 1.8 pu that will simulate CT saturation. Accounting for the group settings of the relay, a good choice for IOP_{OP} would be 1.2 pu. *Figure 3.27* shows the selected point P2(3,1.2) and the area between the two slopes (shaded area).

Step 4. Calculate IAS and IAT for the point P2(3,1.2):

$$IAS = \frac{IRT + IOP_{OP}}{2} = \frac{3 + 1.2}{2} = 2.1$$

<div align="right">**Equation 3.19**</div>

$$IAT = \frac{IRT - IOP_{OP}}{2} = \frac{3 - 1.2}{2} = 0.9$$

<div align="right">**Equation 3.20**</div>

As before, convert the pu values to ampere values by multiplying by the appropriate TAP values, as shown in *Table 3.12*.

Table 3.12   Calculate the Current Values in Amperes (Case 2, Stage 2)

Current (per unit)	Current (Amperes)
IAS = 2.1∠0°pu • 2.1	IAS = 4.41∠0°A
IBS = 2.1∠–120°pu • 2.1	IBS = 4.41∠–120°A
ICS = 2.1∠120°pu • 2.1	ICS = 4.41∠120°A
IAT = 0.9∠180°pu • 4.37	IAT = 3.93∠180°A
IBT = 0.9∠60°pu • 4.37	IBT = 3.93∠60°A
ICT = 0.9∠–60°pu • 4.37	ICT = 3.93∠–60°A

Step 5. Inject the currents for Stage 1 shown in *Table 3.11* into Winding S and Winding T for 1.8 cycles, and then inject the currents for Stage 2 shown in *Table 3.12* into Winding S and Winding T for 800 ms.

Step 6. Verify that LEDs 3, 4, and 5 are NOT illuminated, i.e., the relay did not trip.

Case 3: Evolving Fault, Causing the Relay to Trip on Slope 2

This test is for a fault that starts out as an external fault (causing the relay to switch to Slope 2), but then evolves into an in-zone fault. The worst case for this fault is when there is only one source, i.e., when the fault moves to an internal fault, the side where the external fault was, does not contribute any fault current.

This test is in two stages: Stage 1 for the external fault (no saturation) and Stage 2 for the evolved fault.

Table 3.13   Current Values in Amperes (Case 3)

Current (Amperes) Stage 1	Current (Amperes) Stage 2
IAS = 4.2∠0°A	IAS = 4.2∠0°A
IBS = 4.2∠–120°A	IBS = 4.2∠–120°A
ICS = 4.2∠120°A	ICS = 4.2∠120°A
IAT = 8.74∠180°A	IAT = 0
IBT = 8.74∠60°A	IBT = 0
ICT = 8.74∠–60°A	ICT = 0

Step 1. Enable an overcurrent element for Winding T, and set the pickup value to 0.5 A, as shown in *Figure 3.28*.

```
=>>SET E50 TE <Enter>
Group 1

Relay Configuration

Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50    := OFF    ?T <Enter>
Enable Inverse Time Overcurrent Elements (N, 1-10)   E51    := N     ?1 <Enter>
Enable Current Unb. Elements (OFF or combo of S,T)   E46    := OFF   ?> <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)        CTRS   := 100   ? <Enter>
Current Trans. Connection Terminal S (Y,D)       CTCONS := Y     ? <Enter>
Current Trans. Ratio Terminal T (1-50000)        CTRT   := 100   ? <Enter>
Current Trans. Connection Terminal T (Y,D)       CTCONT := Y     ? <Enter>

Winding T
Overcurrent Elements Terminal T

Type of O/C Elements Enabled Term. T (Combo of P,Q,G)
E50T   := "P"   ? <Enter>
Enable Directional elements Terminal T (Y,N)      E67T   := N     ? <Enter>

Terminal T Phase Overcurrent Element Level 1

Phase Inst O/C pickup Level 1 (OFF,0.25-100)      50TP1P := OFF   ?0.5 <Enter>
Phase Inst O/C Level 1 Torque Ctrl (SELogic Eqn)
67TP1TC := TF32P
?  END <Enter>


Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait..........
Settings Saved

=>>
```

Figure 3.28   Enable Overcurrent Element for Winding T

Step 2. Enter the setting in *Figure 3.29* to include the overcurrent element in the SER.

```
=>>SET R TE <Enter>
Report

SER Chatter Criteria

Automatic Removal of Chattering SER Points (Y,N)     ESERDEL := N      ?

SER Points
(Relay Word Bit, Reporting Name, Set State Name, Clear State Name, HMI Alarm)

1:
?  50TP1 <Enter>
2:
?  TRPXFMR <Enter>
3:
?  END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait..........
Settings Saved

=>>
```

Figure 3.29   Enter Overcurrent Element in the SER

Step 3. Inject the current shown in the Stage 1 column of *Table 3.13* into Winding S and Winding T for 200 ms, then inject the Stage 2 currents for 200 ms.

Step 4. Issue the **SER** command and calculate the time difference between the deassertion of 50TP1 and the assertion of TRPXFMR. This must be less than two cycles.

Negative-Sequence Differential Element

Use the settings shown in *Table 3.14* for the negative-sequence differential element test.

Table 3.14   Settings for the Negative-Sequence Test

Settings	Setting Group	Comment
E87Q = Y	Group	Enable negative-sequence differential element
MVA = 100	Group	Transformer rating
VTERMS = 275	Group	HV rated voltage
VTERMT = 132	Group	LV rated voltage
E87 = S, T	Group	Enable Windings S and T in the differential element
E87TS = 1	Group	
E87TT = 1	Group	

Be sure that the compensation settings (TSCTC = TTCTC = 0) and the negative-sequence elements (87QP = 0.3, SLPQ1 = 25) are at default settings.

Step 1.   Inject the currents shown in *Table 3.15* in the relay.

Table 3.15   Currents for Negative-Sequence Differential Test

Winding S	Winding T
IAS = 0.55 A	IAT = 0
IBS = 0	IBT = 0
ICS = 0	ICT = 0

Step 2.   Issue the **TAR 87Q 9999** command as shown below.

```
=>>TAR 87Q 9999 <Enter>

87Q      87PQ      *        *        *        *        *        *
0        0         0        0        0        0        0        0
0        0         0        0        0        0        0        0
0        0         0        0        0        0        0        0
0        0         0        0        0        0        0        0
0        0         0        0        0        0        0        0
0        0         0        0        0        0        0        0
```

Step 3.   Slowly increase IAS current in 10 mA steps. 87Q asserts (87Q = 1) when IAS is approximately 0.63 A.

At threshold:

$$3I2S = IAS = 87QP \cdot TAPS$$
$$= 0.3 \cdot 2.1$$
$$= 0.63$$

Negative-Sequence Directional Element for Phase Faults

Use the phase directional element (represented by Relay Word bits kF32P/kR32P, k = S, T, U, W, X) to convert non-directional phase overcurrent elements to directional phase overcurrent elements. The negative-sequence directional element, kF32Q/kR32Q, is a part of the phase directional element, and provides directional

control for all shunt faults except for bolted, three-phase faults. Because the negative-sequence element is part of the phase element, the phase directional element asserts whenever the negative-sequence directional element asserts.

The SEL-487E calculates the negative-sequence impedance Z2 from the magnitudes and angles of the negative-sequence voltage and current. *Equation 3.21* defines this function (the "c" in Z2c indicates "calculated").

$$Z2c = \frac{Re[V_2 \bullet (1\angle Z1ANG \bullet I_2)^*]}{|I_2|^2}$$

$$= \frac{|V_2|}{|I_2|} \bullet \cos(\angle V_2 - \angle Z1ANG - \angle I_2)$$

Equation 3.21

where:

V_2 = the negative-sequence voltage

I_2 = the negative-sequence current

$Z1ANG$ = the positive-sequence line impedance angle

Re = the real part of the term in brackets, for example,
$(Re[A + jB] = A)$

$*$ = the complex conjugate of the expression in parentheses,
$(A + jB)^* = (A - jB)$

The result of *Equation 3.21* is an impedance magnitude that varies with the magnitude and angle of the applied current. Normally, a forward fault results in a negative Z2c relay calculation.

Test Current

Solve *Equation 3.22* to find the test current values that you need to apply to the relay to test the element. For the negative-sequence current I_2, the result is

$$|I_2| = \frac{|V_2|}{Z2c}$$

Equation 3.22

when:

$$\angle I_2 = \angle V_2 - \angle Z1ANG$$

Equation 3.23

Multiply the quantities in *Equation 3.22* by three to obtain $3I_2$, the negative-sequence current that the relay processes. With a fixed applied negative-sequence voltage VA, the relay negative-sequence voltage is 3V2. Set Z2c = Z2FT to find the test current magnitude at the point where the impedance calculation equals the forward fault impedance threshold as follows:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2c} = \frac{|3V_2|}{Z2FT}$$

Equation 3.24

when:

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG$$

<div align="right">**Equation 3.25**</div>

Use *Equation 3.26* for a reverse fault impedance threshold, where Z2c = Z2R:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2c} = \frac{|3V_2|}{Z2R}$$

<div align="right">**Equation 3.26**</div>

when the angle calculation is the same as *Equation 3.25*.

Checking the Negative-Sequence Directional Element (Phase Faults Clear of Ground)

NOTE: As you perform this test, other protection elements can assert. This causes the relay to assert other targets and possibly close control outputs. Be sure to isolate the relay from the power system to avoid unexpected system effects.

This test confirms operation of the TF32Q and the TR32Q negative-sequence directional element for Terminal T, using a 5 A relay; scale values appropriately for a 1 A relay. This example assumes that you have successfully established communication with the relay, and that you are familiar with relay access levels and passwords. *Table 3.16* shows the settings necessary for the test.

Table 3.16   Settings to Test the Negative-Sequence Directional Element for Terminal T

Settings	Description	Category
EPTTERM = V	Enables the PT inputs (V or Z)	Group
E50 = T	Enables the directional element for Terminal T	Group
VREFT = V	Declares which PT to use (V or Z)	Group
E50T = Q	Specifies which overcurrent elements to enable for Terminal T (P, Q, G)	Group
E67T = Y	Enables the directional logic for Terminal T	Group
Z1ANGT = 84 degrees	Positive-sequence line impedance angle	Group
EADVST = Y	Enable advanced settings Terminal T	Group
50FPT = 0.6 A	Forward directional overcurrent pickup	Group
50RPT = 0.4 A	Reverse directional overcurrent pickup	Group
Z2FT = 3.9 Ω	Forward directional Z2 Threshold	Group
Z2RT = 4.4 Ω	Reverse directional Z2 Threshold	Group
A2T = 0.10	Positive-sequence Restraint Factor	Group

Step 1.   Configure the relay.

Set the Group settings for Terminal T (see *Figure 3.30*).

```
=>>SET <Enter>
Group 1

Relay Configuration

Enable Current Terminals (OFF or combo of S,T,U,W,X)
ECTTERM := "S,T"   ? <Enter>
Enable Voltage Terminals (OFF or combo of V,Z)      EPTTERM := OFF    ?V <Enter>
Enable Diff Elem. Prot. Terms (OFF or combo of S,T)
E87     := OFF    ? <Enter>
Enable Restricted Earth Fault Element (N,1-3)       EREF    := N      ? <Enter>
Enable Def. Time Dir. O/C Ele. (OFF or combo of S,T)
E50     := OFF    ?T <Enter>
Enable Inverse Time Overcurrent Elements (N, 1-10)  E51     := N      ? <Enter>
Enable Current Unb. Elements (OFF or combo of S,T)  E46     := OFF    ? <Enter>
Enable Over Voltage Elements (N,1-5)                E59     := N      ? <Enter>
Enable Under Voltage Elements (N,1-5)               E27     := N      ? <Enter>
Enable Frequency Elements (N,1-6)                   E81     := N      ? <Enter>
Enable Volts per Hertz Element (Y,N)                E24     := N      ? <Enter>
Enable Bkr Fail. Prot. (OFF or combo of S,T)        EBFL    := OFF    ? <Enter>
Enable Power Calc. Term (OFF or combo of S,T)       EPCAL   := OFF    ? <Enter>
Enable Demand Metering (N, 1-10)                    EDEM    := N      ? <Enter>

Current Transformer Data

Current Trans. Ratio Terminal S (1-50000)           CTRS    := 100    ? <Enter>
Current Trans. Connection Terminal S (Y,D)          CTCONS  := Y      ? <Enter>
Current Trans. Ratio Terminal T (1-50000)           CTRT    := 100    ? <Enter>
Current Trans. Connection Terminal T (Y,D)          CTCONT  := Y      ? <Enter>

Potential Transformer Data

Potential Trans. Ratio Terminal V (1.0-10000.0)     PTRV    := 2000.0 ? <Enter>
Potential Trans. Connection Terminal V (Y,D)        PTCONV  := Y      ? <Enter>
PT Comp. Angle Terminal V (-179.99 to +180 deg)     PTCOMPV := 0.00   ? <Enter>
PT Nominal Voltage (L-L) Term. V (30-300 V,sec)     VNOMV   := 110    ? <Enter>

Voltage Reference Terminal Selection

Voltage Reference For Terminal S (OFF,V)            VREFS   := OFF    ? <Enter>
Voltage Reference For Terminal T (OFF,V)            VREFT   := OFF    ?V <Enter>

Winding T
Overcurrent Elements Terminal T

Type of O/C Elements Enabled Term. T (Combo of P,Q,G)
E50T    := "P"    ?
Enable Directional elements Terminal T (Y,N)        E67T    := N      ?Y <Enter>
Current Transformer Polarity Terminal T (P,N)       CTPT    := P      ? <Enter>
Pos.-Seq. Line Impedance Angle (5.00-90 deg)        Z1ANGT  := 89.00  ?84 <Enter>
Enable Advanced Setting Terminal T (Y,N)            EADVST  := N      ?Y <Enter>
Forward Dir. O/C Pickup (0.25-5 A,sec)              50FPT   := 0.25   ?0.6 <Enter>
Reverse Dir. O/C Pickup (0.25-5 A,sec)              50RPT   := 0.25   ?0.4 <Enter>
Fwd Dir Z2 Threshold (-64.00-64 ohms,sec)           Z2FT    := -0.10  ?3.9 <Enter>
Rev Dir Z2 Threshold (-64.00-64 ohms,sec)           Z2RT    := 0.10   ?4.4 <Enter>
Pos.-Seq. Restraint Factor, I2/I1 (0.02-0.50)       A2T     := 0.10   ?

Terminal T Phase Overcurrent Element Level 1

Phase Inst O/C pickup level 1 (OFF,0.25-100)        50TP1P  := 0.50   ?END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait..........
Settings Saved

=>>
```

Figure 3.30   Group Settings for the Directional Test

Step 2.   Set test values in the relay.

Step 3.   Set the front-panel LED to show the directional element word bits, as in *Figure 3.31*. With these settings, the LEDs are green when TF32Q and TR32Q are deasserted, and red when TF32Q and TR32Q are asserted.

```
=>>SET F PB8_LED TE <Enter>
Front Panel


Front Panel Settings


Pushbutton LED 8 (SELOGIC Equation)
PB8_LED := NA
?  TF32Q <Enter>
PB8_LED Assert & Deassert Color (Enter 2: R,G,A,O)   PB8_COL := AO     ?RG
Pushbutton LED 9 (SELOGIC Equation)
PB9_LED := NA
?  TR32Q <Enter>
PB9_LED Assert & Deassert Color (Enter 2: R,G,A,O)   PB9_COL := AO     ?RG
Pushbutton LED 10 (SELOGIC Equation)
PB10LED := NA
?  END <Enter>

Save settings (Y,N)  ?Y <Enter>
Saving Settings, Please Wait...........
Settings Saved

=>>
```

Figure 3.31 Front-Panel Settings

Step 4. Display the F32Q and R32Q Relay Word bits on the front-panel LCD screen.

a. Access the front-panel LCD MAIN MENU.

b. Highlight RELAY ELEMENTS and press **ENT**.

You will see a RELAY ELEMENTS screen with SEARCH highlighted at the bottom of the screen.

c. Press **ENT** to go to the ELEMENT SEARCH submenu.

d. Enter characters in the text input field using the navigation keys.

e. Highlight T and press **ENT** to enter the T character.

f. Highlight F and press **ENT** to enter the F character.

g. Enter the 3, 2, and Q characters in like manner.

h. Highlight ACCEPT and press **ENT**.

The relay displays the screen containing the TF32Q and TR32Q elements, as shown in *Figure 3.32*.
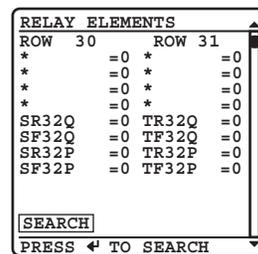
Figure 3.32 RELAY ELEMENTS LCD Screen Containing Elements TF32Q and TR32Q

Step 5. Calculate impedance thresholds.

a. For this test, apply an A-Phase voltage of VAV = 3V2 = 18.0 ∠180° V secondary.

b. Use *Equation 3.27* to find the current that is equal to the reverse impedance threshold Z2R.

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2RT} = \frac{|18.0\angle180°\,V|}{4.4} = 4.1\ A$$

Equation 3.27

Step 6. Use *Equation 3.28* to find the current that is equal to the forward impedance threshold Z2F:

$$|I_{TEST}| = |3I_2| = \frac{|3V_2|}{Z2RFT} = \frac{|18.0\angle180°V|}{3.90} = 4.62 \text{ A}$$

Equation 3.28

Step 7. Use *Equation 3.29* to determine the applied current angle ($\angle I_{TEST}$):

$$\angle I_{TEST} = \angle 3I_2 = \angle 3V_2 - \angle Z1ANG = 180° - 84° = 96°$$

Equation 3.29

Step 8. Apply a test current to confirm operation of TR32Q and TF32Q.

a. Connect a test source as shown in *Figure 3.33*.

b. Apply an A-Phase voltage of VA = 18.0∠180° V secondary.
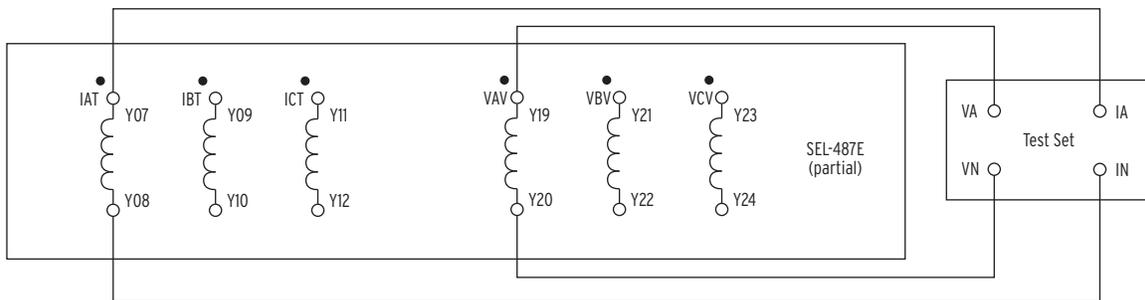
Figure 3.33   Connections for Directional Element Test

c. Set the current source for IA = 0.0∠96° A.

d. Slowly increase the magnitude of IAT to apply the source test current.

e. Observe the RELAY ELEMENT LCD screen. Relay Word bit TR32Q asserts when |IA| = 0.4 A, indicating that the relay negative-sequence current is greater than the 50RPT pickup threshold. TR32Q deasserts when |IA| = 4.1 A, indicating that the relay negative-sequence calculation Z2c is now less than the Z2 reverse threshold Z2RT.

f. Continue to increase the current source while you observe the RELAY ELEMENT LCD screen. Relay Word bit TF32Q asserts when |IA| = 4.62 A, indicating that the relay negative-sequence calculation Z2c is less than the Z2 forward threshold Z2FT.

Commissioning Testing

When: When installing a new protection system.

Goal:

➤ Ensure that all system ac and dc connections are correct.

➤ Ensure that the relay functions as intended using your settings.

➤ Ensure that all auxiliary equipment operates as intended.

⚠ **WARNING**
Before working on a CT circuit, first apply a short to the secondary winding of the CT.

What to test: All connected or monitored inputs and outputs; polarity and phase rotation of ac current connections; simple check of protection elements.

SEL performs a complete functional check and calibration of each relay before it is shipped. This helps ensure that you receive a relay that operates correctly and accurately. Commissioning tests should verify that the relay is properly connected to the power system and all auxiliary equipment. Verify control signal inputs and outputs. Check breaker auxiliary inputs, SCADA control inputs, and monitoring outputs. Use an ac connection check to verify that the relay current inputs are of the proper magnitude and phase rotation.

Brief fault tests ensure that the relay settings are correct. It is not necessary to test every relay element, timer, and function in these tests.

Use the *SEL-487E Relay Commissioning Test Worksheet on page 3.44* to verify correct CT connections and settings when placing the relay in service. The worksheet shows how using software commands or the front-panel display can replace the need for the traditional phase angle meter and ammeter.

At commissioning time, use the relay **METER DIF** command to record the measured operate and restraint values for through-load currents. Use the **PULSE** command to verify relay output contact operation.

Commissioning Assistant

Commissioning Assistant is a software tool that checks for single-contingency wiring errors and then calculates a matching compensation matrix for a test winding with respect to a user-defined reference winding.

Use Commissioning Assistant to further assist you during commissioning. In general, commissioning tools to check the differential element are limited to measuring the differential current. However, use of the operating current as a catchall indicator of all commissioning errors can result in ambiguous conclusions. For example, both incorrect CT polarity and a CT connected to the incorrect CT tap result in the presence of operating current.

Therefore, although the presence of excessive operating current indicates commissioning error(s), the commissioning engineer cannot identify the specific cause of the unbalance by the mere presence of operating current. Clearly, we need to take measurements other than just the differential current to identify the specific cause of the operating current. *Table 3.17* shows the measurement methods we use in the Commissioning Assistant.

Table 3.17   Measurement Methods to Identify Various Causes of Operating Current

Error	Measuring Method
Insufficient load current	Current magnitude measurement
Two crossed phases	Negative-sequence current measurement
CT connected to the incorrect tap	Expected current to measured current magnitude comparison; negative-sequence current measurement
Incorrect CT polarity	Angular comparison between a reference phase and all other phases
Vector-group compensation selection	Operating current and phase angle measurement

Be aware of the following limits:

1. The matrix calculations are reliable when no wiring errors are present and the transformer is on the nominal tap.

2. The error-detection algorithm is designed to identify single errors; it may or may not correctly identify multiple errors.

3. The error-detection algorithm is reliable for a system unbalance as great as 25 percent.

4. The incorrect CT tap that the consistent CT ratio error calculations can detect is inversely proportional to the magnitude of the load current. At the minimum load current (five percent of full-load current), the CT ratio error must exceed 30 percent for the consistent CT ratio error check to detect the error. At 20 percent load, the CT ratio error must exceed only 10 percent. At full load, this value drops to 4 percent.

Flow Diagram

Figure 3.34 shows the flow diagram of the process.
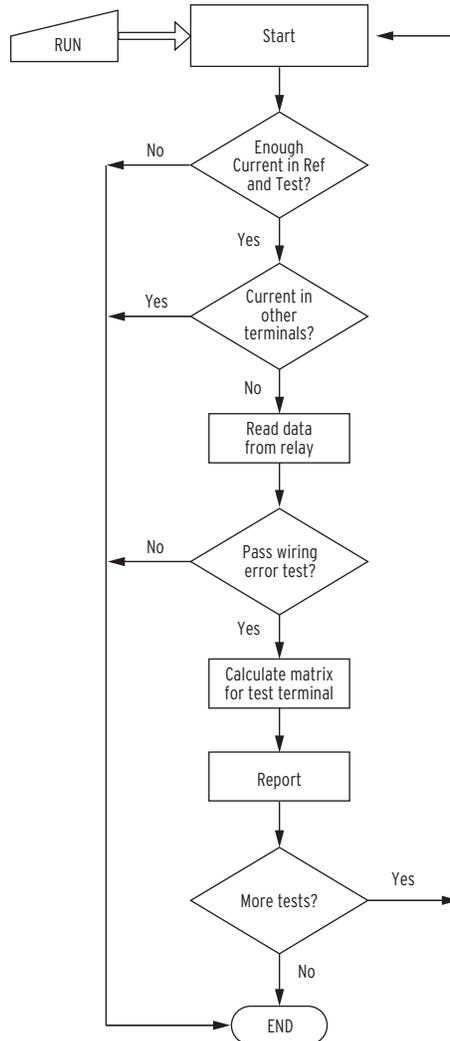
Figure 3.34   Process Flow Diagram

In general, Commissioning Assistant compares quantities from a test terminal against quantities from a reference terminal. To avoid ambiguous results, Commissioning Assistant processes only two terminals in each test. For multiterminal applications, use one of the terminals from the first test in subsequent tests for the remaining windings.

As an example, consider the station shown in *Figure 3.35*. This station has a breaker-and-a-half busbar on the HV side of the wye/wye (star/star) transformer, and a single busbar on the LV side. All CTs are wye (star) connected.
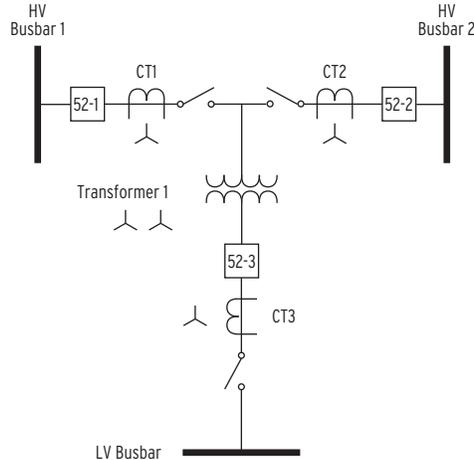
Figure 3.35 Example Substation

Launch Commissioning Assistant from QuickSet under the **Tools** menu, as in *Figure 3.36*. Notice the tree on the left side of the figure. Presently, the **Select Transformer Terminals** is highlighted. As you complete a step in the process, the highlight moves to the next step to guide you through the selection process.
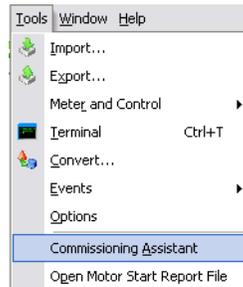
Figure 3.36 Launch Commissioning Assistant

Click on the **I Agree** button of the Disclaimer to continue with the testing (*Figure 3.37*), and click **OK** to select **487E** (*Figure 3.38*).
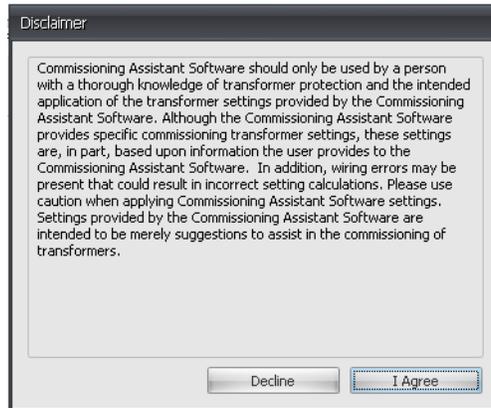
Figure 3.37   Disclaimer
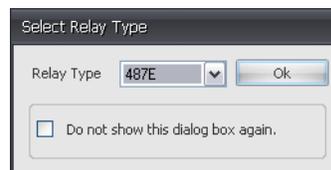
Figure 3.38   SEL-487E Relay Selection

Figure 3.39 shows the configuration screen, consisting of the following four areas:

> ➤ Control Area—Run tests, reset/start a new diagram, and save the report.

> ➤ Test Step Area—This area shows all the steps in the testing procedure, and highlights the present step. Presently, the **Select Transformer Terminals** is highlighted. As you complete a step in the process, the highlight moves to the next step to guide you through the selection process.

> ➤ Configuration Selection Area—Select the HV and LV CT configuration, and the transformer type in this area.

> ➤ Configuration Reference Area—This area displays the selections from the Configuration Selection Area to give you an overall picture of the bay configuration.
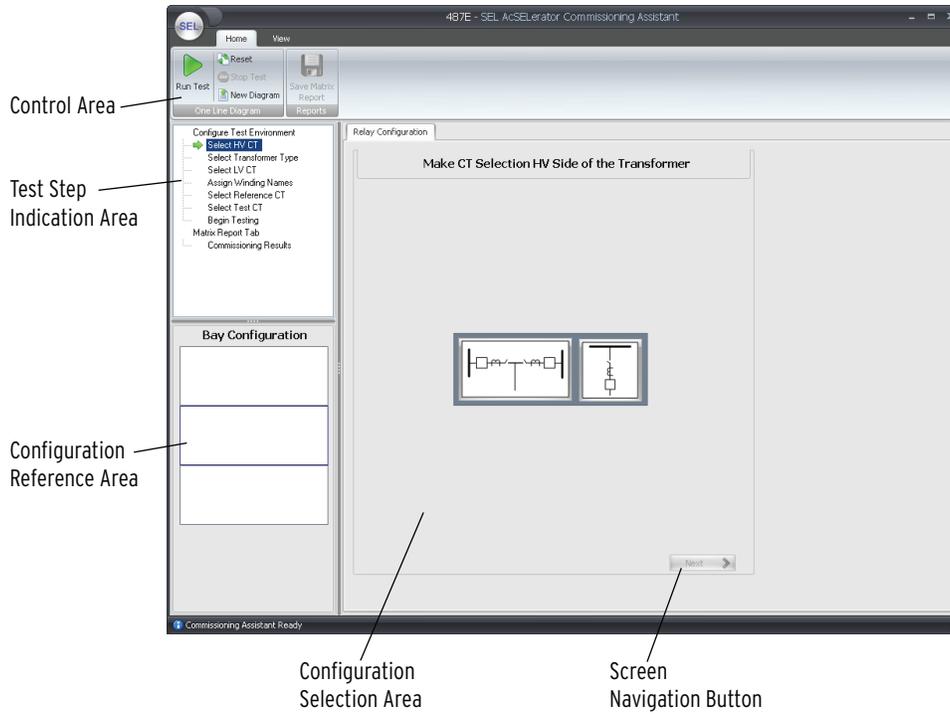
Figure 3.39   Configuration Screen

To configure the HV part of the example substation, select the encircled image (*Figure 3.40*). Notice that the selection appears in the Reference Area.
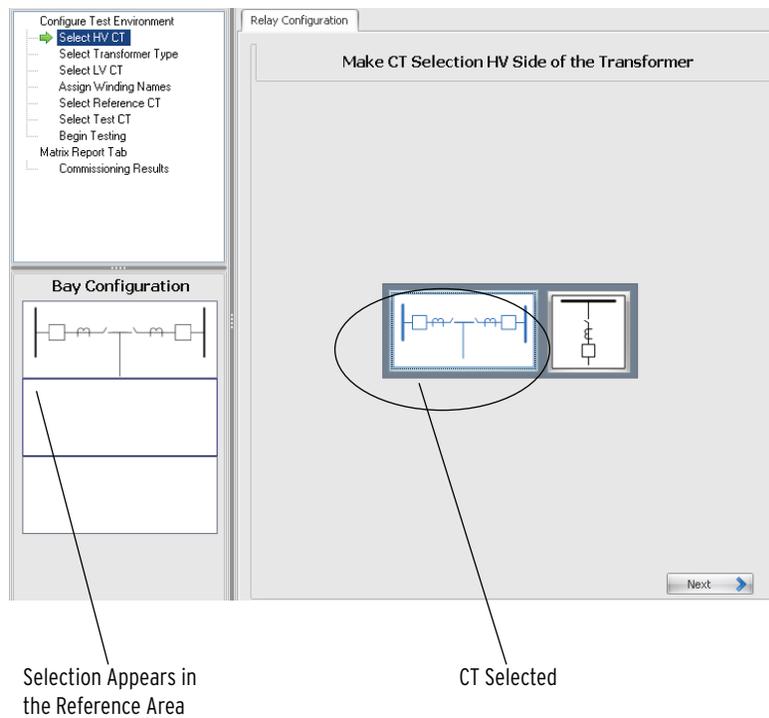
Figure 3.40   HV CT Selection

Click the **Next** button to move to the screen displayed in *Figure 3.41*. Select the appropriate transformer type, and notice that the selection appears in the Reference Area. Also notice that the **Select Transformer Type** is highlighted in the Test Step Area. If you want to select a different HV CT arrangement, click the **Previous** button to go to the previous screen.
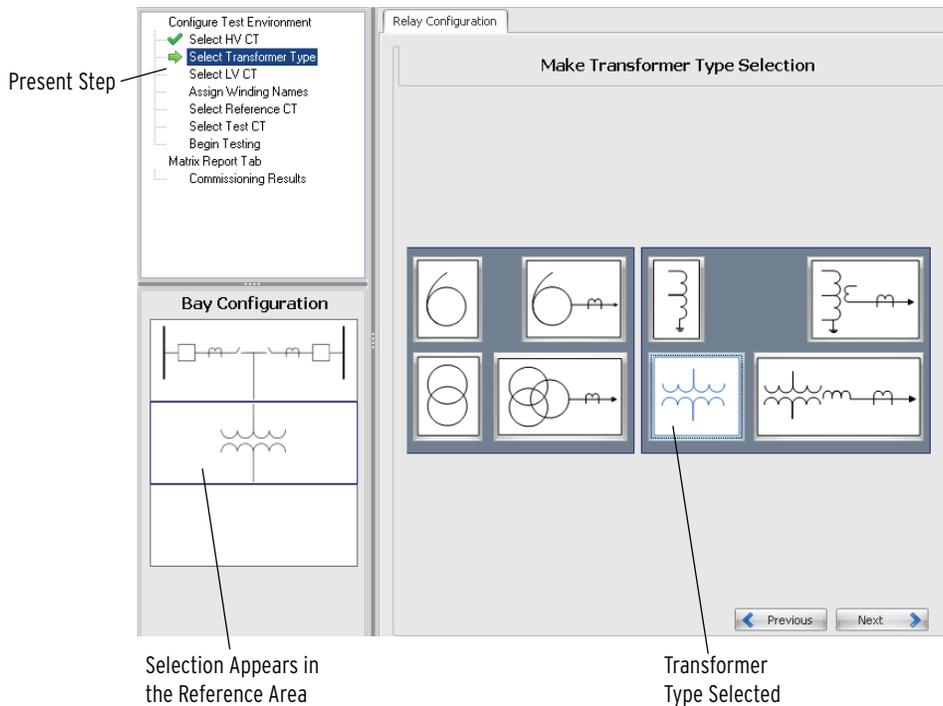
Figure 3.41   Transformer Type Selection

Click the **Next** button, and select the LV CT configuration as in *Figure 3.42*. This completes the configuration of the transformer bay.
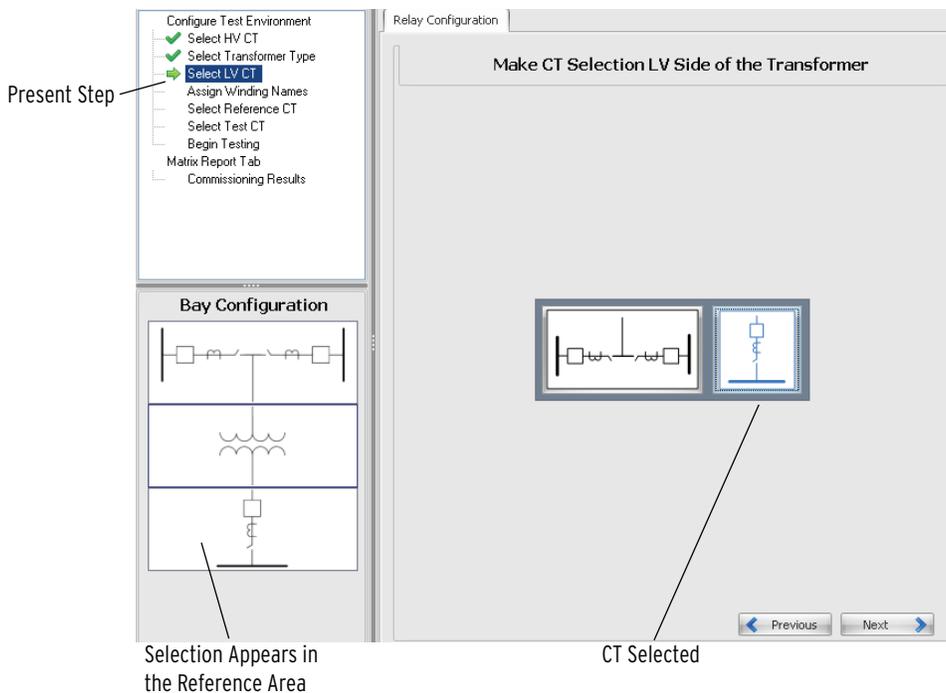
Figure 3.42   LV CT Selection

Click the **Next** button to move to the screen displayed in *Figure 3.42*. Because you can install the SEL-487E in widely varying substation configurations with differing CT allocations, the terminals and CTs are not fixed. Therefore, you must associate a terminal with each CT.
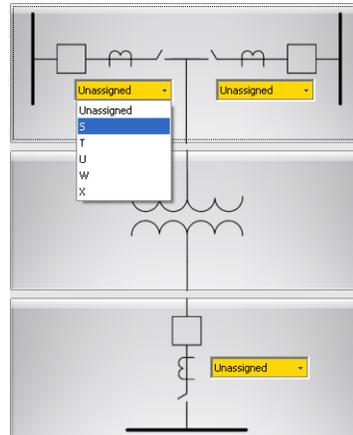
Figure 3.43   CT S Assignment
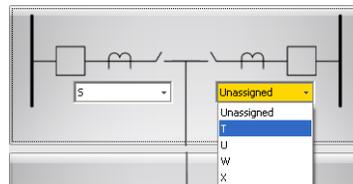
Figure 3.44   CT T Assignment

Make sure you assign the CTs to match the wiring of each terminal. Assume the following for this example:

➤ Terminal S: HV left-hand CT (CT1 in *Figure 3.35*)

➤ Terminal T: HV right-hand CT (CT2 in *Figure 3.35*)

➤ Terminal U: LV CT (CT3 in *Figure 3.35*)

Figure 3.43 shows the screen that appears after you click in the box below CTS. All five windings are available at this point. Move the cursor down to **S** and left-click the mouse.

Click on the box below CTT, as shown in *Figure 3.44*. Notice that, because **S** is already assigned, only T, U, W, and X are available. Move the cursor down to **T** and left-click the mouse.

If you want to reassign an already assigned winding, first unassign the winding (*Figure 3.45*), then choose from the available windings.
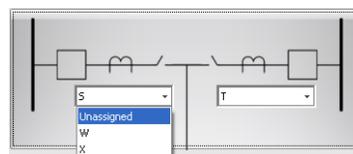
Figure 3.45   Unassign Winding S

In a similar way, assign Terminal U to the LV CT (CTU), as shown in *Figure 3.46*.
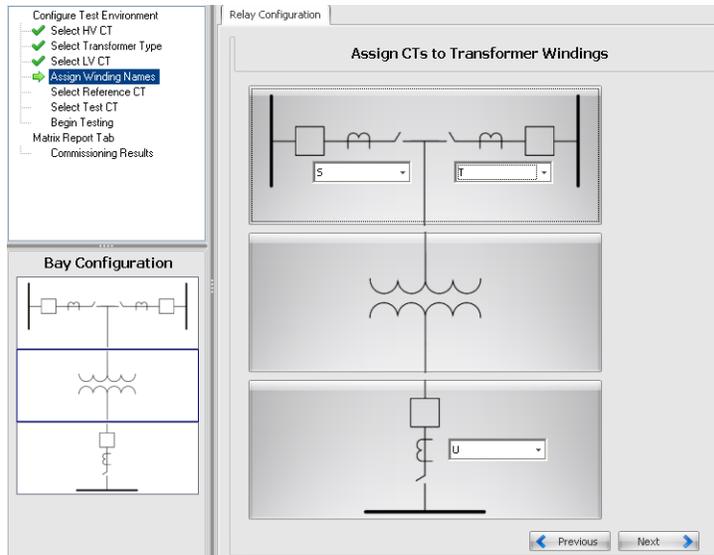
Figure 3.46   Completed CT Assignment

The final step in the configuration process is to choose a reference winding and a test winding. For example, arbitrarily select **Winding S** as reference and **Winding U** as test. *Figure 3.47* shows the selection of S as reference winding. Notice that the text "Reference Winding S" appears below CTS.
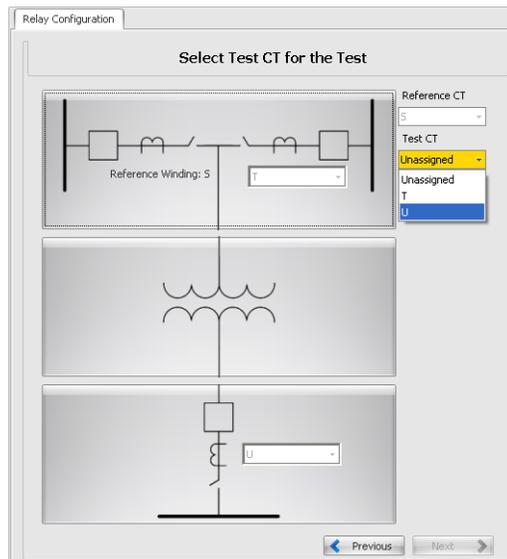
Figure 3.47   Selection of S as Reference Winding

After assigning Winding U as test winding, click **Next** to move to the screen shown in *Figure 3.48*. Notice that the text "Test Winding U" appears next to CT U.
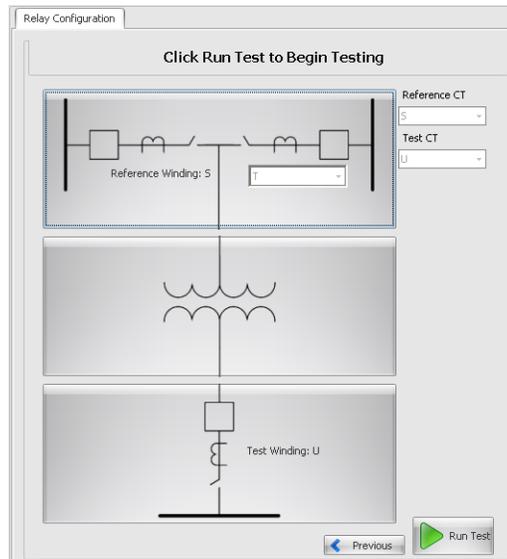
Figure 3.48   Ready to Run the Test

Because Commissioning Assistant allows only two windings per test, open Breaker 52-2 and the disconnect to ensure that no current flows through CTT. *Figure 3.49* shows the correct flow of current for this test.
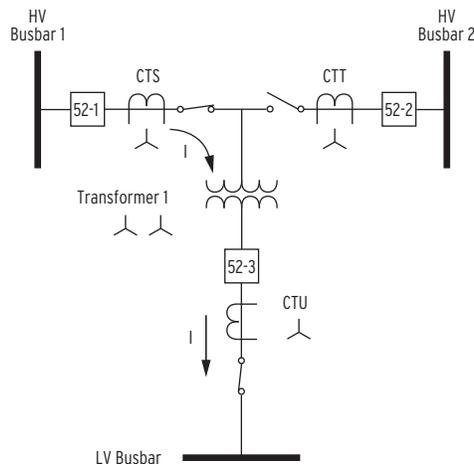
Figure 3.49   Current Flow Through CTS and CTU Only

After clicking the **Run Test** button, the message shown in *Figure 3.50* appears. Commissioning Assistant uses the voltage ratio to calculate certain quantities, so please ensure that the transformer is on the nominal tap. Nominal tap is where the transformer turns ratio equals the system voltage ratio.
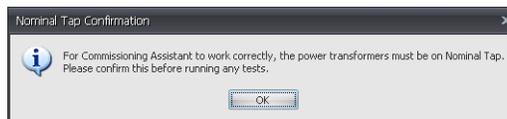
Figure 3.50   Nominal Tap Position Reminder

After clicking on the **OK** button, the screen with communication parameters (*Figure 3.51*) appears. Select the correct values and click **OK**.
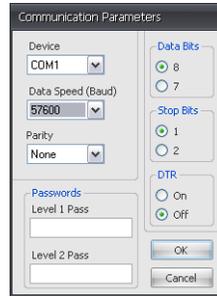
Figure 3.51   Communication Parameters

Click **Run Test** to start the matrix calculation process. Commissioning Assistant now reads selected information from the relay using ASCII **MET** commands.

Commissioning Assistant first performs two current checks: Check 1 ensures that more than five percent of the full load current flows in both Terminal S and Terminal U; Check 2 ensures that no current flows in Terminal T. If either check fails, the relay reports the error and aborts the test, as in *Figure 3.52*.
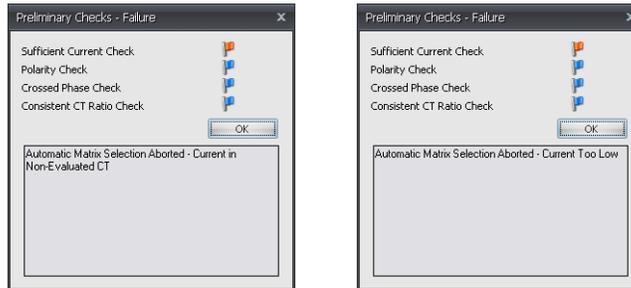
Figure 3.52   Current in Non-Evaluated CT and Current Too Low Error Screens

Commissioning Assistant then tests for the following before calculating the matrix for the test winding.

➤ Correct polarities

➤ Consistent CT ratio

➤ Two crossed phases

If the installation fails any of these wiring tests, Commissioning Assistant flags the error and aborts the test. For example, assume that the B-Phase HV CT has an incorrect polarity. Commissioning Assistant finds this error and specifies the offending CT. *Figure 3.53* shows the error messages for the three wiring checks.

➤ Green—passed

➤ Red—failed

➤ Blue—not tested yet
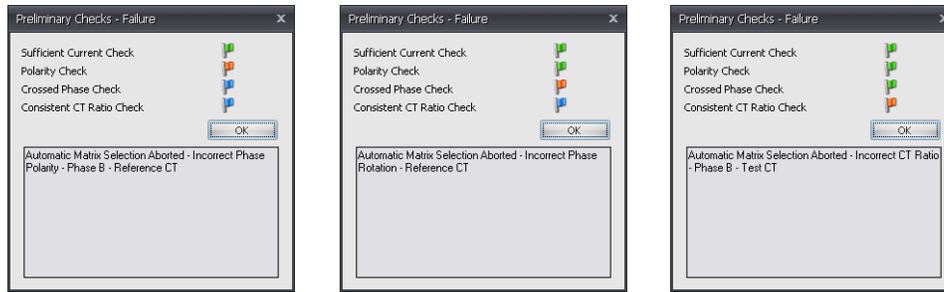
Figure 3.53   Failed Wiring Checks

If the relay passes the wiring tests, Commissioning Assistant calculates the matrix for the test winding. Using the present settings in the relay, Commissioning Assistant assigns the existing matrix setting to the reference winding. Assume that the following are the present compensation settings in the relay.

➤ TSCTC = 11

➤ TTCTC = 12

➤ TUCTC = 10

With a wye/wye-connected transformer and all CTs connected in wye, these settings are clearly wrong. For the differential elements to balance, all compensation settings must have the same value: all set to 11, 12, or 10. Because Commissioning Assistant uses the present settings for the reference terminal (11 in this case since Terminal S is the reference), all compensation settings must equal 11. For the first test (testing Terminal S and Terminal U), Commissioning Assistant must therefore calculate a matrix value of 11 for Terminal U. *Figure 3.54* shows the report of the first test, with the expected result.
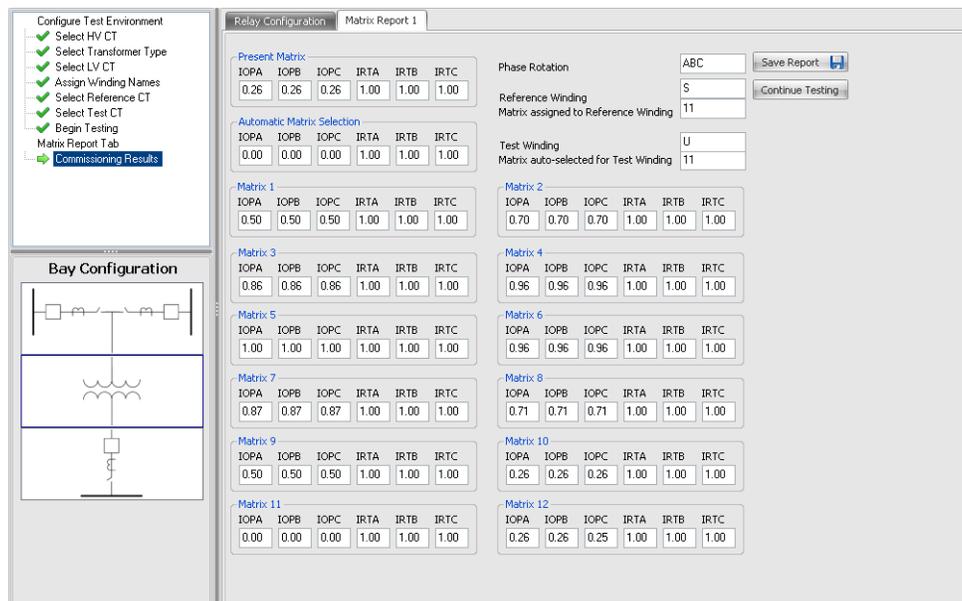
Figure 3.54   Results of Testing Terminal S and Terminal U

The report shows the relevant information for this test:

➤ Operate and restraint current with the present settings

➤ Operate and restraint current with the calculated matrix

➤ Phase rotation

➤ Matrix number of the reference winding

➤ Calculated matrix number of the test winding

➤ Results of all other matrix combinations

Click on **Save Report** to save the report to your hard drive or to any other convenient location, then click on Continue Testing to also test Terminal T. For subsequent tests, any qualified winding can be used as reference. Qualified windings are windings that have already been successfully matched with matrices that produce (almost) zero differential current. In this case, either Winding S or Winding U are qualified windings, but not Winding T. For the next test, assign Terminal U as reference winding and Terminal T as test winding, as shown in *Figure 3.55*.
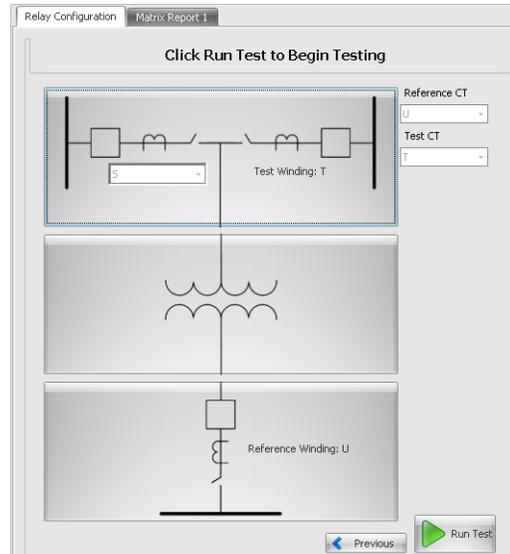
Figure 3.55   Assign Terminal U as Reference Winding and Terminal T as Test Winding

For this test, be sure that current flows only in Terminal T and Terminal U, as shown in *Figure 3.56*.
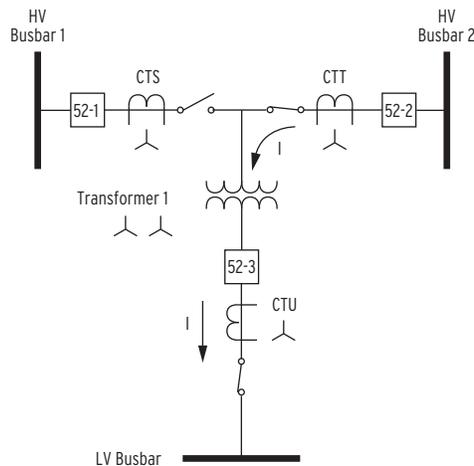
Figure 3.56   Current Flow Through CTT and CTU Only

Follow the steps described in Test 1. As with Test 1, the correct matrix number for Terminal T is 11, as shown in *Figure 3.57*.
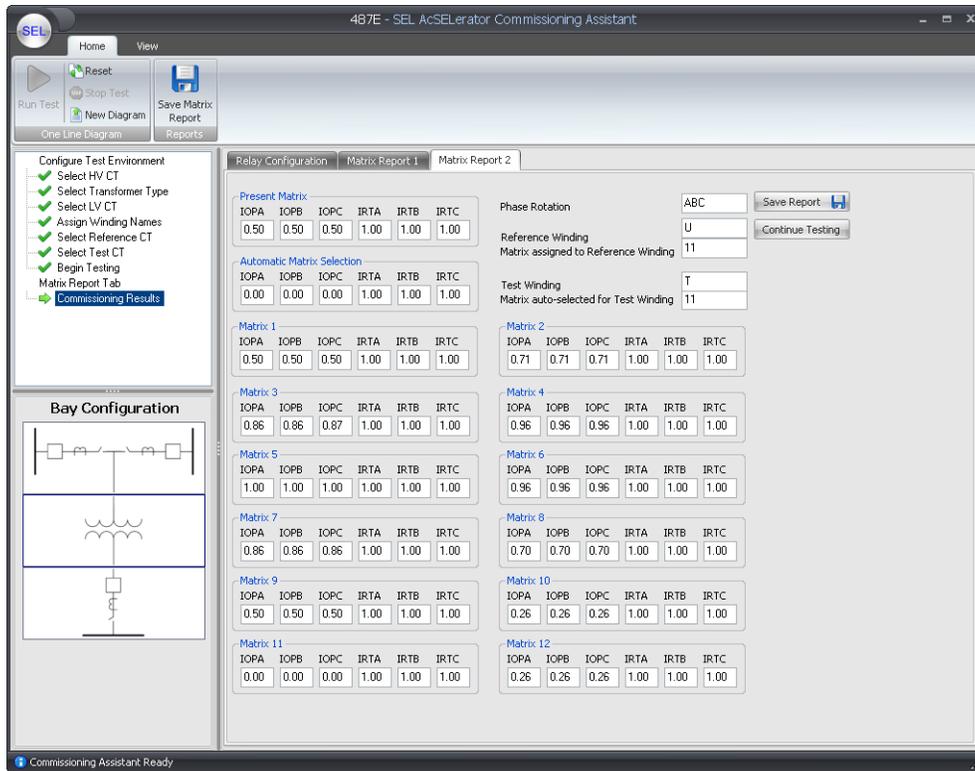
Figure 3.57 Results of Testing Terminal S and Terminal T

Be sure to save all test results. After you save these results, the screen shown in *Figure 3.58* appears. Click on **No** to conclude the tests.
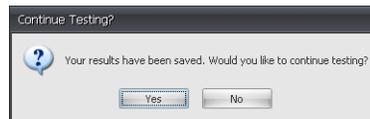
Figure 3.58 Conclusion of the Testing

Technical Support

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

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Pullman, WA 99163-5603 U.S.A.
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SEL-487E Relay Commissioning Test Worksheet

System Information

System Settings

RID (Relay identification) = _____

TID (Terminal identification) = _____

MVA (Maximum transformer Rating) = _____

	Winding S		Winding T		Winding U		Winding W		Winding X	
Current transformer connection:	CTCONS =		CTCONT =		CTCONU =		CTCONW =		CTCONX =	
Current transformer ratio:	CTRS =		CTRT =		CTRU =		CTRW =		CTRX =	
Connection compensation:	TSCTC =		TTCTC =		TUCTC =		TWCTC =		TXCTC =	
Nominal line-to-line voltage (kV):	VTERMS =		VTERMT =		VTERMU =		VTERMW =		VTERMX =	
TAP calculation:	TAPS =		TAPT =		TAPU =		TAPW =		TAPX =	

Differential Settings

087P =		SLP1 =		SLP2 =		U87P =	

Metered Load (Data taken from substation panel meters, not the SEL-487E)

± Readings from meters	Winding S		Winding T		Winding U		Winding W		Winding X	
Megawatts:	MWS =		MWT =		MWU =		MWW =		MWX =	
Megavars:	MVARS =		MVART =		MVARU =		MVARW =		MVARX =	
MVA calculation:	MVAS =		MVAT =		MVAU =		MVAW =		MVAX =	

MVA calculation:

$$MVAn = \sqrt{MWn^2 + MVARn^2}$$

Calculated Relay Load

	Winding S		Winding T		Winding U		Winding W		Winding X	
Primary Amperes calculation:	ISpri =		ITpri =		IUpri =		IWpri =		IXpri =	
Secondary Amperes calculation:	ISsec =		ITsec =		IUsec =		IWsec =		IXsec =	

Primary Amperes calculation:

$$\text{Inpri} = \frac{MVAn \cdot 1000}{\sqrt{3} \cdot VTERMn}$$

Secondary Amperes calculation:

$$CTCONn = Y, \text{In sec} = \frac{\text{Inpri}}{CTRn}$$

$$CTCONn = D, \text{In sec} = \frac{\text{Inpri} \cdot \sqrt{3}}{CTRn}$$

Connection Check

System load conditions should be higher than 0.1 A secondary. 0.5 A secondary is recommended for the best results.

Differential Connection (issue MET DIF <Enter> to serial port or front panel)

Operate Current:	IOPA =		IOPB =		IOPC =
Restraint Current:	IRTA =		IRTB =		IRTC =
Mismatch Calculation:	MMA =		MMB =		MMC =

Check individual current magnitudes, phase angles, and operate and restraint currents in an event report if mismatch is not less than 0.10.

Mismatch Calculation:

$$MMn = \frac{IOPn}{IRTn}$$

Magnitude, Angle, and Phase Rotation Check

Issue **MET SEC <Enter>** to the serial port or front panel.

	Winding S	Winding T	Winding U	Winding W	Winding X
A-Phase Secondary Amperes:	IAWS =	IAWT =	IAWU =	IAWW =	IAWX =
A-Phase Angle:					
B-Phase Secondary Amperes:	IBWS =	IBWT =	IBWU =	IBWW =	IBWX =
B-Phase Angle:					
C-Phase Secondary Amperes:	ICWS =	ICWT =	ICWU =	ICWW =	ICWX =
C-Phase Angle:					

Winding 1

Winding 2
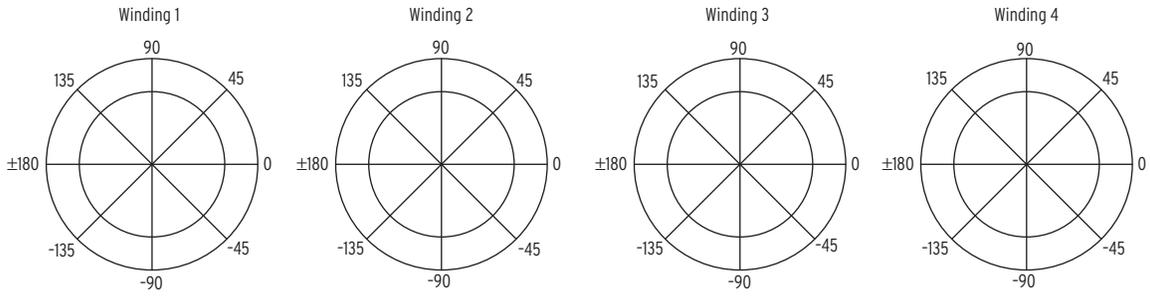
Winding 3

Winding 4

1. Calculated relay amperes match MET SEC amperes?

2. Phase rotation is as expected for each winding?

3. Do angular relationships among windings correspond to expected results? (Remember that secondary current values for load current flowing out of a winding will be 180° out-of-phase with the reference phase position for that winding. The reason is that CT polarity marks normally face away from the transformer on all windings.)

Front-Panel Operations

There are two prominent functions of the front panel, i.e., front-panel operations and the bay controller. This section describes the front-panel operations, and *Bay Control Front-Panel Operations on page 5.12 in the SEL-400 Series Relays Instruction Manual* describes the bay controller. Using the front panel, you can analyze power system operating information, view and change relay settings, collect power system data, and perform relay control functions. For ease of navigation, the front-panel menu is a straightforward menu driven control structure presented on the front-panel liquid crystal display (LCD). Front-panel targets and other LED indicators give a quick look at SEL-487E relay operation status. You can perform often-used control actions rapidly by using the large direct-action pushbuttons. All of these features help you operate the relay from the front panel and include:

➤ Reading metering

➤ Inspecting targets

➤ Accessing settings

➤ Controlling relay operations

This section includes the following:

Front-Panel LCD Default Displays

The SEL-487E has two screen scrolling modes: autoscrolling and manual scrolling. After front-panel time-out, the relay enters the autoscrolling mode, and the LCD presents each of the display screens in this sequence:

➤ Any active (filled) alarm points screens

➤ Any active (filled) display points screens

➤ Enabled metering screens

➤ One-line diagrams

NOTE: Some versions of the firmware only display the high voltage one-line diagram when ONELINE is selected as an autoscrolling screen.

Table 4.1 shows the high voltage and low-voltage side screen selection, and *Table 4.2* through *Table 4.5* show the meter screen available for display on the front panel in the autoscrolling mode.

Table 4.1   Metering Screens Enable Settings

Screen	Description
ONELINE	Bay Control screen

Table 4.2   RMS Values

Screen	Description
Individual Windings (Values)	
RMS_VLL	Line-to-line rms voltage
RMSW*m*VI[a]	Winding *m* rms current and voltage screens
Combined Windings	
STRMSVI	Combined Windings S and T current and voltage screens
TURMSVI	Combined Windings T and U current and voltage screens
UWRMSVI	Combined Windings U and W current and voltage screens
WXRMSVI	Combined Windings W and X current and voltage screens

[a] *m* = S, T, U, W, X.

Table 4.3   Fundamental Values

Screen	Description
Individual Windings (Values)	
FUN_VLL	Fundamental Line-to-Line Voltage, Frequency, and VDC screen
FUNW*m*VI[a]	Winding *m* Fundamental Phase current and voltage screen
FUNW*m*SQ[a]	Winding *m* Fundamental Sequence voltage and current screens
FUNW*m*PQ[a]	Winding *m* Fundamental real (P) and reactive (Q) screen
FUNW*m*VA[a]	Winding *m* Fundamental Apparent Power and pf screen
Combined Windings	
STFUNVI	Combined Windings S and T current and voltage screen
TUFUNVI	Combined Windings T and U current and voltage screen
UWFUNVI	Combined Windings U and W current and voltage screen
WXFUNVI	Combined Windings W and X current and voltage screen
STFUNSQ	Combined Windings S and T Fundamental Sequence voltage and current screen
TUFUNSQ	Combined Windings T and U Fundamental Sequence voltage and current screen
UWFUNSQ	Combined Windings U and W Fundamental Sequence voltage and current screen
WXFUNSQ	Combined Windings W and X Fundamental Sequence voltage and current screen
STFUNPQ	Combined Windings S and T real (P) and reactive (Q) screen
TUFUNPQ	Combined Windings T and U real (P) and reactive (Q) screen
UWFUNPQ	Combined Windings U and W real (P) and reactive (Q) screen
WXFUNPQ	Combined Windings W and X real (P) and reactive (Q) screen
STFUNVA	Combined Windings S and T Apparent Power and Power Factor Screen
TUFUNVA	Combined Windings T and U Apparent Power and Power Factor Screen
UWFUNVA	Combined Windings U and W Apparent Power and Power Factor Screen
WXFUNVA	Combined Windings W and X Apparent Power and Power Factor Screen

[a] *m* = S, T, U, W, X.

Table 4.4 Energy Quantities

Screen	Description
ENRMET*m*[a]	Winding *m* energy screen
STENERM	Combined Windings S and T energy screen
TUENERM	Combined Windings T and U energy screen
UWENERM	Combined Windings U and W energy screen
WXENERM	Combined Windings W and X energy screen

[a] *m* = S, T, U, W, X.

Table 4.5 Differential Quantities

Screen	Description
DIFFMET	Differential quantities screen

Use the front-panel settings (the **SET F RDD** command from a communications port or the **Front Panel** settings in QuickSet Software) to access the metering screen enables. Enter each of the desired screens on a separate line. The relay will display the screens in the sequence that you enter. *Figure 4.1* shows a sample ROTATING DISPLAY consisting of an example alarm points screen (see *Alarm Points on page 4.7 in the SEL-400 Series Relays Instruction Manual*), an example display points screen (see *Display Points on page 4.10 in the SEL-400 Series Relays Instruction Manual*), and the metering screen RMSWSVI (see *Table 4.2*).
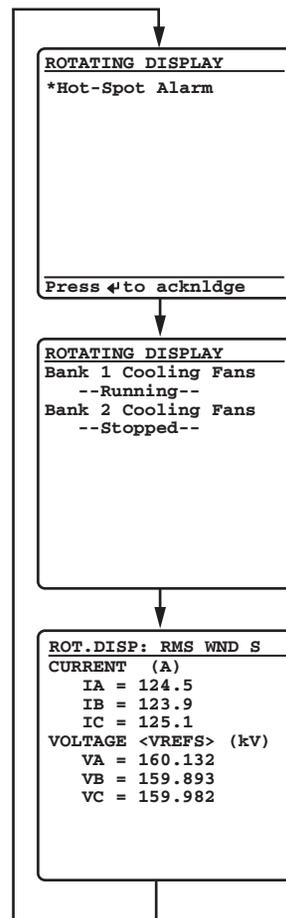
Figure 4.1 Sample ROTATING DISPLAY

Front-Panel Menus and Screens

Operate the SEL-487E front panel through a sequence of menus that you view on the front-panel display. The MAIN MENU is the introductory menu for other front-panel menus. These additional menus allow you on-site access to metering, control, and settings for configuring the SEL-487E to your specific application needs. Use the following menus and screens to set the relay, perform local control actions, and read metering:

➤ Support Screens
  ➢ Contrast
  ➢ Password
➤ MAIN MENU
  ➢ METER
  ➢ EVENTS
  ➢ BREAKER MONITOR
  ➢ RELAY ELEMENTS
  ➢ LOCAL CONTROL
  ➢ SET/SHOW
  ➢ RELAY STATUS
  ➢ VIEW CONFIGURATION
  ➢ DISPLAY TEST
  ➢ RESET ACCESS LEVEL
  ➢ ONELINE DIAGRAM

See *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual* for information on most of these screens. The following screen descriptions are unique to the SEL-487E.

Meter

The SEL-487E displays metering screens on the LCD. Highlight METER on the MAIN MENU screen to select these screens. The METER MENU, shown in *Figure 4.2*, allows you to choose the following metering screens corresponding to the relay metering modes:

➤ RMS METER
➤ FUNDAMENTAL METER
➤ DEMAND METER
➤ ENERGY METER
➤ DIFFERENTIAL METER
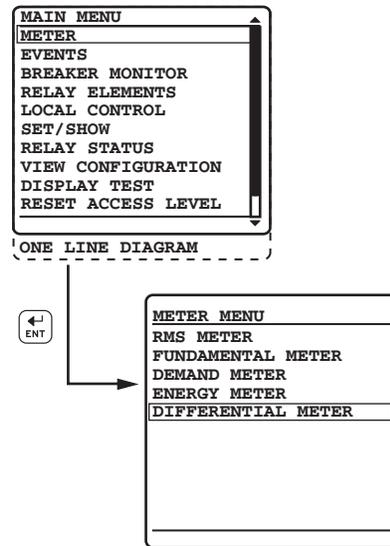
Figure 4.2   METER Menus

Figure 4.2 shows the five categories of meter screens available in the SEL-487E, as well as the prerequisite(s) for each screen. *Table 4.6* summarizes these prerequisite(s) and also states how the VREF*m*, PTCON*k* (*k* = V, Z), and CTCON*m* (*m* = S, T, U, W, X) settings influence the displays. *Table 4.6* also shows the sequence in which the screens appear on the front panel.

Table 4.6   Meter Availability Conditions

Meter	Prerequisite
RMS Meter	Neither ECTTERM nor EPTTERM is to be set to OFF.
Fundamental Meter	Neither ECTTERM nor EPTTERM is to be set to OFF.
Demand Meter	EDEM is not set to OFF.
Energy Meter	None of EPCAL or VREF*m* is set to OFF.
Differential Meter	E87 is not set to OFF.
VREF*m* setting[a]	Power screens (apparent, real, and reactive) are displayed only for those windings that specified a PT in the VREF*m* settings.
PTCON*k*[b]	If PTCON*k* = D (delta-connected PTs), then 3V0 is not displayed.
CTCON*m*[a]	If CTCON*m* = D (delta-connected CTs), then 3I0 is not displayed.

[a]   *m* = S, T, U, W, X.

[b]   *k* = V, Z.

RMS Meter

To view the rms meter values, select METER from the main menu and press **ENT**, then press **ENT** with RMS METER highlighted, as shown in *Figure 4.3(a)*. *Figure 4.3(b)* shows the screen with the LINE VOLTAGES, SINGLE WINDING, and COMBINED WINDING options. With the LINE VOLTAGES highlighted, press **ENT** to see the line-to-line voltages of the enabled PTs, as shown in *Figure 4.3(c)*. In this example, both PT V and PT Z are enabled (included in the EPTTERM Group setting), and values from both PTs are available. If no PTs are enabled (EPTTERM = OFF), then this screen is not displayed.

```
┌─────────────────────────────┐
│ METER MENU                  │
│ ┌─────────────────────────┐ │
│ │ RMS METER               │ │
│ └─────────────────────────┘ │
│ FUNDAMENTAL METER           │
│ DEMAND METER                │
│ ENERGY METER                │
│ DIFFERENTIAL METER          │
│                             │
│                             │
│  ─────────────────────────  │
└─────────────────────────────┘
            (a)
```

```
┌─────────────────────────────┐
│ RMS METER                   │
│ ┌─────────────────────────┐ │
│ │ LINE VOLTAGES           │ │
│ └─────────────────────────┘ │
│ SINGLE WINDING              │
│ COMBINED WINDING            │
│                             │
│                             │
│                             │
│  ─────────────────────────  │
└─────────────────────────────┘
            (b)
```

```
┌─────────────────────────────┐
│ RMS: LINE VOLTS (kV)        │
│ LINE-TO-LINE PT V           │
│  VAB = 000.000              │
│  VBC = 000.000              │
│  VCA = 000.000              │
│                             │
│ LINE-TO-LINE PT Z           │
│  VAB = 000.000              │
│  VBC = 000.000              │
│  VCA = 000.000              │
│ FREQ = 00.00 Hz             │
│ VDC  = 000.0 V              │
│  ─────────────────────────  │
└─────────────────────────────┘
            (c)
```
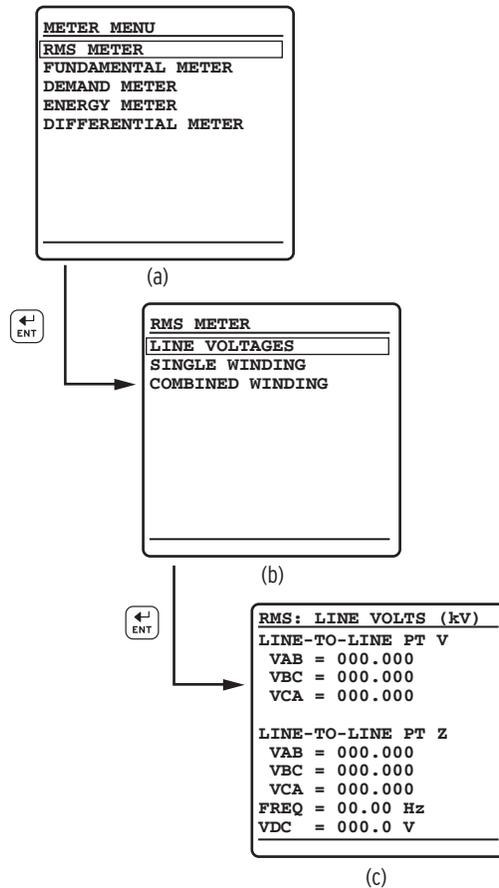
Figure 4.3 Line Voltages, Single Winding, and Combined Winding Options

With the SINGLE WINDING highlighted, press **ENT** to go to screen *(a)* in *Figure 4.4*, showing the single windings. Only windings that are included in the ECTTERM Group setting appear on this screen. In this example, all five windings are included in the ECTTERM setting (ECTTERM = S, T, U, W, X). With WINDING S highlighted, press **ENT** to move to the RMS METER: WINDING S and VOLTAGE screen (screen *(b)*) in *Figure 4.4*. If no voltages are enabled, then only current values are shown.

```
RMS METER
LINE VOLTAGES
SINGLE WINDING
COMBINED WINDING
```

⏎ ENT

```
RMS METER
WINDING S
WINDING T
WINDING U
WINDING W
WINDING X
```

(a)

⏎ ENT

```
RMS METER: WINDING S
CURRENT (A)

  IA = 00000.0
  IB = 00000.0
  IC = 00000.0

VOLTAGE <VREFS> (kV)

  VA = 000.000
  VB = 000.000
  VC = 000.000
```

(b)
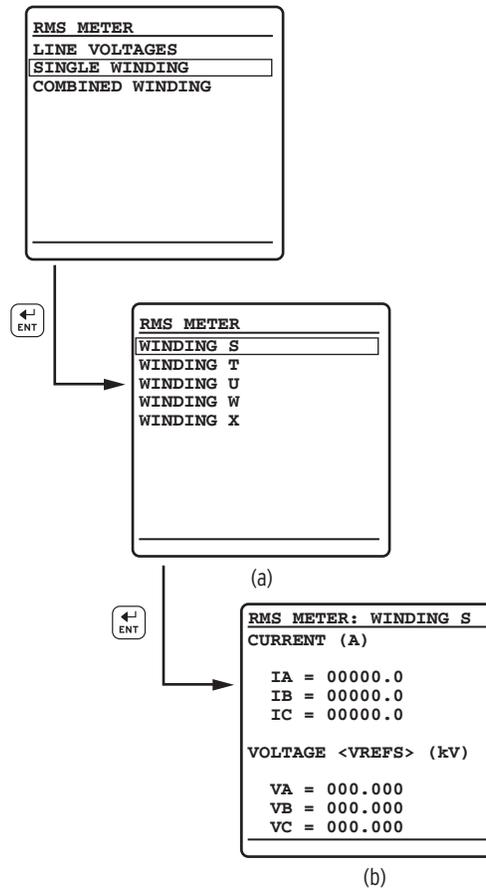
Figure 4.4   RMS Meter Screens

In screen *(b),* <VREFS> displays the value of the PT specified (VREFS = V or Z) for Winding S. If no PT is specified for Winding S (VREFS = OFF), then the voltage is not displayed. Winding T through Winding X have similar screens.

Combined winding screens are similar to the winding specific screens, as shown in *Figure 4.5* (combined Winding ST). Valid combinations are ST, TU, UW, and WX, and the content of *Table 4.6* also applies to the combined windings.

```
RMS METER: WINDNG ST
CURRENT(A)

 IA = 00000.0
 IB = 00000.0
 IC = 00000.0

VOLTAGE<VREFS>(kV)

 VA = 000.000
 VB = 000.000
 VC = 000.000
```

(a)
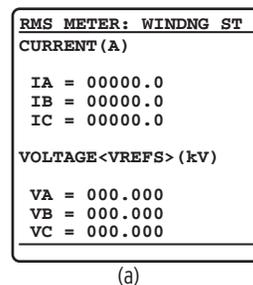
Figure 4.5   RMS Combined Windings

Fundamental Meter

The fundamental voltage and single winding screens provide similar information as shown in *Figure 4.3* and *Figure 4.4*. However, the fundamental meter also includes active, reactive, and apparent power screens, as well as sequence component screens, as shown in *Figure 4.6*. *Figure 4.6(a)* shows the fundamental

metering screen for Winding S. Notice that the fundamental meter includes the angular relationships, using the positive-sequence voltage of Terminal V as reference (VREFS = V in this example). Press the **Down Arrow** to move to the Winding S sequence screen. This screen shows the positive, negative, and zero-sequence voltage and currents for Winding S. Zero-sequence values are not shown when the CTs or PTs are connected in delta. Press the **Down Arrow** repeatedly to move through the remaining enabled winding, until screen *(c)*. Screens *(c)* and *(d)* shows the fundamental real, reactive and apparent power, and the power factors.

```
FND METER: WINDING S
CURRENT(A)

 IA =   502.4  23°
 IB =   502.1 -97°
 IC =   502.3 143°

VOLTAGE V (kV)

VA = 39.890    3°
VB = 39.932 -122°
VC = 39.875  118°
```
(a)

```
FND METER: WINDING S
CURRENT (A)
  I1 =    502.93  23°
 3I2 = 00000.00 000°
 3I0 = 00000.00 000°

 VOLTAGE V (kV)
  V1 = 39.86    0°
 3V2 =  3.50   91°
 3V0 =  3.46   91°
```
(b)

```
FND METER: WINDING S
 ACTIVE POWER (MW)
  A =  18.8
  B =  18.2
  C =  18.2
 3P =  55.3

 REACTIVE POWER(MVAr)
  A =  -6.8
  B =  -8.4
  C =  -8.4
 3Q = -23.6
```
(c)

```
FND METER: WINDING S
 APPARENT POWER(MVA)
  A =  20.0
  B =  20.1
  C =  20.1
 3S =  60.2

 POWER FACTOR
  A = 0.94   LEAD
  B = 0.91   LEAD
  C = 0.91   LEAD
 3P = 0.92   LEAD
```
(d)

Figure 4.6   Fundamental Single Winding Screens

Screens for the combined winding are the fundamental meter combined winding screens, including positive-, negative-, and zero-sequence screens.

Demand Meter

Following the fundamental meter screens are the demand meter screens. In the SEL-487E, the demand meter operate quantities are not fixed. Instead of fixed operating quantities, select a suitable operating quantity (see *Section 12: Analog Quantities*) for each of the 10 demand elements (see *Demand Meter on page 7.10* for more information).

Because you can select the number of demand elements, there will be either one or two sets of demand meter screens. If you select five or fewer demand elements, then there is only one screen; for greater than five demand elements, there are two screens. *Figure 4.7* shows the four demand screens. Screen *(a)* shows the selected demand element operating quantities. Also, each operating quantity can be either a rolling or a thermal calculation. This selection is shown by ROLL PK or THERM PK following the operating quantity in screen *(a)*. Screen *(b)* and screen *(c)* show reset options for demand and maximum demand quantities. Use the **Left Arrow** and **Right Arrow** pushbuttons to select a NO or YES response to the reset prompt, and then press **ENT** to reset all of the metering quantities.
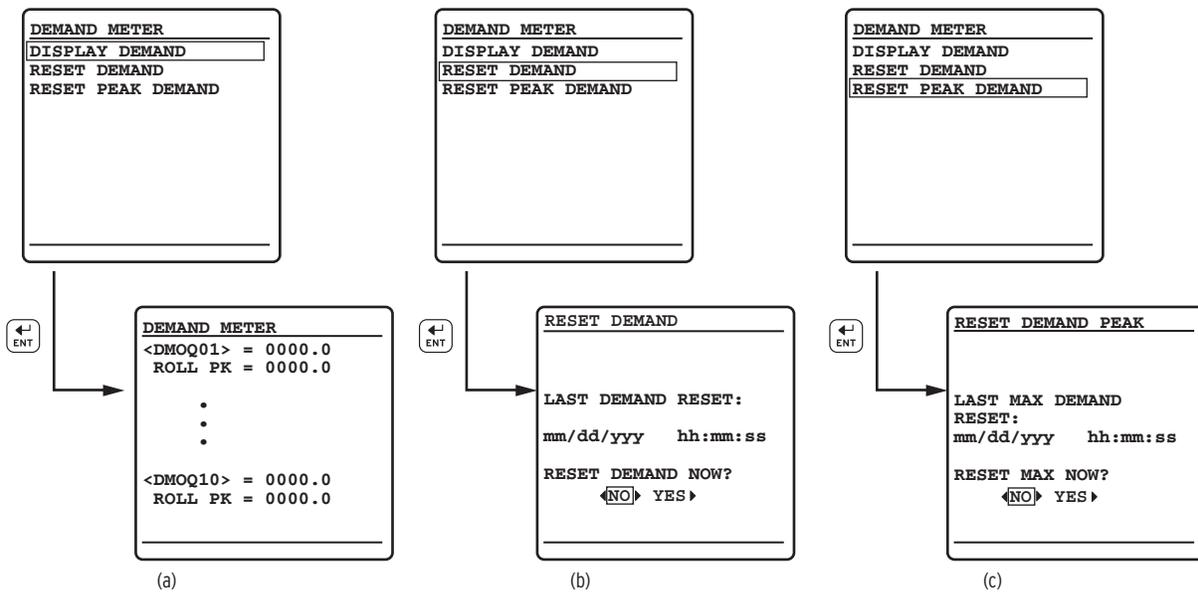
Figure 4.7   Demand Meter Screens

Energy Meter

Energy metering is the final front-panel display screen. *Figure 4.8(a)* shows the screen for a single winding, and *Figure 4.8(b)* shows the energy reset screen. Use the **Left Arrow** and **Right Arrow** pushbuttons to select a NO or YES response to the reset prompt, and then press **ENT** to reset all of the metering quantities.

When metering combined quantities, the individual windings must have the same reference voltage. For example, for Winding ST, VREFS and VREFT must both be set to the same reference voltage.
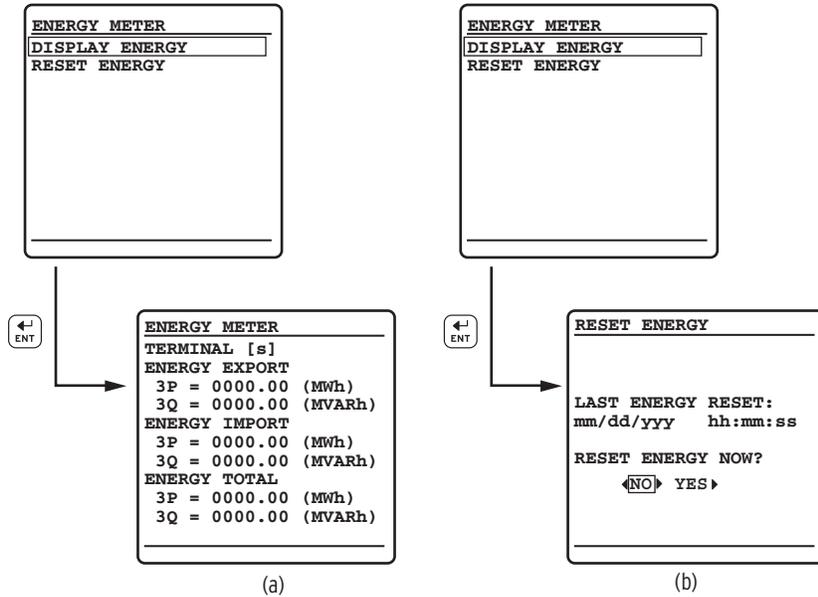
Figure 4.8   Energy Meter Screens

Events

The SEL-487E front panel features summary event reporting, which simplifies post-fault analysis. These summary event reports include the items shown in *Table 4.7*.

Table 4.7   Event Elements

Event	Description
87RA, 87RB, 87RC, REF	Differential elements involvement for event reports generated by 87A, 87B, or 87C. REF is the OR combination of REFF1, REFF2, and REFF3
TRIP	Rising edge of Relay Word bit TRIP
ER (event report trigger)	Rising edge of ER (SELOGIC control equation)
TRIG	Execution of the **TRIGGER** (**TRI**) command (manually triggered)
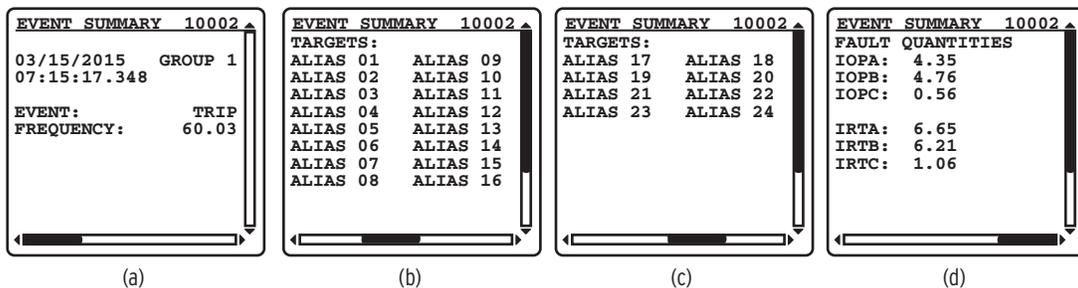
Figure 4.9   EVENT SUMMARY Screen

To assist with fault analysis, the SEL-487E displays the targets that asserted during the event on the front panel. Use the **Right Arrow** pushbutton to move from screen *(a)* to screen *(b)* in *Figure 4.9*. There are 24 alias items (ALIAS 01 through ALIAS 24), one for each of the front-panel LEDs. Use the **SET T** command to enter alias settings for Relay Word bits TLED_1 through TLED_24. If

no alias is defined for a particular TLED_x (x = 1 through 24), then the TLED_x Relay Word bit name is displayed. Also, if the particular TLED_x target is not set to be a tripping target, (i.e., TxLEDL setting is N), then it is not displayed. *Figure 4.9(d)* shows the differential quantities for the event.

Breaker Monitor

The SEL-487E features an advanced circuit breaker monitor. Select `BREAKER MONITOR` screens from the `MAIN MENU` to view circuit breaker monitor alarm data on the front-panel display. *Figure 4.10* shows the case where Monitor setting EBMON = S T U, i.e., three breakers are enabled. (If only one breaker is enabled [e.g., EBMON = S], then *Figure 4.10(b)* is not shown, and *Figure 4.10(c)* appears directly). Use the navigation pushbuttons to choose between `BREAKER S`, `BREAKER T`, or `BREAKER U`. Press **ENT** to view the selected circuit breaker monitor information, as shown in *Figure 4.10(c)*. The `BKR n ALARM COUNTER` screen displays the number of times the circuit breaker exceeded certain alarm thresholds (see *Circuit Breaker Monitor on page 7.13*).

```
┌────────────────────────────┐
│ MAIN MENU                  │
│ METER                      │
│ EVENTS                     │
│┌──────────────┐            │
││BREAKER MONITOR│           │
│└──────────────┘            │
│ RELAY ELEMENTS             │
│ LOCAL CONTROL              │
│ SET/SHOW                   │
│ RELAY STATUS               │
│ VIEW                       │
│ CONFIGURATION              │
│ DISPLAY TEST               │
│ RESET ACCESS LEVEL         │
│ ONE LINE DIAGRAM           │
└────────────────────────────┘
            (a)
```

```
┌────────────────────────────┐
│ BKR ALARM SUBMENU          │
│┌──────────────┐            │
││BREAKER S     │            │
│└──────────────┘            │
│ BREAKER T                  │
│ BREAKER U                  │
│                            │
│                            │
│                            │
└────────────────────────────┘
            (b)
```

```
┌────────────────────────────┐
│ BKR S ALARM COUNTER        │
│    ALARM          COUNT    │
│ MECH. OP. TIME    0        │
│ ELEC. OP. TIME    0        │
│ BKR INACTIVITY    0        │
│ MOTOR RUNTIME     0        │
│ CURRENT                    │
│ INTERRUPTED       0        │
│                            │
│ LAST RESET:                │
│ 02/03/2008                 │
│                            │
└────────────────────────────┘
            (c)
```

```
┌────────────────────────────┐
│ BKR ALARM COUNTER          │
│                            │
│  NONE OF THE BREAKER       │
│  ALARMS ARE ENABLED.       │
│                            │
│                            │
│                            │
│                            │
└────────────────────────────┘
            (d)
```

Figure 4.10   BREAKER MONITOR Report Screens

Figure 4.10(d) shows the screen when no breaker monitors are enabled
(EBMON = OFF).

View Configuration

You can use the front panel to view detailed information about the configuration
of the firmware and hardware components in the SEL-487E. In the MAIN MENU,
highlight the VIEW CONFIGURATION option by using the navigation pushbuttons
and press ENT. The relay presents seven screens in the order shown in *Figure 4.11*.
Use the navigation pushbuttons to scroll through these screens. When finished
viewing these screens, press ESC to return to the MAIN MENU.

```
┌─────────────────────────┐
│CONFIGURATION INFO      ▲│
│FID=SEL-487E-3-R307-    ▓│
│V0-Z104101-D20130315    ▓│
│                         │
│PART NUMBER: 0487E3X    ┌─────────────────────────┐
│  61112COB4H7444X       │CONFIGURATION INFO      ▲│
│S/N=2008099371          │MAINBOARD:              ▓│
│SELBOOT:                │  CODE FLASH: 12 MB      │
│  BFID=SLBT-4XX-        │  DATA FLASH: 52 MB      │
│  X209-V0-Z001002-      │  RAM:        64 MB     ┌─────────────────────────┐
│  D20150130             │  EEPROM:    128 KB     │CONFIGURATION INFO      ▲│
│  CHECKSUM: 3796        │                         │                        ▓│
└─────────────────────────┘                        │ANALOG BOARD A:         ▓│
          ▼                                         │S: CURRENTS:     5 A     │
                                                    │T: CURRENTS:     5 A     │
                          ▼                         │U: CURRENTS:     5 A    ┌─────────────────────────┐
                                                    │V: VOLTAGE :    67 V    │CONFIGURATION INFO      ▲│
                                                    └─────────────────────────┘                        │
                                                              ▼             │ANALOG BOARD B:         ▓│
                                                                            │W:  CURRENTS:    5 A     │
                                                                            │X:  CURRENTS:    5 A     │
                                                                            │Y1: CURRENTS:    5 A     │
                                                                            │Y2: CURRENTS:    5 A     │
                                                                            │Y3: CURRENTS:    5 A    ▓│
                                                                            │Z:  VOLTAGE :   67 V     │
                                                                            └─────────────────────────┘
                                                                                      ▼
```

```
┌─────────────────────────┐
│CONFIGURATION INFO      ▲│
│                         │
│INTERFACE BOARDS:        │
│ BOARD 1:XX INPUTS       │
│     XX OUTPUTS          │
│ BOARD 2:NOT            ┌─────────────────────────┐
│     INSTALLED          │CONFIGURATION INFO      ▲│
│EXTENDED FEATURES:       │                         │
│ IEC 61850              │COMMUNICATIONS CARD:     │
│                        │ETHERNET                 │
│                        │ PORT A: NA             ┌─────────────────────────┐
│                        │ PORT B: NA             │CONFIGURATION INFO      ▲│
│                        │ PORT C: COPPER         │IF THE CONFIGURATION    ▓│
│                        │ PORT D: COPPER         │IS NOT WHAT YOU          │
└─────────────────────────┘                        │EXPECTED, CONTACT        │
          ▼                                         │SEL FOR ASSISTANCE.      │
                          ▼                         │                         │
                                                    │                         │
                                                    └─────────────────────────┘
                                                              ▼
```

Figure 4.11   VIEW CONFIGURATION Sample Screens

Target LEDs

The SEL-487E gives you at-a-glance confirmation of relay conditions via 24 color-programmable operation and target LEDs, located in the middle of the relay front panel, as shown in *Figure 4.12*. To provide clear visual indication, choose between red and green for the ENABLED and TRIP LED colors. For the remaining LEDs, choose among red, green, or amber.
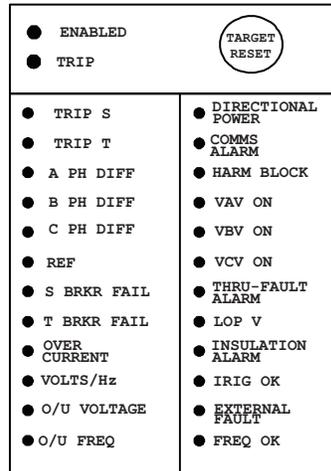
Figure 4.12   Factory-Default Front-Panel Target LEDs

A description of the general operation and configuration of these LEDs is provided in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*. Please note that the SEL-487E has alternate behavior on the T*n*_LED bits: they latch independent of the trip condition.

Table 4.8 shows the LED labels (top to bottom in *Figure 4.12*) and the actual settings. These settings are based on a two-winding transformer with directional overcurrent elements and REF protection enabled. All voltage elements are with reference to PT V.

Table 4.8   LED Settings (Sheet 1 of 2)

LED Label	Settings	Comment
TRIP S	TRIPS	Trip logic asserted, Terminal S
TRIP T	TRIPT	Trip logic asserted, Terminal T
A PH DIFF	87RA OR 87UA	Restraint or unrestraint differential element A
B PH DIFF	87RB OR 87UB	Restraint or unrestraint differential element B
C PH DIFF	87RC OR 87UC	Restraint or unrestraint differential element C
REF	REF51T1	REF Element 1 TOC element timed out
S BRKR FAIL	FBFS	Breaker failure, Terminal S
T BRKR FAIL	FBFT	Breaker failure, Terminal T
OVER CURRENT	50TP1 OR 67TPT1 OR 51T01	Overcurrent
VOLTS/HZ	24D1T OR 24D2T OR 24U1T OR 24U2T	Volts/hertz
U/O VOLTAGE	271P1T OR 591P1T	Voltage Element 1 under- or overvoltage function asserted
U/O FREQUENCY	81D1T	Frequency Element 1 under- or overpower function asserted
DIRECTIONAL POWER	32OPT01 OR 32UPT01	Power Element 1 under- or overvoltage function asserted
COMMS ALARM	NA	Communications Alarm. NA by default. Select Relay Word bits associated with your communications scheme.
HARM BLOCK	87ABK5 OR 87BBK5 OR 87CBK5 OR 87XBK2	Harmonic-block or harmonic-restraint differential element A, B, or C
VAV ON	VAVFM > 55	A-Phase from PT V present

Table 4.8 LED Settings (Sheet 2 of 2)

LED Label	Settings	Comment
VBV ON	VBVFM > 55	B-Phase from PT V present
VCV ON	VCVFM > 55	C-Phase from PT V present
THRU-FAULT ALARM	TFLTALA OR TFLTALB OR TFLTALC	Through-fault element asserted, phase A, B, or C
LOP V	LOPV or LOPZ	Loss-of-potential, PT V or PT Z
INSULATION ALARM	FAA1	Thermal Element 1 aging acceleration factor asserted
IRIG OK	TIRIG	
EXTERNAL FAULT	CON	External fault detected; relay in high-security mode
FREQ OK	FREQOK	Frequency OK

You can reprogram all of these indicators except the **ENABLED** and **TRIP** LEDs to reflect other operating conditions than the factory-default programming described in this section. Settings Tn_LED are SELOGIC control equations that, when asserted during a relay trip event, light the corresponding LED. Parameter n is a number from 1 through 24 that indicates each LED.

Program settings TnLEDL := Y to latch the LEDs when the Tn_LED SELOGIC control equation is true, regardless of the status of TRIP. The LEDs will reset with a subsequent **TRIP** or a **TARGET RESET** via the front panel or the **TAR R** command. When you set TnLEDL := N, the trip latch supervision has no effect and the LED follows the state of the Tn_LED SELOGIC control equation. The relay reports these targets in event report summaries. The asserted and deasserted colors for the LED are determined with settings TnLEDC. Options include red, green, amber, or off.

After setting the target LEDs, issue the **TAR R** command or press the **TARGET RESET** button on the front panel to reset the target LEDs.

Use the slide-in labels to mark the LEDs with custom names. Included on the SEL-400 Series Product Literature DVD is a custom label template to print labels for the slide-in label areas.

Front-Panel Operator Control Pushbuttons

The SEL-487E front panel features large operator control pushbuttons coupled with color-programmable annunciator LEDs for local control. *Figure 4.13* shows this region of the relay front panel with factory-default configurable front-panel label text.
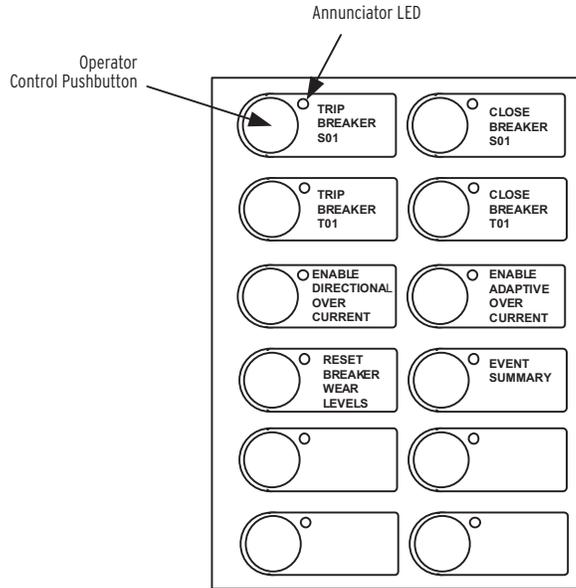
Figure 4.13   Operator Control Pushbuttons and LEDs

Table 4.9 shows the LED labels and the actual settings. These settings are based on a two-winding transformer with directional overcurrent elements and REF protection enabled.

Table 4.9   Pushbutton LED Settings

LED Number	LED Label	Settings	Assert and Deassert Color
1	Trip Breaker S01	NOT 52CLS	GO
2	Trip Breaker T01	NOT 52CLT	GO
3	Enable Directional Overcurrent	PLT03	AO
4	Reset Breaker Wear Levels	RST_BKS OR RST_BKT	AO
5	Blank	NA	AO
6	Blank	NA	AO
7	Close Breaker S01	52CLS	RO
8	Close Breaker T01	52CLT	RO
9	Enable Adaptive Overcurrent	PLT09	AO
10	Event Summary	NA	AO
11	Blank	NA	AO
12	Blank	NA	AO

Press the operator control pushbuttons momentarily to toggle on and off the functions listed adjacent to each LED/pushbutton combination.

There are two ways to program the operator control pushbuttons. The first is through front-panel settings PB*nn*_HMI (*nn* = 1–12). These settings allow any of the operator control pushbuttons to be programmed to display a particular HMI screen category. The HMI screen categories available are Alarm Points, Display Points, Event Summaries, SER, and Bay Control. Front-panel setting NUM_ER allows the user to define the number of event summaries that are displayed via

the operator control pushbutton; it has no effect on the event summaries automatically displayed or the event summaries available through the main menu. Each HMI screen category can be assigned to a single pushbutton.

Attempting to program more than one pushbutton to a single HMI screen category will result in an error. After assigning a pushbutton to an HMI screen category, pressing the pushbutton will jump to the first available HMI screen in that particular category. If more than one screen is available, a navigation scroll bar will be displayed. Pressing the navigation arrows will scroll through the available screens. Subsequent pressing of the operator control pushbutton will advance through the available screens, behaving the same as the **Right Arrow** or **Down Arrow** pushbutton. Pressing the **ESC** pushbutton will return the user to the ROTATING DISPLAY. The second way to program the operator control pushbutton is through SELOGIC control equations, using the pushbutton output as a programming element.

Using SELOGIC control equations, you can readily change the default LED functions. Use the slide-in labels to mark the pushbuttons and pushbutton LEDs with custom names to reflect any programming changes that you make. The labels are keyed; you can insert each Operator Control Label in only one position on the front of the relay. Included on the SEL-400 Series Product Literature DVD is a template for printing slide-in labels. See the instructions included in the Configurable Label kit for more information on changing the slide-in labels.

The SEL-487E has two types of outputs for each of the front-panel pushbuttons. Relay Word bits represent the pushbutton presses. One set of Relay Word bits follows the pushbutton and another set pulses for one processing interval when the button is pressed. Relay Word bits PB1–PB12 are the "follow" outputs of operator control pushbuttons. Relay Word bits PB1_PUL–PB12PUL are the pulsed outputs.

Annunciator LEDs for each operator control pushbutton are PB1_LED–PB12_LED. The asserted and deasserted colors for the LED are determined with settings PB*nn*COL. Options include red, green, amber, or off. You can change the LED indications to fit your specific control and operational requirements. This programmability allows great flexibility and provides operator confidence and safety, especially in indicating the status of functions that are controlled both locally and remotely.

SEL_{OGIC} Factory Setting	Operator Control Pushbutton	LED	Description

PB1_LED
= NOT 52CLS — **● TRIP BREAKER S01** — Press and hold this operator control pushbutton for one second to close OUT101 to trip Circuit Breaker S. The corresponding **TRIP BREAKER S01** LED is illuminated green, indicating that Circuit Breaker S is open based on the status of 52CLS. 52CLS is driven by the 52A_S SEL_{OGIC} equation, which is set to IN101 by default. Therefore, if IN101 is not connected, IN101 = 0, 52CLS = 0, and the LED will stay illuminated. If the LED is off, IN101 is asserted.

PB2_LED
= NOT 52CLT — **● TRIP BREAKER T01** — Press and hold this operator control pushbutton for one second to close OUT102 to trip Circuit Breaker T. The corresponding **TRIP BREAKER T01** LED is illuminated green, indicating that Circuit Breaker T is open based on the status of 52CLT. 52CLT is driven by the 52A_T SEL_{OGIC} equation, which is set to IN102 by default. Therefore, if IN102 is not connected, IN102 = 0, 52CLT = 0, and the LED will stay illuminated. If the LED is off, IN102 is asserted.

PB3_LED
= PLT03 — **● ENABLE DIRECTIONAL OVER CURRENT** — Press this operator control pushbutton to supervise the phase instantaneous overcurrent Level 1, 2, and 3 torque-control elements 67mP1TC, 67mP2TC, and 67mP3TC (m = S, T, U, W, or X). Default Protection Logic settings are programmed to latch Relay Word bit PLT03 with the pulse of this pushbutton. Pressing PB3 again while PLT03 is asserted will reset the latch.

The **ENABLE DIRECTIONAL OVERCURRENT** LED is illuminated amber indicating that PLT03 is asserted.

Note: By default, E50 = OFF and 50mP1P = OFF. These settings must also be enabled to run the 67mP1TC element.

PB4_LED
= RST_BKS OR
RST_BKT — **● RESET BREAKER WEAR LEVELS** — Press this operator control pushbutton to reset (clear) the circuit breaker monitoring data for Breaker m (m = S, T, U, W, or X). By default, Breaker S and T are enabled (BK_SEL = S, T). However, the breaker monitor is disabled by default (EBMON = N), so you must set EBMON to enable the breaker reset logic. Default Protection Logic settings are programmed to latch Relay Word bit PLT04 with the pulse of this pushbutton.

Any condition that results in a true result in the RST_BKS or RST_BKT SEL_{OGIC} equation will reset the latch. Because RST_BKS and RST_BKT are set to PLT04 by default, the latch is reset one processing interval after it is set. However, RST_BKS and RST_BKT remain true for a few seconds until the reset logic clears. The **RESET BREAKER WEAR LEVELS** LED is illuminated amber until the reset logic clears. The LED will not illuminate if EBMON = OFF.

Note: By default, E50 = OFF and 50mP1P = OFF. These settings must also be enabled to run the 67mP1TC element.

PB5_LED = NA
PB6_LED = NA — **●**

PB7_LED
= 52CLS — **● CLOSE BREAKER S01** — Press and hold this operator control pushbutton for one second to close OUT102 to close Circuit Breaker S. The corresponding **CLOSE BREAKER S01** LED is illuminated red, indicating that Circuit Breaker S is closed based on the status of 52CLS. 52CLS is driven by the 52A_S SEL_{OGIC} equation, which is set to IN101 by default. Therefore, if IN101 is not connected, IN101 = 0, 52CLS = 0, and the LED will not illuminate. If the LED is on, IN101 is asserted.

PB8_LED
= 52CLT — **● CLOSE BREAKER T01** — Press and hold this operator control pushbutton for one second to close OUT104 to close Circuit Breaker T. The corresponding **CLOSE BREAKER T01** LED is illuminated red, indicating that Circuit Breaker T is closed based on the status of 52CLT. 52CLT is driven by the 52A_T SEL_{OGIC} equation, which is set to IN102 by default. Therefore, if IN102 is not connected, IN102 = 0, 52CLT = 0, and the LED will not illuminate. If the LED is on, IN102 is asserted.

PB9_LED
= PLT09 — **● ENABLE ADAPTIVE OVER CURRENT** — Press this operator control pushbutton to enable the inverse-time overcurrent torque-control elements 51TCxx (xx = 01–10). Default Protection Logic settings are programmed to latch Relay Word bit PLT09 with the pulse of this pushbutton. Pressing PB9 again while PLT09 is asserted will reset the latch.

The **ENABLE ADAPTIVE OVERCURRENT** LED is illuminated amber indicating that PLT09 is asserted.

Note: By default, E51 = OFF. This setting must also be enabled to run the 51TCxx elements.

PB10LED = NA — **● EVENT SUMMARY** — Press this operator control pushbutton to display the Event Summaries HMI screen. The corresponding LED is not programmed to illuminate when the pushbutton is pressed. If there are no event summaries, the front panel will display the message, "NO EVENT SUMMARIES EXIST."

PB11LED = NA
PB12LED = NA — **●**

Figure 4.14   Factory-Default Operator Control Pushbuttons

One-Line Diagrams

One-line diagrams are fully explained in *Section 5: Control in the SEL-400 Series Relays Instruction Manual*. The SEL-487E supports a three-part one-line diagram: an HV portion selected with the HVMIMIC setting, a transformer section selected with a T_MIMIC setting, and an LV portion selected with the LVMIMIC setting.

By using QuickSet, you can include the bay control screens in the rotating display. Select ONELINE (found under Front Panel settings), selectable screens, as shown in *Figure 4.15*.
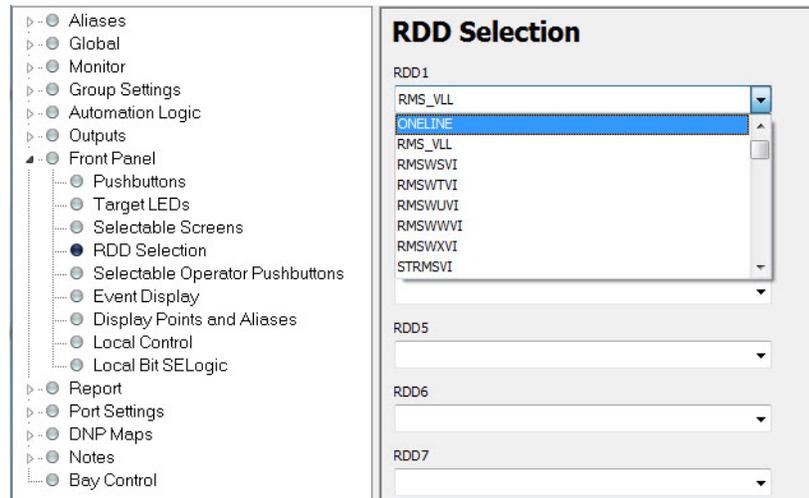
Figure 4.15   Bay Control Screen Selected for Rotating Display

You can also configure an HMI pushbutton to give you direct access to the bay control screen. *Figure 4.16* shows an example of how to configure HMI Pushbutton 1 to provide this access by selecting the BC option from the drop-down menu.
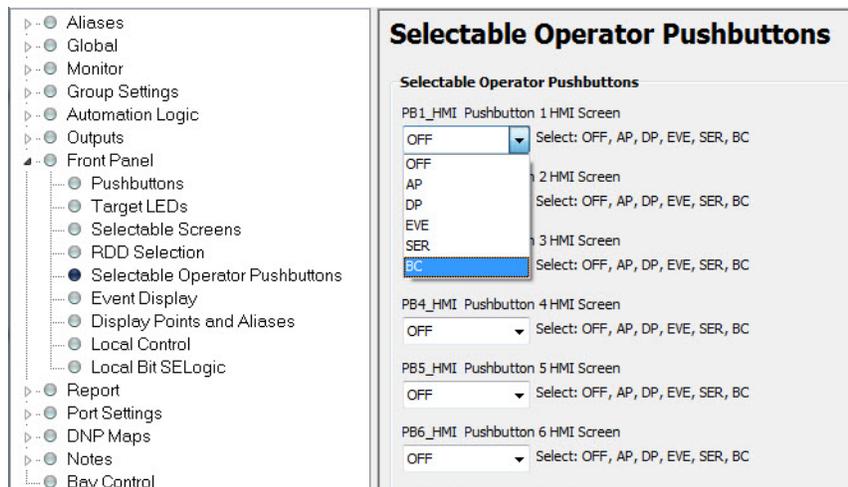
Figure 4.16   Configuring PB1_HMI for Direct Bay Control Access

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Protection Functions

This section provides a detailed explanation of the SEL-487E relay protection functions. Each section provides an explanation of the function, along with a list of the corresponding settings and Relay Word bits. Logic diagrams and other figures are included.

Functions discussed in this section are listed below.

➤ *Close Logic on page 5.138*

➤ *Loss-of-Potential (LOP) Logic on page 5.139*

➤ *Circuit Breaker Status on page 5.142*

Potential Transformer (PT) Ratio Settings With LEA Inputs

PT Ratio Setting Adjustments

The SEL-487E can be ordered with different secondary input voltage configurations. Low-Energy Analog (LEA) voltage inputs are suitable for C37.92-compliant high-impedance sensors, such as capacitive voltage dividers and resistive voltage dividers (see *Figure 5.1*).
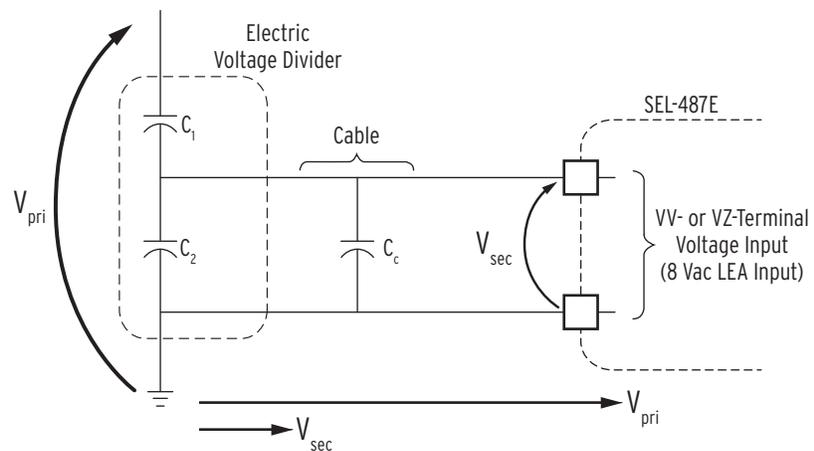
Figure 5.1   Low-Energy Analog (LEA) Voltage Sensor

Derive PT Ratio Settings for 8 Vac LEA Voltage Inputs

Refer to *Figure 5.1*.

V_{pri} / V_{sec} = true ratio of voltage divider when connected to the VV-terminal or VZ-terminal (8 Vac LEA) voltage inputs.

The SEL-487E sees 8 Vac on the VV-terminal or VZ-terminal (8 Vac LEA) voltage inputs as 300 Vac. To realize accurate primary voltage metering, the corresponding potential transformer ratio settings (PTRV or PTRZ), are set as follows:

PTRV or PTRZ = V_{pri} / V_{sec} • (8/300)

For example, if an LEA sensor has a PTR of 1400:1,

PTRV or PTRZ = 1400 • (8/300) = 37.3

PT Ratio = 37.3

Voltage-Related Settings and LEA Inputs (Group Settings)

Study *Figure 5.1* in preparation for *Example 5.1*.

When the V-terminal voltage inputs are 8 Vac LEA inputs, any voltage-related setting tied to the V-terminal voltage inputs is adjusted by a factor of 300/8.

Example 5.1   Voltage Setting Conversion to 300 V Base

A voltage divider (10000 ratio) is connected between a 12.47 kV system (7.2 kV line-to-neutral) and the LEA inputs.

7200 V / 10000V = 0.72 V
(actual voltage divider output to the 8 Vac LEA inputs; 8 V base)

0.72 V • (300/8) = 27 V
(the relay thinks it is looking at 27 V on a 300 V base, not 0.72 V on an 8 V base)

27 V is the nominal adjusted secondary voltage—adjusted by the 300/8 factor from an 8 V base to a 300 V base. For this same example, if a 0.8 V output of the 8 Vac LEA (8 V base) is deemed an overvoltage condition, then an overvoltage element pickup setting (e.g., 59P1P1) could be set at 59P1P1 := 0.8 V • (300/8) = 30 V (300 V base).

LEA Ratio Correction Factors

In the SEL-487E with LEA voltage inputs, RCF values for V terminals (Global settings VAVRCF, VBVRCF, and VCVRCF) are applied to respective voltage inputs VAV, VBV, and VCV, and the RCF values for VZ terminals (Global settings VAZRCF, VBZRCF, and VCZRCF) are applied to respective voltage inputs VAZ, VBZ, and VCZ. The resultant secondary voltages from these voltage inputs are normalized by the RCF values. These normalized secondary voltages are used throughout the SEL-487E.

Voltage Ratio Correction Factors for V- and Z-Terminal Voltage Inputs (Global Settings)

Use the VAVRCF, VBVRCF, and VCVRCF ratio correction factor Global settings for the V-terminal voltage inputs (VAV, VBV, and VCV, respectively) when they are ordered as LEA voltage inputs (see *Figure 5.1*). Use the VAZRCF, VBZRCF, and VCZRCF ratio correction factor Global settings for VZ-terminal voltage inputs (VAZ, VBZ, and VCZ, respectively) when they are ordered as LEA voltage inputs (see *Figure 5.1*). Ratio correction factor (RCF) settings compensate for irregularities (on a per-phase basis) of voltage dividers connected between the primary voltage system and the LEA inputs. The derivation of the RCF value for a voltage divider for a particular phase is defined as follows:

$$RCF = \frac{\text{true ratio}}{\text{marked ratio}}$$

$$= \frac{(V_{pri}/V_{sec})}{PTR_{LEA}}$$

$$= \frac{V_{pri}}{V_{sec} \cdot PTR_{LEA}}$$

Equation 5.1

where:

V_{pri} = test voltage applied to the primary side of the voltage divider

V_{sec} = resultant voltage measured on the secondary side of the voltage divider

true ratio = V_{pri} / V_{sec}

marked ratio = PTR_{LEA}

= effective nominal potential transformer (PT) ratio of the voltage divider connected between the primary voltage system and the LEA input.

The marked ratio of the voltage divider (PTR_{LEA}) is always provided by the manufacturer and often the per-phase RCF values are also provided.

If the voltage divider is perfect, then,

$V_{\text{pri}} / V_{\text{sec}} = \text{PTR}_{\text{LEA}}$ and RCF = 1.000

Therefore, the measured voltage divider performance equals the marked ratio of the voltage divider, as given by the manufacturer. But such perfect conditions are usually not the case.

If the voltage divider is putting out more voltage (V_{sec}) than nominally expected for an applied voltage input (V_{pri}), then,

$V_{\text{pri}} / V_{\text{sec}} < \text{PTR}_{\text{LEA}}$ and RCF < 1.000

An example of an RCF value less than 1.000 is found in *Example 5.2*. In this example, setting VBVRCF := 0.883 brings down the too-high voltage on voltage input VBV (0.82 V is brought down to nominal 0.72 V).

If the voltage divider is putting out less voltage (V_{sec}) than nominally expected for an applied voltage input (V_{pri}), then,

$V_{\text{pri}} / V_{\text{sec}} > \text{PTR}_{\text{LEA}}$ and RCF > 1.000

Example 5.2   Normalizing Voltages With Ratio Correction Factors

A voltage divider is connected to the 8 Vac LEA voltage inputs (see *Figure 5.1*). The RCF values per phase for the voltage divider are as follows:

VAVRCF := **1.078**   (voltage input VAV)

VBVRCF := **0.883**   (voltage input VBV)

VCVRCF := **1.112**   (voltage input VCV)

The marked ratio of the voltage divider is as follows:

PTRLEA = 10000

What are the true ratios of each phase of the voltage divider?

true ratio (for a given phase) = $V_{\text{pri}} / V_{\text{sec}}$

V_{pri} and V_{sec} are measured in manufacturer tests to derive RCF values as shown in *Equation 5.1* and accompanying explanation. From *Equation 5.1* we obtain the following:

RCF • $\text{PTR}_{\text{LEA}} = V_{\text{pri}} / V_{\text{sec}}$ = true ratio

1.078 • 10000 = 10780 (true ratio for voltage input VAV)

0.883 • 10000 = 8830 (true ratio for voltage input VBV)

1.112 • 10000 = 11120 (true ratio for voltage input VCV)

Note that these true ratios vary from 8830 to 11120, while the marked ratio of the voltage divider is 10000.

Consider what is happening in *Example 5.2*. First, assume the primary voltage (V_{pri}) is the same magnitude for each phase. When this primary voltage is run through the respective true ratios, the secondary voltage outputs vary widely. Presuming primary voltage of 12.47 kV (7.2 kV line-to-neutral), the resultant secondary voltages are listed as follows:

7200 V / 10780 = 0.67 V (true secondary voltage to voltage input VAV)

7200 V / 8830 = 0.82 V (true secondary voltage to voltage input VBV)

7200 V / 11120 = 0.65 V (true secondary voltage to voltage input VCV)

Note that the true secondary voltages to voltage inputs VAV and VCV are running low (below normalized secondary voltage 0.72 V = 7200 V / 10000), while the voltage to voltage input VBV is running high (above normalized secondary voltage 0.72 V). But the RCF values adjust these true secondary voltages to normalized secondary voltages:

0.67 V • 1.078 = 0.72 V (normalized voltage from voltage input VAV)

0.82 V • 0.883 = 0.72 V (normalized voltage from voltage input VBV)

0.65 V • 1.112 = 0.72 V (normalized voltage from voltage input VCV)

Again, the normalized secondary voltage (0.72 V) is the same for all three phases in this example, because the primary voltage is assumed to be the same magnitude for each phase (7200 V). These normalized secondary voltages are used throughout the SEL-487E. The true secondary voltages cannot be seen (via the SEL-487E) unless the RCF values are set to unity (RCF = 1.000).

Group setting PTRV is the potential transformer ratio from the primary system to the SEL-487E VV-Terminal voltage inputs. Group setting PTRZ is the potential transformer ratio from the primary system to the SEL-487E VZ-terminal voltage inputs. To make these settings for traditional 300 Vac voltage inputs is straightforward.

For example, on a 12.47 kV phase-to-phase primary system with wye-connected 7200:120 V PTs, the correct PTRV or PTRZ setting is 7200 / 120 = 60.00.

RCF Impact on COMTRADE Files

Relay event recordings in the COMTRADE format apply the RCF as a multiplier to the incoming low-level analog signal. The maximum range of the LEA input is 8 V_{rms}, which is scaled in relay firmware to represent 300 V_{rms} secondary voltage at the relay.

The COMTRADE recordings used by the relay have a maximum limit of 350 V_{rms} (495 V_{pk}). Because the RCF is a multiplier applied to the LEA input measurement, the RCF is present in the voltage values shown in the COMTRADE file, and a large RCF could have the effect of driving the COMTRADE voltage values to their maximum value even though the applied LEA input is below this level.

If voltage waveform clipping in the COMTRADE event report is apparent to the relay at nominal LEA voltage inputs, check the affected phase ratio correction factor. If the LEA scaling factor multiplied by the RCF and the LEA voltage input exceeds 350 V_{rms}, the COMTRADE waveform will be clipped.

Example 5.3

LEA voltage input (V_{LEA}) = 6 V_{rms}

LEA Scaling Factor (K_{LEA}) = 300/8

Phase RCF (RCF) = 1.5

Maximum COMTRADE Voltage (V_{max}) = 350 V_{rms}

$V_{LEA} \bullet K_{LEA} \bullet RCF < V_{max}$

6 • 300/8 • 1.5 = 337.5 V_{rms}

This value will display in COMTRADE correctly.

Example 5.4

LEA voltage input (V_{LEA}) = 7 V_{rms}

LEA Scaling Factor (K_{LEA}) = 300/8

Phase RCF (RCF) = 1.5

Maximum COMTRADE Voltage (V_{max}) = 350 V_{rms}

$V_{LEA} \bullet K_{LEA} \bullet RCF < V_{max}$

7 • 300/8 • 1.5 = 393.75 V_{rms}

This value will appear as a clipped waveform in the COMTRADE event file. Relay metering and protection will continue to work properly. Only the COMTRADE file is affected.

Note that the RCF is typically used on a per-phase basis to fine tune the relay measurement systems to small variations in secondary voltage from the voltage sensor. RCF correction values outside of the range of 0.800 to 1.200 are not typical. If the RCF does exceed these ranges on all three voltage phases, consider changing the PTR for the voltage input to compensate for high or low RCF values. If abnormally high RCF factors are present on only one or two voltage phase inputs, check the LEA sensor wiring and functionality as this may indicate a problem with the field device.

LEA ratio correction factor (RCF) settings are only available if the LEA option is supported by the relay part number.

Inverting Polarity of Current and Voltage Inputs

The relay can change the polarity of the CT and PT inputs. This ability allows the user to change CT and PT polarity digitally to correct for incorrect wiring to the input on the back of the relay. You can change the polarity on a per-terminal or per-phase basis, but you must practice extreme caution when using this function. The change of polarity applies directly to the input terminal and is carried throughout all calculations, metering, and protection logic.

The EINVPOL setting is always hidden on the front-panel HMI.

Table 5.1   Inverting Polarity Setting

Setting	Prompt	Range	Default Value
EINVPOL	Enable Invert Polarity (Off or combo of terminals)	OFF, Combo of S[p][a], T[p], U[p], W[p], X[p], Y[3][b], V[p] and Z[p]	OFF

[a] Where [p] = A, B, C. Entering a terminal without specifying a phase designation applies the setting to all phases of that terminal. For example, EINVPOL := SA,SB,X inverts the polarity of the A- and B-Phases for Terminal S and all phases for Terminal X.

[b] Where [3] = 1, 2, 3. For example, EINVPOL := Y1, Y3 inverts the polarity of the Y1 and Y3 terminals.

If redundant entries of terminals are used, such as W, WA or X, XC, the relay displays the following error message: `Redundant entries for terminal [m]`.

Inverse Polarity in Event Reports

In COMTRADE event reports, terminals that have EINVPOL enabled do not show the polarity as inverted. The COMTRADE must display the values as they are applied to the back of the relay. This also ensures that when you use an event playback, the setting is applied to the signals coming in the back of the relay and recreates the event properly.

Compressed event reports (CEV), show the polarity as inverted. The CEV displays the analogs as the relay uses them in processed logic; therefore, the inverted polarity is shown.

Transformer Differential Protection Overview

Power transformers need protection from three types of faults: phase-to phase faults, phase-to-ground faults, and turn-to-turn faults. To provide overall transformer protection for all fault types, fault levels, and operating conditions, the SEL-487E offers three different types of differential protection elements:

➤ Phase percentage-restrained differential elements (87R)

➤ A negative-sequence percentage-restrained differential element (87Q)

➤ Unrestrained phase differential elements (87U)

The phase percentage-restrained differential elements use an adaptive-slope percentage differential characteristic for increased security and sensitivity. To add security during transformer inrush conditions, the relay provides harmonic blocking, harmonic restraint, or both. Second and fourth harmonics provide security during energization, and fifth-harmonic blocking provides security for overexcitation conditions. In the event of low harmonic content during energization, which can occur with new transformer core materials, the waveshape-based inrush detection logic provides security during energization where the traditional harmonic-blocking and restraint methods may fail. An optional unblocking logic, which uses a waveshape-based bipolar differential overcurrent element, quickly and securely detects internal faults and cancels the inrush blocking action, improving element operating times, especially for faults occurring during energization.

The negative-sequence differential element provides sensitive protection for low-magnitude faults such as turn-to-turn faults. The sensitivity of the phase-percentage differential element is tied to the transformer loading, making turn-to-turn

faults particularly difficult to detect. The negative-sequence differential element is unaffected by load and, therefore, very sensitive to the small unbalance caused by turn-to-turn faults regardless of operating conditions. The negative-sequence differential element requires appropriate blocking during energization or overexcitation conditions. The relay provides the option to block the element through use of either harmonic- or waveshape-based inrush detection methods, and provides the option to cancel the inrush blocking action upon assertion of the waveshape-based unblocking logic.

The unrestrained differential elements are intended to operate very quickly for faults with high differential current, occurring above the worst-case inrush current magnitude. The SEL-487E provides three different types of unrestrained differential elements. The first is a filtered unrestrained element that operates on filtered differential currents. The second is a raw unrestrained element that operates on raw (unfiltered) differential current and can operate substantially faster than the filtered unrestrained element. The third is a waveshape-based bipolar differential overcurrent element that is significantly more sensitive than the other two elements because it differentiates between inrush current and internal fault current. The SEL-487E allows you to enable any combination of these three unrestrained differential elements.

Differential-Element Speed and Security Features

In general, the differential elements in the relay use filtered and unfiltered (raw) analog quantities. *Figure 5.2* illustrates the two analog quantity chains for each terminal current. Both chains process only the current inputs from those terminals that you select via Group setting E87T*m*. After dividing each input current with the applicable TAP*m* value to convert from ampere values to per unit, the relay compensates each current channel according to the T*m*CTC Group setting. Group setting T*m*CTC uses 3x3 matrix compensation to provide round-the-clock angle compensation for each current input. In this way, you can connect all CTs in wye regardless of transformer winding configurations. As indicated in *Figure 5.2*, the filtered differential elements (i.e., the phase-restrained differential elements, negative-sequence differential element, and the filtered unrestrained differential elements) use the filtered analog quantity chain. The Internal and External Fault Detection Logic uses the unfiltered analog quantity chain and serves as the data source of the waveshape-based logic and the raw unrestrained differential elements.
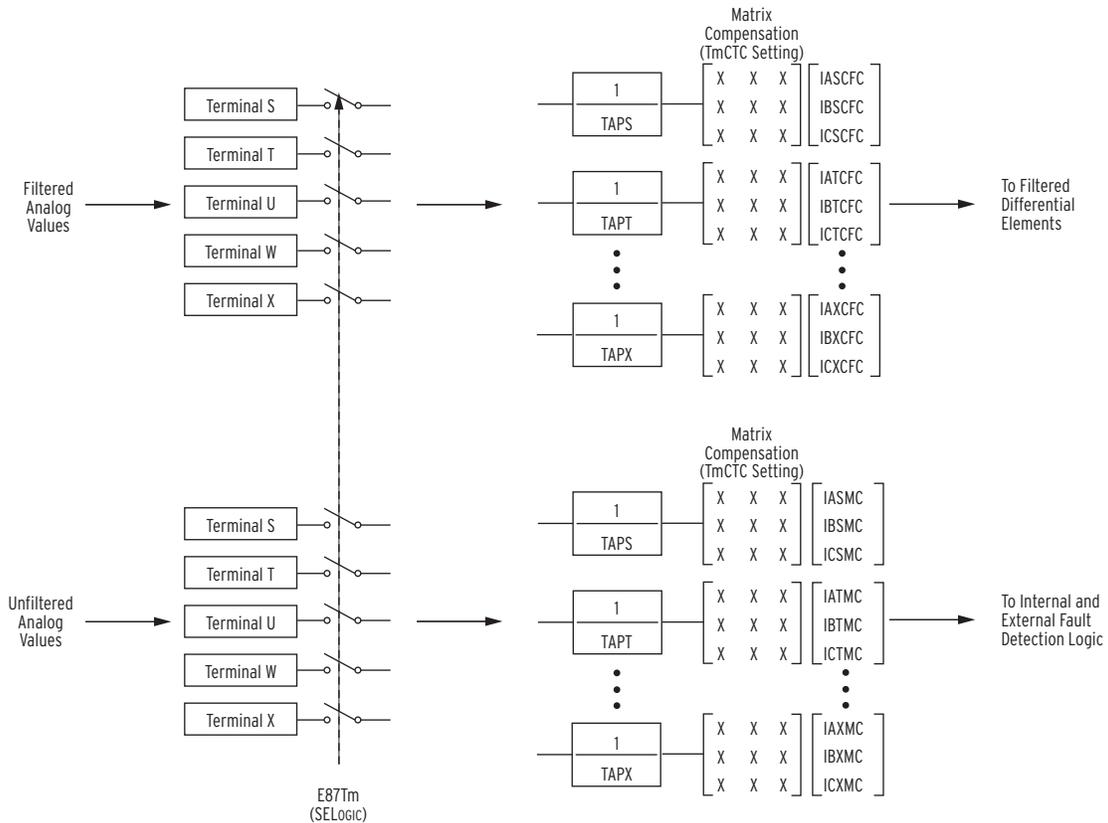
Figure 5.2   Terminal Selection and Matrix Compensation

Adaptive-Slope Phase Percentage-Restrained Characteristic

To provide increased security and sensitivity for the phase percentage-restrained differential elements, the relay employs an adaptive-slope characteristic that uses a more secure slope when there is danger of CT saturation during an external fault and that uses a more sensitive slope for all other operating conditions. The relay forms filtered and unfiltered phase-restrained differential elements by using operate and restraint quantities from the appropriate analog quantity data chain (see *Figure 5.2*). *Figure 5.3* illustrates the characteristic of the A-Phase filtered differential element as a straight line through the origin of the form:

$$IOPA = k \cdot SLPc \cdot IRTA$$

Equation 5.2

NOTE: Factor *k* is 0.5 in the SEL-387 and SEL-587 relays. Take this into consideration when calculating the slope setting. Also see *SLP1, SLP2 (Restraint Slope Percentage) on page 5.28*.

where:

IOPA = filtered operating current

IRTA = filtered restraint current

c = 1 or 2 (1 if in normal mode, 2 if in high-security mode)

SLP1 = initial slope, beginning at origin

SLP2 = second slope, also starts at the origin

k = 1
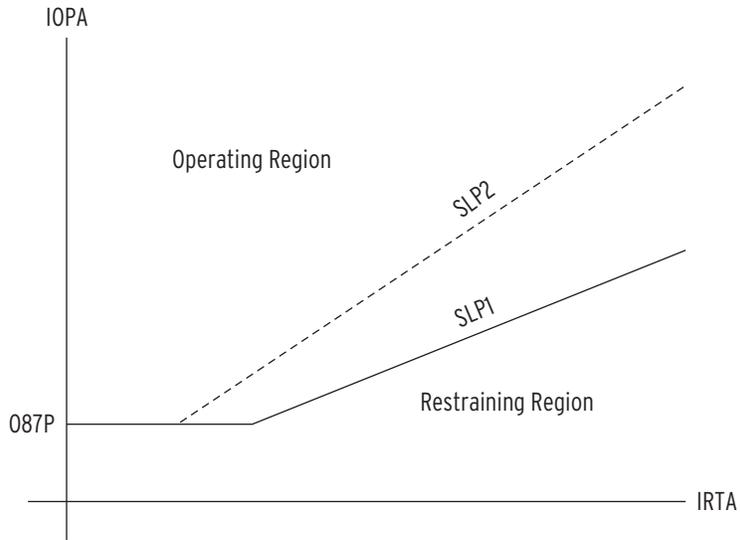
Figure 5.3 Filtered Differential-Element Characteristic

NOTE: The relay does not block for external faults, but changes to high security.

For operating quantities (IOPA) exceeding the threshold level O87P and falling in the operate region of *Figure 5.3*, the filtered differential element issues an output. There are two slope settings: Slope 1 (SLP1) and Slope 2 (SLP2). Slope 1 is effective during normal operating conditions, and Slope 2 is effective when the fault detection logic detects an external fault condition.

Internal and External Fault Detection Logic
Internal Fault Detection Logic

Figure 5.4 shows logic that uses unfiltered (raw) quantities to detect an A-Phase internal fault (IFTLA) and external fault (CONA). Other phases have similar logic. Elements in the fault detection logic use unfiltered, compensated per-unit currents to calculate a raw restraint quantity, IRTRA, and a raw operating quantity, IOPRA, according to *Equation 5.3* and *Equation 5.4*.

$$IOPRA = |\Sigma IAmMC|$$

Equation 5.3

$$IRTRA = \Sigma |IAmMC|$$

Equation 5.4

where:

IA*m*MC = A-Phase unfiltered, compensated per-unit current
(m = S, T, U, W, X)
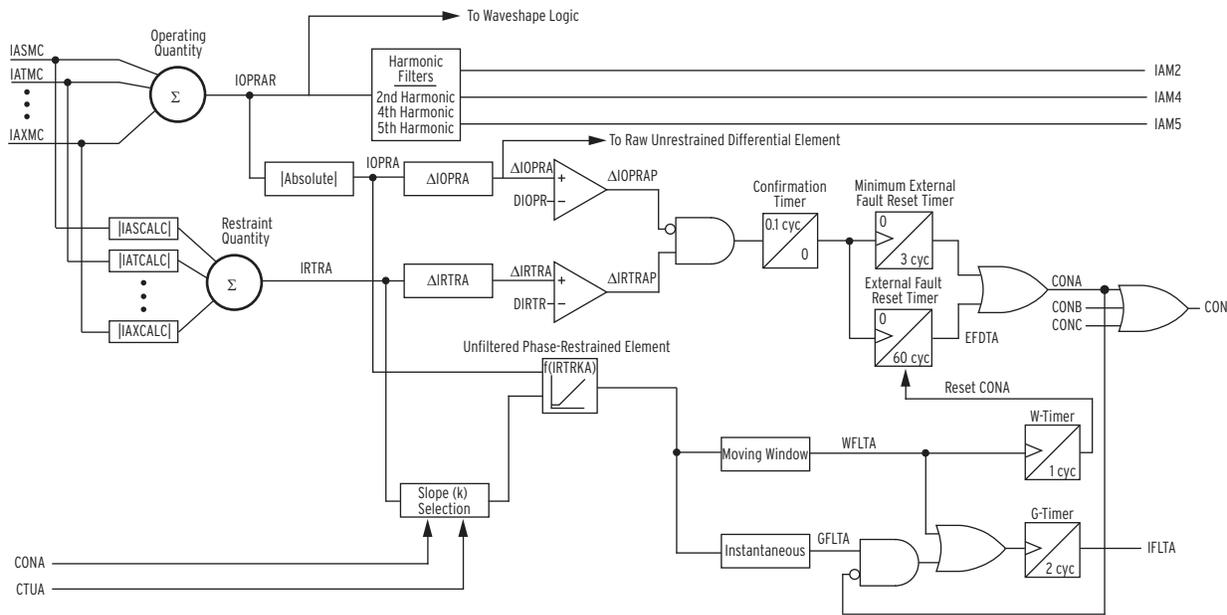
Figure 5.4   A-Phase Internal and External Fault Detection Logic and Harmonic Filtering

Both fault detection logics use the principle that operating and restraint currents increase simultaneously for internal faults, but that only the restraint current increases for external faults (if there is no CT saturation). By comparing the change in operating current (ΔIOPRAP) to the change in restraint current (ΔIRTRAP), the relay distinguishes between external and internal faults. In particular, if ΔIRTRAP asserts, and ΔIOPRAP remains deasserted for 0.1 cycles, then the relay declares the fault as external and asserts Relay Word bit CONA. Conversely, if both ΔIRTRAP and ΔIOPRAP assert, then the relay does not assert CONA, ruling out an external fault condition.

Two further measurements (instantaneous fault detection and moving window fault detection) ensure that the relay identifies an internal fault correctly. The output from the unfiltered phase percentage-restrained differential element forms the input into both fault detection modules.

The moving window fault detection logic declares an internal fault when differential current still exists on a consecutive measurement one-half cycle after the unfiltered phase percentage-restrained differential element asserts. Relay Word bit WFLTA asserts when the moving window fault detector logic declares an internal fault.

When an internal fault is declared, the expected behavior of the instantaneous and moving window fault detection along with the G-Timer cause the IFLTA Relay Word bit to assert for two cycles then deassert for approximately one half-cycle before reasserting again for two cycles (see *Figure 5.4*).

As shown in *Figure 5.18*, IFLTA contributes to the A-Phase percentage-restrained differential elements (87AHB, 87AHR). Note that even though the expected behavior of IFLTA causes the 87AHB and 87AHR Relay Word bits to deassert momentarily, it does not affect the speed of protection. Once a Relay Word bit assigned to the trip equation asserts, the trip result is sealed in and does not reset. The two-cycle window is sufficient time for the relay to detect the fault, issue a trip, and seal in the trip signal. To prevent a chattering Relay Word bit from filling up the SER, set Enable SER Delete (ESERDEL) to Y for automatic removal of chattering SER points. For more information on ESERDEL, see *Setting SER Points on page 9.30 in the SEL-400 Series Relays Instruction Manual.*

Alternatively, include the 87AHB, 87BHB, 87CHB, 87AHR, 87BHR, and 87CHR Relay Word bits in the event report digitals list and omit them from the SER.

If surge (lightning) arresters are installed within the differential zone, a path to ground exists when these devices conduct, resulting in operating current in the differential elements. The instantaneous fault detection logic qualifies the operating current for a power system quarter cycle to differentiate between operating current resulting from surge arrester conduction and operating current because of internal faults. Relay Word bit GFLTA asserts when the instantaneous fault detection logic detects an internal fault.

External Fault Detection Logic

Relay Word bit CONA changes the operating mode of the relay to high-security mode, primarily to avoid misoperation resulting from CT saturation for external faults. High security causes the following in the relay:

➤ Slope *k* selection changes from Slope 1 to Slope 2 for both the unfiltered and filtered phase percentage-restrained differential elements (see *Figure 5.4* and *Figure 5.18*).

➤ Delay time of the adaptive security timer increases (see *Figure 5.18*).

While the high-security mode provides satisfactory security for through faults, this mode can cause the relay to operate slower for evolving faults (where the fault starts as an external fault and then develops into an internal fault).

To avoid this delayed tripping, the relay uses two timers (minimum external fault reset timer and external fault reset timer) and CT unsaturate logic to switch the relay back to normal operating mode as soon as possible. The minimum external fault reset timer resets after three cycles, ensuring that the relay stays in the high-security mode for at least three cycles after it detects an external fault. The external fault reset timer resets after 60 cycles, or when the Reset CONA signal asserts. Finally, when there is no danger of CT saturation following the external fault, Relay Word bit CTUA asserts and resets the internal fault detector logic to normal mode (see *Figure 5.4*), which resets the slope latch and causes the unfiltered phase-restrained differential elements to use the Slope 1 value. However, the filtered phase-restrained differential element resets the slope latch and returns to using the Slope 1 value only when CONA resets (see *Figure 5.18*).

Figure 5.4 also shows the filter function block where the relay calculates the magnitudes of the various harmonics for use in the harmonic-blocking, harmonic-restraint, and overexcitation functions.

Inrush and Overexcitation Blocking Logic
Harmonic Logic

NOTE: For more information regarding inrush currents, refer to the technical paper, *Transformer Modeling as Applied to Differential Protection* by Stanley E. Zocholl, Armando Guzmán, and Daqing Hou (available at selinc.com).

The second- and fourth-harmonic content present in the differential current is used to block the differential (harmonic-blocking method) or to boost the restraining signal (harmonic-restraint method) during inrush conditions to prevent misoperation, and the fifth-harmonic differential current is used to prevent misoperation during transformer overexcitation. *Figure 5.4* shows the filter function block where the relay calculates the various harmonic magnitudes of the differential current.

Figure 5.5 illustrates the logic for the A-Phase harmonic-based inrush and overexcitation functions.
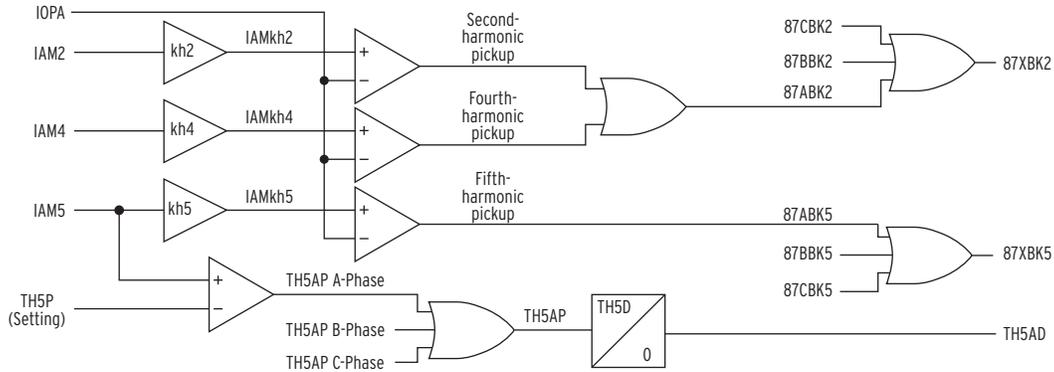
where:
kh2 = the second-harmonic setting 100/PCT2
kh4 = the fourth-harmonic setting 100/PCT4
kh5 = the fifth-harmonic setting 100/PCT5

Figure 5.5   A-Phase Harmonic Logic

In *Figure 5.5*, the relay scales the magnitudes of the harmonic quantities (IAM2, IAM4, and IAM5) by the per-unit value of their respective harmonic percentage settings (PCT2, PCT4, and PCT5). The scaled second- and fourth-harmonic magnitudes (IAMkh2 and IAMkh4, respectively) are used by the harmonic-restrained differential element (see *Equation 5.7* and *Figure 5.18*). For the harmonic-blocking functions, the relay compares each scaled harmonic magnitude against the fundamental operate current, IOPA (*Figure 5.18*), and asserts the appropriate binary signals (second-, fourth-, or fifth-harmonic pickup) when the harmonic content exceeds the settings.

When either (or both) the A-Phase second- or fourth-harmonic content exceeds the setting, Relay Word bit 87ABK2 asserts. The harmonic-blocked differential elements and the negative-sequence differential element operate in a cross-blocking mode and, therefore, use output 87XBK2, which is the OR combination of the second- or fourth-harmonic blocking bits from all three phases (see *Figure 5.18* and *Figure 5.22*). When the A-Phase fifth-harmonic content exceeds the fundamental operate current, Relay Word bit 87ABK5 asserts and prevents the A-Phase percentage-restrained elements from misoperating during an overexcitation condition (see *Figure 5.18*). The fifth-harmonic cross-blocking Relay Word bit, 87XBK5, is used to properly block the negative-sequence differential element during overexcitation (see *Figure 5.22*).

An overexcitation alarm function compares the fifth harmonic against a fifth-harmonic alarm threshold (TH5P) and uses an adjustable timer (TH5D). This threshold and timer may be useful for transformer applications in or near generating stations.

Waveshape-Based Inrush Detection Logic

Although inrush currents are typically rich in even-numbered harmonics (the second harmonic in particular) some power transformers, especially new designs with the core material improved for lower losses, produce low levels of these harmonics. These low harmonic levels can challenge the effectiveness of traditional harmonic-blocking and harmonic-restraint schemes.

The waveshape-based inrush detection element addresses inrush conditions that contain low second and fourth-harmonic content by using a dwell-time algorithm. The magnetizing currents of a three-phase, three-legged transformer exhibit intervals where the currents are both small and flat (see *Figure 5.6*), called dwell-times, which coincide with one another in each phase. The dwell-

time algorithm uses this small and flat interval to detect transformer inrush and supervise the percentage-restrained differential elements. For three-phase transformers built from single-phase units or four- or five-legged cores, the dwell times still exist in each phase but do not necessarily coincide. Thus the dwell-time algorithm requires information about the transformer construction, established via the 87CORE setting before it can activate the appropriate logic.
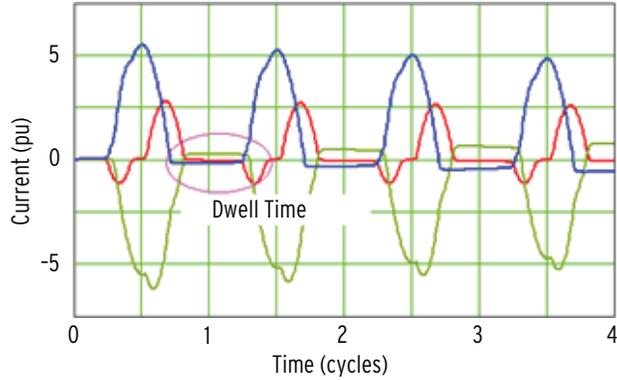
Figure 5.6   Dwell-Time Intervals in the Inrush Currents

Dwell-Time Algorithm for Three-Legged, Three-Phase Transformers

Setting 87CORE = T enables the dwell-time algorithm for three-legged, three-phase transformers.

The dwell-time logic first performs a supervisory check whereby it confirms that there is sufficient differential current to activate the dwell-time algorithm. If either the filtered A-Phase operate current or the negative-sequence operate current is above half of their respective pickup thresholds, 87T_MA asserts to indicate sufficient operate current magnitude, as shown in *Figure 5.7*. If any phase has sufficient operate current, the three-legged operate current magnitude check, 87T_M, asserts. Assertion of 87T_M is a required condition for operation of the three-legged dwell-time logic, as shown in *Figure 5.8*.
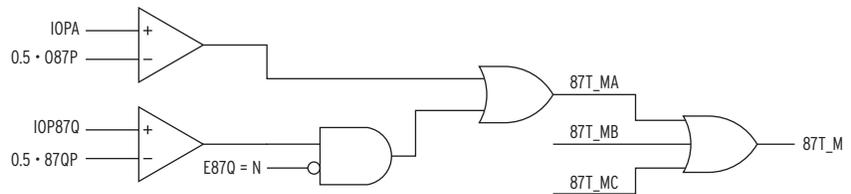
Figure 5.7   Sufficient Operate Current Check
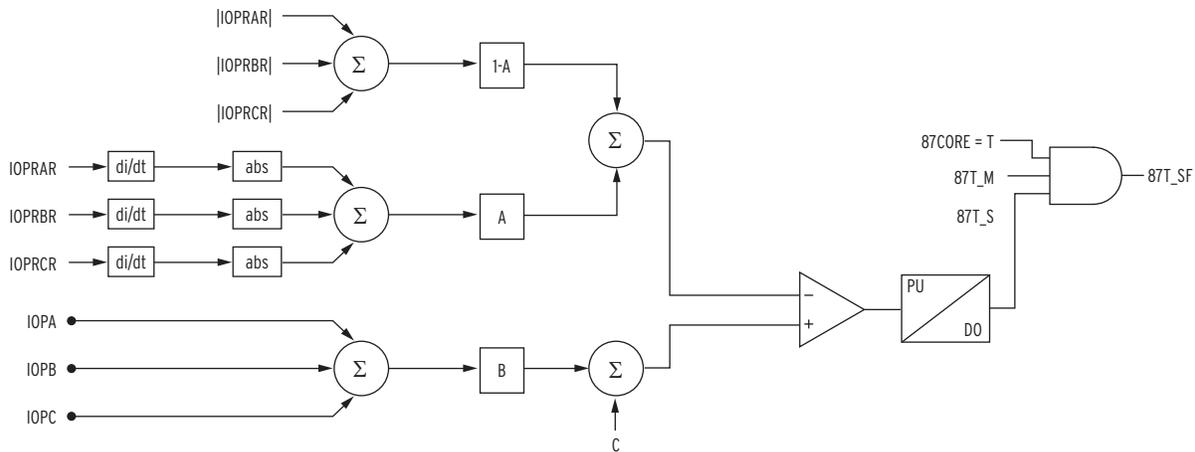
Figure 5.8   Waveshape Dwell-Time Inrush Detection Logic for Three-Legged, Three-Phase Transformers

The three-legged dwell-time algorithm executes on a sample-by-sample basis and works as follows:

➤ The relay adds the absolute values of the raw (unfiltered) differential current in all three phases (IOPRAR, IOPRBR, and IOPRCR) (see *Figure 5.4*) to form a portion of the dwell-time identifier signal. During inrush conditions, this signal is low for the duration of the dwell-time periods because all three differential currents exhibit their dwell periods at the same time.

➤ To provide resiliency against gradual CT saturation that may occur during inrush, the relay forms a second measure of the dwell-time pattern by summing the absolute values of the derivatives of the raw differential currents. Because all three inrush currents are coincidentally flat during the dwell-time periods, this signal is low during the dwell-time periods of the inrush currents.

➤ The two portions of the dwell-time identifier signal are multiplied by a scaling factor and added together. The resulting signal is low during the dwell-time periods, high during internal faults, and resilient to gradual CT saturation during inrush.

➤ The relay creates an adaptive threshold by taking a fraction of the three-phase sum of the filtered operating currents (IOPA, IOPB, and IOPC) (see *Figure 5.18*). A comparator checks if the level of the dwell-time identifier signal is below the adaptive threshold for the duration of the pickup time (PU). If so, then 87T_S asserts, indicating that the relay has identified an inrush condition through use of waveshape recognition. The dropout time (DO) is set for one power system cycle and is necessary to keep 87T_S continually asserted until the dwell-time of the next subsequent cycle, maintaining reliable inrush detection.

Dwell-Time Algorithm for Single-Phase Units, or Four- or Five-Legged Three-Phase Transformers

When a three-phase transformer is constructed with single-phase transformers or with a four- or five-legged core, the individual phase dwell-time intervals are not aligned in time. In a transformer built with single-phase units or with a four- or five-legged core, the flux in each core can be independent, meaning the three cores go in and out of saturation independently. Therefore, one instance of the dwell-time algorithm is required for each phase of the transformer.

Setting 87CORE = S segregates the inrush detection dwell-time logic into individual phases, such as in the A-Phase logic shown in *Figure 5.9*. The logic is identical to the three-legged core logic shown in *Figure 5.8*, except that it only uses a single-phase current rather than a three-phase sum.
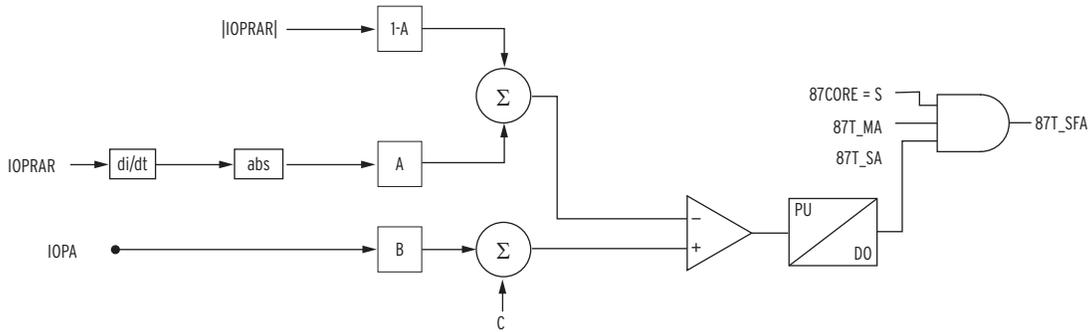
Figure 5.9   Waveshape Dwell-Time Inrush Detection Logic for A-Phase

NOTE: For a more detailed discussion and analysis of the waveshape inrush detection method, refer to the technical paper, *Low Second-Harmonic Content in Transformer Inrush Currents – Analysis and Practical Solutions for Protection Security* by Steven Hodder, Bogdan Kasztenny, Normann Fischer, and Yu Xia (available at selinc.com).

Figure 5.10 shows the waveshape-based inrush blocking logic used by the differential elements. If the logic identifies magnetizing inrush current through use of waveshape recognition, the 87WB Relay Word bit asserts. The logic uses phase-specific Relay Word bits (87WBA, 87WBB, and 87WBC) to block the percentage-restrained differential elements, as shown in *Figure 5.18*. The negative-sequence differential element is blocked by the 87WB Relay Word bit, as shown in *Figure 5.22*.
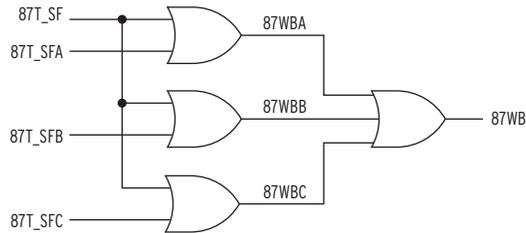
Figure 5.10   Waveshape Blocking Logic

Waveshape-Based Bipolar Unblocking Logic

A waveshape-based bipolar differential overcurrent element allows for improvements in the operation of the restrained and unrestrained differential elements. *Figure 5.11* shows the differential currents for an internal transformer fault that develops during transformer energization. The first part of the figure shows the unipolar characteristic of the differential currents during an inrush condition. When the internal fault occurs on one phase, the resulting waveform has a bipolar characteristic as shown in blue.
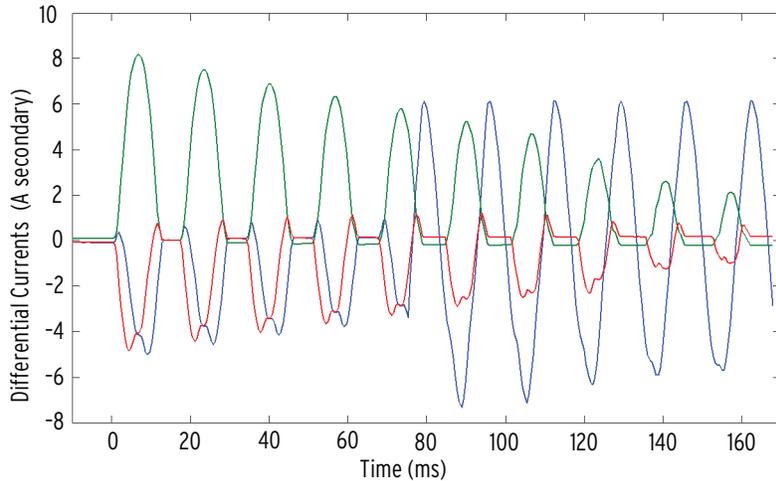
Figure 5.11   Differential Currents for an Internal Fault During Inrush Conditions

Figure 5.12 shows the differential current of the faulted phase of *Figure 5.11* superimposed on two thresholds. Note that during inrush conditions (the first 72 milliseconds), the current is negative and it repeatedly crosses the negative threshold (the dashed blue line in *Figure 5.12*). The current during this time does not cross the symmetrically placed positive threshold (the dashed red line). When the internal fault occurs, the current crosses the negative threshold and then crosses the positive threshold shortly afterwards. Using this information, we create a pair of bipolar differential overcurrent elements: a low-set element that we can use to unblock the inrush blocking functions of the relay and a high-set element that we can use for unrestrained differential protection. Because the elements work on a bipolar principle, we set the thresholds relatively sensitively and still ensure security during inrush conditions.
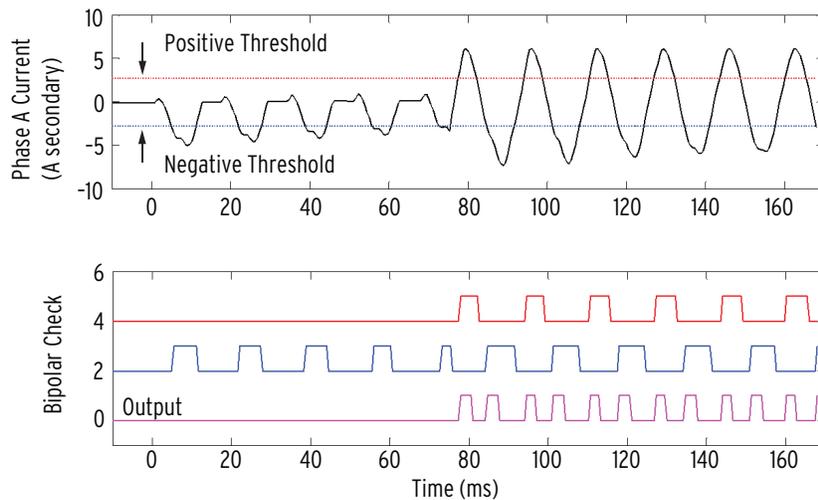
Figure 5.12   Fault Current During Energization (Black) Compared With Positive (Red) and Negative (Blue) Thresholds

As shown in *Figure 5.13*, the A-Phase, low-set bipolar differential overcurrent element compares the unfiltered (raw) operate current, IOPRAR (see *Figure 5.4*), against positive (+L) and negative (−L) thresholds. The B- and C-Phase logic is similar. If the current exceeds the positive threshold for a short duration (PKPBP timer), a window equal to the DPOBP timer opens to wait for the current to decrease below the negative threshold. If it does, the relay declares the current to

be symmetrical and not an inrush current. Mirrored logic covers the negative polarity. The magenta trace in *Figure 5.12* is the output of the bipolar low-set overcurrent element, shown in *Figure 5.13* as 87T_B1A.
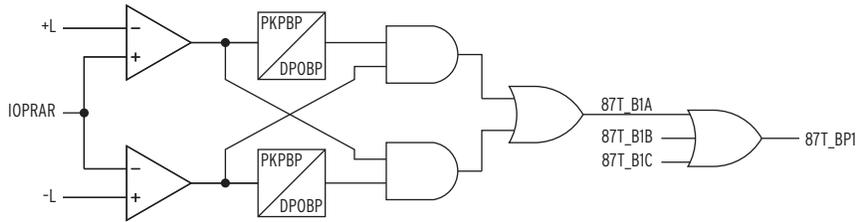
Figure 5.13   A-Phase Bipolar Low-Set Signature Detection Logic

Prior to using the low-set bipolar overcurrent element as an unblocking function, the relay performs additional security checks, as shown in *Figure 5.14*, to ensure that the bipolar logic is asserting properly. The first is a sudden change detection logic, which confirms that the bipolar nature of the differential current is caused by an internal short circuit rather than by gradual CT saturation occurring during inrush conditions. The sudden change detection logic monitors the absolute value of the per-cycle difference of the operate current and checks that this difference is significant (above the +L threshold). The output of the comparator passes through a pickup timer (PKPS) for security, and a dropout timer (DPOS) ensures that the sudden change detection logic coordinates with the input from the unsupervised bipolar low-set logic, 87T_B1A.

The other security check (shown in *Figure 5.14*) ensures that the bipolar logic does not assert because of CT saturation when an external fault condition is detected (CONA must be deasserted, see *Figure 5.4*). However, if the CT is deemed to be in an unsaturated state following the external fault, as indicated by CTUA asserting, the bipolar logic can assert. When the bipolar low-set logic, 87T_B1A, asserts, along with the security checks, the bipolar low-set element, 87BPLA, asserts. The B- and C-Phase supervised low-set logic is similar to the A-Phase logic.
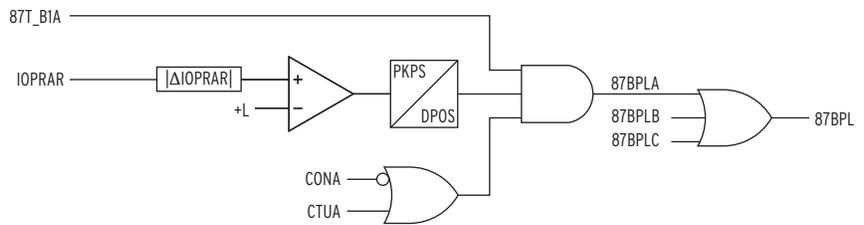
Figure 5.14   A-Phase Bipolar Low-Set Logic

The unblocking logic makes direct use of the bipolar low-set element, as shown in *Figure 5.15*. When you enable the unblocking logic via the E87UNB setting, the unblocking Relay Word bit, 87UNBLA, asserts for one cycle following the assertion of the bipolar low-set element, 87BPLA. The B- and C-Phase unblocking logic is similar to the A-Phase logic.
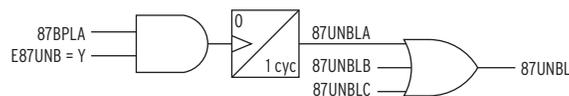
Figure 5.15   A-Phase Unblocking Logic

When the unblocking logic asserts, the following changes occur to the phase-restrained differential elements, as shown in *Figure 5.18*:

➤ The second- and fourth-harmonic cross blocking, 87XBK2, and waveshape-based inrush blocking, 87WBA, are canceled in the harmonic-blocked differential element.

➤ The waveshape-based inrush blocking, 87WBA, is canceled in the harmonic-restrained differential element.

➤ The second- and fourth-harmonic magnitudes are removed from the restraint current, IRTHRA, of the harmonic-restrained differential element.

➤ The fifth-harmonic integrity timer used by the phase-restrained elements is bypassed (although direct assertions of the 87ABK5 Relay Word bit still block the elements).

➤ The delay time of the adaptive security timer decreases.

The following changes are made to the negative-sequence differential element when the unblocking logic asserts, as shown in *Figure 5.21* and *Figure 5.22*:

➤ The second- and fourth-harmonic cross blocking, 87XBK2, and waveshape-based inrush blocking, 87WB, are canceled.

➤ The negative-sequence differential element delay timer, 87QD, is bypassed.

A high-set version of the bipolar differential overcurrent element is available for use as an unrestrained differential element and is identical to the low-set version except that it uses a threshold that is a multiple of the low-set threshold, as shown in *Figure 5.16* and *Figure 5.17*.
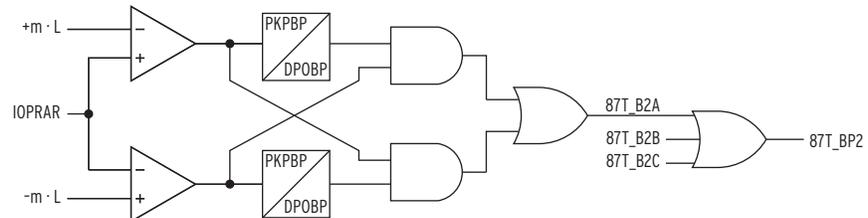
Figure 5.16   A-Phase Bipolar High-Set Signature Detection Logic
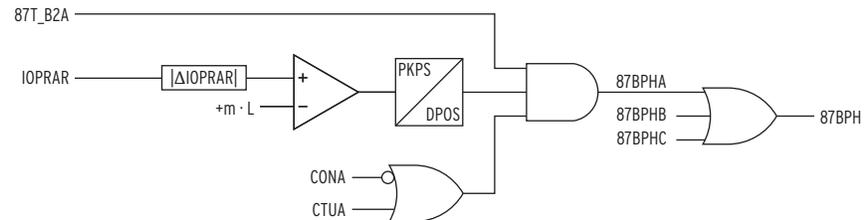
Figure 5.17   A-Phase Bipolar High-Set Logic

As shown in *Figure 5.23*, the unrestrained differential element can use the bipolar high-set element, 87BPHA, for unrestrained tripping.

Utilizing Harmonic and Waveshape Logic in the Differential Elements

The enable settings options for the various percentage-restrained differential elements (E87HB, E87HR, and E87Q) allow for each element to provide inrush security by using only the harmonic-based method (setting option Y), by using either the harmonic- or waveshape-based blocking methods for the harmonic-

blocked differential element and negative-sequence differential element (setting option E), or by adding waveshape-based blocking to the harmonic-restrained differential element (setting option W). As shown in *Figure 5.18* and *Figure 5.22*, the appropriate inrush blocking methods are activated or deactivated depending on the enable settings option. Note that for the harmonic-restrained differential element, setting option **W** enables the waveshape-based blocking method (87WBA) but does not remove the harmonic boost to the restraining current from the scaled second- and fourth-harmonic magnitudes (IAMkh2 and IAMkh4, respectively). Consider using the **E** and **W** settings option to provide the benefit of both the harmonic- and waveshape-based inrush blocking methods.

> **NOTE:** Consider enabling all of the harmonic and waveshape functions through the **E** and **W** settings options for the settings E87HB, E87HR, and E87Q as well as setting E87UNBL = Y to gain the best security and speed performance from the differential elements.

The waveshape-based unblocking logic is separate from the inrush blocking logic and is enabled in all the percentage-restrained differential elements (87HB, 87HR, and 87Q) when setting E87UNBL = Y (see *Waveshape-Based Bipolar Unblocking Logic on page 5.16*). Should the unblocking logic assert, indicating that the logic detected an internal fault, the relay cancels the inrush security checks and modifies the security timers in the differential elements (see *Figure 5.18*, *Figure 5.21*, and *Figure 5.22*), allowing for improved element operating times. Consider enabling the unblocking logic to gain speed improvements for all internal fault types and conditions.

Phase Percentage-Restrained Differential Element (87R)

Because of differing harmonic philosophies, the SEL-487E includes harmonic-blocking and harmonic-restraint functions to avoid relay misoperation during inrush current conditions. The harmonic-blocking functions always operate in cross-blocking mode, whereby the relay blocks all phases when the harmonic magnitude of any phase exceeds the harmonic setting. By contrast, the harmonic-restraint functions always operate in independent blocking mode, i.e., there is no cross blocking between phases.

> **NOTE:** The SEL-487E restraint quantity IRTp calculation differs from the SEL-587 and SEL-387 by a factor of 2.

> **NOTE:** The 87R element currents are in per unit of the TAPm values (see *Figure 5.2*).

Figure 5.18 shows the A-Phase percentage-restrained differential element. Using the compensated output quantities from the digital band-pass filter (full-cycle cosine filter), the relay calculates an operating quantity, IOPA (*Equation 5.5*), and a restraint quantity, IRTA (*Equation 5.6*), both of which are used by the harmonic-blocked differential element and the harmonic-restrained differential element.

$$IOPA = |\Sigma IAmCFC|$$

Equation 5.5

$$IRTA = \Sigma|IAmCFC|$$

Equation 5.6

where:

    IAmCFC = A-Phase filtered, compensated per-unit current
               (m = S, T, U, W, X) (see *Figure 5.2*)

Figure 5.18   A-Phase Percentage-Restrained Differential Element

As shown in *Figure 5.18*, the harmonic-blocked and harmonic-restrained differential elements are run independently of one another. Enable whichever element is best suited for your application by using the E87HB (harmonic-blocked element) or E87HR (harmonic-restrained element) enable settings. Because the two elements are complementary, consider enabling both elements to allow them to run in parallel. The harmonic-blocked element is generally faster, but because of cross blocking, it has reduced dependability when energizing a faulted transformer. The harmonic-restraint element is generally slower because of the additional restraint, but it has improved dependability when energizing a faulted transformer. Also, because the harmonics are summed, harmonic restraint is more secure during inrush conditions.

From *Figure 5.18*, the relay calculates the filtered operating (IOPA) and restraining (IRTA) quantities from the filtered, compensated terminal currents (see *Figure 5.2*). After selecting the appropriate slope (SLP2 if CONA is asserted or SLP1 if CONA is deasserted), the relay calculates the biased restraint current, IRTFKA, for use by the harmonic-blocked element and then adds the scaled second- and fourth-harmonic quantities (IAMkh2 and IAMkh4, respectively, see *Figure 5.5*) to IRTFKA to form IRTHRA for use by the harmonic-restrained element.

Both of the differential elements are supervised by the IO87PA Relay Word bit, which asserts when the fault detection logic detects an internal fault, IFLTA, (see *Figure 5.4*) and IOPA exceeds the O87P pickup value. The harmonic-blocked and harmonic-restrained differential elements each have a preliminary Relay Word bit (87HBPA and 87HRPA, respectively) that asserts when the minimum operate current check is satisfied (IO87PA is asserted) and the operate current is greater than the appropriate biased restraint current (indicating that the operating condition lies within the operate region of the percentage-restrained characteristic). You can use these 87HBPA and 87HRPA Relay Word bits for testing and troubleshooting purposes.

For the harmonic-blocked differential element, the remaining checks are tied to the AND gate that is controlling the 87AHB Relay Word bit, and they pertain to inrush and overexcitation security. The inrush security checks are enabled or disabled via the E87HB setting option. If you have selected harmonic-based inrush security by setting E87HB = Y or E, an assertion of the second- and fourth-harmonic cross-blocking logic, 87XBK2, (see *Figure 5.5*) blocks the differential element. If you have also enabled waveshape-based inrush security by setting E87HB = E, an assertion of the waveshape inrush blocking logic, 87WBA, (see *Figure 5.10*) blocks the differential element. If you have enabled the unblocking logic and 87UNBLA asserts (see *Figure 5.15*), indicating detection of an internal fault, the relay cancels the inrush blocking of both the harmonic- and waveshape-based methods. If the fifth-harmonic overexcitation logic, 87ABK5, asserts (see *Figure 5.5*), the differential element will be blocked.

For the harmonic-restrained differential element, the relay makes similar inrush and overexcitation security checks prior to asserting the 87AHR Relay Word bit. If you have selected harmonic-based inrush security by setting E87HR = Y, the differential element is secured against inrush by the harmonic-boosted restraint signal, IRTHRA. If you have selected waveshape-based inrush security by setting E87HR = W, an assertion of the waveshape inrush-blocking logic, 87WBA, blocks the differential element, and the element will also use the harmonic-boosted restraint current, IRTHRA, to provide additional inrush security. If you have enabled the unblocking logic and 87UNBLA asserts, indicating detection of an internal fault, the relay removes harmonic content from the IRTHRA signal and cancels the inrush blocking of the waveshape-based method. If the fifth-harmonic overexcitation logic, 87ABK5, asserts, the differential element will be blocked.

The harmonic integrity timers in *Figure 5.18* prevent differential element misoperation if the harmonic content momentarily drops below the harmonic threshold setting. If the timer input asserts continuously for at least 1.5 cycles, the relay activates the dropout timer and keeps the timer output asserted for an additional 1 cycle. However, this 1 cycle does not need to be continuous. For example, if 87XBK2 has been asserted for 1.5 cycles, drops out for 0.125 cycles, and then asserts again, the dropout timer value changes from 1 cycle to 0.875 cycles.

When either the harmonic-blocked (87AHB) or harmonic-restrained (87AHR) output asserts, the adaptive security timer is loaded with the pickup timer value t, which depends on the state of the 87UNBLA and CONA Relay Word bits at the moment the timer output asserts (P87A), as shown in *Figure 5.18*. When the adaptive security timer pickup time expires, the A-Phase restrained differential element, 87RA, asserts along with the overall phase-restrained differential element, 87R. The B- and C-Phase percentage-restrained differential element logic is similar to the A-Phase logic. Note that the 87R Relay Word bit is an input to the overall transformer differential tripping logic, 87T, as shown in *Figure 5.25*.

Note that even if you have disabled one of the phase differential-element outputs (87AHB or 87AHR Relay Word bits) by setting E87HB = N or E87HR = N, the analog quantities and Relay Word bits for that differential element are still active, allowing you to analyze or evaluate the element performance in an event report or with the SER even though the element is not enabled for tripping.

Setting Descriptions

When one considers the SEL-487E as a device with five sets of three-phase current inputs, three single-phase current inputs, and two sets of three-phase voltage inputs, the application possibilities are considerable. For example, a wye/delta, two-winding transformer requires only two sets of three-phase current inputs for differential protection and one single-phase current input for REF. This leaves three three-phase current inputs and two single-phase current inputs available for other functions, such as overcurrent protection for a distribution feeder or frame leakage protection for metal-clad switchgear. To simplify the setting process, the settings are arranged in a multitier structure to allow enabling and control of input currents for the appropriate application.

Tier 1

First-tier settings identify which of the 21 analog inputs (CTs and PTs), excluding the three REF (IY1, IY2, IY3) channels, the relay processes. Enable the REF channels under the restricted earth fault settings category. Settings on the first tier include the following settings:

ECTTERM, EPTTERM

Terminals entered here are function independent. Entering a terminal here does not indicate the intended functional use (differential, REF, etc.); such entry instructs the relay to process the analog inputs from these terminals.

Tier 2

After you select the appropriate analog channels, use Tier 2 settings to enable the protection functions required for your particular application. Settings on the second tier include the following enable settings:

E87, EREF, E50, E51, E46, E59, E27, E81, E24, E25, EBFL, EPCAL, E32, EDEM

Tier 3

The third tier is usually in the form of a torque control (TC) SELOGIC control equation, and is not available for all protection functions. This tier provides conditional availability of protection elements, because the settings are function-dependent. For example, Terminal S is enabled (ECTTERM = S, T,…) and assigned to the differential element (E87 = S, T,…). Third-tier setting E87T provides a method to dynamically enable/disable current S in the differential element. Settings on the third tier include the following settings:

E87T[S,T,U,W,X], TCREF[1–3], 51TC[1–10], 24TC, 27TC[1–5], 59TC[1–5], EXBF[S,T,U,W,X], BFI[S,T,U,W,X], E32OP[01–10], EDM[01–10]

ECTTERM, EPTTERM (CT and PT Terminal Enable)

Identify which of the 21 analog inputs (CTs and PTs), excluding the three REF (IY1, IY2, IY3) channels, the relay processes. Enable the REF channels under the restricted earth fault settings category.

E87 (Enable Differential-Element Protection Terminals)

The SEL-487E has five sets of three-phase current inputs. Depending on the application, you may not need all of these inputs for the differential protection. All terminals not included in the differential element are available for other protection such as stand-alone overcurrent protection. The E87 setting specifies which of the terminals the relay is to include in the differential calculation.

E87Tm (Terminals Included in the 87 Element)

Use this SELOGIC control equation to specify operational conditions to include/exclude those terminals specified with the E87 setting in the differential calculations. For example, assume you have a three-winding autotransformer and the 22 kV tertiary delta of the autotransformer is a standby supply for a small 22 kV network. Further, assume that the tertiary delta winding connects to the 22 kV busbar through a circuit breaker (CBD) that is normally open, and will only be closed under emergency conditions. You assign Terminal S (HV), Terminal T (LV), and Terminal U (tertiary delta) as the terminals for the differential element. Because the default settings are set to 1, Terminals S and T are already part of the differential element, i.e.:

E87TS = 1

E87TT = 1

Terminal U is only part of the differential element if CBD is closed. Wire a 52A contact to input IN101, and set the SELOGIC control equations for Terminal U as follows:

E87TU = IN101

With this setting, Terminal U is part of the differential element only when CBD is closed.

ICOM (Internal CT Connection Compensation)

This Yes/No setting defines whether the input currents need any correction, either to accommodate phase shifts in the transformer or CTs or to remove zero-sequence components from the secondary currents. If this setting is Yes (Y), the relay permits you (see *TmCTC (Internal CT Connection Compensation) on page 5.24*) to define the amount of shift needed to properly align the secondary currents for the differential calculation.

TmCTC (Internal CT Connection Compensation)

These settings define the amount of compensation the relay applies to each set of winding currents to properly account for phase shifts in transformer winding connections and CT connections. For example, this correction is needed if both wye and delta power transformer windings are present, but all of the CTs are connected in wye. The effect of the compensation is to create phase shift and to remove zero-sequence current components.

The general expression for current compensation is as follows:

$$\begin{bmatrix} IAmCFC \\ IBmCFC \\ ICmCFC \end{bmatrix} = \begin{bmatrix} X & X & X \\ X & X & X \\ X & X & X \end{bmatrix} \cdot \begin{bmatrix} IAmCF \\ IBmCF \\ ICmCF \end{bmatrix}$$

where:

IA*m*CF, etc. = the three-phase currents entering terminal m of the relay

IA*m*CFC, etc. = the corresponding phase currents after compensation

$$\begin{bmatrix} X & X & X \\ X & X & X \\ X & X & X \end{bmatrix} = [CTC(m)]$$

= a three-by-three compensation matrix (*m* = 0, 1, 2, …, 11, 12)

Setting T*m*CTC specifies which compensation matrix the differential element is to use. The setting values are 0–12. These values physically represent the number of increments of 30 degrees that a *balanced set of currents with ABC phase rotation* will be rotated in a *counterclockwise* direction when multiplied by Matrix CTC(*m*). For example, setting TSCTC = 1 rotates the Terminal S set of currents counterclockwise by 30 degrees. If a *balanced set of currents with ACB phase rotation* undergoes the same exercise, the rotations by the CTC(*m*) matrices are in the clockwise direction.

The 0 setting value creates no changes at all in the currents but multiplies them by an identity matrix. Thus, for T*m*CTC = 0, we obtain the following:

$$CTC(0) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

that is,

IA*m*CFC = IA*m*CF
IB*m*CFC = IB*m*CF
IC*m*CFC = IC*m*CF

Assuming ABC phase rotation, the CTC(1) setting performs a 30-degree compensation in the counterclockwise direction, as would a delta CT connection of type DAB (Dy1). The name for this connection comes from the fact that the polarity end of the A-Phase CT connects to the nonpolarity end of the B-Phase CT, and so on, in forming the delta. Therefore, the DAB (Dy1) connection results from the following relationships:

$$IAmCFC = \frac{(IAmCF - IBmCF)}{\sqrt{3}}$$

$$IBmCFC = \frac{(IBmCF - ICmCF)}{\sqrt{3}}$$

$$ICmCFC = \frac{(ICmCF - IAmCF)}{\sqrt{3}}$$

Setting TmCTC = 1 realizes the above-mentioned relationships, and the relay uses the following CTC(1) matrix to compensate the currents:

$$[CTC(1)] = \frac{1}{\sqrt{3}} \bullet \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

Similarly, assuming ABC phase rotation, a setting of TmCTC = 11 performs a 330-degree compensation (11 • 30 degrees) in the counterclockwise direction, or a 30-degree compensation in the clockwise direction, as would a delta CT connection of type DAC (Dy11). The name for this connection comes from the fact that the polarity end of the A-Phase CT connects to the nonpolarity end of the C-phase CT, and so on, in forming the delta. Thus, for TmCTC = 11, the relay uses the following CTC(11) matrix:

$$[CTC(11)] = \frac{1}{\sqrt{3}} \bullet \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$$

that is,

$$IAmCFC = \frac{(IAmCF - ICmCF)}{\sqrt{3}}$$

$$IBmCFC = \frac{(IBmCF - IAmCF)}{\sqrt{3}}$$

$$ICmCFC = \frac{(ICmCF - IBmCF)}{\sqrt{3}}$$

The compensation matrix CTC(12) is similar to CTC(0), in that it produces no phase shift (or, more correctly, 360 degrees of shift) in a balanced set of phasors. However, it removes zero-sequence components from the winding currents, as do all of the matrices having nonzero values of m, i.e., all matrices except CTC(0).

$$[CTC(12)] = \frac{1}{3} \bullet \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

that is,

$$IAmCFC = \frac{(2 \bullet IAmCF - IBmCF - ICmCF)}{3}$$

$$IBmCFC = \frac{(-IAmCF + 2 \bullet IBmCF - ICmCF)}{3}$$

$$ICmCFC = \frac{(-IAmCF - IBmCF + 2 \bullet ICmCF)}{3}$$

The effect of each compensation on balanced three-phase currents is to rotate the currents m • 30 degrees without a magnitude change. *Table 5.2* shows the complete list of compensation matrices.

Table 5.2   Complete List of Compensation Matrices (*m* = 0 to 12)

$$[\mathrm{CTC}(0)] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$[\mathrm{CTC}(1)] = \frac{1}{\sqrt{3}} \bullet \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

$$[\mathrm{CTC}(2)] = \frac{1}{3} \bullet \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \\ -2 & 1 & 1 \end{bmatrix}$$

$$[\mathrm{CTC}(3)] = \frac{1}{\sqrt{3}} \bullet \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix}$$

$$[\mathrm{CTC}(4)] = \frac{1}{3} \bullet \begin{bmatrix} -1 & -1 & 2 \\ 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}$$

$$[\mathrm{CTC}(5)] = \frac{1}{\sqrt{3}} \bullet \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}$$

$$[\mathrm{CTC}(6)] = \frac{1}{3} \bullet \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix}$$

$$[\mathrm{CTC}(7)] = \frac{1}{\sqrt{3}} \bullet \begin{bmatrix} -1 & 1 & 0 \\ 0 & -1 & 1 \\ 1 & 0 & -1 \end{bmatrix}$$

$$[\mathrm{CTC}(8)] = \frac{1}{3} \bullet \begin{bmatrix} -1 & 2 & -1 \\ -1 & -1 & 2 \\ 2 & -1 & -1 \end{bmatrix}$$

$$[\mathrm{CTC}(9)] = \frac{1}{\sqrt{3}} \bullet \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}$$

$$[\mathrm{CTC}(10)] = \frac{1}{3} \bullet \begin{bmatrix} 1 & 1 & -2 \\ -2 & 1 & 1 \\ 1 & -2 & 1 \end{bmatrix}$$

$$[\mathrm{CTC}(11)] = \frac{1}{\sqrt{3}} \bullet \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$$

$$[\mathrm{CTC}(12)] = \frac{1}{3} \bullet \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

For further information, see *Section 6: Protection Application Examples* for detailed settings guidelines for transformer winding and CT connection and compensation settings.

MVA (Maximum Transformer Capacity, Three-Phase MVA)

Use the highest expected transformer rating, such as the forced oil and air cooled (FOA) rating or a higher emergency rating, when setting the maximum transformer capacity.

VTERM*m* (Terminal Line-to-Line Voltage)

Enter the nominal line-to-line transformer terminal voltages. If the transformer differential zone includes a load tap-changer, assume that the tap-changer is in the neutral position. The setting units are kilovolts.

TAP*m* (Terminal *m* Current Tap)

The TAP*m* values are used to convert the terminal currents bounding the differential zone to a common per-unit system. Upon your entry of an MVA setting (i.e., MVA is not set to "OFF"), the relay uses the MVA, winding voltage, CT ratio, and CT connection settings you have entered and calculates the TAP*m* values automatically, per *Equation 5.7*. You can also enter tap values directly. Set MVA = OFF, and enter the TAPS–TAPX values directly, along with the other pertinent settings.

$$TAP = \frac{MVA \cdot 1000}{\sqrt{3} \cdot VTERM \cdot CTR} \cdot C$$

Equation 5.7

where:

$$
\begin{aligned}
MVA &= \text{Transformer maximum MVA (MVA)} \\
VTERM &= \text{Terminal line-to-line voltage of the winding (kV)} \\
CTR &= \text{CT ratio} \\
C &= \text{1 if CTCON = Y (wye- or star-connected CTs)} \\
C &= \sqrt{3} \text{ if CTCON = D (delta-connected CTs)}
\end{aligned}
$$

The relay calculates TAP with the following limitations:

1. The TAP settings are within the range $0.1 \cdot I_{NOM}$ and $35 \cdot I_{NOM}$ (I_{NOM} = 1 A or 5 A).
2. The ratio $TAP_{MAX} / TAP_{MIN} \leq 35$.

O87P (Restrained Element Operating Current Pickup)

O87P is set in per unit of the TAP_{MIN} value. Set the operating current pickup at a minimum for increased sensitivity but high enough to avoid operation because of steady-state CT error and transformer excitation current. To ensure proper relay operation, be sure to select a setting value that satisfies the following equation:

$$O87P \geq \frac{0.02 \cdot I_{NOM}}{TAP_{MIN}}$$

Equation 5.8

SLP1, SLP2 (Restraint Slope Percentage)

Use restraint slope percentage settings to discriminate between internal and external faults. Set SLP1 and SLP2 to accommodate differential current resulting from power transformer tap-changer, CT saturation, CT errors, and relay error.

We derive the Slope 1 setting (SLP1) as follows:

Assume the CT error, ε, is equal to ±10 percent. In per unit:

$\varepsilon = 0.1$

Assume the voltage ratio variation of the power transformer load tap-changer (LTC), *a*, is from 90 percent to 110 percent. In per unit:

$a = 0.1$

In a through-current situation, the worst-case theoretical differential current occurs when all of the input currents are measured with maximum positive CT error, and all of the output currents are measured with maximum negative CT error while also being offset by maximum LTC variation. Therefore, the greatest differential current one can expect for through-current conditions is as follows:

$$Id\text{max} = \left[(1 + \varepsilon) \bullet \frac{\Sigma ITn}{"IN"}\right] - \left[\frac{(1 - \varepsilon)}{1 + a} \bullet \frac{\Sigma ITn}{"OUT"}\right]$$

Equation 5.9

where the summation terms are the total input and output power transformer secondary currents after tap compensation. Per-unit current entering the transformer equals the per-unit current exiting the transformer, so the summation terms cancel, and we can express the maximum differential current (Idmax) as a percentage of winding current:

$$
\begin{aligned}
Id\text{max} &= (1 + \varepsilon) - \frac{(1 - \varepsilon)}{(1 + a)} \\
&= \frac{(2 \bullet \varepsilon) + a + (\varepsilon \bullet a)}{(1 + a)} \bullet 100 \\
&= 28.18\%
\end{aligned}
$$

Equation 5.10

In addition to the error we just calculated, we must consider additional errors from transformer excitation current ($\cong 2$ percent) and relay measurement error (<5 percent). The maximum total error is 35 percent.

In the following text, we briefly discuss the correlation between the percentage error and the relay slope setting (also see *87RA, 87RB, and 87RC Restrained Differential Elements on page 3.17*). For this discussion, consider a two-winding transformer, with I1 flowing toward the transformer and I2 flowing away from the transformer (see *Figure 5.19*).
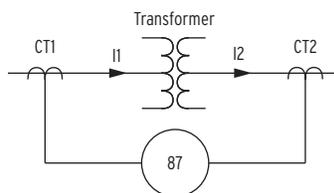
Figure 5.19   Two-Winding Transformer

In general, Slope 1 of the differential element characteristic in SEL percentage differential elements is a straight line through the origin, as *Equation 5.11* represents.

$$IOP(IRT) = k \bullet SLP1 \bullet IRT$$

Equation 5.11

where:

$$
\begin{aligned}
k &= \text{design constant (k = 1)} \\
SLP1 &= \text{Slope 1} \\
IRT &= \text{restraint current}
\end{aligned}
$$

The relay uses *Equation 5.12* to calculate the differential current (Idiff), and it uses *Equation 5.13* to calculate the restraint current (IRT).

$$\text{Idiff} = \left| \overline{\text{I1}} + \overline{\text{I2}} \right|$$

Equation 5.12

$$\text{IRT} = \left| \overline{\text{I1}} \right| + \left| \overline{\text{I2}} \right|$$

Equation 5.13

where I1 and I2 are per-unit vector quantities.

To calculate I1 and I2, evaluate the IN (I1) and OUT (I2) values of *Equation 5.9* separately.

$$\text{I1} = (1 + \varepsilon) = 1.1 \text{ pu}$$

and

$$\text{I2} = \frac{(1 - \varepsilon)}{(1 + a)} = 0.818 \text{ pu}$$

Use *Equation 5.12* to calculate Idiff.

$$\text{Idiff} = \left| \overline{\text{I1}} + \overline{\text{I2}} \right|$$

$$\text{Idiff} = \left| 1.1 - 0.818 \right| = 0.282 \text{ pu (or 28.18 percent as before)}$$

Use *Equation 5.13* to calculate the restraint current.

$$\text{IRT} = \left| \overline{\text{I1}} \right| + \left| \overline{\text{I2}} \right|$$

$$\text{IRT} = \left| 1.1 \right| + \left| 0.818 \right| = 1.918 \text{ pu}$$

The maximum differential error is 0.282 pu, and the restraint current is 1.918 pu. Evaluate *Equation 5.11* with SLP1 = 0.35 (35%) and $k = 1$. Remember that k is not a setting, it is a design constant.

$$\text{IOP(IRT)} = k \cdot \text{SLP1} \cdot \text{IRT}$$

$$\text{IOP(IRT)} = 1 \cdot 0.35 \cdot 1.918$$

$$\text{IOP(IRT)} = 0.67 \text{ pu}$$

The value of 0.67 pu is much greater than 0.282, and is an extremely conservative setting. For the SEL-487E, reducing the SLP1 setting by half still provides an adequate margin for an anticipated maximum differential error of 0.282 pu, as calculated above.

$$\text{IOP(IRT)} = 1 \cdot 0.18 \cdot 1.918$$

$$\text{IOP(IRT)} = 0.345 \text{ pu}$$

During external faults, the relay changes to high-security mode and switches from Slope 1 to Slope 2 to avoid relay misoperation resulting from CT saturation. In contrast to small CT errors for load current, CT errors during external faults can be quite large. Although CT saturation resulting from high-current magnitude is less likely to occur with low-impedance relays, the dc component of the primary current can still cause severe CT saturation. During CT saturation, current resulting from CT errors appears as differential current and can cause relay misoperation.

To avoid relay misoperation, set Slope 2 as high as possible. Normally, a high Slope 2 setting causes slow tripping for evolving faults (external-to-internal faults). However, because the differential element in the SEL-487E requires less than 1.5 cycles to return to normal mode for an evolving fault, a Slope 2 setting as high as 90 percent is acceptable.

Differential-Element Settings in SEL-487E, SEL-387, and SEL-587

NOTE: The SEL-487E uses the total value of the restraint current, which is accounted for with the design constant k = 1. The SEL-387 and SEL-587 relays use half the restraint current (IRT/2), which is accounted for with a design constant of k = 0.5. For more information, refer to the technical paper, *Percentage Restrained Differential, Percentage of What?* by Michael J. Thompson (available at selinc.com).

The SEL-487E restraint quantity IRTn calculation differs from the SEL-587 and SEL-387 by a factor of 2. In order to achieve the same characteristics for the differential elements in the SEL-487E, SEL-387, and SEL-587, this factor of 2 has to be accounted for. The relationships between differential element settings for the three relays are shown next.

Convert SEL-387 and SEL-587 Relay Settings to the SEL-487E Relay

$$O87P_{487E} = O87P_{387/587}$$

$$SLP1_{487E} = 1/2 \bullet SLP1_{387/587}$$

$$SLP2_{487E} = 1/2 \bullet SLP2_{387/587}$$

$$U87P_{487E} = U87P_{387/587}$$

Convert SEL-487E Relay Settings to the SEL-387 and SEL-587 Relays

$$O87P_{387/587} = O87P_{487E}$$

$$SLP1_{387/587} = 2 \bullet SLP1_{487E}$$

$$SLP2_{387/587} = 2 \bullet SLP2_{487E}$$

$$U87P_{387/587} = U87P_{487E}$$

DIOPR and DIRTR (Incremental Operate and Restraint Threshold)

The relationship between the change in operating current and the change in restraint current determines the relay mode of operation. A change in restraint current without a change in operating current causes the relay to change to high-security mode, while a change in both restraint current and operating current causes the relay to trip. In setting the incremental quantities (DIOPR and DIRTR), we must consider the effect of load current on relay operation.

For low DIRTR settings, the relay enters the high-security mode for small changes in load current. Although the relay detects evolving faults (external to internal) in a short time, there is a time delay (less than one cycle) when the relay changes to internal fault detection. We should, therefore, select a step value that indicates an external fault rather than an increase in load current.

In general, we want to enter the high-security mode of operation when there is a danger of CT saturation for external faults. DIOPR and DIRTR default settings of 1.2 per unit provide satisfactory results in most applications.

E87HB (Enable Harmonic-Blocked Differential Element)

Choose among harmonic blocking, harmonic restraint, or both to obtain relay stability during transformer inrush conditions (see *Figure 5.18*). Setting E87HB enables the harmonic-blocked differential element, and the setting options control the method of inrush security. Set E87HB = Y to provide inrush blocking from only the harmonic-based method. Set E87HB = E to provide inrush blocking from either the harmonic- or waveshape-based methods.

Note that the harmonic-blocked element always operates in cross-blocking mode when using the harmonic-based inrush blocking method.

E87HR (Enable Harmonic-Restrained Differential Element)

Choose among harmonic blocking, harmonic restraint, or both to obtain relay stability during transformer inrush conditions (see *Figure 5.18*). Setting E87HR enables the harmonic-restrained differential element, and the setting option controls the method of inrush security. Set E87HR = Y to provide inrush security that uses only the harmonic-based method. Set E87HR = W to provide additional inrush security with the waveshape-based inrush blocking method.

Note that the harmonic-restrained element always operates in an independent-blocking mode, i.e., no cross blocking between phases.

At least one of E87HB or E87HR must be enabled (both settings cannot be set to N). Because the two elements are complementary, it is possible to enable both elements and allow them to run in parallel.

E87UNB (Enable Waveshape Unblocking Logic)

The waveshape-unblocking logic provides sensitive detection of internal faults and cancels the inrush blocking functions used by the phrase-restrained and negative-sequence differential elements, improving element operation times for internal faults. Enable the unblocking logic by setting E87UNB = Y.

PCT2, PCT4, PCT5 (Second-, Fourth-, and Fifth-Harmonic Percentage of Fundamental)

NOTE: The larger the PCT2, PCT4, or PCT5 setting, the smaller the effect of the setting.

The SEL-487E measures the amount of second-, fourth-, and fifth-harmonic current flowing in the transformer (see *Figure 5.5*). Set PCT2 and PCT4 based on the amount of harmonic content, in percentage of fundamental, the transformer produces during energization to provide security for inrush conditions. Set PCT5 based on the amount of harmonic content, in percentage of fundamental, that is expected during overexcitation conditions and is above the rated transformer excitation current. These settings are only used by the phase-restrained and negative-sequence differential elements.

To disable a harmonic function, set that setting to OFF.

TH5P, TH5D (Fifth-Harmonic Alarm Threshold and Delay)

When the volts/hertz function is unavailable, use the fifth-harmonic measurement to assert an alarm output during startup. This alarm indicates current in excess of the rated transformer excitation current. At full load, a TH5P setting of 0.1 corresponds to 10 percent of the fundamental current. Use Timer TH5D to prevent the relay from indicating transient presence of fifth-harmonic currents. You might consider triggering an event report if transformer excitation current exceeds the fifth-harmonic threshold.

NOTE: Beginning with the R316 firmware release, the E87T_WS setting is no longer used. During the firmware upgrade process, the relay automatically sets the new waveshape settings options appropriately based on the E87T_WS setting status to yield similar behavior (see SEL Application Guide AG2018-05, *Enhancements to the SEL-487E Differential Elements* for more information). The E87T_WS is retained for firmware upgrade settings comparison purposes, but it no longer has any active function.

There are two criteria for setting TH5P:

➤ $\text{TH5P} \cdot \text{TAP}_{MIN} \geq 0.05 \cdot I_{NOM}$

➤ $\text{TH5P} \cdot \text{TAP}_{MAX} \leq 35 \cdot I_{NOM}$

where TAP_{MIN} and TAP_{MAX} are the least and greatest, respectively, of the tap settings.

To disable a harmonic function, set that setting to OFF.

87CORE (Transformer Core Type, Three-Legged or Individual Cores)

NOTE: Firmware releases prior to R316 used 87T_TYP (rather than 87CORE) as the setting name. During the firmware upgrade process, the relay automatically maps the 87T_TYP setting into the new 87CORE setting (see SEL Application Guide AG2018-05, *Enhancements to the SEL-487E Differential Elements* for more information). The 87T_TYP setting is retained for settings comparisons, but it no longer has any active function.

The waveshape-based dwell-time algorithm for inrush detection has to be adjusted based on the transformer core type. 87CORE defaults to T for three-legged, three-phase transformers. The setting 87CORE = S is for transformers made with single-phase units or with a four- or five-legged core.

Negative-Sequence Percentage-Restrained Differential Element (87Q)

During heavy load conditions, the resulting increase in restraint current renders the phase-differential element less sensitive, particularly from detecting transformer winding interturn faults. Because negative-sequence currents are unaffected by load in a balanced system, the negative-sequence percentage differential element provides sensitive protection for winding interturn faults.

Figure 5.20 shows the trajectory of a fault that shorts out 2 percent of the A-Phase winding of a three-phase transformer. In the phase-differential operation portion of *Figure 5.20*, the transformer is fully loaded, and the phase-differential relay operates when the operate current reaches around 0.43 per unit. *Figure 5.20* also shows the negative-sequence differential element response for the same fault. Because balanced load does not affect negative-sequence current, the negative-sequence element operates when the operate current reaches 0.3 per unit.
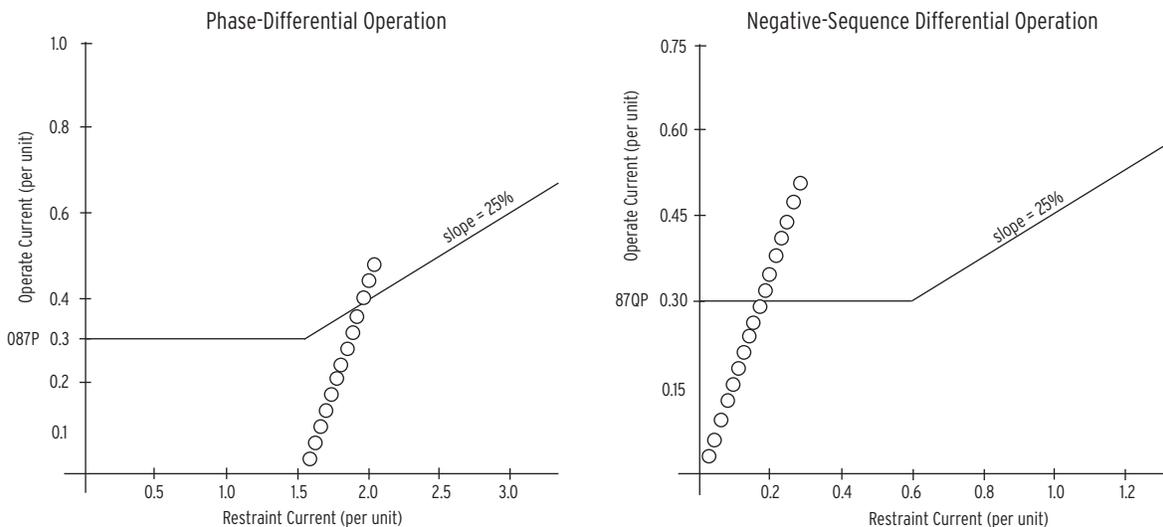
Figure 5.20 Differential Operations

The relay uses filtered compensated currents (see *Figure 5.2*) and *Equation 5.14* to calculate the negative-sequence currents for each terminal included in the differential element (ABC phase rotation) when you have enabled the element

through the E87Q setting. The element calculates the negative-sequence operating and restraint current as shown in *Equation 5.15* and *Equation 5.16*, respectively.

> **NOTE:** The 87Q element currents are set in per unit of the TAP*m* values (see *Figure 5.2*).

$$3I2mC = \begin{bmatrix} 1 & a^2 & a \end{bmatrix} \cdot \begin{bmatrix} IAmCFC \\ IBmCFC \\ ICmCFC \end{bmatrix}$$

Equation 5.14

where:

$$a = e^{j120}$$
$$a^2 = e^{j240}$$

$$IOP87Q = |\Sigma 3I2mC|$$

Equation 5.15

$$IRT87Q = \max(|3I2mC|)$$

Equation 5.16

> **NOTE:** CON is the OR combination of CONA, CONB, CONC (see *Figure 5.4*).

Figure 5.21 shows the logic that forms the negative-sequence differential element. In the figure, the relay calculates the operating current in a similar manner to that of the phase-restrained differential element. However, the restraint current is the maximum of the negative-sequence currents among the terminals that are part of the differential calculations. After evaluating the operating and restraint currents in the differential element, the relay verifies that the fault is indeed internal (CON is deasserted) and that the negative-sequence differential element blocking logic (87QB) is deasserted (see *Figure 5.22*).
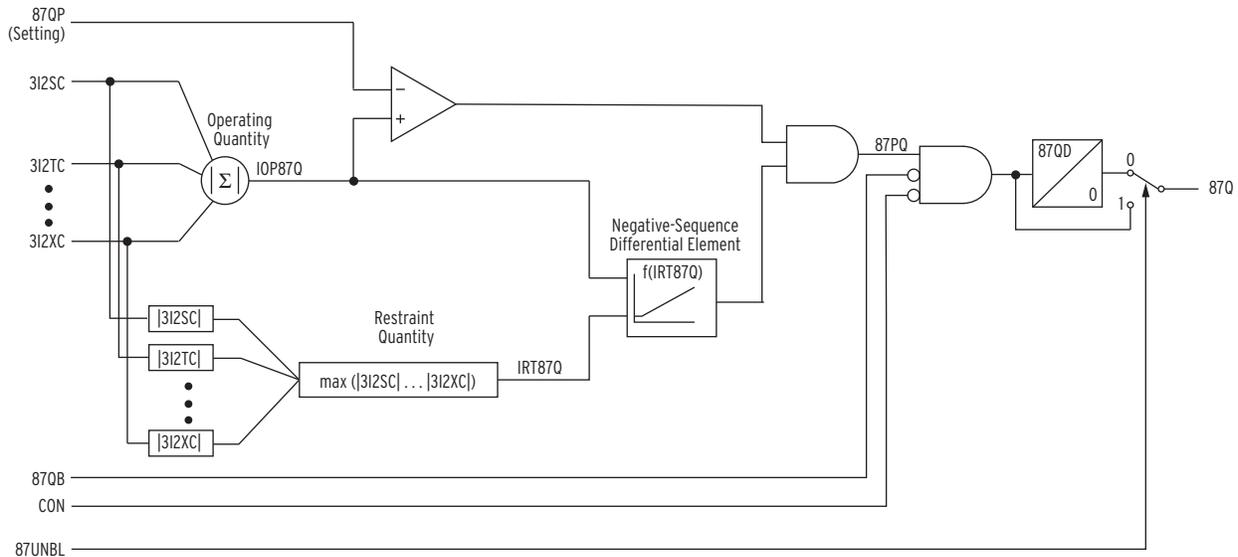
Figure 5.21 Negative-Sequence Percentage-Restrained Differential Element
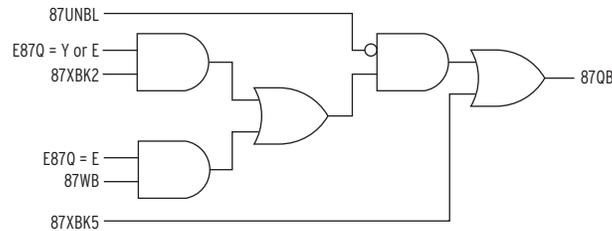
Figure 5.22   Negative-Sequence Differential-Element Blocking Logic

The negative-sequence differential element blocking logic illustrated in *Figure 5.22* secures the element during inrush or overexcitation conditions. Enable or disable the inrush security checks via the negative-sequence differential element enable setting (E87Q). If you have selected harmonic-based inrush security by setting E87Q = Y or E, an assertion of the second- and fourth-harmonic cross-blocking logic, 87XBK2, (see *Figure 5.5*) asserts 87QB and blocks the element. If you have also enabled waveshape-based inrush security by setting E87Q = E, an assertion of the waveshape inrush blocking logic, 87WB, (see *Figure 5.10*) asserts 87QB and blocks the element. If you have enabled the unblocking logic and 87UNBL asserts (see *Figure 5.15*), indicating detection of an internal fault, the relay cancels the inrush blocking of both the harmonic- and waveshape-based methods. If the fifth-harmonic overexcitation cross-blocking logic (87XBK5) asserts, 87QB asserts and blocks the element.

As shown in *Figure 5.21*, if you have enabled the unblocking logic and 87UNBL asserts, the relay bypasses the 87QD timer, allowing the negative-sequence differential element to operate faster.

The 87Q Relay Word bit is an input to the overall transformer differential tripping logic, 87T, as shown in *Figure 5.25*.

E87Q Enable Negative-Sequence Differential Element

The E87Q setting enables the negative-sequence differential element, and the setting option controls the method of inrush security. Set E87Q = Y to provide inrush blocking that uses only the harmonic-based method. Set E87Q = E to provide inrush blocking from either the harmonic- or waveshape-based methods.

87QP Negative-Sequence Differential-Element Operating Current Pickup

Set the negative-sequence differential element to improve sensitivity to internal transformer winding turn-to-turn faults during heavy load conditions. 87QP is the negative-sequence pickup threshold of the element, and is set in per unit of the TAP*m* values.

If 87QP is set lower than the default value, you should perform an analysis to determine how much negative sequence operating current is present because of CT measurement errors. This analysis is assures the security of the 87Q element.

SLPQ1 Negative-Sequence Deferential Slope

The SLPQ1 setting defines the slope of the negative-sequence differential element. Unlike the phase-restrained differential elements, there is only one slope to set because the negative-sequence element is blocked if an external fault is detected (when the CON Relay Word bit asserts).

87QD Negative-Sequence Differential-Element Delay

The output of the negative-sequence differential element can be delayed for added security. Set the negative-sequence differential element delay to the recommended delay of 10 cycles.

Unrestrained Phase Differential Element (87U)

The relay provides three types of unrestrained differential elements intended to rapidly detect very high magnitude currents that clearly indicate an internal fault. *Figure 5.23* illustrates the logic for the A-Phase unrestrained differential element. The B- and C-Phase logics are similar to the A-Phase.

NOTE: The 87U element currents are in per unit of the TAP*m* values (see *Figure 5.2*).
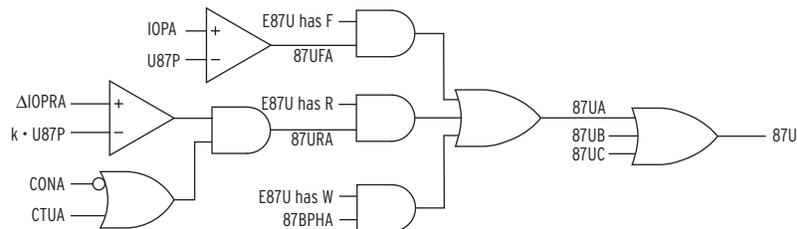
Figure 5.23 A-Phase Unrestrained Differential Element

As shown in *Figure 5.23*, the filtered unrestrained element (87UFA) is a traditional unrestrained differential element and operates when the filtered operating current, IOPA, (see *Figure 5.18*) exceeds the U87P setting value. The raw unrestrained element (87URA) operates when the raw (unfiltered) incremental change in operating current, ΔIOPRA, (see *Figure 5.4*) exceeds the threshold $k \cdot$ U87P and there is no external fault detected, as evidenced by CONA being deasserted (see *Figure 5.4*) or the CT is deemed to be in an unsaturated state following an external fault, as indicated by CTUA asserting. The k value is an internal setting equal to $\sqrt{2} \cdot 2$ that secures 87URA against unfiltered inrush currents (see *U87P (Unrestrained Element Current Pickup) on page 5.37* for more information). Because 87URA operates on raw currents, it can operate substantially faster compared to 87UFA. The waveshape-based bipolar high-set differential overcurrent element, 87BPHA, (see *Figure 5.16*) serves as an input to the unrestrained differential-element logic. Because 87BPHA can differentiate between inrush and internal fault current, it is more sensitive than 87UFA and 87URA.

The A-Phase unrestrained differential element (87UA) will operate from any combination of these three unrestrained elements, depending on the E87U combo setting.

➤ When the E87U combo setting includes F, the unrestrained element operates on filtered operate current.

➤ When the E87U combo setting includes R, the unrestrained element operates on raw operate current.

➤ When the E87U combo setting includes W, the unrestrained element operates on the output of the waveshape-based bipolar high-set logic.

Note that even if a particular unrestrained element is not set to assert the 87U Relay Word bit via the E87U setting, the Relay Word bits for the individual unrestrained elements (87UFA, 87URA, and 87BPHA in *Figure 5.23*) are still active and available for evaluation and analysis purposes.

Relay Word bit 87U is the OR combination of the outputs from the A-, B-, and C-Phase unrestrained differential elements. The 87U Relay Word bit is an input to the overall transformer differential tripping logic, 87T, as shown in *Figure 5.25*.

E87U Enable Unrestrained Differential Element

The E87U combination setting enables the unrestrained differential element and controls for which types of unrestrained elements it will operate. When the E87U setting includes F, the unrestrained element operates on the filtered unrestrained element. When the E87U setting includes R, the unrestrained element operates on the raw unrestrained element. When the E87U setting includes W, the unrestrained element operates on the waveshape-based bipolar high-set differential overcurrent element.

The unrestrained element can be set to trip for any combination of these three elements.

U87P (Unrestrained Element Current Pickup)

NOTE: If you apply the SEL-487E with a dual breaker terminal, it is possible that spurious differential current that occurs from CT saturation during an external fault is the limiting factor in setting U87P. In this case, take the maximum bus fault in per-unit of the TAP*m* value and multiply by your estimate for CT saturation (e.g., 50%), setting U87P to the result after rounding up to the nearest integer value.

The purpose of the instantaneous unrestrained current element is to react quickly to very high-magnitude currents that clearly indicate an internal fault. The unrestrained differential elements only respond to the differential operating current. They are unaffected by the SLP1, SLP2, PCT2, PCT4, PCT5 settings, so there is no harmonic blocking/restraint for this element during inrush conditions. Thus, you must set the element pickup level high enough (set in per unit of the TAP*m* values) that the element does not react to through faults or transformer inrush currents. In cases where the maximum through-fault current is limited by the impedance of the transformer, inrush current is usually the governing limit. The 87UFA Relay Word bit is the output of the comparison of U87P (a pickup threshold) against a full-cycle cosine-filtered quantity, IOPA. For this reason, you can set U87P below the peak inrush current. See *Equation 5.17* for information on how to determine the value of U87P.

Figure 5.24 is an oscillographic capture of the worst-case inrush currents during energization of a 120MVA 275/33 kV YDAC (Yd1) transformer (50 Hz nominal), as measured by the SEL-487E. The transformer was energized via the wye-side breaker with the delta-side breaker open. Relay Terminal S measured the wye-side (star-side) currents. The A-Phase experienced the largest inrush current, with a peak value exceeding 5 pu, as recorded by the raw (unfiltered) IAS_PU trace in *Figure 5.24*. Terminal S winding compensation was set with TSCTC = 11 to properly compensate for the phase shift across the transformer. The IASMC trace records the raw, compensated current while the IASCFC trace is the filtered, compensated current (see *Figure 5.2* for the filtered and unfiltered compensated current definitions). Because the inrush current represents a single-feed condition, the magnitude of IOPA is equal to the magnitude of the filtered, compensated Terminal S current, IASCFC. U87P needs to properly coordinate with the magnitude of the IOPA under the worst-case inrush current.
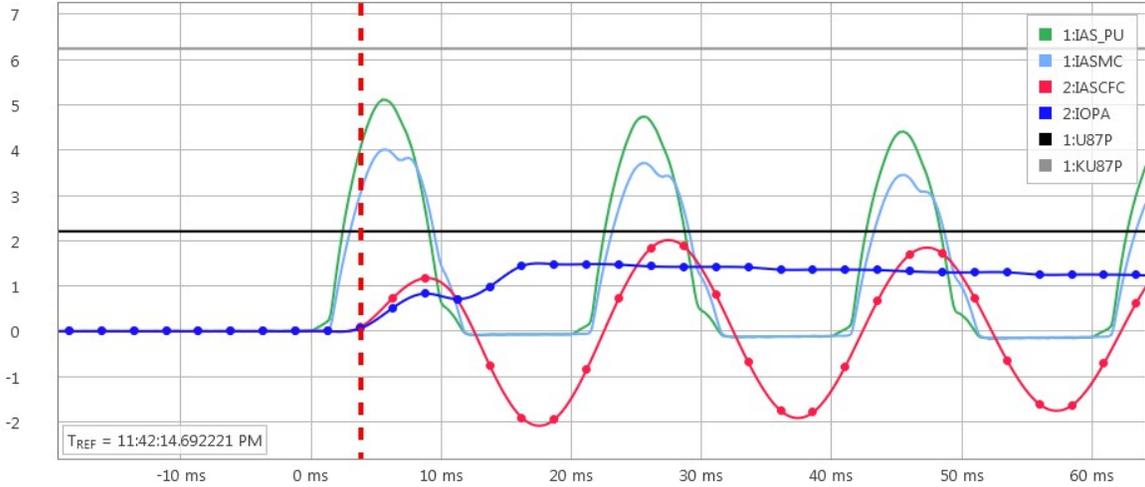
Figure 5.24 Worst-Case Inrush Current for Setting U87P

Notice the effect that the cosine filter has on the inrush current, as recorded by the IASCFC and IOPA values in *Figure 5.24*. The peak current of the compensated Terminal S current, IASMC, is 4 pu, but the cosine filter removes the dc component and the harmonics and produces an output IASCFC. The IOPA signal is the magnitude of the operating current (see *Figure 5.18*), so it is reduced by a factor of √2 compared to the IASCFC peak value. Therefore, we recommend a setting rule for U87P as given by *Equation 5.17*.

$$U87P \ = \ \frac{1.2 \bullet \ IPKIR}{\sqrt{2} \bullet \ 2}$$

<div align="right">**Equation 5.17**</div>

where:

> IPKIR is the worst-case peak inrush current

The 1.2 factor in *Equation 5.17* is added for security. For the waveforms captured in *Figure 5.24*, the worst-case inrush current captured by IAS_PU is around 5.2 pu. We use this for the value of IPKIR in *Equation 5.17*, and we solve for a value of U87P = 2.21 pu, as shown in *Figure 5.24*. This provides an adequate margin when comparing against the IOPA waveform and secures the filtered unrestrained element for the worst-case inrush current.

Note that the raw unrestrained differential element, 87URA, (see *Figure 5.23*) boosts the U87P setting by the factor *k* (equal to √2 • 2) to provide coordination with the inrush waveform measured by the raw, compensated Terminal S current in *Figure 5.24*, IASMC. Thus, given a setting value of U87P = 2.21 pu, the raw unrestrained element threshold shown in *Figure 5.23* is 6.24 pu and secures the raw unrestrained element for the worst-case inrush current shown in *Figure 5.24*.

Combined Differential Element (87T)

The relay combines the outputs of the phase-restrained differential elements, the negative-sequence differential element, and the unrestrained differential elements into an overall transformer differential short-circuit trip logic, given by 87T, as shown in *Figure 5.25*. The 87WS RWB is preserved for legacy users of the waveshape logic and is the combination of the phase-restrained and unrestrained differential elements.
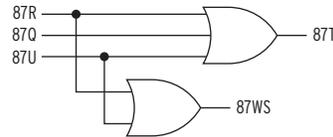
Figure 5.25 Combined Differential Tripping

You can apply the 87T Relay Word bit to the transformer trip equation, TRXFMR.

CT Sizing

It is vital that you select adequate current transformers for a transformer differential application. Use the following procedure (based on ANSI/IEEE Std C37.110-1996): IEEE Guide for the Application of Current Transformers Used for Protective Relaying Purposes.

Sizing a CT to avoid saturation for the maximum asymmetrical fault current is ideal but not always possible. Such sizing requires CTs with C-voltage ratings greater than $(1 + X/R)$ times the burden voltage for the maximum symmetrical fault current, where X/R is the reactance-to-resistance ratio of the primary system.

CT Ratio Selection for a Multiwinding Transformer

Step 1. Determine the secondary side burdens in ohms for all current transformers connected to the relay.

Step 2. Select the CT ratio for the highest-rated winding (CTRS, for example) by considering the maximum continuous secondary current, I_{HS}, based on the highest MVA rating of the transformer.

For wye-connected CTs, the relay current, I_{REL}, equals I_{HS}. For delta-connected CTs, I_{REL} equals $\sqrt{3} \bullet I_{HS}$. Select the nearest standard ratio such that I_{REL} is between $0.1 \bullet I_{NOM}$ and $1.0 \bullet I_{NOM}$ A secondary, where I_{NOM} is the relay nominal secondary current, 1 A or 5 A.

Step 3. Select the remaining CT ratios (CTRT–CTRX) by considering the maximum continuous secondary current, I_{LS}, for each winding.

Typically, the CT ratio is based on the rated maximum MVA of the particular winding. If the MVA rating is much smaller than the rating of the largest winding (typically the case for the tertiary delta winding), you can violate the tap ratio limit for the SEL-487E (see *Step 4* and *Step 5*). As before, for wye-connected CTs, I_{REL} equals I_{LS}. For delta-connected CTs, I_{REL} equals $\sqrt{3} \bullet I_{LS}$. Select the nearest standard ratio such that I_{REL} is between $0.1 \bullet I_{NOM}$ and $1.0 \bullet I_{NOM}$ A secondary.

Step 4. The SEL-487E calculates settings TAPS–TAPX if the ratio TAP_{MAX}/TAP_{MIN} is less than or equal to 35.

When the relay calculates the tap settings, it reduces CT mismatch to less than 1 percent. Allowable tap settings are in the range $(0.1–35) \bullet I_{NOM}$.

Step 5. If the ratio $\text{TAP}_{MAX}/\text{TAP}_{MIN}$ is greater than 35, select a different CT ratio to meet the above conditions.

You can often do this by selecting a higher CT ratio for the smallest rated winding, but you may need to apply auxiliary CTs to achieve the required ratio. Repeat *Step 2–Step 5*.

Step 6. Calculate the maximum symmetrical fault current for an external fault, and verify that the CT secondary currents do not exceed your utility standard maximum allowed CT current, typically $20 \cdot I_{NOM}$.

If necessary, reselect the CT ratios and repeat *Step 2–Step 6*.

Step 7. For each CT, multiply the burdens you calculated in Step 1 by the magnitude, in secondary amperes, of the maximum symmetrical fault current you expect for an external fault.

Select a nominal accuracy class voltage for each CT that is greater than twice the calculated voltage. If necessary, select a higher CT ratio to meet this requirement, then repeat *Step 2–Step 7*. This selection criterion helps reduce the likelihood of CT saturation for a fully offset fault current signal.

Note that the effective C-voltage rating of a CT is lower than the nameplate rating if you use a tap other than the maximum. Derate the CT C-voltage rating by a factor of ratio used/ratio maximum.

Delta-Connected CTs

Connecting CTs in delta affects different metering and elements in different ways. In general, delta-connected CTs remove zero-sequence quantities and cause a phase shift and a $\sqrt{3}$ increase in magnitude (with respect to the balanced quantities used in the delta connection). Removing the zero-sequence quantities impacts all ground elements, a phase shift impacts all calculations based on quantities from delta-connected CTs, and the increase in magnitude affects all elements that operate on primary values.

Directional Element

Delta-connected CTs remove zero-sequence quantities, so directional elements are not available for those terminals with delta-connected CTs. For example, if the CTs from Terminal S are delta connected, then directional elements are not available for Terminal S. If the CTs of the remaining terminals are wye-connected, then directional elements are available for the remaining terminals.

Combined Terminals, Thermal Element, and Through-Fault Element

⚠️**WARNING**
Be sure to connect both sets of CTs in the same delta configuration (AB, BC, CA, for example). When you connect the two sets of CTs in different delta configurations (AB, BC, CA, and AC, BA, CB), the phase difference results in incorrect combined current values.

Delta-connected CTs cause a phase shift, so currents from the combined windings (ST, TU, UW, WX) are not available when CTs from one of the two terminals are delta connected. Currents from the combined windings are available if CTs from both terminals are delta-connected. However, be sure to connect both sets of CTs in the same delta configuration because the relay does not check for this condition.

Combined Terminals, Thermal Element, Through-Fault Element, and Event Reporting

Because of the √3 increase in magnitude resulting from the delta-connected CTs, elements that operate on primary current values use the incorrect current values. To correct this, the relay divides the secondary currents by √3 before multiplying by the CT ratio to convert to primary currents.

For the event report, the relay also divides the secondary currents by √3 before multiplying by the CT ratio to convert to primary currents.

In the COMTRADE report, the relay divides the CT ratio in the .cfg file by √3 to compensate for the delta connection. This compensation applies to primary values only. Changing the CT ratio instead of the stored data do not change the secondary current values, so you can inject the secondary values into the relay without any change.

In summary, the relay compensates for delta-connected CTs when reporting or using primary values. No secondary currents are compensated; the relay processes secondary currents at the values the relay terminals measure.

Restricted Earth Fault Element

Restricted earth fault (REF) protection comes from a zero-sequence directional element that provides sensitive detection of ground faults near the neutral of a grounded wye-connected transformer winding. To provide REF protection, the element compares the direction of a reference current, derived from the line-end CTs, with the operating current, obtained from the neutral CT. *Figure 5.26* shows the characteristic of the REF element, with the shaded area indicating the tripping area.
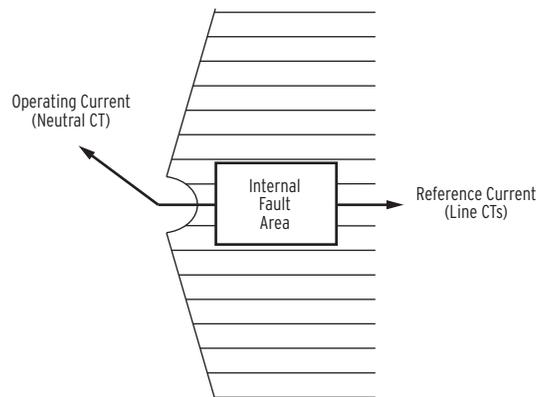
Figure 5.26 REF Directional Element

Because the REF element employs a neutral CT at one end of the winding and a set of three CTs at the line end of the winding, REF protection can detect only ground faults within that particular wye-connected winding. The element is restricted in the sense that protection is limited to ground faults within a zone defined by neutral and line CT placement. This element is intended to be used with solidly grounded transformers; using neutral grounding resistors can effect performance.

The REF element uses a comparison of zero-sequence currents, so the line-end CTs must be connected in wye for the element to function. Delta-connected CTs cancel out all zero-sequence components of the currents, eliminating one of the quantities the REF element needs for comparison.

Figure 5.27 shows the 24 analog inputs of the SEL-487E. Terminal Y consists of three single-phase current inputs that provide three separate inputs for as many as three REF operating quantities.

REF Single-Phase Input
Terminals
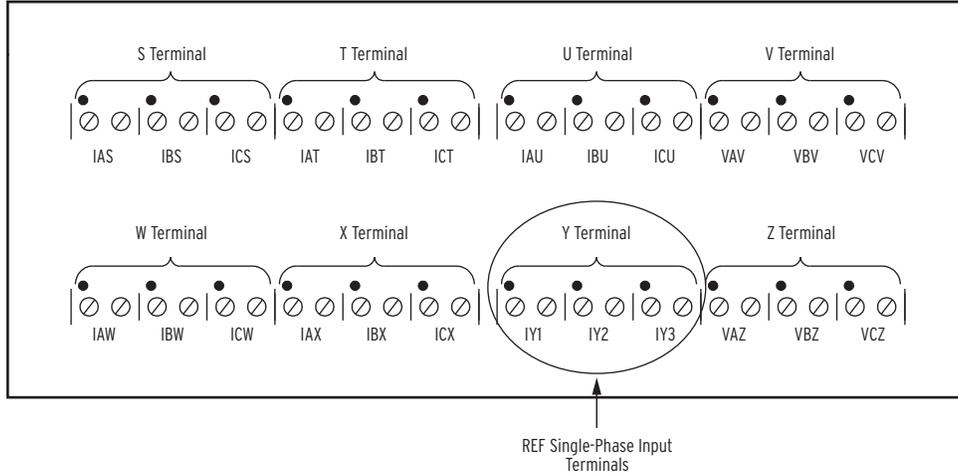
Figure 5.27   REF Terminals

Table 5.3 shows the relationships among the input currents of the Y Terminal and the REF elements. These relationships are not settable; they are fixed and must be observed when you use the REF function. For example, if you select REF 1 for your application, be sure to wire the input current from the neutral CT to IY1.

Table 5.3   Relationships Among Input Currents and REF Elements

Input Current	REF Element
IY1	REF Element 1
IY2	REF Element 2
IY3	REF Element 3

Figure 5.28 shows the REF 1 element logic diagram (REF 2 and REF 3 have similar diagrams) that produces the REF enable output, RF1TCE, and the two bypass outputs IOPNRF1 and IRFFR1P. Note that some of the signal labels below are not Relay Word bits, but are included with this diagram for ease of discussion.

* Signals are labeled in this figure for ease of discussion. These are not Relay Word bits.
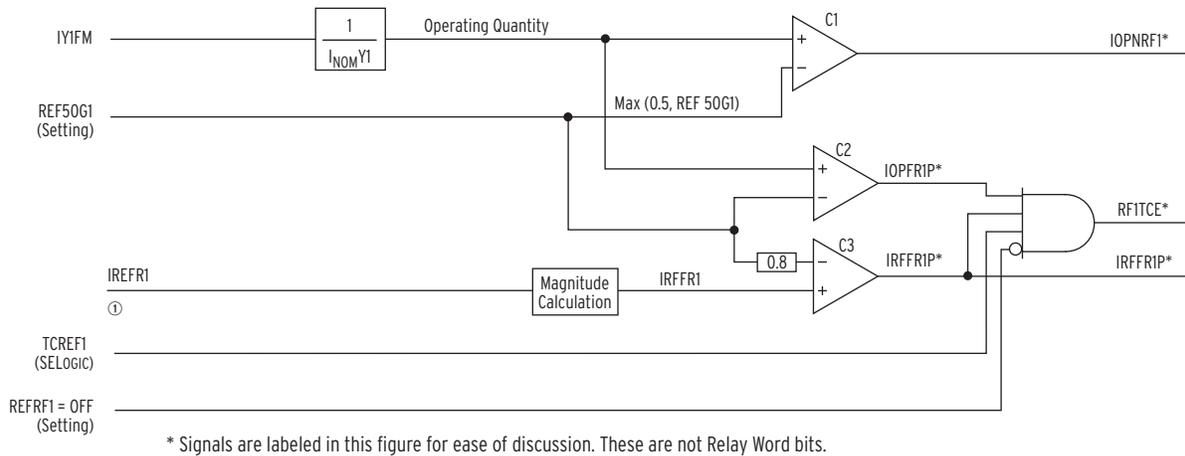
① See *Figure 5.29*.

Figure 5.28 REF 1 Element Enable Logic

IY1FM is the magnitude of the input current from the neutral CT connected to Terminal IY1. The quantity resulting from normalization of the current to 1 A follows two paths. In the top path, Comparator C1 compares the value against the larger of 0.5 (50 percent of the nominal current) and the REF50G1 Group setting. IOPNRF1 asserts if the measured quantity exceeds the threshold. The bypass logic (see *Figure 5.30*) uses IOPNRF1.

In the lower path, Comparator C2 compares the normalized IY1FM value against the REF50G1 Group setting and asserts the signal labeled IOPFR1P if the measured quantity exceeds the threshold. Comparator C3 compares 0.8 of the REF50G1 setting value against IRFFR1, the magnitude of the reference current. The 0.8 multiplier secures the operation of the REFF1 element by ensuring that the IRFFR1P signal always asserts before the IOPFR1P signal.

Switch S2(a–e) selects the zero-sequence vector currents from those line CTs that are part of the REF calculations, as determined by Group setting REFRF*a*, where *a* = 1–3. As an example, refer to *Figure 5.31*. For a single-wye winding, the logic requires one neutral CT and one set of line CTs for the REF function. If this set of line CTs is from Terminal S, then Switch S2a is in position 2, while all other cells of Switch S2 remain in position 1. Current inputs from those terminals in position 1 are not included in any REF element calculations.

After closing the appropriate cells of Switch S2, the relay normalizes the selected input currents to 1 A and sums these currents vectorially to produce the reference current in vector form. In the following step, the relay calculates IRFFR1, the magnitude of the reference current for REF 1.

IOPFR1P and IRFFR1P, together with the torque control equation TCREF1 and setting REFR1, assert output RF1TCE. When RF1TCE asserts, the relay enables the algorithm that performs the directional calculations (see *Figure 5.29*).

Figure 5.29 shows the logic that performs the directional calculations. Switch S operates according to the previous discussion and the logic in *Figure 5.28*. After closing the appropriate cells of Switch S2, the relay converts the currents to primary values by multiplying each current times the appropriate CT ratio. The relay then sums these currents vectorially to produce the reference current in vector form. To bring this value to the same base as the neutral CT, the algorithm divides the reference current by the product of the CT ratio and the neutral CT nominal current. These calculations produce IREFR1, the reference current in vector form. For the operating current, the algorithm normalizes IY1CF to produce IOPR1, the operating current in vector form.
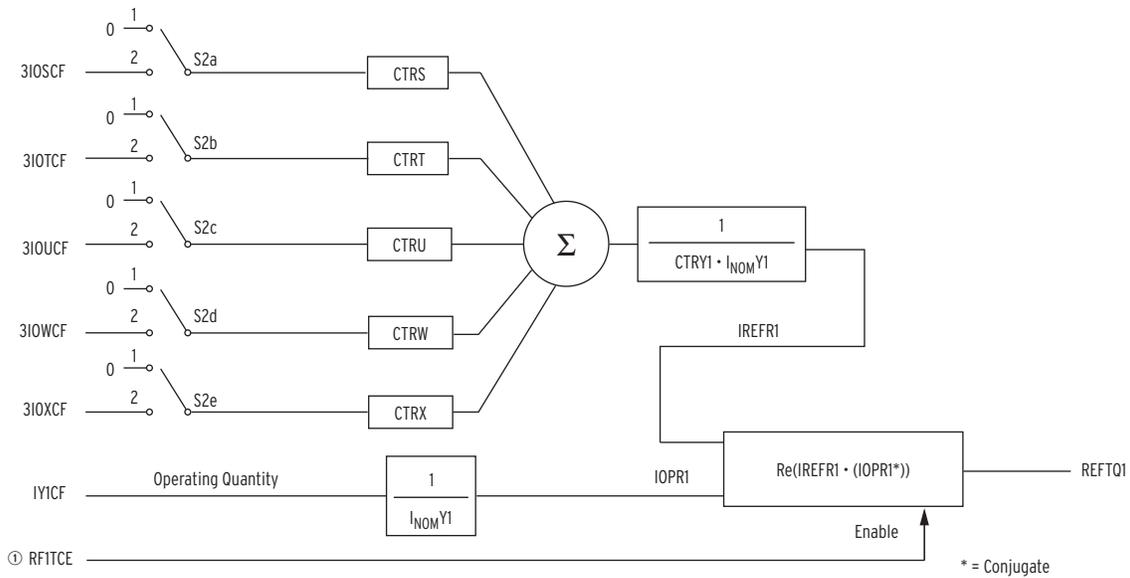
① See *Figure 5.28*.

Figure 5.29   Algorithm That Performs the Directional Calculations

When the algorithm meets the conditions in *Figure 5.28*, the torque control signal asserts and enables the calculations of the directional element. To determine the direction, the algorithm calculates the real part of the product of the reference quantity and the conjugate of the operating quantity. This calculation yields the signed torque quantity REFTQ1 (this calculation is equivalent to |IOPR1| times |IREFR1| times the cosine of the angle between them). REFTQ1 is positive if the angle is within ±90 degrees, indicating a forward or internal fault. Conversely, REFTQ1 is negative if the angle is greater than +90 or less than −90 degrees, indicating a reverse or external fault.

Figure 5.30 shows the logic that compares REFTQ1 to a positive threshold (THRES1P) and a negative threshold (THRES1N). These thresholds are dynamic and are designed to widen the operating angle (e.g., 85 degrees) when sufficient current is present, and they restrict the operating angle (e.g., 30 degrees) for very small currents. This adaptive behavior assures secure and reliable operation of the element under a wide variety of loading conditions. The threshold reference values are equal and opposite to one another.
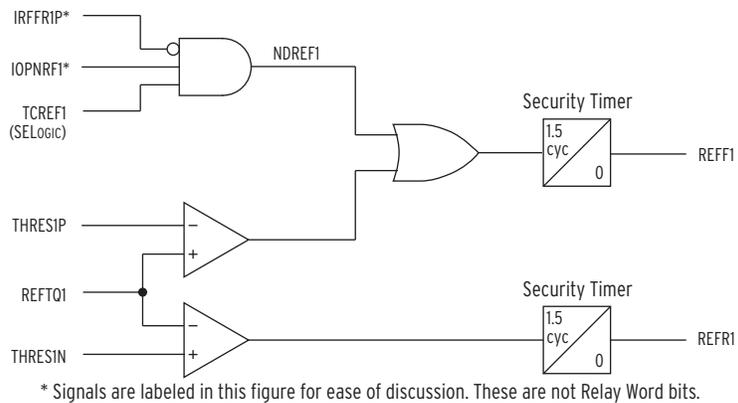
Figure 5.30   REF Element Trip Output

If REFTQ1 exceeds either threshold, it must persist for the duration of the security timer before Relay Word bit REFF1 (forward) or REFR1 (reverse) asserts. Assertion of REFF1 constitutes an internal ground fault.

Figure 5.31 shows the need for the bypass logic (C1) in *Figure 5.28*. For the directional element to produce a meaningful result, both operating and restraint quantities must be present. If Fault F1 occurs with the LV breaker open, no current flows through the LV CT, and there is no reference quantity present.
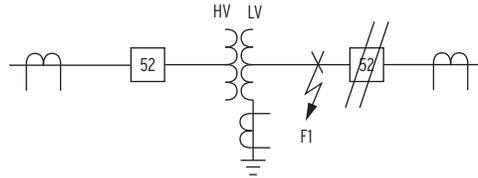
Figure 5.31   Internal Fault With LV Breaker Open

In *Figure 5.30*, the top AND gate has three inputs, namely IOPNRF1 and IRF-FR1P (see *Figure 5.28*), and a SELOGIC control equation TCREF1. IOPNRF1 and negated IRFFR1P identify the condition in *Figure 5.31* in which current flows in the neutral but no current flows in the line. Use TCREF1 to further qualify the bypass condition by checking, for example, the status of the LV breaker. Therefore, when Fault F1 occurs, NDREF1 asserts and clears the fault.

For fast tripping, include REFF1, the output of the REF element, into one or more of the trip equations (Group settings TR*k*) as appropriate. If you want additional security, use the programmable 51 element in *Figure 5.32* to delay tripping. In *Figure 5.32*, the overcurrent element uses the neutral current (IY1FM) as an input quantity. To avoid inadvertent tripping for external faults, use REFF1 (see *Figure 5.30*) in the torque control equation (RF51TC1) of the overcurrent element.
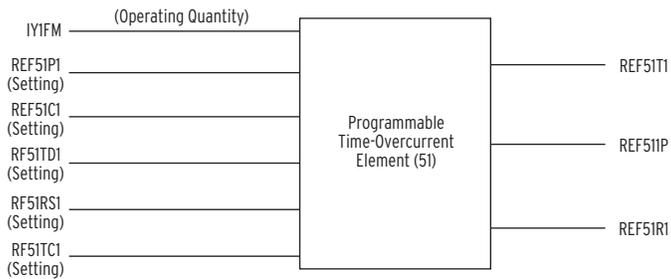
Figure 5.32   Programmable 51 REF Element

REF511P in *Figure 5.32* shows that the inverse-time overcurrent element has picked up. REF51T1 indicates that the element has timed out and REF51R1 is used to indicate that the element has been reset.

Neutral Element

For applications such as frame leakage protection or sustained ground fault protection, the REF element includes a definite-time overcurrent (50) element. *Figure 5.33* shows the REF 50 element, with neutral current IY1FM as an input quantity. If IY1FM exceeds the REF50P1 setting, REF501 asserts and starts the REF Definite-Time Timer. If IY1FM exceeds the REF50P1 setting for a period exceeding the REF50D1 timer setting, REF50T1 asserts. Disable this element by setting REF50P1 = OFF.
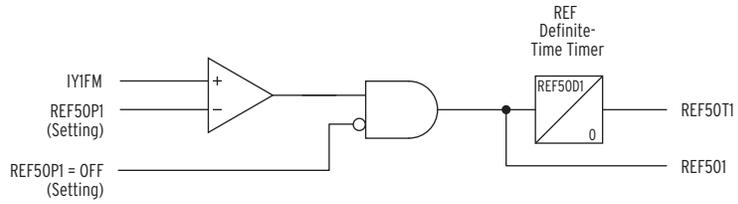
Figure 5.33 REF Neutral Element

Applications and Setting Descriptions
REF Directional Element Enable (EREF)

Use the EREF setting to enable the number of REF elements appropriate for the application. Setting EREF = N disables all REF elements, but not the neutral element. There are no neutral input current/REF element assignment settings: the relationships are fixed as in *Table 5.3*.

Therefore, when you set EREF = 1, the REF element evaluates only an input connected to Terminal IY1; the element ignores inputs connected to IY2 and IY3.

Restraint (Reference) Quantity (REFRFa)

Setting REFRFa (a = 1–3) identifies the terminal or combination of terminals the REF element must include when it calculates the reference current (closing the cells of Switch S in *Figure 5.28* and *Figure 5.29*). Available terminals are those enabled by the ECTTERM setting.

Residual Current Sensitivity Threshold (REF50Ga)

You can set the residual current sensitivity threshold to as low as 0.05 times nominal current (0.25 A for 5 A nominal CT current), the minimum residual current sensitivity of the relay. However, the minimum acceptable value of REF50Ga must be greater than any natural 3I0 unbalance resulting from load conditions.

REF Torque Control (TCREFa)

SELOGIC control equation TCREFa provides a method to externally control the enabling of the directional calculations (see *Figure 5.28*).

REF Neutral Element Instantaneous Overcurrent Pickup (REF50Pa)

REF50Pa is the instantaneous overcurrent pickup setting for the neutral element (see *Figure 5.33*).

REF Neutral Element Overcurrent Time Delay (REF50Da)

REF50Da is the time delay setting for the instantaneous overcurrent element of the neutral element (see *Figure 5.33*).

REF TOC (51) Pickup (REF51Pa)

REF51Pa is the time-overcurrent pickup setting for the programmable 51 element (see *Figure 5.32*).

REF TOC (51) Curve (REF51C*a*)

REF51C*a* is the time-overcurrent curve selection setting for the programmable 51 element (see *Figure 5.32*).

REF TOC (51) Time Dial (RF51TD*a*)

RF51TD*a* is the time-dial (time multiplier) setting for the programmable 51 element (see *Figure 5.32*).

REF TOC (51) Electromechanical Reset (RF51RS*a*)

RF51RS*a* is the time-dial (time multiplier) electromechanical reset setting for the programmable 51 element (see *Figure 5.32*).

REF TOC (51) Torque Control (RF51TC*a*)

RF51TC*a* is the torque control setting for the programmable 51 element (see *Figure 5.32*).

Selection of the Restraint Quantity

The operating quantity/reference quantity relationship is according to software assignment (instead of a fixed relationship), so you can apply the REF elements to any primary plant configuration with the correct CT arrangement. In general, identify all lines that are electrically connected to the grounded winding that you want to protect with the REF element. Then enter those terminals at the REFRF*a* setting. Following are examples of a few applications, assuming that both differential and REF elements protect the transformer in each example.

Figure 5.34 shows an ungrounded HV winding and a grounded-wye LV winding. Because we need two terminals for the differential protection, set ECTTERM = S, T, and assign Terminal S to the HV side and Terminal T to the LV side. Set EREF = 1 to enable one REF element (this setting dictates that we connect the neutral CT to Terminal IY1). Although Terminals S and T are enabled, only Terminal T electrically connects to the winding earmarked for REF protection. Therefore, set REFRF1 = T.
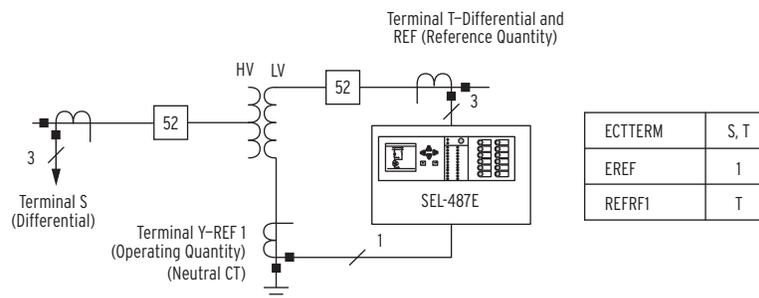
Figure 5.34 Single-Wye Winding REF Application

Figure 5.35 shows an autotransformer. Because we need two terminals for the differential protection, set ECTTERM = S, T, and assign Terminal S to the HV side and Terminal T to the LV side. Set EREF = 1 to enable one REF element (this setting dictates that we use IY1). In this case, both Terminal S and Terminal T connect electrically to the winding earmarked for REF protection. Therefore, set REFRF1 = S, T.
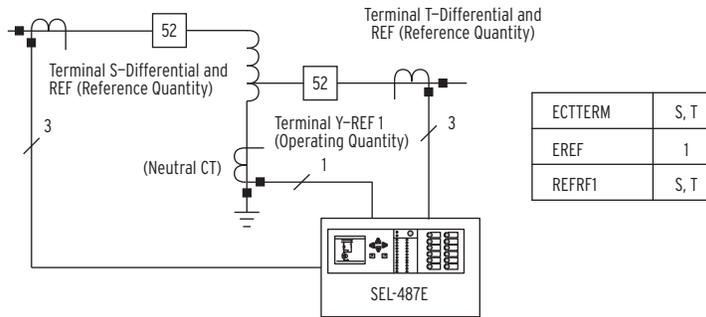
Figure 5.35 Autotransformer REF Application

Figure 5.36 also shows an autotransformer, but in this application, the HV side has two CTs (breaker-and-a-half application). Because we need three terminals for the differential protection, set ECTTERM = S, T, U, and assign Terminals S and T to the HV side and Terminal U to the LV side. Set EREF = 1 to enable one REF element (this setting dictates that we use IY1). In this case, Terminal S, Terminal T, and Terminal U connect electrically to the winding earmarked for REF protection. Therefore, set REFRF1 = S, T, U.
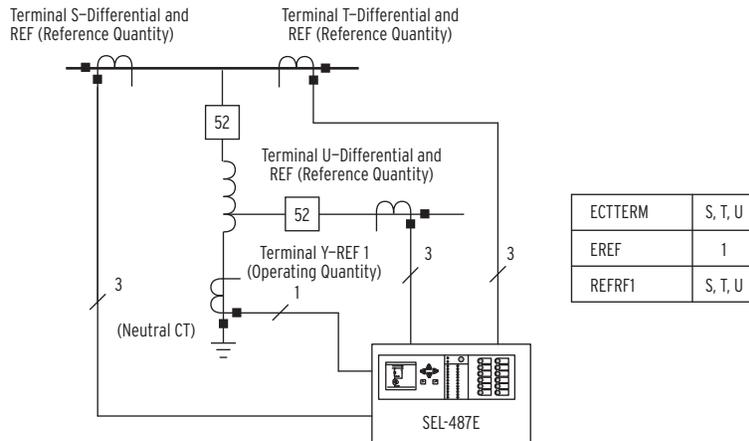
Figure 5.36 Autotransformer With Two-HV Current Transformer REF Application

Figure 5.37 shows a three-winding wye-wye transformer with tertiary delta. Assume that no load connects to the delta, so that the differential calculations exclude the delta. Because we need two terminals for the differential protection, set ECTTERM = S, T, and assign Terminals S to the HV side and Terminal T to the MV side. In contrast to an autotransformer, the HV and MV windings of this transformer are not connected electrically, and we need a separate REF for each winding. Set EREF = 2 to enable two REF elements (this setting dictates that we use IY1 and IY2). On the assumption that we assign REF 1 to the HV side, set REFRF1 = S, and set REFRF2 = T for the MV side.
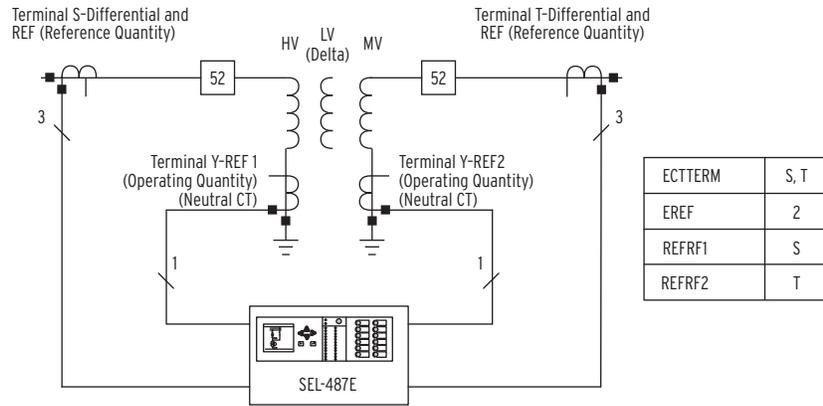
Figure 5.37   Three-Winding Transformer With Two REF Elements

Combined Overcurrent Values

Figure 5.38 shows a breaker-and-a-half layout on the transformer HV side and a single busbar on the LV side. On the HV side, the HV current flows through both CTS and CTT, but the total current flows through CTU and the LV side. Current distribution through CTS and CTT is a function of system conditions, so the proper coordination with CTU involves using the sum of CTS and CTT. *Figure 5.39* shows the result of the combined current values in the SEL-487E. The relay adds the currents from CTS and CTT to form the equivalent of a single CT.

Be aware that the relay combines the current values only if the corresponding terminal current settings for the CT ratio, CT winding connection type, and voltage reference terminal are identical (CTR*m*, CTCON*m*, and VREF*m* settings, respectively) and the terminals have the same nominal current rating (i.e., 5 A or 1 A). For example, Terminals S and T could not be combined if CTCONS = Y and CTCONT = D.

Furthermore, when both CTs are delta connected, be sure to connect both sets of CTs in the same delta configuration, because the relay does not check for this condition (see *Delta-Connected CTs on page 5.40*).

You can configure the overcurrent, time-overcurrent, and directional overcurrent elements to use predefined combinations of secondary currents, namely the ST, TU, UW, and WX combinations.
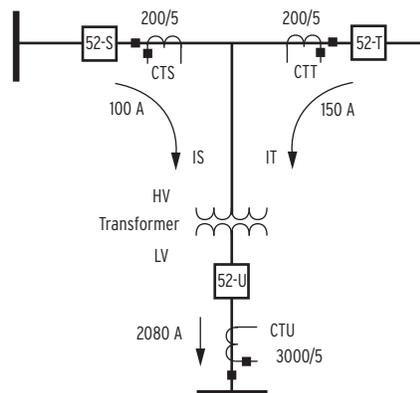
Figure 5.38   Two CTs on HV Side
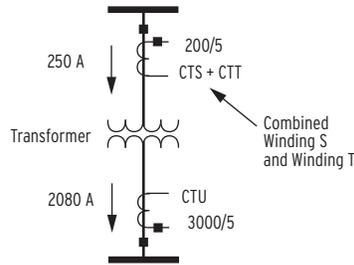
Figure 5.39   Equivalent Single CT on HV Side

Overcurrent Elements

NOTE: If the relay is using a remote data acquisition system, such as TiDL, the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

The SEL-487E provides three levels of instantaneous overcurrent elements (50) for phase, negative-sequence, and zero-sequence currents for each of the five terminals (S, T, U, W, X), combined terminals (ST, TU, UW, WX), and 10 configurable time-overcurrent (51) elements. These overcurrent elements are nondirectional, but you can make any of the 50 or 51 elements directional with a choice of phase and sequence directional elements (see *Directional Element on page 5.40*).

Phase Instantaneous Overcurrent Elements

Figure 5.40 shows the logic for the phase instantaneous overcurrent element. At the top of the logic are four settings that enable the overcurrent element. All four settings must evaluate to a logical 1 to enable the overcurrent element. To enable the Level 1 instantaneous overcurrent element for Terminal S, apply the following settings: ECTTERM = S, … , E50 = S, … , E50S = P, and 50SP1P = 4 (any setting within the range other than OFF).
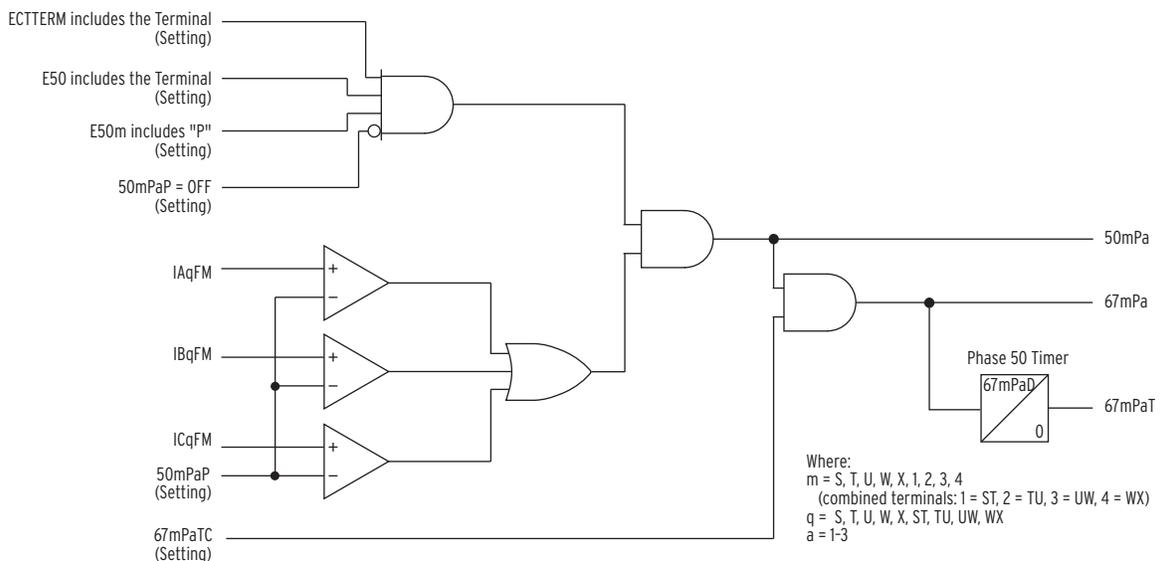
Figure 5.40   Phase Instantaneous Overcurrent Element

Setting 50SP1P also provides the reference value against which three comparators test the three phase currents (IAqFM, IBqFM, ICqFM). If the element is enabled, and any phase current exceeds the 50SP1P setting value, then Relay Word bit 50SP1 asserts.

Use the torque-control setting 67*m*P*a*TC to combine the 50 element with other functions such as the directional element, or to add a time delay. For a time delay (Terminal S, Level 1), set 67SP1TC = 1 (or any other appropriate condition such as the directional element or a breaker auxiliary contact status), and set 67SP1D to the desired time delay. If the element is enabled, and any phase current exceeds the 50SP1P setting value, then Relay Word bits 50SP1 and 67SP1 assert instantaneously, and Relay Word bit 67SP1T asserts when the Phase 50 timer times out.

Negative-Sequence Instantaneous Overcurrent Elements

Figure 5.41 shows the logic for the negative-sequence instantaneous overcurrent element. This element operates similarly to the phase instantaneous overcurrent element, except that the element uses negative-sequence values instead of phase values.

Where: m = S, T, U, W, X, 1, 2, 3, 4
                     (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX)
           q = S, T, U, W, X, ST, TU, UW, WX
           a = 1-3
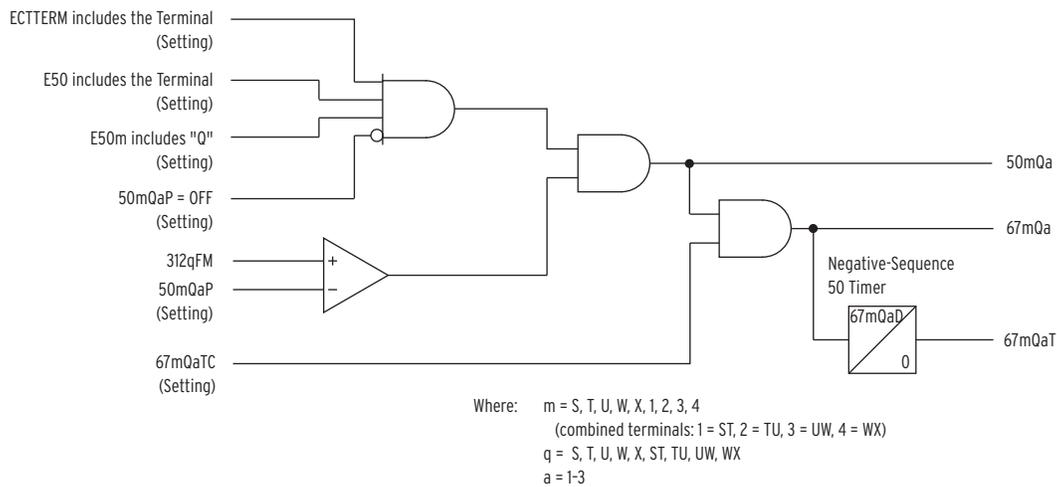
Figure 5.41   Negative-Sequence Instantaneous Overcurrent Element

Zero-Sequence Instantaneous Overcurrent Elements

Figure 5.42 shows the logic for the zero-sequence instantaneous overcurrent element. This element operates similarly to the phase instantaneous overcurrent element, except that the element uses zero-sequence values instead of phase values.

Where: m = S, T, U, W, X, 1, 2, 3, 4
                     (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX)
           q = S, T, U, W, X, ST, TU, UW, WX
           a = 1-3
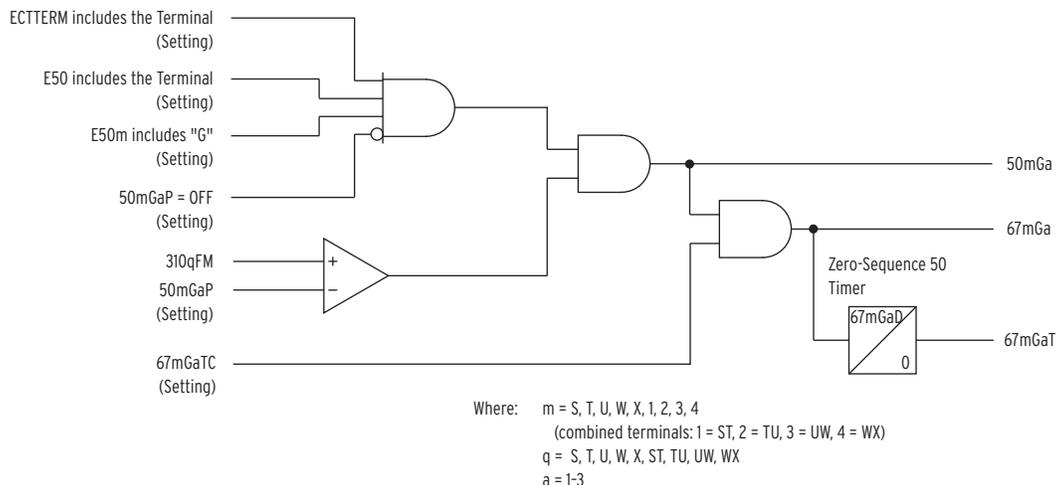
Figure 5.42   Zero-Sequence Instantaneous Overcurrent Element

Setting Descriptions
E50 (Definite-Time Overcurrent and Directional Element Enable)

Setting E50 is a composite setting that identifies the following three protection options for each winding:

➤ Windings that require only definite-time overcurrent elements

➤ Windings that require only directional elements

➤ Windings that require both definite-time overcurrent elements and directional elements

For example, at a particular substation you want the following protection:

➤ Winding S: negative-sequence definite-time overcurrent only

➤ Winding T: only directional control (directional elements for time overcurrent [51] protection)

➤ Winding U: both definite-time overcurrent protection (Level 1) and directional control

➤ Windings W and X: not used

Figure 5.43 shows the flow diagram for setting the three protection options (gray blocks are not used).
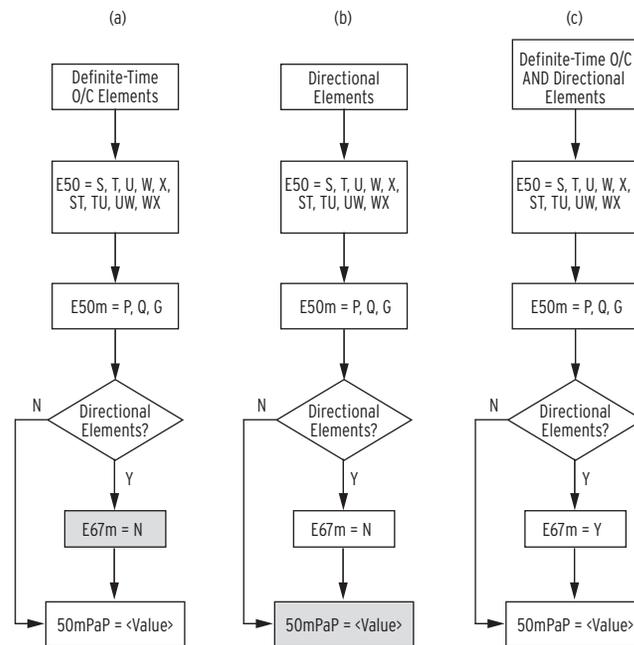
Figure 5.43   Three Settings Possibilities

In general, regardless of the function you want (overcurrent or directional), always enter the E50 and E50*m* settings. In this example, include Windings S, T, and U in the Group setting ECTTERM to enable these windings for processing, as shown in *Figure 5.44*. Also select the PT for the directional element polarizing (EPTTERM setting). The voltage reference terminal selection setting, VREF*n* (*n* = S, T, U, W, X), also needs to be set to the PT to enable the directional elements E67*m*.
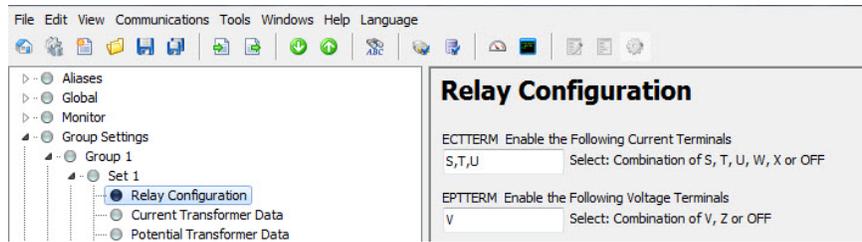
Figure 5.44   ECTTERM and EPTTERM Settings

After enabling the CTs for processing, enter Windings S, T, and U in the Group setting E50 (see *Figure 5.45*). *Figure 5.45* also shows the selection of the 51 element that must have directional control. The 51 elements are not winding specific, so setting the winding CT/51 elements correlation occurs later.
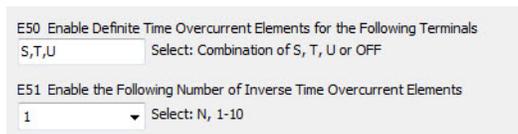
Figure 5.45   E50 and E51 Enables

Use the E50*m* setting to specify the type of overcurrent elements you want to use, both for overcurrent elements and for directional elements. Because Winding S requires negative-sequence definite-time overcurrent only, set E50S = Q.
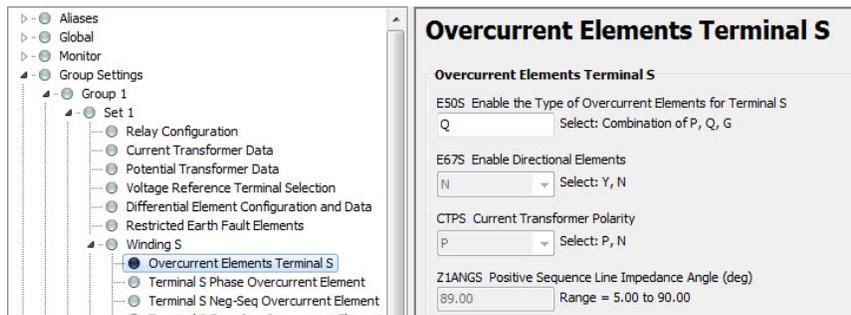
Figure 5.46   Enable Negative-Sequence Definite-Time Overcurrent for Winding S

Figure 5.47 shows the negative-sequence definite-time overcurrent settings. The setting 50SQ1P is the Level 1 negative-sequence overcurrent element pickup value (arbitrarily set at 12). The setting 67SQ1TC is the torque-control setting for the negative-sequence overcurrent element (refer to *Figure 5.41* for the logic diagram). In this example, set 67SQ1TC = 1 (permanently enabled) to assert the bottom input of the timer AND gate in *Figure 5.41*. The last setting is 67SQ1D, the negative-sequence overcurrent element time delay, set in *Figure 5.47* to an arbitrary value of 20 cycles.
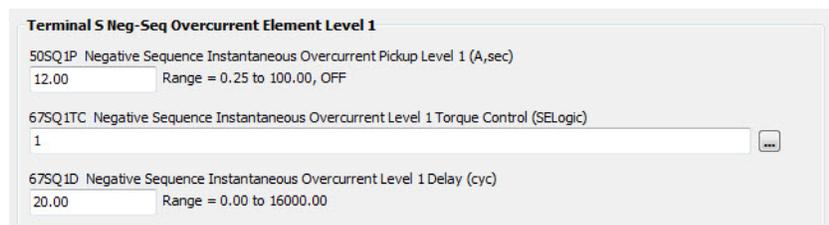
Figure 5.47   Negative-Sequence Definite-Time Overcurrent Settings

This concludes the negative-sequence definite-time overcurrent settings for Winding S.

Winding T protection calls for a directional element 51. To enable the T-terminal directional element, the voltage reference terminal selection setting, VREFT, must be set to a voltage. In this example, V is the only voltage terminal available in EPTTERM, so VREFT = V as shown in *Figure 5.48*. *Figure 5.49* shows the settings to enable the directional element (E50T = P, G, Q), and *Figure 5.50* shows the settings to disable the definite-time overcurrent Level 1 elements (50TP1P = OFF) for Winding T.

VREFT Select Voltage Reference for Terminal T
V   Select: OFF, V
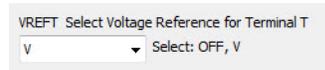
Figure 5.48   Voltage Reference Selection Setting

Overcurrent Elements Terminal T

Overcurrent Elements Terminal T

E50T Enable the Type of Overcurrent Elements for Terminal T
P,Q,G   Select: Combination of P, Q, G

E67T Enable Directional Elements
Y   Select: Y, N

CTPT Current Transformer Polarity
P   Select: P, N

Z1ANGT Positive Sequence Line Impedance Angle (deg)
89.00   Range = 5.00 to 90.00

Z0ANGT Zero Sequence Line Impedance Angle (deg)
85.00   Range = 5.00 to 90.00

EADVST Enable Advanced Setting
N   Select: Y, N

Figure 5.49   Enable Directional Elements

Terminal T Phase Overcurrent Element Level 1

50TP1P Phase Instantaneous Overcurrent Pickup Level 1
OFF   Range = 0.25 to 100.00, OFF

Figure 5.50   Disable Definite-Time Overcurrent Elements

Enable the directional elements by setting E67T = Y. This makes the CTPT, Z1ANGT, Z0ANGT (E50T includes both P and G) and EADVST settings available. With 50TP1P = OFF, the phase overcurrent elements are disabled, so that only the directional elements are active for Winding T.

Figure 5.51 shows the settings for the Winding T directional 51 element. For this example, do not use adaptive settings for the pickup and time-dial settings. Set the operating quantity (51O01 = IMAXTF), the pickup setting (51P01), Curve type (51C01), time dial (51TD01), and the type of reset (51RS01).

Use setting 51TC01 to add directional control to the 51 element. Setting 51TC01 = TF32G (negative- and zero-sequence direction) OR TF32P (phase direction) causes the 51 element to be active only for forward faults.
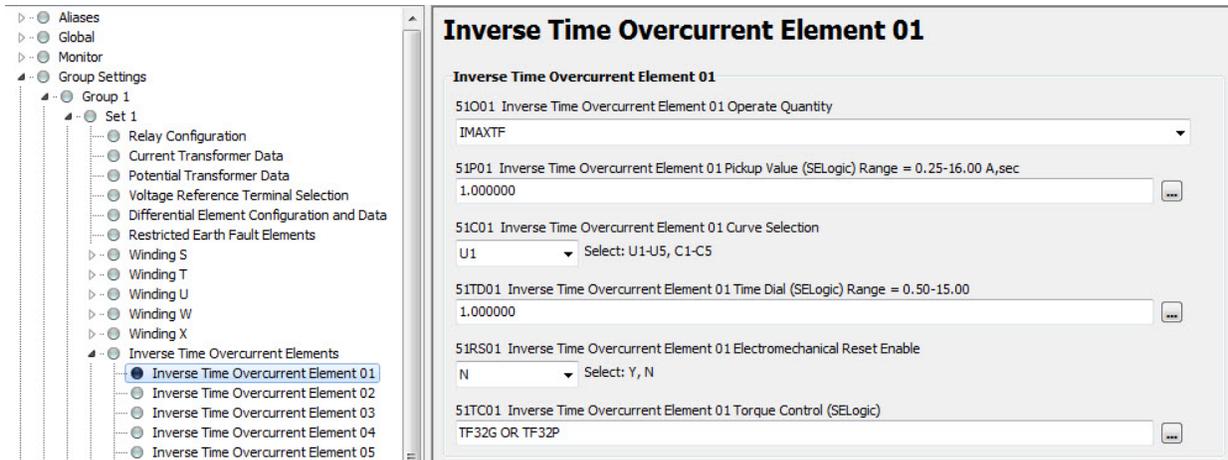
Figure 5.51 Winding T Directional 51 Element Settings

This concludes the directional 51 settings for Winding T.

Winding T protection calls for one level of directional definite-time overcurrent protection. Similar to *Figure 5.48*, VREFU must be set to an enabled voltage terminal to enable the E67U directional element. *Figure 5.52* shows the settings to enable the directional element (E50U = P, G, Q and E67U = Y).
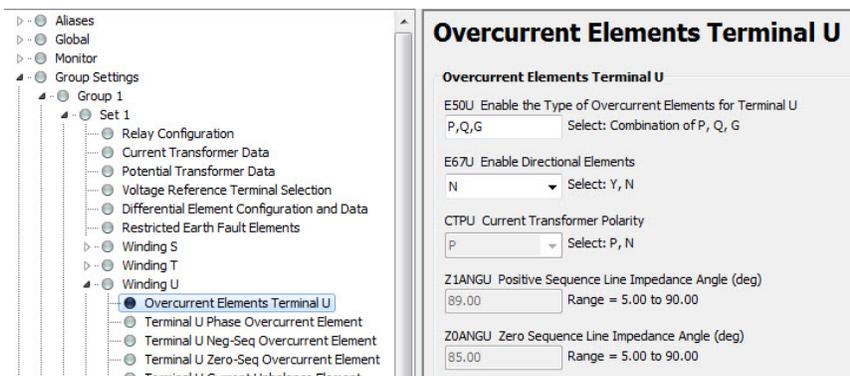
Figure 5.52 Enable Directional Elements for Winding U

With the directional elements enabled, set the 50 elements settings, as shown in *Figure 5.53*. To make the 50 elements directional, enter the forward directional Relay Word bits (UF32P and UF32G) in the 67UP1TC torque equation.

Figure 5.53   Winding U Directional 50 Element Setting

Only one level of overcurrent protection is necessary, so leave 50UP2P = OFF. This concludes the directional 50 settings for Winding U.

E50*m* (50 Function Enable)

After identifying the terminal(s) that requires definite-time overcurrent/directional protection with the E50 setting, select here the specific instantaneous overcurrent element(s)/directional type for each terminal(s). Choose from among phase (P), negative-sequence (Q), zero-sequence (G), or any combination of P, Q, and G.

50*m*P*a*P (Phase Element Pickup)

Setting 50*m*P*a*P is the current pickup setting in secondary amperes for the phase instantaneous overcurrent element. For a 5 A relay, the range is 0.25–100.00 A, sec. The range for a 1 A relay is 0.05–20.00 A, sec.

67*m*P*a*TC (Phase Element Torque Control)

NOTE: This setting does not affect the 50*m*P*a* outputs (see *Figure 5.40*).

Use the torque-control setting to specify conditions under which the element must be active. The default setting is *m*F32P, so that the 67*m*P*a* and 67*m*P*a*T functions can only assert if the phase directional element declares a fault in the forward direction. With the torque equation set to 1 (67SP1TC = 1, Terminal S, Level 1), the overcurrent element is nondirectional and active constantly.

67*m*P*a*D (Phase Element Time Delay)

NOTE: This setting is active only if 67*m*P*a*TC asserts.

Set the duration of the phase element time delay with this setting.

50*m*Q*a*P (Negative-Sequence Element Pickup)

Setting 50*m*Q*a*P is the current pickup setting in secondary amperes for the negative-sequence instantaneous overcurrent element. For a 5 A relay, the range is 0.25–100.00 A, sec. The range for a 1 A relay is 0.05–20.00 A, sec.

67*m*Q*a*TC (Negative-Sequence Element Torque Control)

NOTE: This setting does not affect the 50*m*Q*a* outputs (see *Figure 5.41*).

Use the torque-control setting to specify conditions under which the element must be active. The default setting is *m*F32Q, so that the 67*m*P*a* and 67*m*P*a*T functions can only assert if the negative-sequence directional element declares a fault in the forward direction. With the torque equation set to 1 (67SQ1TC = 1, Terminal S, Level 1), the overcurrent element is nondirectional and active constantly.

67*m*Q*a*D (Negative-Sequence Element Time Delay)

NOTE: This setting is active only if 67*m*Q*a*TC asserts.

Set the duration of the negative-sequence element time delay with this setting.

50*m*G*a*P (Zero-Sequence Element Pickup)

50*m*G*a*P is the current pickup setting in secondary amperes for the zero-sequence instantaneous overcurrent element (shown is the range for a 5 A relay; the range is 0.05 to 20 for a 1 A relay).

67*m*G*a*TC (Zero-Sequence Element Torque Control)

NOTE: This setting does not affect the 50*m*G*a* outputs (see *Figure 5.42*).

Use the torque-control setting to specify conditions under which the element must be active. The default setting is *m*F32G, so that the 67*m*P*a* and 67*m*P*a*T functions can only assert if the zero-sequence directional element declares a fault in the forward direction. With the torque equation set to 1 (67SG1TC = 1, Terminal S, Level 1), the overcurrent element is nondirectional and active constantly.

67*m*G*a*D (Zero-Sequence Element Time Delay)

NOTE: This setting is active only if 67*m*G*a*TC asserts.

Set the duration of the zero-sequence element time delay with this setting.

Selectable Time-Overcurrent Element (51)

NOTE: If the relay is using a remote data acquisition system, such as TiDL, the operating times will be delayed by 1.5 ms. Use caution when setting the relay coordination times to account for this added delay.

Instead of having dedicated inverse-time overcurrent elements (also known as Inverse Definite Minimum Time or IDMT) for each winding, the SEL-487E offers the flexibility of 10 unassigned time-overcurrent elements, each with the choice of five U.S. and five IEC operating curves. Unassigned means that the 51 elements are not assigned to a specific transformer winding, but they are available for assignment, as the application requires (see *Table 5.6*).

Be sure to include the windings selected as 51 element input quantities in the ECTTERM setting. For example, if IMAXSF (see *Table 5.6*) is the input for element 51O01 and if IMAXTF is the input for element 51O02, then set ECTTERM = S, T.

Inverse-time overcurrent elements are not enabled in the default settings. Enable the inverse-time overcurrent elements by setting E51 = *xx* (*xx* = 01–10). After you enable these elements, the inverse-time overcurrent elements up to and including the number *xx* you entered at the E51 = prompt are active. For example, if you want to use six inverse-time overcurrent elements for your application, set E51 = 6. Inverse-time overcurrent elements 1–6 become active.

Table 5.4 shows the five U.S. characteristics, and *Table 5.5* shows the five IEC characteristics. Each table shows the five operating time equations, together with the five electromechanical reset characteristic equations.

Table 5.4 U.S. Operate and Reset Curve Equations

Curve Type	Operating Time	Reset Time
U1 (Moderately Inverse)	$T_P = TD \cdot \left(0.0226 + \dfrac{0.0104}{M^{0.02} - 1}\right)$	$T_R = TD \cdot \left(\dfrac{1.08}{1 - M^2}\right)$
U2 (Inverse)	$T_P = TD \cdot \left(0.180 + \dfrac{5.95}{M^2 - 1}\right)$	$T_R = TD \cdot \left(\dfrac{5.95}{1 - M^2}\right)$
U3 (Very Inverse)	$T_P = TD \cdot \left(0.0963 + \dfrac{3.88}{M^2 - 1}\right)$	$T_R = TD \cdot \left(\dfrac{3.88}{1 - M^2}\right)$
U4 (Extremely Inverse)	$T_P = TD \cdot \left(0.02434 + \dfrac{5.64}{M^2 - 1}\right)$	$T_R = TD \cdot \left(\dfrac{5.64}{1 - M^2}\right)$
U5 (Short-Time Inverse)	$T_P = TD \cdot \left(0.00262 + \dfrac{0.00342}{M^{0.02} - 1}\right)$	$T_R = TD \cdot \left(\dfrac{0.323}{1 - M^2}\right)$

Table 5.5 IEC Operate and Reset Curve Equations

Curve Type	Operating Time	Reset Time
C1 (Standard Inverse)	$T_P = TD \cdot \left(\dfrac{0.14}{M^{0.02} - 1}\right)$	$T_R = TD \cdot \left(\dfrac{13.5}{1 - M^2}\right)$
C2 (Very Inverse)	$T_P = TD \cdot \left(\dfrac{13.5}{M - 1}\right)$	$T_R = TD \cdot \left(\dfrac{47.3}{1 - M^2}\right)$
C3 (Extremely Inverse)	$T_P = TD \cdot \left(\dfrac{80}{M^2 - 1}\right)$	$T_R = TD \cdot \left(\dfrac{80}{1 - M^2}\right)$
C4 (Long-Time Inverse)	$T_P = TD \cdot \left(\dfrac{120}{M - 1}\right)$	$T_R = TD \cdot \left(\dfrac{120}{1 - M}\right)$
C5 (Short-Time Inverse)	$T_P = TD \cdot \left(\dfrac{0.05}{M^{0.04} - 1}\right)$	$T_R = TD \cdot \left(\dfrac{4.85}{1 - M^2}\right)$

where:

T_P = Operate time

T_R = Reset time

TD = Time dial (multiplier)

M = Multiple of pickup current ($I_{measured}/I_{pickup}$)

Figure 5.54–Figure 5.56 show the five U.S. curves and the five IEC curves.

U.S. Moderately Inverse Curve: U1

U.S. Inverse Curve: U2

U.S. Very Inverse Curve: U3

U.S. Extremely Inverse Curve: U4
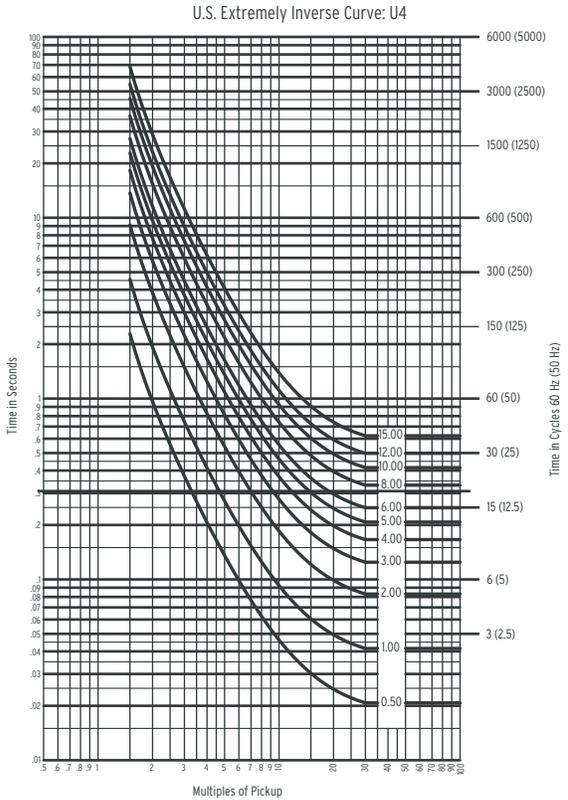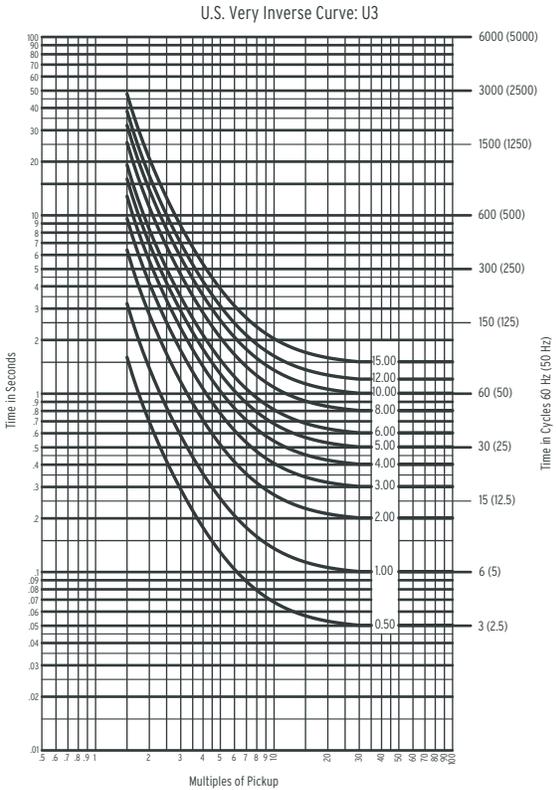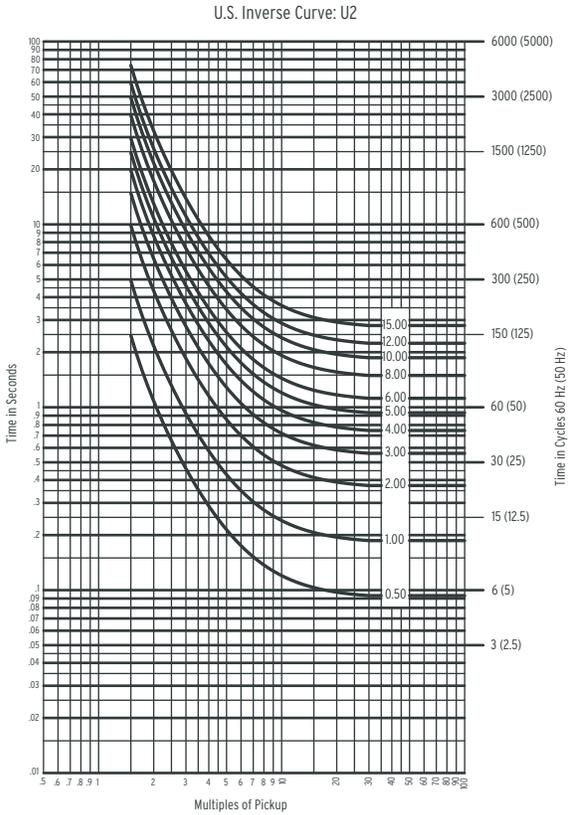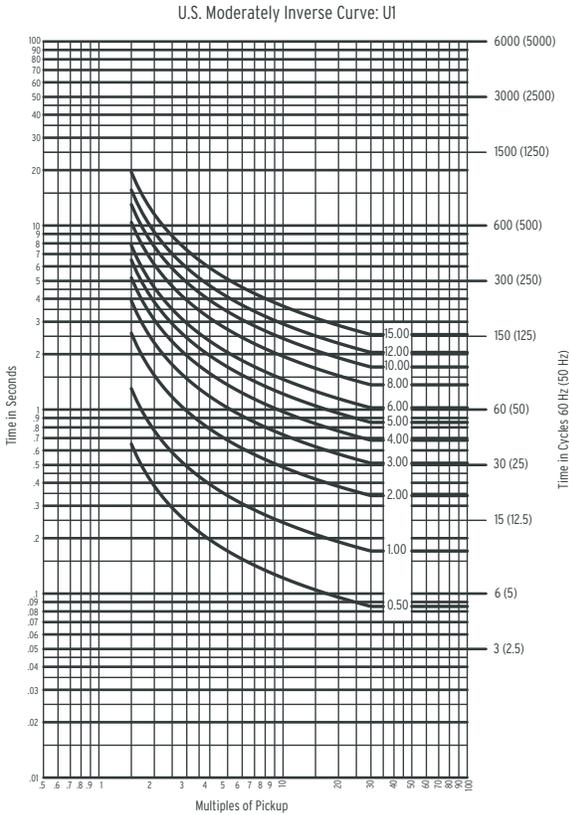
Figure 5.54   U.S. Curves: U1, U2, U3, and U4

U.S. Short-Time Inverse Curve: U5

IEC Class A Curve (Standard Inverse): C1

IEC Class B Curve (Very Inverse): C2

IEC Class C Curve (Extremely Inverse): C3
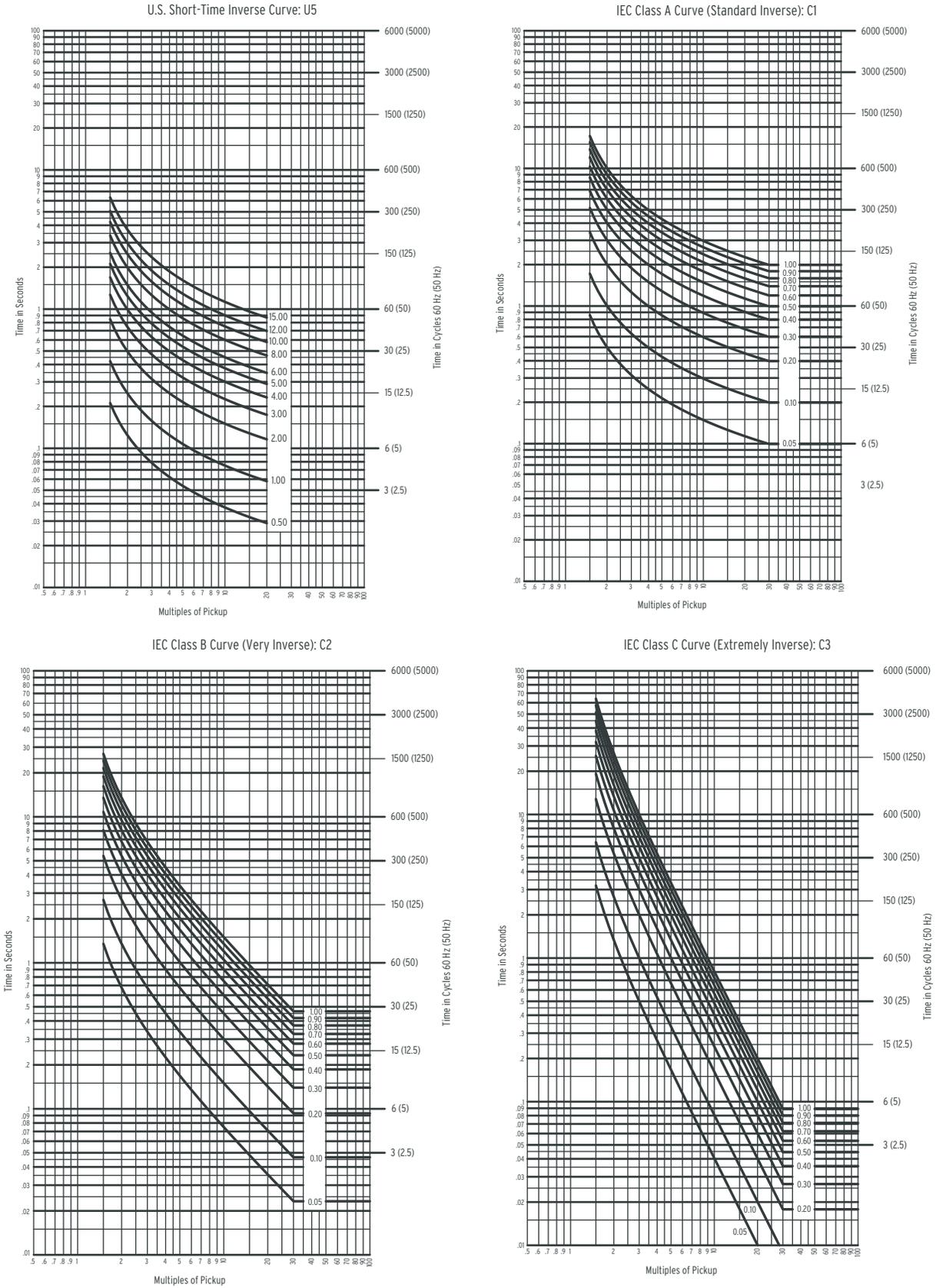
Figure 5.55   U.S. Curve U5 and IEC Curves C1, C2, and C3
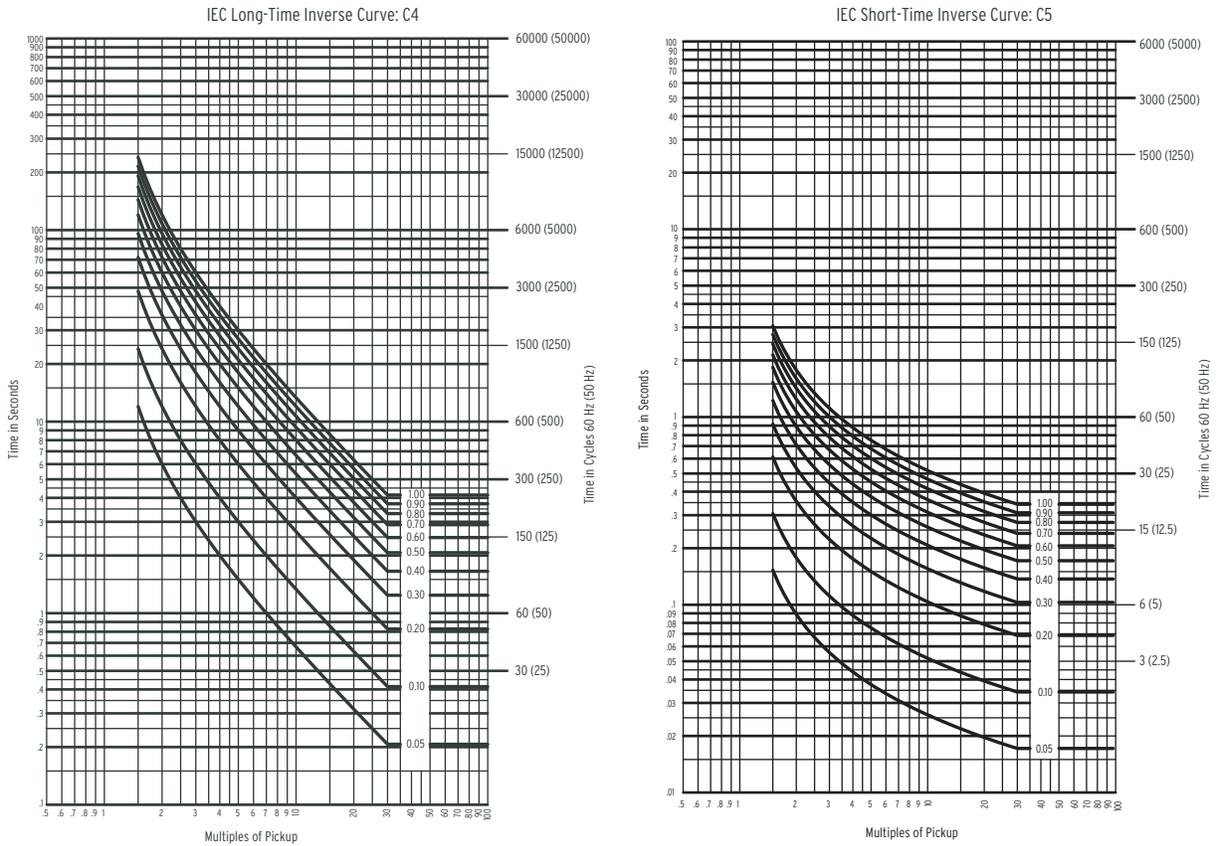
Figure 5.56   IEC Curves C4 and C5

Figure 5.57 uses Element 01 as an example to show the logic for the 51 element. All five inputs are Group settings. Essentially, the logic compares the magnitude of an operating quantity (51O01) to pickup setting 51P01.
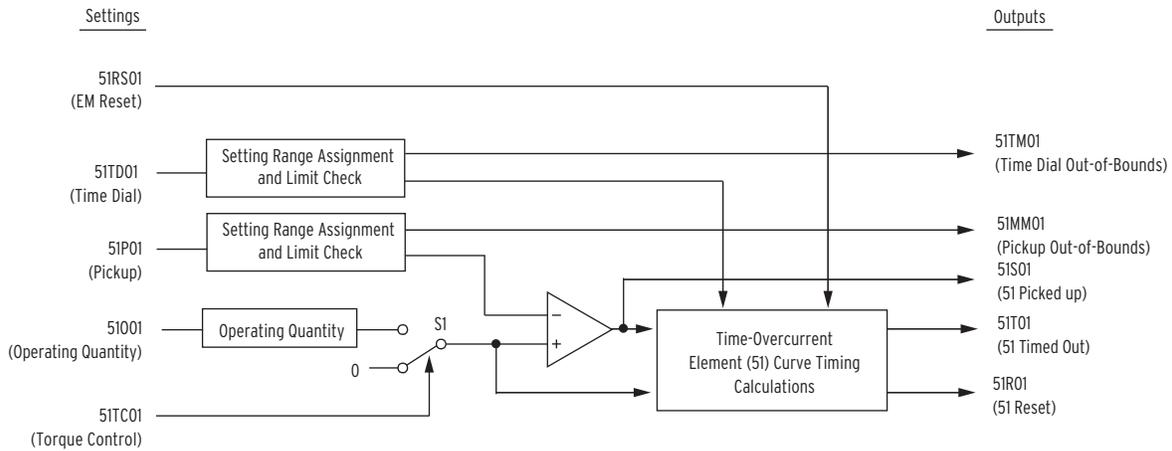
Figure 5.57   Time-Overcurrent Element

Operating Quantity

The 51 elements are unassigned, so you can select the operating quantity from many phase and sequence quantities, either fundamental or root-mean-square (rms), as *Table 5.6* shows.

Table 5.6 Fundamental or RMS Operating Quantities[a]

	Fundamental Quantities	RMS Quantities
Phase	IpmFM, IMAXmF	IpmRMS, IMAXmR
Combined	IpqpFM, IMAXqpF	IpqpRMS, IMAXqpR
Sequence	I1mM, 3I2mM, 3I0mM, I1qpM, 3I2qpM, 3I0qpM	

[a] Where:
p = A, B, C
m = S, T, U, W, X
qp = ST, TU, UW, WX

Pickup and Time-Dial Settings

NOTE: The 51 elements can combine terminals with mismatched CT ratios. In such a case, use the larger of the two CT ratios when selecting your multiple of pickup setting.

Pickup setting 51P01, operating on the ratio of the measured current to the pickup setting (multiple of pickup setting), moves the characteristic horizontally to vary the pickup current; time-dial (multiplier) setting 51TD01 moves the curve vertically to vary the operating time for a given multiple of pickup.

Both pickup (51P01) and time-dial (51TD01) settings are math variables instead of fixed settings. SEL math variables, unlike fixed settings that cannot be dynamically changed, allow for the adaptive changing of pickup and time-dial settings without the need for changing relay setting groups.

However, if your installation does not require adaptive pickup and/or time-dial settings changes, use the time-overcurrent element as a conventional 51 element. For a conventional element, simply enter the pickup and time-dial settings as numbers, such as:

51P01 := **1.5**
51TD01 := **1**

Setting Range Assignment and Limit Checks

Because the relay accepts both 1 A and 5 A secondary CTs, the relay assigns the element pickup setting range only after you select the operating quantity. For example, if the relay determines (from the part number) that Winding S is a 5 A CT, then the relay assigns the range 0.25 to 16.00 as the pickup range of all 51 elements that use any of the Winding S quantities.

Example 5.5

Single Terminal S—5 A CT secondary

Terminal S has a 5 A nominal CT input, so the range is 0.25 (lower limit) to 16.0 (upper limit).

Example 5.6

Single Terminal T—1 A CT secondary

Terminal T has a 1 A nominal CT input, so the range is 0.05 (lower limit) to 3.2 (upper limit).

Upper and Lower Range Limits

When you use SEL math variables, the selected analog value can exceed the upper value of the pickup range, or it can fall below the lower value of the pickup range. When this happens, the relay assigns the appropriate threshold value to the element and continues to calculate the trip time. For the 51P*nn* pickup settings, the upper threshold is 3.2 for 1 A relays and 16 for 5 A relays. The lower threshold is 0.05 for 1 A relays and 0.25 for 5 A relays. For the 51TD*nn* time-dial settings, the U.S. curve thresholds are 0.5 and 15, and the IEC thresholds are 0.05 and 1.0. In addition, the relay also asserts the appropriate Relay Word bits: 51MM01 (pickup value out of bounds) and/or 51TM01 (time-dial value out of bounds).

Example 5.7

For example, you want a 1 A relay to pick up at 1.5 A when IN101 asserts and to pick up at 2 A when IN102 asserts (IN101 deasserted). Program the following:

51P01 := IN101 • 1.5 + IN102 • 2

With IN101 asserted (logical 1), and IN102 deasserted (logical 0), the 51P01 setting is:

$(1 • 1.5) + (0 • 2) = 1.5 + 0 = 1.5$

When IN102 asserts (IN101 deasserted), the 51P01 setting is:

$(0 • 1.5) + (1 • 2) = 0 + 2 = 2$

If, however, IN102 asserts while IN101 is still asserted, the 51P01 setting is:

$(1 • 1.5) + (1 • 2) = 1.5 + 2 = 3.5$

Because 3.5 exceeds the upper range value of 3.2, the relay clamps the setting at 3.2 and asserts Relay Word bit 51MM01.

Torque Control

SELOGIC control equation 51TC01 allows you to state the conditions when the element must run. When 51TC01 asserts (logical 1), Switch S1 in *Figure 5.57* closes and the relay evaluates input 51O01. For example, if the element should only measure when the HV circuit breaker (Winding S, for example) is closed, enter the following:

51TC01 := **52CLS**

With this setting, Switch S1 closes only when 52CLS is a logical 1. If the element must measure all the time, enter the following:

51TC01 := **1**

To prevent the inadvertent omission of the inverse-time overcurrent protection, the relay does not permit a torque control SELOGIC control equation (51TC*xx*) setting of 0 or NA.

EM Reset

Setting 51RS01 defines whether the curve resets slowly like an electromechanical disk or after one power system cycle when current drops below pickup. If you set 51RS01 = Y, then the relay resets according to the Reset Timer equations for that particular curve (see *Table 5.4* or *Table 5.5*). If you set 51RS01 = N, then the relay resets after one power system cycle when current drops below pickup.

Fault Identification Logic

The purpose of the Fault Identification Logic is to determine, on a per-terminal basis, which phase(s) was involved in a fault for which the transformer tripped. Determining the faulted phase is based on current inputs from wye-connected CTs.

The logic does not determine the faulted phase for the following cases:

➤ Delta-connected CTs (CTCON*m* = D)

➤ Where only zero-sequence current flows through the relay terminal (no negative-sequence current and no positive-sequence current)

This logic identifies a sector in which a faulted phase(s) can appear by comparing the angle between the negative- and zero-sequence currents I2*m* and I0*m* (*m* = S, T, U, W, X). *Table 5.7* shows the Relay Word bits for the three sectors and the phases associated with each sector.

Table 5.7   Fault Identification Logic Relay Word Bits

Relay Word Bit	Sector	Description
FIDEN		Fault Identification logic enabled—asserts when the relay has internally enabled the sector calculations
FSA	Sector A	A-Phase-to-ground fault or B-Phase to C-Phase-to-ground fault selected
FSB	Sector B	B-Phase-to-ground fault or C-Phase to A-Phase-to-ground fault selected
FSC	Sector C	C-Phase-to-ground fault or A-Phase to B-Phase-to-ground fault selected

Figure 5.58 shows a block diagram of the sector determination in which a faulted phase(s) can appear.

Figure 5.58   Sector Determination Block Diagram

When any of the terminal-specific trip equations asserts (TRIPS, TRIPT, TRIPU, TRIPW, or TRIPX), the relay uses the output from *Figure 5.58* to determine which particular phase(s) is involved in the fault for that particular terminal. *Figure 5.59* shows a block diagram for this step.

NOTE: Please note that the logic resets Relay Word bits PHA_*m*, PHB_*m*, PHC_*m*, and GROUND*m* only at the beginning of the algorithm. If any of these Relay Word bits assert, they remain asserted until a subsequent fault on the same terminal occurs. For example, if the relay determines that a fault occurred on A-Phase of Terminal T, then PHA_T asserts and remains asserted until a subsequent fault occurs on Terminal T. Also, only the Relay Word bits of the faulted terminal are cleared; if Relay Word bits on other terminals are asserted, they remain asserted until a fault on that particular terminal occurs.
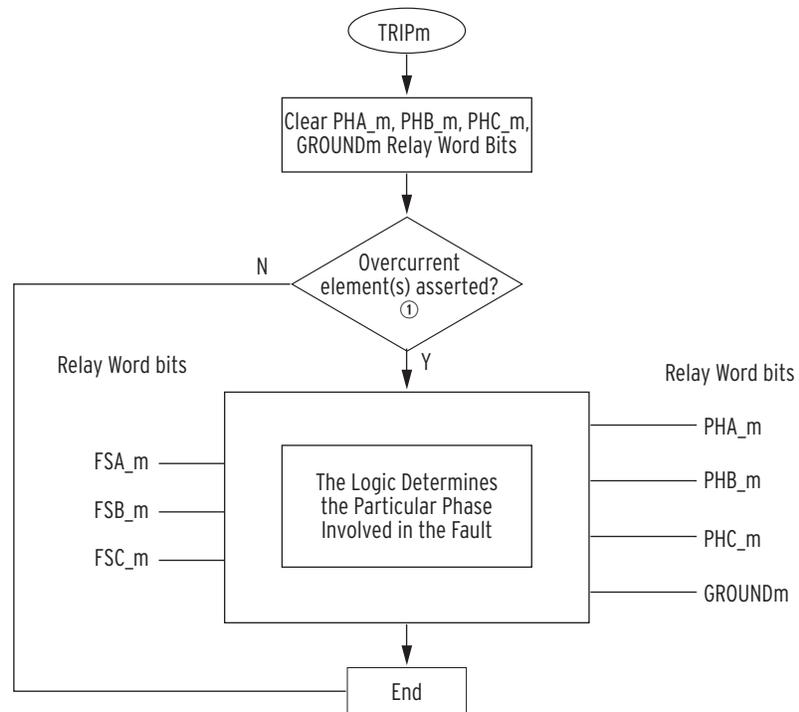
① See *Table 5.8*.

Figure 5.59   Block Diagram Showing Determination of the Particular Phase(s) Involved in the Fault

The steps for determining the faulted phase(s) for Terminal S are as follows:

➤ TRIPS asserts

➤ The relay clears Relay Word bits PHA_S, PHB_S, PHC_S, and GROUNDS

➤ The relay verifies that an overcurrent element listed in *Table 5.8* from Terminal S asserted

➤ The relay uses the sector outputs to determine the faulted phase(s)

Table 5.8 shows the overcurrent elements that the relay considers when determining the faulted phase(s). If any one of these elements is asserted, the relay determines the faulted phase.

NOTE: Be certain to include the output(s) of the 51 element (51S*xx*, *xx* = 01-10) in both the trip equations of the two terminals of the combined overcurrent element. For example, for 51O06 = IATUFM, include 51T06 in TRT and TRU.

Table 5.8   Overcurrent Element the Relay Considers When Determining the Faulted Phase(s)

Element	Description
50*m*P*a*, 50*m*Q*a*, 50*m*G*a* (*a* = 1, 2, 3)	Instantaneous overcurrent elements
51S01–51S10	Time-overcurrent elements

Whereas the instantaneous overcurrent elements (50) are terminal specific, the Time-Overcurrent (51) elements can be assigned to any of the five terminals. The logic automatically associates the 51 element with the correct terminal by inspecting the operating quantity. For example, if 51 Element 05 was assigned Operating Quantity 51O05 = IAUFM, then the relay associates Terminal U with 51S05. When TRIPU and 51S05 assert, the relay determines the faulted phase for Terminal U.

For combined terminal operating quantities such as IATUFM, the relay associates both Terminal T and Terminal U with the 51 element. For example, if you assign 51 Element 06 Operating Quantity 51O06 = IATUFM, then the relay associates both Terminal T and Terminal U with 51 Element 06.

Directional Control for Ground-Overcurrent Elements

For each terminal, the SEL-487E offers a choice of two independent voltage-polarized directional elements (negative-sequence and zero-sequence) to supervise the ground-overcurrent elements. In addition, you can also use the REF elements if you prefer current polarization instead of voltage polarization. You can use either negative-sequence (Q) or zero-sequence polarization (V), or a combination of the two (QV or VQ). When using the combination setting, select your polarization preference with the ORDER setting. *Table 5.9* shows the two directional elements, their availability as a function of the potential transformer (PT) connections, and the effect of the ORDER setting in terms of the preferred directional element. Be aware that directional elements are not available for PTs or CTs connected in delta (PTCONk = D or CTCONm = D, see *Delta-Connected CTs on page 5.40*).

Table 5.9   Availability of Directional Elements

ORDER Settings	Corresponding Ground Directional Element	CT Connection PTCONk =[a]	PT Connection PTCONk =[a]	Polarization Preference	
				First Choice	Second Choice
Q	Negative-sequence	Y or D	Y or D	—	—
QV	Negative- and zero-sequence	Y	Y	Q (m32QGE)[b]	V (m32VE)[b]
V	Zero-sequence	Y	Y	V (m32VE)[b]	—
VQ	Negative- and zero-sequence	Y	Y	V (m32VE)[b]	Q (m32QGE)[b]

[a] k = V, Z.

[b] m = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

Figure 5.60 shows a block diagram of the directional elements. Note that the order in which the ORDER setting lists directional elements (Q and V) determines the priority in which these elements operate, as selected by the Best Choice Ground Directional Element logic. See the discussion on setting ORDER under *Directional Control Settings on page 5.80*.
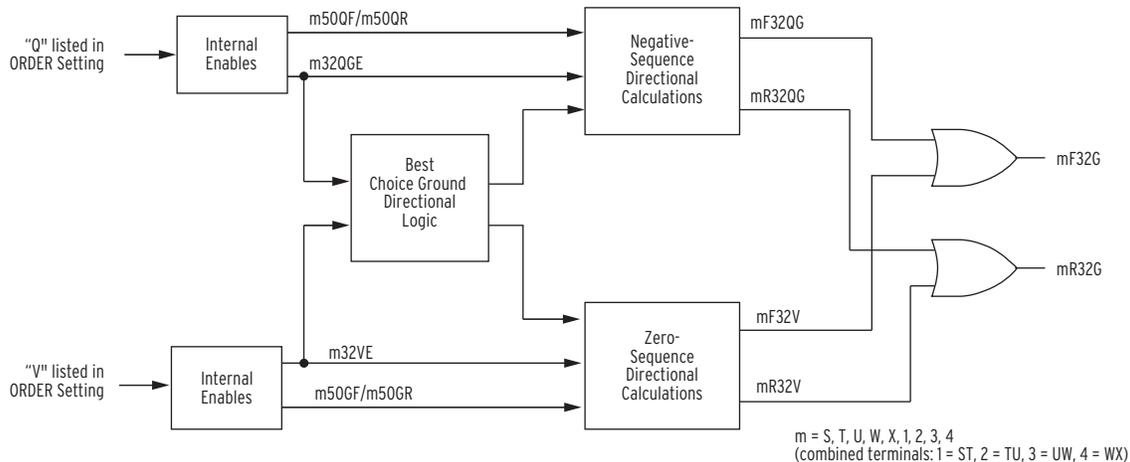
Figure 5.60   Block Diagram of the Directional Elements

Following is a discussion of each of the function blocks in *Figure 5.60*.

Negative-Sequence Internal Enable Function Block

Figure 5.61 shows the enable logic for the negative-sequence directional element. This logic checks the validity of the settings in *Table 5.10*, checks for a loss-of-potential condition, and compares the negative-sequence current, $3I2q$FM (q = S, T, U, W, X, ST, TU, UW, WX), against the following four values:

NOTE: *Figure 5.61* has internal enables 32QE and 32QGE, which the directional element logic uses to control negative-sequence and zero-sequence overcurrent elements.

➤ 50FPm—the forward current threshold

➤ 50RPm—the reverse current threshold

➤ a2m • 3I1qFM—the positive-sequence current (adjusted by a2, the positive-sequence restraint factor)

➤ k2m • 3I0qFM—the zero-sequence current (adjusted by k2, the zero-sequence restraint factor)

Table 5.10 Enable Logic Checks for Negative-Sequence Element

Setting	Value Required for Valid Setting
E50m[a]	Q (enable negative-sequence overcurrent element)
VREFn[b]	V or Z (voltage terminals)
ORDERm[a]	Includes Q (negative sequence)
E50[c]	Terminal Name (S, T, U, W, X, ST, TU, UW, or WX)
E67m[a]	Y
E50m[a]	Includes G (enable zero-sequence overcurrent element)

[a] m = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX)

[b] n = S, T, U, W, X

[c] Combination terminals are only available for channels with the same nominal current rating, same CT connection (CTCON), same current transformer ratio (CTR), and same voltage reference (VREF).
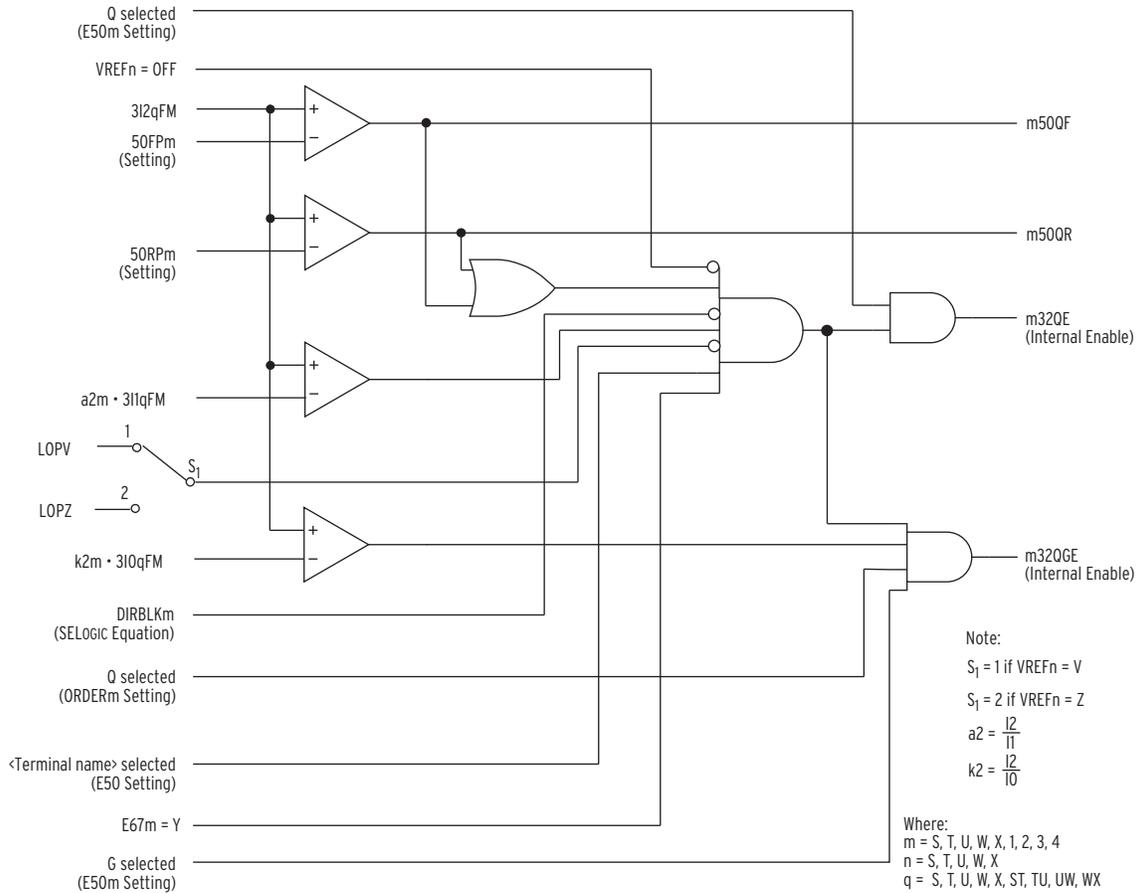
Figure 5.61   Internal Enables for Negative-Sequence (*m*32QE) and Zero-Sequence (*m*32QGE) Directional Elements

When a loss-of-potential condition occurs (Relay Word bit LOPV or LOPZ asserts), all the internal enables are disabled. Also, the directional element blocking SELOGIC equation (DIRBLK*m*) is set to 87QB by default and blocks the element when the second-harmonic and fifth-harmonic elements pick up, avoiding relay misoperations during transformer inrush conditions (see *Directional Control Settings on page 5.80* for the restraint factors).

Zero-Sequence Internal Enable Functional Block

Figure 5.62 shows the enable logic for the zero-sequence directional element. This logic checks the validity of the settings in *Table 5.11*, selects the appropriate voltage source, checks for a loss-of-potential condition, and compares the zero-sequence current, 3I0*q*FM (*q* = S, T, U, W, X, ST, TU, UW, WX), against the following three values:

➤ 50FP*m*—the forward current threshold

➤ 50RP*m*—the reverse current threshold

➤ a0*m* • 3I1*q*FM—the positive-sequence current (adjusted by a0, the positive-sequence restraint factor)

The logic also compares the zero-sequence voltage (3V0VFM or 3V0ZFM) against a fixed value of 7.5.

Table 5.11   Enable Logic Checks for Zero-Sequence Element

Setting	Value Required for Valid Setting
E50m[a]	G (enable zero-sequence overcurrent element)
VREFn[b]	V or Z (voltage terminals)
ORDERm[a]	Includes V (zero sequence)
E50[c]	Terminal Name (S, T, U, W, X, ST, TU, UW, or WX)
E67m[a]	Y

[a] m = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX)

[b] n = S, T, U, W, X

[c] Combination terminals are only available for channels with the same nominal current rating, same CT connection (CTCON), same current transformer ratio (CTR), and same voltage reference (VREF).
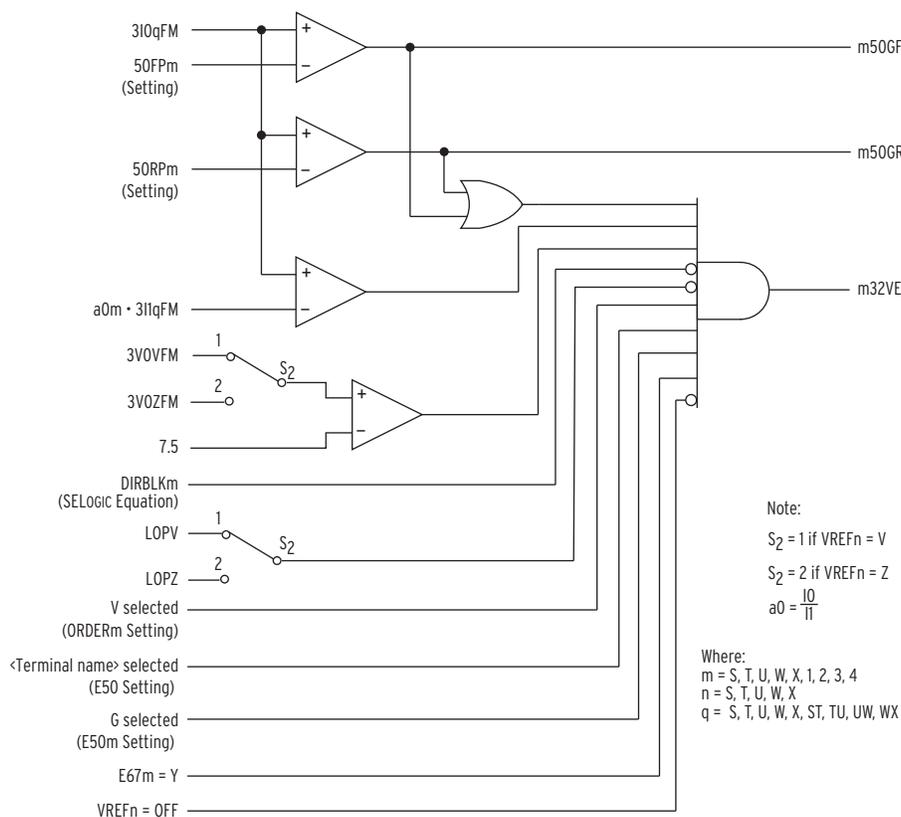
Figure 5.62   Internal Enable (m32VE) for Zero-Sequence Directional Element

Negative-Sequence Directional Calculation Block

Figure 5.63 shows the negative-sequence directional element logic. For each terminal, Group setting VREFn determines which loss-of-potential (LOPV or LOPZ) value and negative-sequence voltage (3V2VCF or 3V2ZCF) value the algorithm uses in the directional calculations. The directional calculations produce a signed impedance Z2m (see *Equation 5.18*) that the logic compares against Z2FTHm, the forward threshold, and Z2RTHm, the reverse threshold (see *Equation 5.19–Equation 5.22* for the threshold calculations). Inputs m50QF and m50QR are from the internal enable logic (see *Figure 5.61*). At the bottom, inputs ORDER and m32VE form the Best Choice Ground Directional Element logic selection.
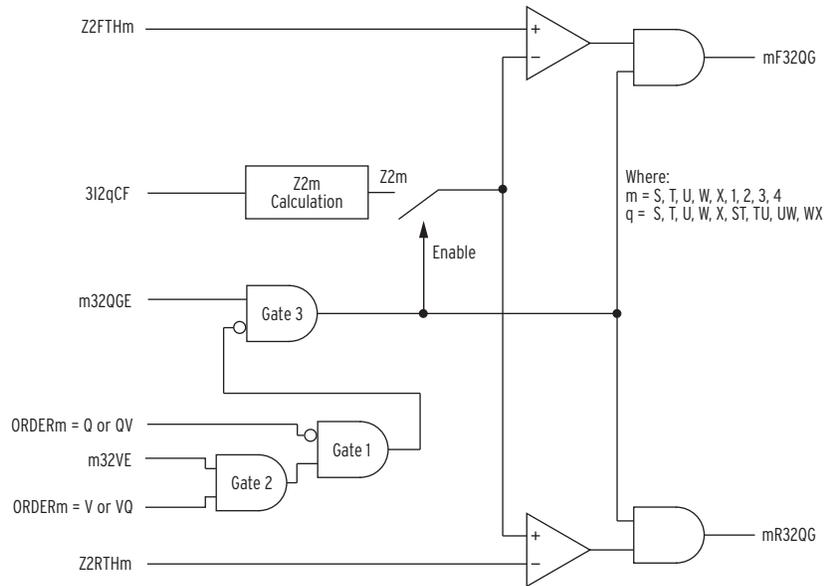
Figure 5.63   Negative-Sequence Directional Calculation Logic (Ground Elements)

Figure 5.64 shows the characteristic of the negative-sequence directional element, consisting of a forward threshold and a reverse threshold.
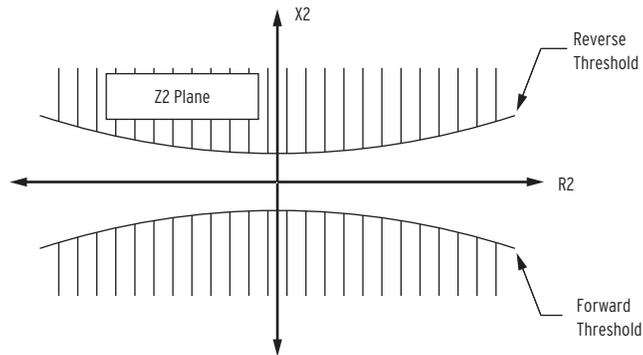
Figure 5.64   Negative-Sequence Directional Element Characteristic

Figure 5.65 shows a system with Fault F1 and Fault F2. These faults are two separate, close-in, A-Phase faults. Fault F1 is in the forward direction with respect to Relay R, and Fault F2 is in the reverse direction with respect to Relay R. For the purpose of the following discussion, assume that both faults are at the line angle.
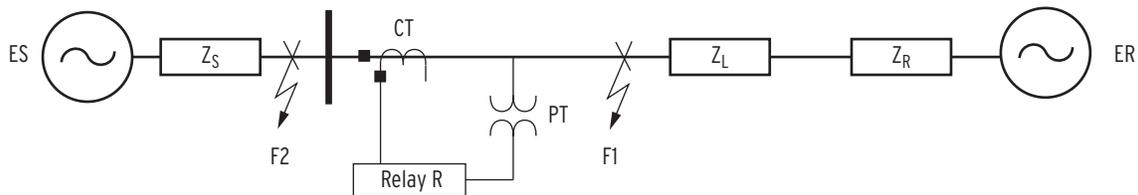
Figure 5.65   Close-In, Single-Phase Fault F1 and Fault F2

Figure 5.66 shows the phasor relationships for Fault F1 at the line angle Z1ANG. Using A-Phase as reference, we see that the fault current lags the A-Phase voltage by the line angle Z1ANG. All three sequence components of the current are

in phase with the A-Phase fault current. However, the negative-sequence voltage and the zero-sequence voltages are 180 degrees out-of-phase with the A-Phase voltage.
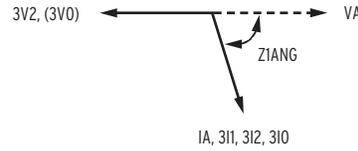
Figure 5.66   Phasor Relationships for an A-Phase-to-Ground Fault

For each phase, the negative-sequence directional element uses *Equation 5.18* to determine the signed quantity Z2*m*.

$$Z2m = \frac{\text{Re}[3V2kCF \cdot (3I2qCF \cdot 1\angle Z1ANGm)^*]}{3I2q\text{FM}^2}$$

Equation 5.18

where:

3V2*k*CF =	negative-sequence voltage in phasor form
3I2*q*CF =	negative-sequence current in phasor form
1∠Z1ANG =	the line angle in degrees
3I2*q*FM =	magnitude of the negative-sequence current (scalar)
* =	complex conjugate
Re =	real part of
m =	S, T, U, W, X, 1, 2, 3, 4
q =	S, T, U, W, X, ST, TU, UW, WX
k =	V, Z

If we assume 3V2VCF = 100∠180°, 3I2SCF = 10∠–80°, 3I2SFM = 10, and Z1ANG = 1∠80°, the directional calculation for Terminal S is as follows:

$$Z2S = \frac{\text{Re}[100\angle 180° \cdot (10\angle -80° \cdot 1\angle 80°)^*]}{(10)^2}$$

$$Z2S = \frac{\text{Re}[100\angle 180° \cdot 10\angle 0°]}{100}$$

$$Z2S = \frac{\text{Re}[1000\angle 180°]}{100}$$

$$Z2S = \frac{\text{Re}[-1000 + j0]}{100}$$

$$Z2S = -10\Omega$$

Therefore, for a fault in the forward direction, Z2S has a negative value.

Figure 5.67 shows the phasor relationships for a reverse Fault 2 at the line angle Z1ANG.
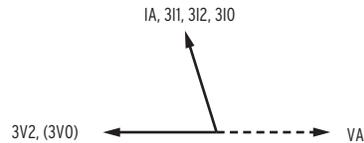
Figure 5.67   Phasor Relationships for a Reverse A-Phase-to-Ground Fault

If we assume 3V2VCF = 100∠180°, 3I2SCF = 10∠100°, 3I2SFM = 10, and Z1ANG =1∠80°, the calculation for Terminal S is as follows:

$$Z2S = \frac{Re[100\angle 180° \bullet (10\angle 100° \bullet 1\angle 80°)^*]}{(10)^2}$$

$$Z2S = \frac{Re[100\angle 180° \bullet 10\angle 180°]}{100}$$

$$Z2S = \frac{Re[1000\angle 0°]}{100}$$

$$Z2S = (10\Omega)$$

Therefore, for a fault in the reverse direction, Z2S has a positive value.

To form the distinct shape of the thresholds, the element computes the forward threshold (Z2FTHm) and the reverse threshold (Z2RTHm) as described below.

Negative-Sequence Directional Element Forward Threshold Calculation

If Z2Fm Setting ≤ 0, Forward Threshold (Z2FTHm) =

$$0.75 \bullet Z2Fm - 0.25 \bullet \left| \frac{3V2kCF}{3I2qCF} \right|$$

Equation 5.19

If Z2Fm Setting > 0, Forward Threshold (Z2FTHm) =

$$1.25 \bullet Z2Fm - 0.25 \bullet \left| \frac{3V2kCF}{3I2qCF} \right|$$

Equation 5.20

Negative-Sequence Directional Element Reverse Threshold Calculation

If Z2Rm Setting ≥ 0, Reverse Threshold (Z2RTHm) =

$$0.75 \bullet Z2Rm + 0.25 \bullet \left| \frac{3V2kCF}{3I2qCF} \right|$$

Equation 5.21

If Z2Rm Setting < 0, Reverse Threshold (Z2RTHm) =

$$1.25 \bullet Z2Rm + 0.25 \bullet \left| \frac{3V2kCF}{3I2qCF} \right|$$

Equation 5.22

Zero-Sequence Directional Calculation Block

Figure 5.68 shows the characteristic of the zero-sequence directional element, consisting of a forward threshold and a reverse threshold. When setting the element, be sure to not overlap the two thresholds because the area between the two thresholds provides security against relay errors.
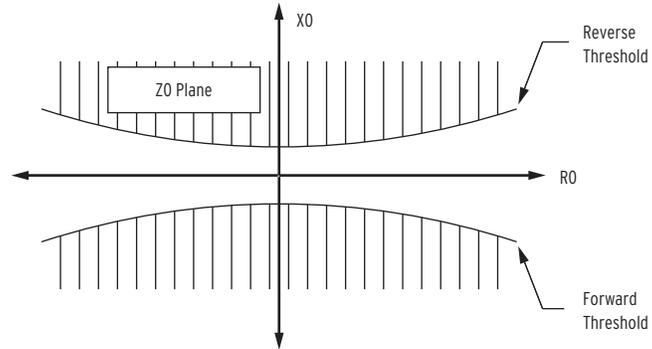
Figure 5.68   Zero-Sequence Directional Element Characteristic

For each phase, the zero-sequence directional element uses *Equation 5.23* to determine the signed quantity Z0*m*.

$$Z0m \ = \ \frac{\mathrm{Re}[3V0k\mathrm{CF} \bullet (3I0q\mathrm{CF} \bullet 1\angle Z0\mathrm{ANG}m)^*]}{3I0q\mathrm{FM}^2}$$

Equation 5.23

where:

3V0*k*CF =		zero-sequence voltage in phasor form
3I0*q*CF =		zero-sequence current in phasor form
1∠Z0ANG =		the line angle in degrees
3I0*q*FM =		magnitude of the zero-sequence current (scalar)
* =		complex conjugate
Re =		real part of

Zero-Sequence Directional Element Forward Threshold Calculation

Calculations for the zero-sequence directional element are identical to those for the negative-sequence directional element, except that the zero-sequence directional element calculations use zero-sequence quantities instead of negative-sequence quantities. The zero-sequence directional element uses *Equation 5.24–Equation 5.27*.

If Z0F*m* Setting ≤ 0, Forward Threshold (Z0FTH*k*) =

$$0.75 \bullet Z0Fm - 0.25 \bullet \left| \frac{3V0k\mathrm{CF}}{3I0q\mathrm{CF}} \right|$$

Equation 5.24

If Z0F*m* Setting > 0, Forward Threshold (Z0FTH*m*) =

$$1.25 \bullet Z0Fm - 0.25 \bullet \left| \frac{3V0k\mathrm{CF}}{3I0q\mathrm{CF}} \right|$$

Equation 5.25

Zero-Sequence Directional Element Reverse Threshold Calculation

If Z0Rm Setting $\geq$ 0, Reverse Threshold (Z0RTHm) =

$$0.75 \cdot Z0Rm + 0.25 \cdot \left| \frac{3V0kCF}{3I0qCF} \right|$$

Equation 5.26

If Z0Rm Setting < 0, Reverse Threshold (Z0RTHm) =

$$1.25 \cdot Z0Rm + 0.25 \cdot \left| \frac{3V0kCF}{3I0qCF} \right|$$

Equation 5.27

Figure 5.69 shows the zero-sequence directional element logic. For each terminal, Group setting VREFn determines which LOPk value and 3V0kCF value the algorithm uses in the calculations. Inputs ORDER and m32QGE form the Best Choice Ground Directional Element logic selection. After calculating the signed impedance Z0m, the logic compares Z0m against Z0FTHm, the forward threshold, and Z0RTHk, the reverse threshold (see *Equation 5.24–Equation 5.27* for the threshold calculations).
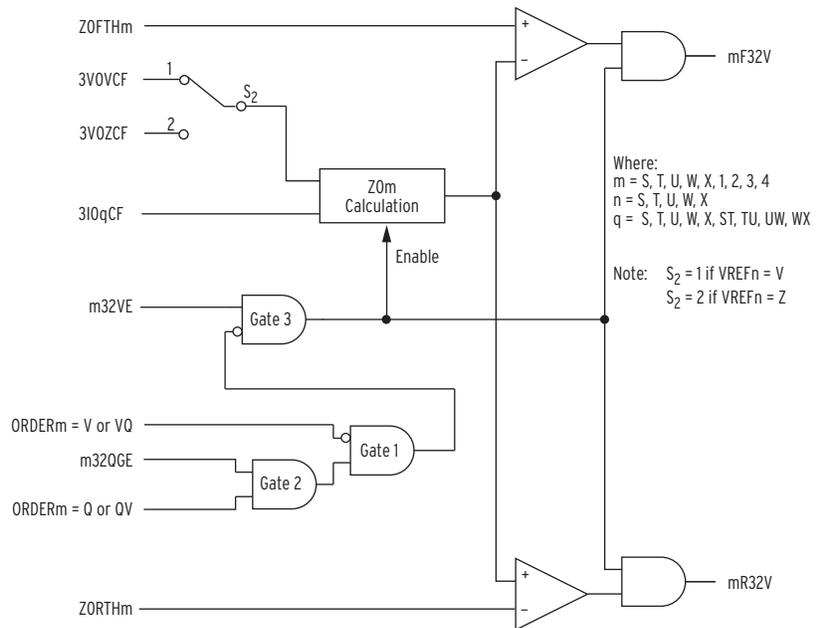
Figure 5.69   Zero-Sequence Directional Calculation Logic

Figure 5.70 combines the logic from *Figure 5.63* and *Figure 5.69* to provide a single directional quantity for the negative-sequence and the zero-sequence directional elements.
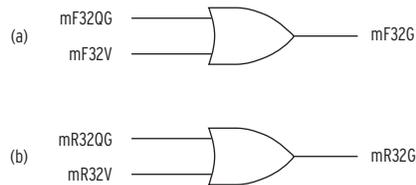
Figure 5.70   Single Negative-Sequence and Zero-Sequence Directional Element Output

Best Choice Function Block

The Best Choice Ground Directional Element logic determines which directional element should operate. This directional element then controls ground-overcurrent elements set for directional control. Although the best choice function is a separate function, the function logic is integrated into both the negative-sequence and zero-sequence directional calculation logic. In *Figure 5.63* and *Figure 5.69*, the two AND gates at the bottom of the figures (Gate 1 and Gate 2) form the best choice function. For the best choice function, the algorithm evaluates the value in the first position of the ORDER setting. In *Figure 5.69*, for example, the ORDER setting for the input into Gate 1 is ORDERm = V (or VQ). Because the algorithm only evaluates the first position of the ORDER setting, V and VQ produce the same result. If the ORDERm setting is set to V or VQ, then the input into Gate 1 asserts permanently to a logical 1 (before the inverter). If the ORDERm setting is set to Q or QV, then the input into Gate 1 asserts permanently to a logical 0.

For example, if you want the Terminal S zero-sequence directional element to take preference over the Terminal S negative-sequence directional element, set the ORDER setting as follows: ORDERS = V (or VQ). This setting asserts the input into Gate 1 permanently to a logical 1, but the inverter at the input of Gate 1 changes the value to a permanent logical 0. This zero input turns Gate 1 permanently off, so that the output from Gate 1 is a permanent logical 0. This logical 0 after the inverter asserts the bottom input into Gate 3 permanently, requiring only m32VE to assert (see *Figure 5.69*) to enable the Z0m calculations.

Consider now the effect of the ORDER setting ORDER = V (or VQ) 1 on the negative-sequence directional logic (see *Figure 5.63*). There are three possible scenarios:

➤ m32VE asserts, but not m32QGE

➤ m32QGE asserts, but not m32VE

➤ both m32QGE and m32VE assert

In general, with the ORDER setting ORDER = V (or VQ), the top input into Gate 1 is a permanent logical 0, but the input turns into a permanent logical 1 through means of the inverter at the input. Also, the bottom input into Gate 2 is a permanent logical 1 because of setting ORDER = V (or VQ).

When m32VE asserts (but not m32QGE), Gate 2 turns on. Then Gate 1 turns Gate 3 off. When Gate 3 turns off, the Z2m calculations cannot be enabled even if m32QGE asserts, so Z0m takes preference.

When m32QGE asserts (but not m32VE), Gate 3 asserts (Gate 1 is still turned off), and the Z2m calculations begin. Therefore, if you select a combined setting (VQ), and the first choice does not assert, the directional calculations still begin if the second choice asserts.

It is when both m32QGE and m32VE assert that the relay calls upon best choice logic to select the appropriate value. As before, when m32VE asserts, Gate 2 turns on. Then Gate 1 turns Gate 3 off. When Gate 3 turns off, the Z2m calculations cannot be enabled, and Z0m takes preference.

Directional Control for Phase and Negative-Sequence Overcurrent Elements

Whereas the previous section describes directional elements for faults that involve ground, this section describes directional elements for faults clear of ground. Because negative-sequence quantities are present in all faults except for three-phase faults, a typical use for negative-sequence elements is as a control for both negative- and positive-sequence overcurrent elements. However, phase overcurrent elements also require positive-sequence directional elements because no negative-sequence quantities exist during three-phase faults.

Negative-Sequence Directional Element

Figure 5.71 shows the negative-sequence directional element, which uses the result of *Equation 5.18* ($Z2m$). This element differs from the negative-sequence element used for ground-fault overcurrent elements by not having zero-sequence directional elements.

Note: $S_1 = 1$ when VREFn = V
$S_1 = 2$ when VREFn = Z
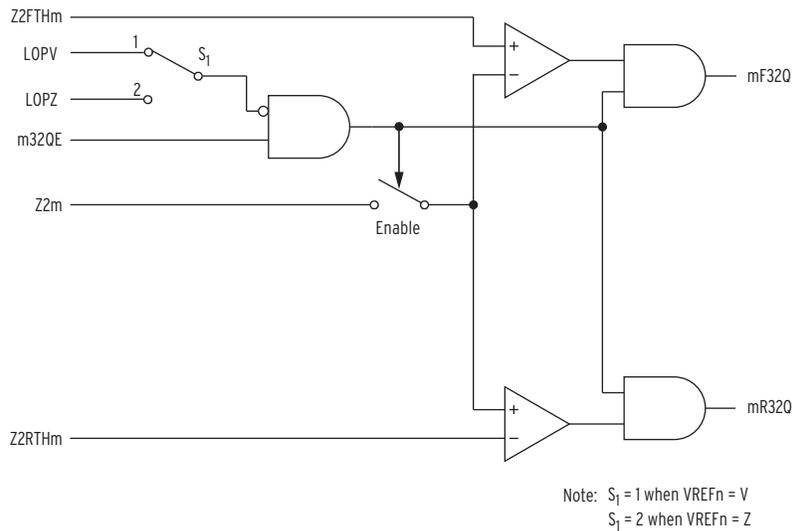
Figure 5.71   Negative-Sequence Directional Element

Phase Directional Element

In general, voltage-polarized elements work well for all types of shunt faults, except for close-in, three-phase faults. Because the voltage goes to zero for these faults, directional elements can lose the reference value and misoperate. To maintain polarizing voltage for close-in, three-phase faults, the SEL-487E uses positive-sequence polarized memory voltage. The complete phase directional element consists of a number of calculations and logic such as that in *Figure 5.72–Figure 5.73*.

Using the positive-sequence voltage as reference, the element declares a forward direction if the angle between the positive-sequence voltage and the positive-sequence current is between 300 degrees and 120 degrees.

Figure 5.72 shows the logic that calculates the positive-sequence forward (Z1F*m*) and reverse (Z1R*m*) directions. If the positive-sequence voltage is greater than 1 V, and if the positive-sequence current is greater than 10 percent of the nominal current (100 mA for a 1 A CT or 500 mA for a 5 A CT), calculation of Z1*m* begins.
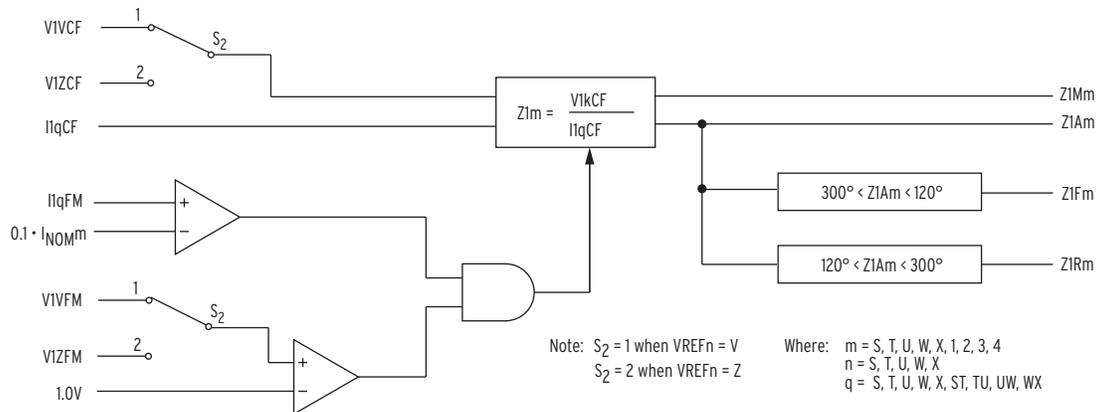
Figure 5.72   Positive-Sequence Directional Element

As for the negative-sequence directional element, the relay calculates a signed quantity to determine the forward and reverse directions. For the positive-sequence directional element, the relay uses positive-sequence phase-to-phase current values and positive-sequence phase-to-phase memory voltage values.

Figure 5.73 shows the algorithm that calculates the positive-sequence memory voltage. This algorithm uses the positive-sequence voltage as a function of the VREF*n* setting. Output VPOL*k* asserts if the absolute value of VA1*k*mem exceeds 1 V.
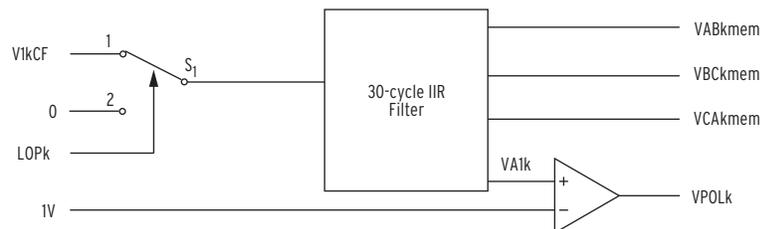
Figure 5.73   Positive-Sequence Memory Voltage

Equation 5.28–Equation 5.30 shows the calculation to determine positive-sequence element direction. In contrast to the similar calculation for the negative-sequence element, a positive result indicates a forward direction. A negative result indicates a reverse direction.

$$\mathrm{MABD}m = \mathrm{Re}[\mathrm{e}^{\mathrm{j.Z1ANG}m} \cdot (-1)^g \mathrm{IAB}q\mathrm{CF} \cdot (\mathrm{VAB}k mem^*)]$$

Equation 5.28

$$\mathrm{MBCD}m = \mathrm{Re}[\mathrm{e}^{\mathrm{j.Z1ANG}m} \cdot (-1)^g \mathrm{IBC}q\mathrm{CF} \cdot (\mathrm{VBC}k mem^*)]$$

Equation 5.29

$$\mathrm{MCAD}m = \mathrm{Re}[\mathrm{e}^{\mathrm{j.Z1ANG}m} \cdot (-1)^g \mathrm{ICA}q\mathrm{CF} \cdot (\mathrm{VCA}k mem^*)]$$

Equation 5.30

where:

$$Re = \text{real part of}$$
$$Z1ANG_m = \text{positive-sequence line angle}$$
$$g = 1 \text{ if } CTP_m = N$$
$$g = 2 \text{ if } CTP_m = P$$
$$CTP_m = \text{CT polarity of Terminal } m$$
$$* = \text{complex conjugate}$$
$$m = \text{S, T, U, W, X, 1, 2, 3, 4}$$
$$q = \text{S, T, U, W, X, ST, TU, UW, WX}$$
$$n = \text{S, T, U, W, X}$$

Figure 5.74 shows the logic that produces the forward phase declaration (mF32P) and the reverse phase declaration (mR32P). For the forward direction, the following conditions must be met:

➤ magnitudes MABDm MBCDm, and MCADm must all be greater than 10 percent of the nominal current,

➤ the directional element function must be enabled (E67m = Y),

➤ VREFn cannot be set to OFF,

➤ there must be sufficient polarizing voltage and no loss of potential,

➤ either the forward positive-sequence load direction (Z1Fm, see *Figure 5.72*) must assert, and

➤ either the positive-sequence current must be below 10 percent of nominal, or the positive-sequence voltage must be below 1 V.

For the reverse direction, the following conditions must be met:

➤ MABDm, MBCDm, and MCADm must all be below –10 percent of the nominal current,

➤ the directional element function must be enabled (E67m = Y),

➤ VREFn cannot be set to OFF,

➤ there must be sufficient polarizing voltage and no loss of potential,

➤ either the reverse positive-sequence load direction (Z1Rm, see *Figure 5.72*) must assert, or

➤ either the positive-sequence current must be below 10 percent of nominal, or the positive-sequence voltage must be below 1 V.

Where: m = S, T, U, W, X, 1, 2, 3, 4
n = S, T, U, W, X
q = S, T, U, W, X, ST, TU, UW, WX

Note: S_3 = 1 when VREFn = V
S_3 = 2 when VREFn = Z
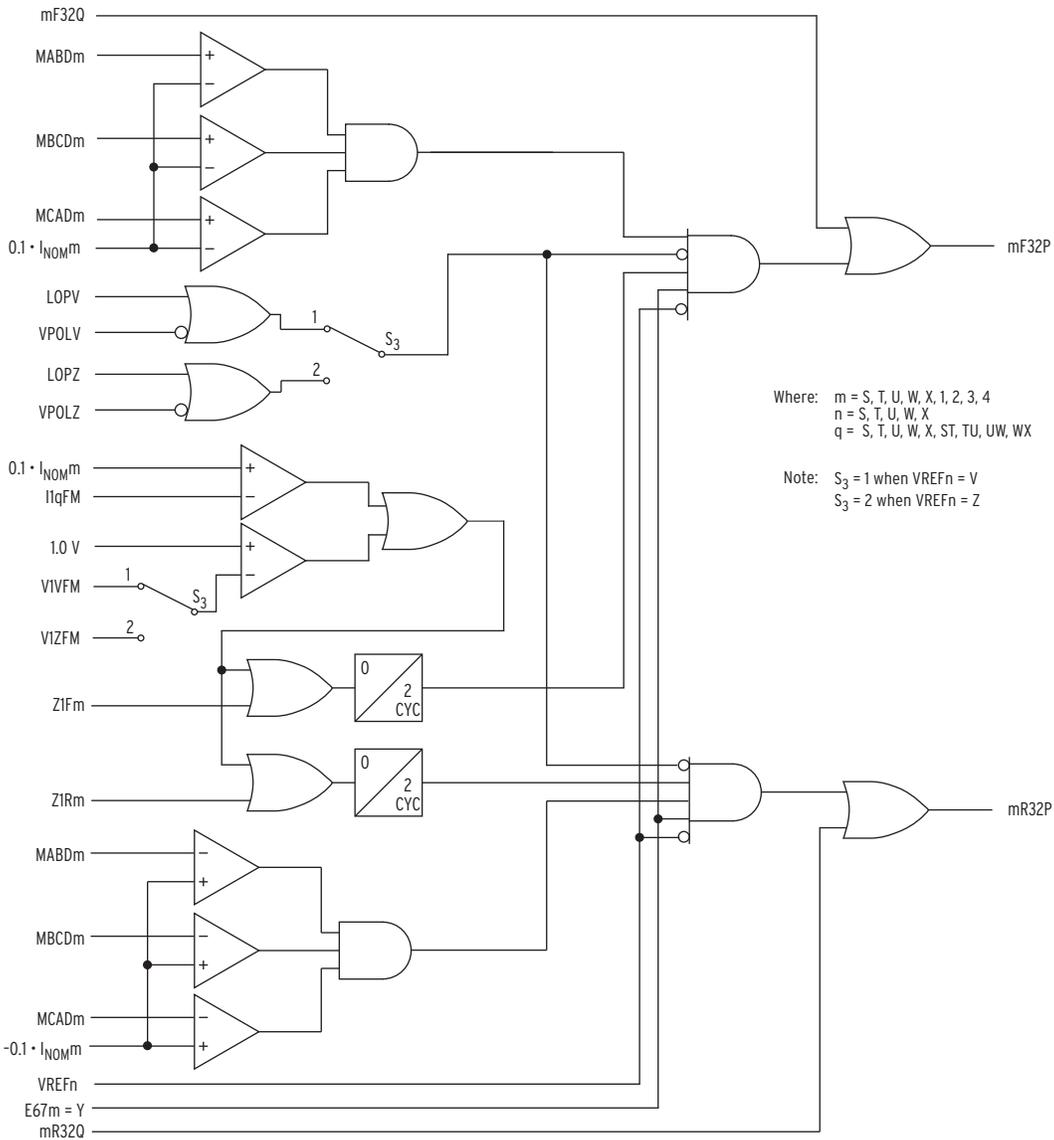
Figure 5.74   Phase Directional Element

Table 5.12 shows examples of torque control equation settings for each overcurrent element (P, Q, G) of Terminal S.

Many utilities prefer to use the current from the transformer neutral as the polarizing quantity. By using the reverse output from the REF elements, you can also use current polarizing as a method of directional control. Be aware that the Best Choice function does not include the REF elements, so include the REF element in specifying the directional control conditions. The last row in *Table 5.12* shows an example that uses the reverse output from REF Element 1 as current polarizing and that includes the REF element in the Best Choice function.

Table 5.12   Directional Element Summary and Example Settings (Terminal S)

E50S Setting	Selected O/C Element	Torque-Control Setting for Selected O/C Element	Comment
P	50SP1	67SP1TC = SF32P	Include SF32P for bolted, three-phase faults.
Q	50SQ1	67SQ1TC = SF32G	No need to include SF32P (no negative-sequence current for three-phase faults), and SF32G includes negative- and zero-sequence directional elements (see *Figure 5.70*).
G	50SG1	67SG1TC = SF32G	No need to include SF32P (no negative-sequence current for three-phase faults), and SF32G includes negative- and zero-sequence directional elements (see *Figure 5.70*).
G	50SG1	67SG1TC = REFR1 or SF32G	Relay Word bit REFR1 asserts when the REF element detects a fault external to the REF zone. See *Restricted Earth Fault Element on page 5.41* for more information.

Directional Control Settings

Setting E50 is a composite setting that determines definite-time overcurrent and directional element settings. *Table 5.13* summarizes the interaction between the E50, E50m, E67m, and the 67mPa TC settings.

Table 5.13   Directional Element Summary

Setting	Range	Purpose
E50[a]	S, T, U, W, X, ST, TU, UW, WX	Select windings that require: 1. definite-time overcurrent elements 2. directional elements (at this point, there is no distinction between selecting overcurrent elements and selecting directional elements).
E50m[b]	P, Q, G	After selecting the winding(s) (E50), select the overcurrent elements directional elements from among phase (P), negative-sequence (Q) and zero-sequence (G) if required for each winding. If overcurrent elements are not required, leave E50m = OFF.
E67m[b]	Y, N	After selecting the winding(s) (E50) and the type of directional elements (E50k), enable the directional elements for the windings. For example, if you set E50 = S, E50S = P, and E67S = N, then Winding S has phase overcurrent elements only, (i.e., no directional elements). Setting E67S = Y enables the directional elements for Winding S.
67mPa TC[b,c]	SELOGIC Control Equation	State the directional conditions for the phase overcurrent elements (see *Table 5.12*).
67mQa TC[b,c]	SELOGIC Control Equation	State the directional conditions for the negative-sequence overcurrent elements (see *Table 5.12*).
67mGa TC[b,c]	SELOGIC Control Equation	State the directional conditions for the zero-sequence overcurrent elements (see *Table 5.12*).

[a] Combination terminals are only available for channels with the same nominal current rating, same CT connection (CTCON), same current transformer ratio (CTR), and same voltage reference (VREF).

[b] m = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

[c] a = 1–3.

E67m (Enable Directional Elements)

For each terminal, enable the directional control for overcurrent elements by setting directional control enable setting E67m. Setting E67m = Y enables the directional element for that winding; disable the directional element for that winding by setting E67m = N.

CTPm (CT Polarity)

Use the CTPm setting, available only if E67m =Y, to select the CT polarity for the directional element of each terminal. You cannot select the polarity of the individual phases; the setting applies to all three phases. In *Figure 5.75*, CTS and

CTT are installed and connected in the conventional way to provide CT information with the correct polarity for the differential element. However, if you want to use CTT for directional control in the same direction as, for example, CTU, then the polarity of CTT is incorrect.
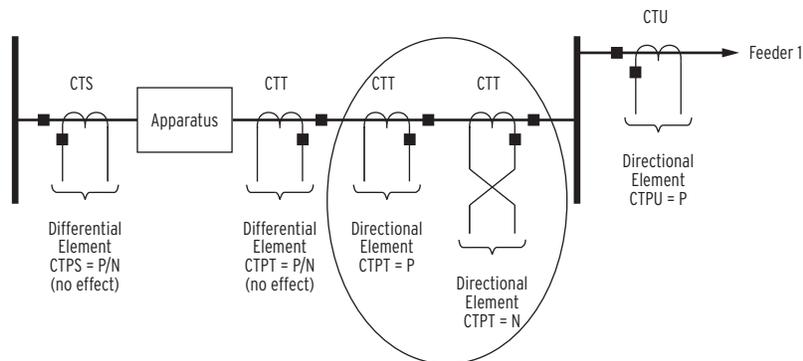
Figure 5.75 CTP*m* Changes the Polarity of the CTs for the Directional Elements

By your setting CTPT = N, the relay internally changes the polarity of CTT for the directional element and interprets the polarity of CTT as if it is the same as the polarity of CTU.

Z1ANG*m* (Positive-Sequence Line Impedance Angle)

For each terminal, set the positive-sequence line angle in degrees. This setting is only available if setting E67*m* = Y.

Z0ANG*m* (Zero-Sequence Line Impedance Angle)

For each terminal, set the zero-sequence line angle in degrees. This setting is only available if setting E67*m* = Y and if setting E50*m* includes G.

EADVS*m* (Enable Advanced Settings)

Enable the advanced settings by setting EADVS*m* = Y. This setting is only available if setting E67*m* = Y. Advanced settings include the following:

➤ 50FP*m*
➤ 50RP*m*

50FP*m* (Forward Direction Overcurrent Pickup)

Setting 50FP*m* is the Forward Direction Overcurrent Pickup value that the negative-sequence current, 3I2*q*FM (*q* = S, T, U, W, X, ST, TU, UW, WX), must exceed, and it is one of the conditions that must be true to assert *m*32QGE (see *Figure 5.61*). This setting is only available if setting E67*m* = Y. If setting EADVS*m* = N, then the relay internally sets 50FP*m* to $0.12 \cdot I_{NOM}m$.

50RP*m* (Reverse Direction Overcurrent Pickup)

Setting 50RP*m* is the Reverse Direction Overcurrent Pickup value that the negative-sequence current (3I2*q*FM) must exceed, and it is one of the conditions that must be true to assert *m*32QGE (see *Figure 5.61*). This setting is only available if setting E67*m* = Y. If setting EADVS*m* = N, then the relay internally sets 50RP*m* to $0.08 \cdot I_{NOM}m$.

Z2F*m* (Forward Direction Z2 Threshold)

Use Z2F to calculate the Forward Threshold for the negative-sequence voltage-polarized directional elements. This setting is only available if setting E67*m* = Y. If setting EADVS*m* = N, then the relay internally sets Z2F*m* to –0.5 / $I_{NOM}m$.

Z2R*m* (Reverse Direction Z2 Threshold)

Use Z2R to calculate the reverse threshold for the negative-sequence voltage-polarized directional elements. This setting is only available if setting E67*m* = Y. If setting EADVS*m* = N, then the relay internally sets Z2R*m* to 0.5 / $I_{NOM}m$. When setting the element, be sure to set Z2R greater in value than setting Z2F by at least Z2F*m* + 0.5 / $I_{NOM}m$ secondary.

a2*m* (Positive-Sequence Restraint Factor—*m*32QE)

The a2 factor is the ratio of the negative-sequence current and the positive-sequence current (I2/I1). This factor increases the security of negative-sequence voltage-polarized directional elements by preventing these elements from operating for negative-sequence current (system unbalance). Negative-sequence current circulates because of line asymmetries, CT saturation during three-phase faults, etc. (see *Figure 5.61*). This setting is only available if setting E67*m* = Y. If setting EADVS*m* = N, then the relay internally sets a2*m* to 0.1.

ORDER*m* (Ground Directional Element Priority)

This setting is hidden when E67*m* = N or if E50*m* does not include G. Also, if the advanced settings EADVS*m* = N, then this setting is set to QV.

Setting ORDER can be set to negative-sequence (Q), zero-sequence control (V), or the combination of the two (i.e., QV or VQ). The order in which you enter the directional elements in setting ORDER determines the priority in which these elements operate to provide Best Choice Ground Directional Element logic control.

For example, if setting:

   ORDER = QV

then the first listed directional element (Q = negative-sequence voltage-polarized directional element) is the first priority directional element to provide directional control for the neutral-ground and residual-ground overcurrent elements.

If the negative-sequence voltage-polarized directional element is inoperable (it does not have sufficient operating quantity, as indicated by its internal enable, 32QGE, not being asserted), then the second listed directional element (V = zero-sequence voltage-polarized directional element) provides directional control for the neutral-ground and residual-ground overcurrent elements.

If the zero-sequence voltage-polarized directional element is inoperable (it does not have sufficient operating quantity, as indicated by its internal enable, 32VE, not being asserted), then no directional control is available.

In another example, if setting:

   ORDER = V

then the zero-sequence voltage-polarized directional element (V = zero-sequence voltage-polarized directional element) provides directional control for the neutral-ground and residual-ground overcurrent elements at all times (assuming it

has sufficient operating quantity). If there is insufficient operating quantity during an event (the internal enable 32VE is not asserted), then no directional control is available.

k2*m* (Zero-Sequence Current Restraint Factor, I2/I0)

Note the internal enable logic outputs in *Figure 5.61*.

➤ *m*32QE, the internal enable for the negative-sequence voltage-polarized directional element that controls the negative-sequence and phase overcurrent elements

➤ *m*32QGE, the internal enable for the negative-sequence voltage-polarized directional element that controls the zero-sequence overcurrent elements

For the 32QGE internal enable to be on, the negative-sequence current magnitude (3I2*q*FM) must be greater than the zero-sequence current (3I0*q*FM) magnitude multiplied by k2:

$$|I2| > k2 \cdot |I0|$$

This check ensures that the relay uses the most robust analog quantities in making directional decisions for the neutral-ground and residual-ground overcurrent elements. The zero-sequence current (3I0*q*FM), to which we refer in the previous application of the k2 factor, is from the residual current, which we derived from phase currents IA, IB, and IC.

The k2 factor increases the security of the zero-sequence voltage-polarized directional elements. It keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc. (see *Figure 5.61*). This setting is only available if setting E67*m* = Y. If setting EADVS*k* = N, then the relay internally sets a2*m* to 0.1.

Z0F*m* (Forward Directional Z0 Threshold)

This setting is only available if setting E67*m* = Y and if setting E50*m* includes G. If setting EADVS*m* = N, then the relay internally sets Z0F*m* to -0.5 / $I_{NOM}m$ (I_{NOM} = 1 for a 1 A relay and 5 for a 5 A relay). When setting Z0F*m* and Z0R*m*, be sure that Z0R is greater in value than setting Z0F by at least 0.1 Ω secondary.

Z0R*m* (Reverse Directional Z0 Threshold)

This setting is only available if setting E67*m* = Y and if setting E50*m* includes G. If setting EADVS*m* = N, then the relay internally sets Z0R*m* to 0.5 / $I_{NOM}m$ (I_{NOM} = 1 for a 1 A relay and 5 for a 5 A relay). When setting Z0F*m* and Z0R*m*, be sure that Z0R is greater in value than setting Z0F by at least 0.1 Ω secondary.

a0*m* (Positive-Sequence Current Restraint Factor, I0/I1)

This setting is only available if setting E67*m* = Y and if setting E50*m* includes G. The a0 factor increases the security of the zero-sequence voltage-polarized directional element. This factor keeps the elements from operating for zero-sequence current (system unbalance), which circulates because of line asymmetries, CT saturation during three-phase faults, etc.

The zero-sequence current (I0), to which we referred in the application of the a0 factor, is from the residual current (IG), which we derived from phase currents IA, IB, and IC: 3I0 = IG = IA + IB + IC.

DIRBLK*m* (Directional Element Blocking)

Customize a SELOGIC equation to determine when to block the phase and ground directional element for Terminal *m* (*m* = S, T, U, W, X, 1, 2, 3, 4). The DIRBLK*m* setting is hidden for the following conditions:

➤ The definite-time overcurrent element E50 = OFF or does not include *m*

➤ E50*m* does not include negative-sequence or ground elements (Q or G)

➤ E67*m* = N. (To enable E67*m*, you must set CTCON*n* = Y [*n* = S, T, U, W, X] and PTCON*k* = Y [*k* = V, Z], and EPTTERM, E50, and VREF*n* cannot be set to OFF.)

Unbalance Current Elements

Use the current unbalance logic to detect unbalance among the three-phase current magnitudes during normal system operating conditions. For each terminal in the E46 setting, the relay uses *Equation 5.31* to calculate the average current.

$$I_{AVEm} = \frac{(IAmFM + IBmFM + ICmFM)}{3}$$

Equation 5.31

where:

m = S, T, U, W, X

Figure 5.76 shows the logic that uses the result of *Equation 5.31* (I_{AVEm}) to calculate the unbalance for the A-Phase. Calculations begin only if the E46 setting includes the terminal and if the average current is larger than five percent of the nominal current. After calculating the percentage difference between the individual phase current and the terminal average current, the logic compares this result to the value of setting 46*m*PU. If the result exceeds the setting value, then 46*m* assert.
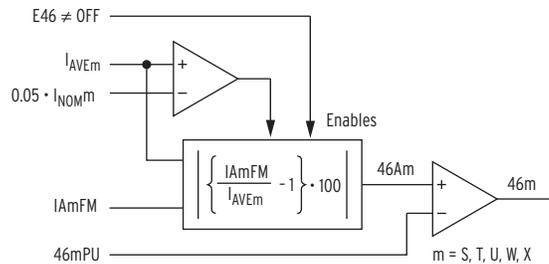
Figure 5.76   Unbalance Logic for Terminal *m*, A-Phase

Figure 5.77 shows the logic that prevents assertion of the unbalance element during fault conditions and after closure of a terminal circuit breaker.
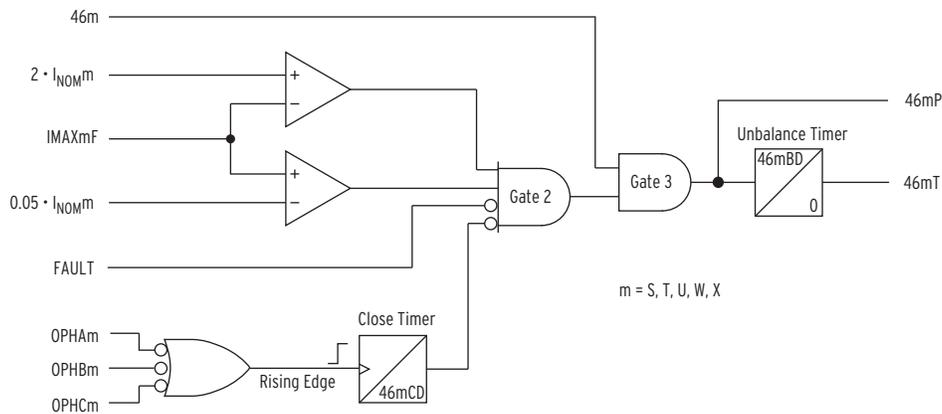
Figure 5.77 Unbalance Blocking Logic for Terminal _m_

The current unbalance logic does not operate if any of the following conditions are true:

➤ The maximum terminal current is greater than $2 \cdot I_{NOM}$, indicating a system fault.

➤ The Relay Word bit FAULT asserts.

➤ The circuit breaker has been closed (open-phase detection elements have deasserted).

After the circuit breaker closes (and current flows), all three open-phase detection elements (OPHA_m_, OPHB_m_, and OPHC_m_) deassert. When the first open-phase detection element deasserts, the Close Timer starts and asserts for a time period equal to the 46_m_CD time setting, during which time Gate 2 is turned off. If one of the phases fails to close, AND Gate 2 is not turned off, and, provided I_{MAX} is above five percent I_{NOM}, but below $2 \cdot I_{NOM}$, Gate 3 turns on. When Gate 3 turns on, Relay Word bit 46_m_P asserts and the Unbalance Timer starts timing. If Gate 3 is turned on for a period equal to the 46_m_BD setting, then Relay Word bit 46_m_T asserts.

Unbalance Current Settings
46_m_PU (Current Unbalance Pickup)

Set the percentage unbalance among the three phases of a particular winding.

46_m_CD (Close Delay)

Set the time for the current to settle after closing the circuit breaker. During this time, Gate 2 in *Figure 5.77* is turned off; the unbalance function is inoperative.

46_m_BD (Current Unbalance Delay)

The unbalance timer starts timing when the unbalance among the three phases exceeds the 46_m_ setting. Use setting 46_m_BD to specify how long unbalance must persist before the elements provide an output.

Open-Phase Detection Logic

Subsidence current results from energy trapped in a CT magnetizing branch after a circuit breaker opens to clear a fault or interrupt load. This current exponentially decays and delays the resetting of instantaneous overcurrent elements used for breaker failure protection. Breaker failure protection requires fast open-phase detection to ensure fast resetting of instantaneous overcurrent elements. *Figure 5.78* shows open-phase logic that asserts SEL-487E open-phase detection elements OPH*pm* (*p* = A, B, C; *m* = S, T, U, W, X) in less than one cycle, even during subsidence current conditions.
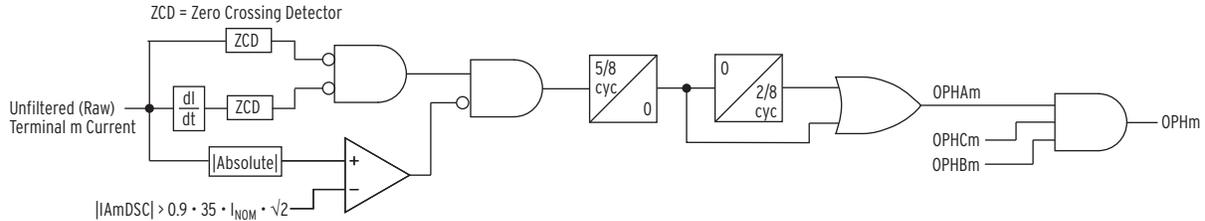
Figure 5.78   A-Phase Open-Phase Detection Logic

The logic measures the zero crossings and maximum and minimum current values of each phase. The relay declares an open phase when the logic does not detect a zero crossing or current value within 5/8 of a power system cycle since the previous measurement. OPH*m*, the output of the logic, asserts when all three phases of a particular winding assert.

Breaker Failure Elements

There are five breaker failure elements in the relay, one for each of the five windings. Use the EBFL Group setting to enable the appropriate windings necessary for your particular application. *Figure 5.79*, *Figure 5.80*, and *Figure 5.81* show the breaker failure logic. In *Figure 5.79*, three comparators test the three-phase currents against the 50FPU*m* settings, and one comparator tests the neutral current against the INFPU*m* setting. SELOGIC setting ENINBF*m* allows the neutral breaker failure function to be conditional if system unbalance conditions could cause inadvertent initiation of the neutral element, such as might occur in single-pole tripping systems. When any phase current exceeds the 50FPU*m* setting, or the neutral current exceeds the INFPU*m* setting, the appropriate Relay Word bit asserts (IA*m*BF, IB*m*BF, IC*m*BF, and/or IN*m*BF). Each phase current comparator is supervised by the associated open-phase detectors OPH*pm*, (*p* = A, B, C; *m* = S, T, U, W, X). The neutral current comparator is supervised by the all three poles open detector (OPH*m*). The open-phase detectors provide subcycle resetting of all input currents, even when subsidence current is present.

① To *Figure 5.80*.
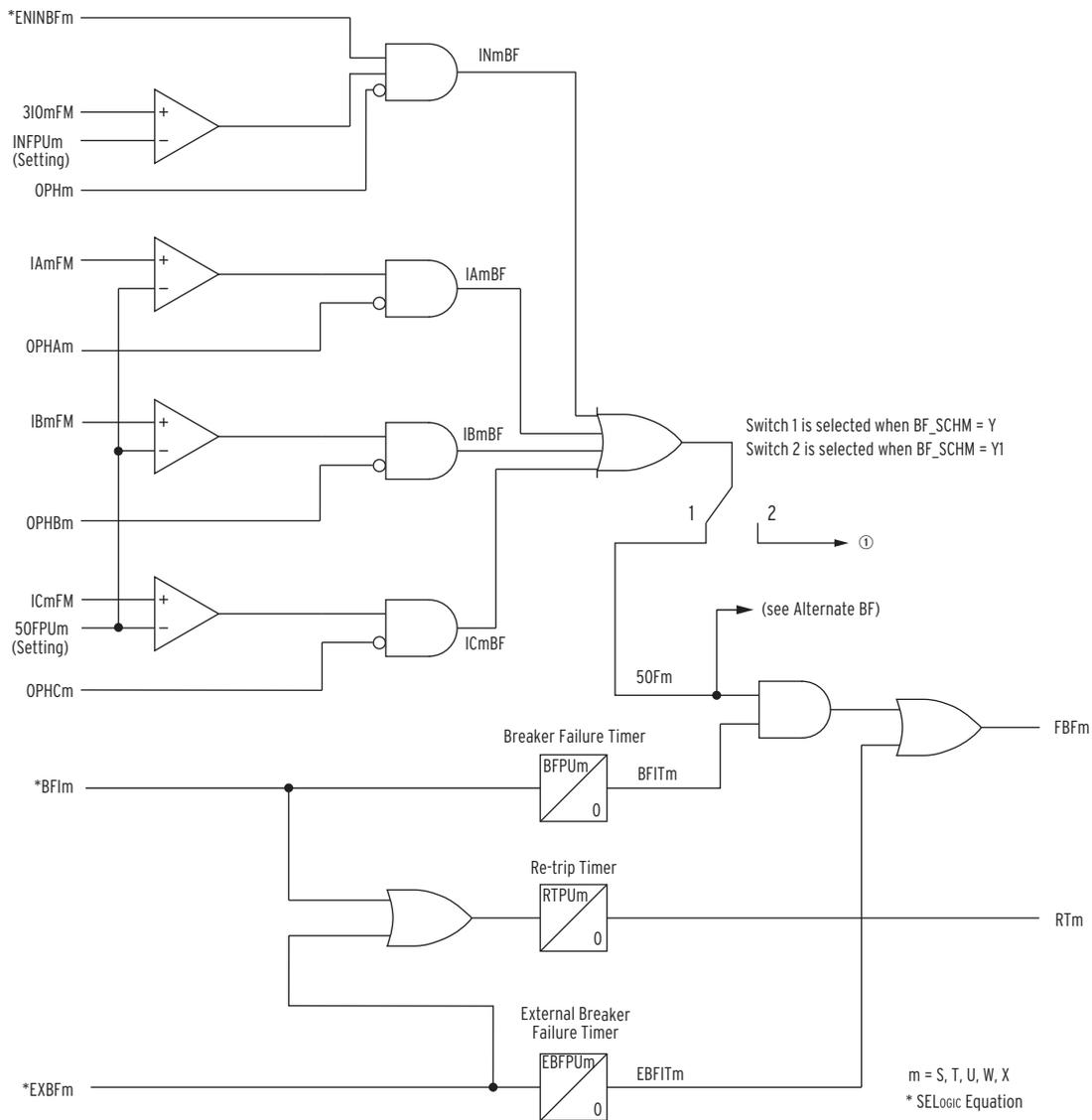
Figure 5.79   Breaker Failure Logic for Terminal *m* When BF_SCHM = Y

Input BFI*m* is a SELOGIC control equation that provides the breaker failure initiate signal. When BFI*m* asserts, both the breaker failure timer and the retrip timer start timing as shown in *Figure 5.79*. When the retrip timer expires, RTm asserts, and when the breaker failure timer expires, BFIT*m* asserts. If 50F*m* is asserted when BFIT*m* asserts, the breaker failure output, FBF*m*, asserts. Note that BFI*m* must be present for the entire duration of the breaker failure timer setting. If BFI*m* is not present constantly, the timers reset when BFI*m* falls away (see alternate initiate logic in *Figure 5.81*).
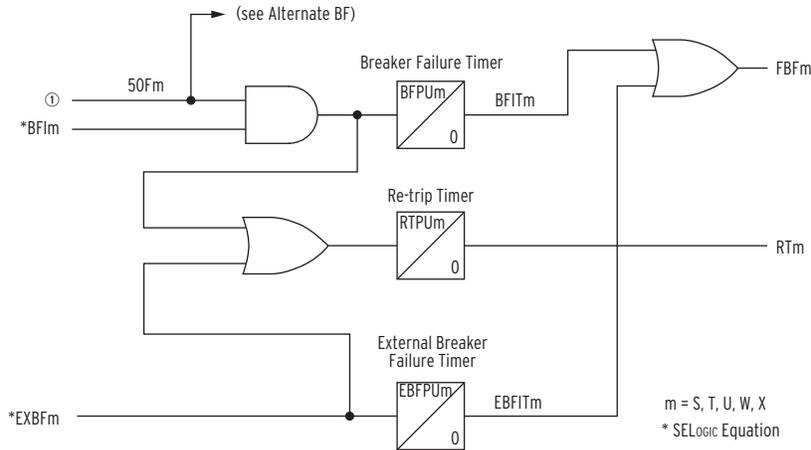
① From *Figure 5.79* when BF_SCHM = Y1.

Figure 5.80   Breaker Failure Logic for Terminal *m* When BF_SCHM = Y1

The logic shown in *Figure 5.80* is enabled when the breaker failure scheme setting is set to Y1 (BF_SCHM = Y1). The logic enabled with option Y1 is similar to that shown in *Figure 5.79*, but the current check (50F*m*) is now part of the breaker failure initiate timer (BFPU*m*) and retrip time delay (RTPU*m*) in addition to the external breaker failure initiate setting (EXBF*m*).

EXBF*m* (SELOGIC control equation) is the input for the case when breaker failure initiates from a protection function alone (when there is no current supervision), such as when the Buchholz relay operates on an unloaded transformer. When EXBF*m* asserts, both the external breaker failure timer and the retrip timer start timing. When the retrip timer expires, RT*m* asserts, and when the external breaker failure timer expires, the breaker failure output, FBF*m*, asserts.

Figure 5.81 shows an alternate breaker failure initiate logic in which one has the flexibility to apply one of many other breaker failure philosophies. When using the alternate initiate logic, connect the breaker failure initiate signal to ATBFI*m* (instead of to BFI*m* in *Figure 5.79*). Then connect the output of the alternate initiate logic, ABFIT*m*, to BFI*m* (*Figure 5.79*). This ensures assertion of the FBF*m* Relay Word bits when a breaker failure occurs.
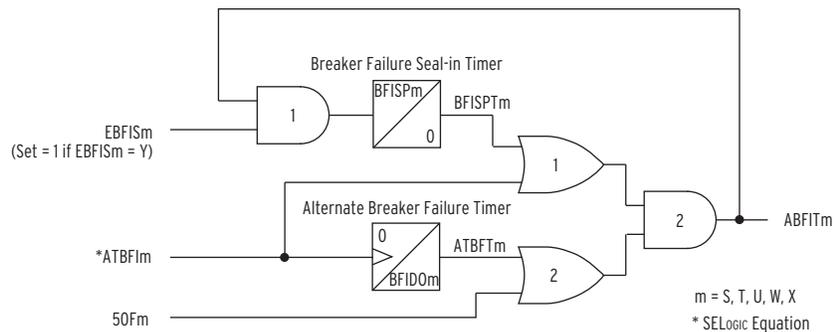
Figure 5.81   Alternate Breaker Failure Logic for Terminal *m*

One use of the alternate initiate logic is to ensure that Relay Word bit ABFIT*m* (and BFI*m*) is asserted for the duration of the breaker failure time. To achieve this goal, we must keep AND Gate 2 asserted for the duration of the breaker failure time. In general, on the rising edge of the initiate signal (ATBFI*m*), the output of the Alternate Breaker Failure Timer (ATBFT*m*) asserts and the output of the logic (ABFIT*m*) asserts for the BFIDO*m* time setting. At this point, ATBFI*m* (through

the bottom input of OR Gate 1) and ATBFT*m* keep AND Gate 2 asserted. However, ATBFI*m* is about to fall away, so we need to commutate ATBFI*m* from the bottom input to the top input of OR Gate 1 via the breaker failure seal-in timer.

For the breaker failure seal-in timer to expire, EBFIS*m* must be set to Y, and ABFIT*m* must be asserted for longer than the BFISP*m* time setting. Therefore, set the BFISP*m* time setting long enough to avoid spurious assertion but shorter than the expected duration of the breaker failure initiate signal. When the breaker failure seal-in timer expires, BFISPT*m* asserts, completing the commutation of ATBFI*m* from the bottom input to the top input of OR Gate 1. This ensures that ABFIT*m* stays asserted when ATBFI*m* falls away.

There are two ways to control the bottom input into AND Gate 2. One can use the drop-off time setting (BFIDO*m*) of the alternate breaker failure timer or the flow of current (50F*m*). Consider carefully the primary application before choosing the current option. Fault current in installations that require the opening of two breakers to clear a fault (breaker-and-a-half or ring-bus installations, for example) may only be available after one of the breakers opens. For these installations, set BFIDO*m* long enough to ensure the availability of that fault current when ATBFT*m* deasserts.

To illustrate this, consider Fault F1 (see *Figure 5.82*), for which both Circuit Breaker 52-S and Circuit Breaker 52-T must operate to clear the fault. For certain faults, the current distribution may be such that Circuit Breaker 52-S carries the bulk of the fault current, with very little current flowing through Circuit Breaker 52-T.
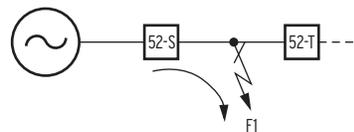
Figure 5.82   Current Distribution for Fault F1 With Circuit Breaker 52-S and Circuit Breaker 52-T Closed

Because of the current distribution, Terminal 52-T may only have enough current to assert the breaker failure current element threshold when Circuit Breaker 52-S opens, as shown in *Figure 5.83*.
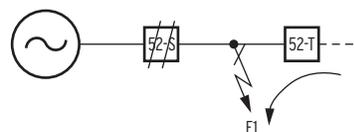
Figure 5.83   Current Flow for Fault F1 After Circuit Breaker 52-S Opened

Use the alternate initiate logic if your protection philosophy calls for the current and initiate signal to be present throughout the breaker failure timing process. In *Figure 5.79*, the logic only checks whether current is present after the breaker failure timer has expired.

Because the breaker failure initiate signal is present all the time, we do not need the seal-in circuit in *Figure 5.81*. Therefore, set EBFIS*m* = N and set BFIDO*m* = 0.00. With these settings, ABFIT*m* asserts only if both the initiate signal and sufficient current are present for the duration of the breaker failure process.

Breaker Failure Settings

EBFL (Enable Breaker Fail)

Set EBFL to enable breaker failure protection for the specific terminals in your application. The EBFL setting considers for selection only terminals that you include in the ECTTERM setting.

BF_SCHM (Breaker Failure Scheme)

Set BF_SCHM to Y or Y1 for your preferred breaker failure scheme for your application. See *Figure 5.79* and *Figure 5.80* for further details. If EBFL = OFF, BK_SCHM is hidden.

EXBFm (Enable External Breaker Fail)

EXBFm (SELOGIC control equation) is the input for the case when breaker failure results from a protection function alone (no current supervision), such as when the Buchholz relay operates on an unloaded transformer. Use the setting to specify conditions under which the external breaker input must be active. There is a setting for each of the enabled terminals. If you set EXBFm = 1, the input is asserted permanently.

EBFPUm (External Breaker Failure Initiation Pickup)

For each enabled terminal, select a time in cycles that you want the external breaker failure element to wait before asserting.

50FPUm (Fault Current Pickup)

The setting 50FPUm is the current pickup setting in amperes secondary for the breaker failure overcurrent element of each enabled terminal.

BFPUm (Breaker Failure Initiation Pickup Delay)

For each enabled terminal, select a time in cycles that you want the breaker failure timer to wait before asserting.

RTPUm (Retrip Delay)

For each enabled terminal, select a time in cycles that you want the retrip timer to wait before asserting.

BFIm (Breaker Fail Initiate)

Use the BFIm setting (SELOGIC control equation) to specify conditions under which the breaker failure initiate input must be active. There is a setting for each of the enabled terminals. If you set BFIm = 1, the input is asserted permanently.

ATBFI*m* (Alternate Breaker Fail Initiate)

Use the ATBFI*m* setting (SELOGIC control equation) to specify conditions under which the alternate breaker failure initiate input must be active. When using the ATBFI*m* setting, be sure to set ABFIT*m* = BFI*m*. There is a setting for each of the enabled terminals. If you set ABFIT*m* = 1, the input is asserted permanently.

ENINBF*m* (Enable Neutral Breaker Fail)

Use the ENINBF*m* setting (SELOGIC control equation) to specify conditions under which the neutral breaker input must be active. There is a setting for each of the enabled terminals. If you set ENINBF*m* = 1, the input is asserted permanently.

INFPU*m* (Neutral Current Pickup)

INFPU*m* is the current pickup setting in secondary amperes for the neutral breaker failure overcurrent element of each enabled terminal. The range is 0.10 to 10 for a 1 A relay.

EBFIS*m* (Breaker Fail Initiate Seal-In)

Enable the breaker failure seal-in timer circuit by setting EBFIS*m* = Y (see *Figure 5.81*).

BFISP*m* (Breaker Fail Initiate Seal-In Delay)

Select a time in cycles that you want the breaker failure seal-in timer to wait before asserting (see *Figure 5.81*).

BFIDO*m* (Alternate Breaker Failure Timer)

Select a time in cycles that you want the alternate breaker failure timer to wait before asserting (see *Figure 5.81*).

Volts/Hertz Elements

Overexcitation occurs when system conditions cause the magnetic core of a transformer to saturate. These system conditions are an overvoltage condition, an underfrequency condition, (or a combination of the two conditions). The volts/hertz function in the SEL-487E combines these two system conditions into one element by calculating the ratio of normalized voltage to normalized frequency (V/Hz). This ratio is proportional to the flux in the transformer core, and therefore, also proportional to any over- or underexcitation of the transformer core. Because transformer core saturation is different for loaded and unloaded transformers, the volts/hertz element provides two levels of definite-time V/Hz protection. In addition, the element also provides two user-defined curves so that you can form an inverse type of V/Hz characteristic.

Definite-Time Elements

Figure 5.84(a) shows the definite-time characteristic when only Level 1 is active, and *Figure 5.84(b)* shows the characteristic when Level 2 is active.
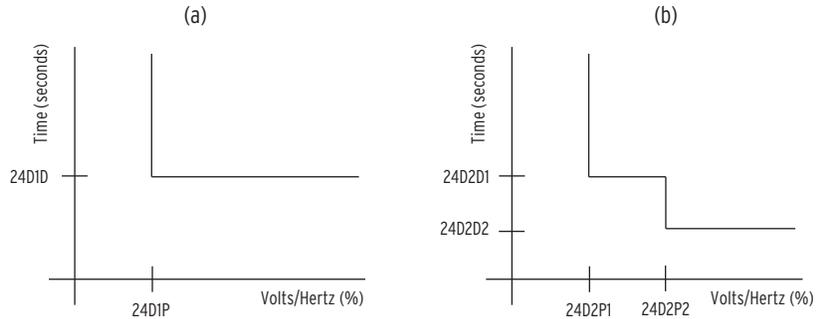
Figure 5.84   Levels 1 and 2 V/Hz

Figure 5.85 shows the definite-time V/Hz logic. To enable the Level 1 element, set Group setting E24 = Y (24CCS is at the default setting = OFF). With the Level 1 element active, only the top part of the logic (up to the V/Hz timer) is active.

After selecting the appropriate voltage (V if 24VSRC = V or Z if 24VSRC = Z), the logic normalizes the measured voltage (maximum of the secondary line-to-line voltages) and the measured frequency to the VNOMk and NFREQ values. To form the V/Hz per-unit value, the logic divides the normalized voltage by the normalized frequency and multiplies the result by 100 to calculate a percentage to form analog quantity 24RPU.

In Comparator C1, the logic compares 24RPU against the 24D1P setting value. If 24RPU exceeds the 24D1P setting value, and if SELOGIC control equation 24TC is asserted, then Gate 1 turns on and the V/Hz conditional timer starts timing. If Gate 1 remains turned on until expiration of the 24D1D time setting, then Relay Word bit 24D1T asserts.

Note that Level 2 of the definite-Time Element uses counters instead of conditional timers, to avoid resetting the conditional timer when 24RPU momentarily dips below the threshold setting. To enable Level 2, set 24CCS = DD. Setting 24CCS to DD asserts one input of both Gate 2 and Gate 3. In Comparator 2, the logic compares 24RPU against the 24D2P1 setting value, and in Comparator 3, the logic compares 24RPU against the 24D2P2 setting value. If SELOGIC control equation 24TC is asserted, Gate 2 turns on when 24RPU exceeds the 24D2P1 setting value, and Gate 3 turns on when 24RPU exceeds the 24D2P2 setting value. In turn, Counter 1 starts when Gate 2 turns on and Counter 2 starts when Gate 3 turns on.

Each counter has two outputs. When either counter reaches a count that equals the timer setting (24D2D1 or 24D2D2), Relay Word bit 24D2T asserts (because these are counters, the time will be longer if 24RPU fell below the threshold setting). When both counters are reset (count = 0), Relay Word bit 24D2R asserts.
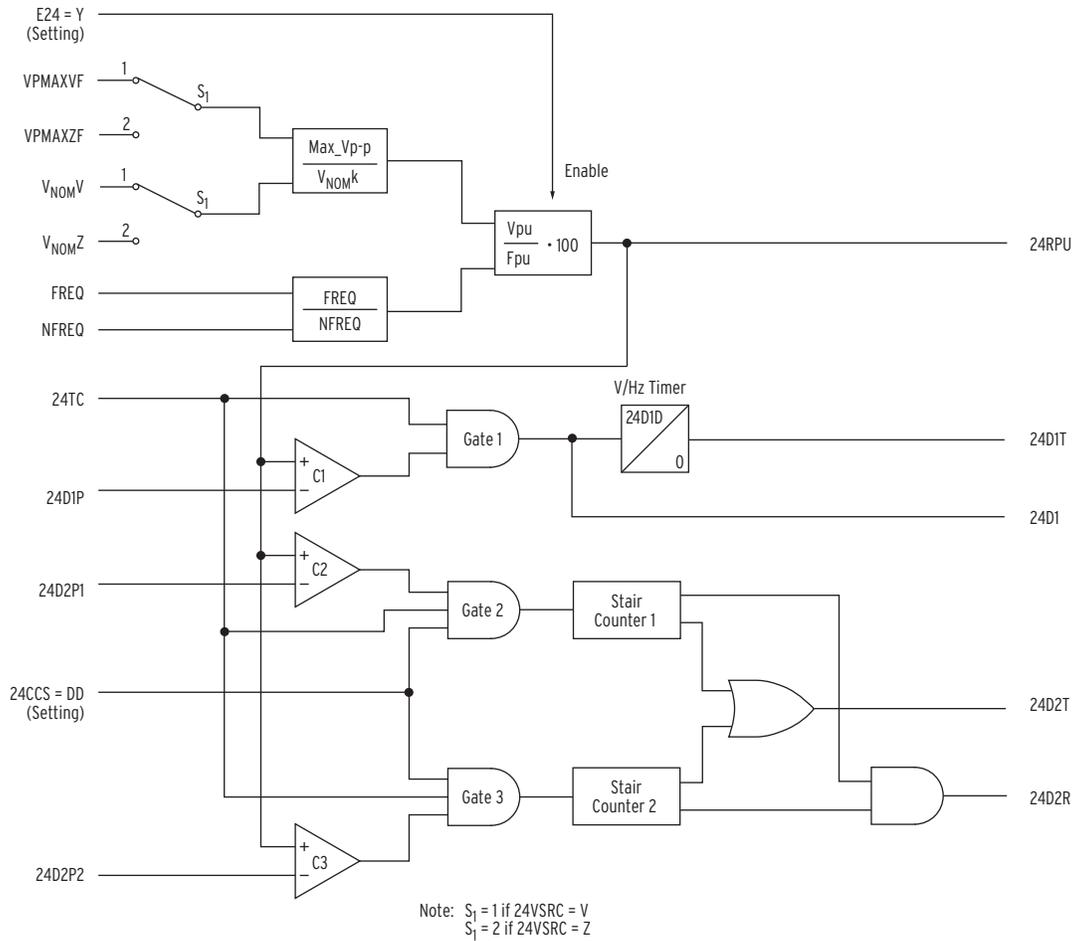
Figure 5.85   Two-Level, Definite-Time V/Hz Logic

User-Defined Curves

Figure 5.86 shows the logic for the user-defined curves. Use setting 24CCS to select either User-Defined Element 1 (24CCS = U1), or both User-Defined Element 1 and User-Defined Element 2 (24CCS = U2). Each element has a separate torque control setting (24U1TC and 24U2TC), and 24RPU is the analog quantity the V/Hz logic calculated in *Figure 5.85*.

These user-defined curves consist of as many as 20 points (24U101–24U120 and 24U201–24U220) to form characteristics suitable for most applications. For each point, enter the V/Hz value and the time associated with that particular V/Hz value. Because the relay calculates the time after linear interpolation of the V/Hz values, enter as many points as possible for accurate time results.
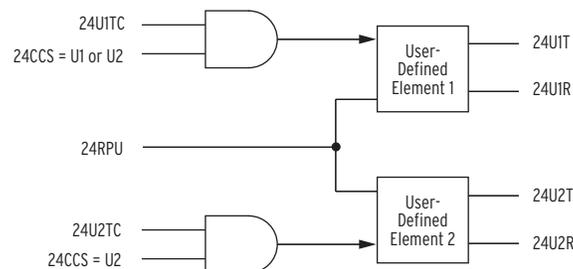
Figure 5.86   Logic for the User-Defined Curves

For example, assume that you obtain the V/Hz characteristic in *Figure 5.87* from a transformer manufacturer. To program this characteristic, you need to enter any number of points between 3 and 20. *Figure 5.87* shows three such points:

➤ Point 24U101: V/Hz = 110 (percentage) and the operate time = 33 (seconds)

➤ Point 24U102: V/Hz = 150 (percentage) and the operate time = 22 (seconds)

➤ Point 24U103: V/Hz = 200 (percentage) and the operate time = 14 (seconds)
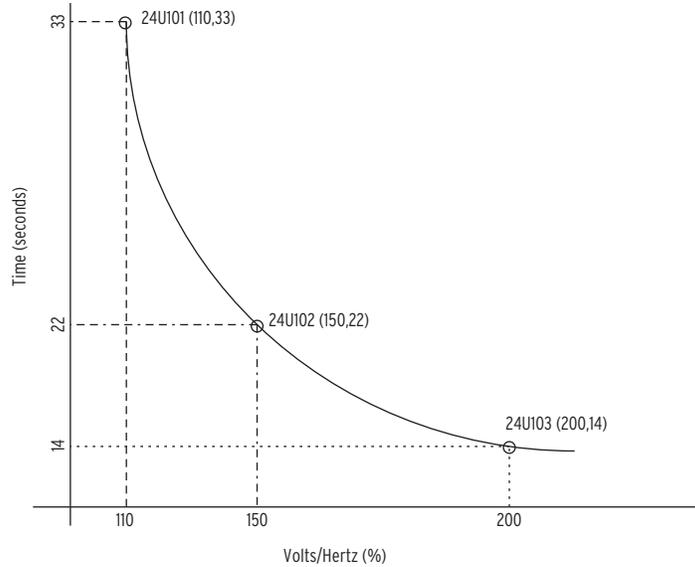
Figure 5.87   V/Hz Curve From Manufacturer

Figure 5.88(a) shows a programmed curve from entry of only three points. Clearly, this programmed curve is much different from the original curve, and the time calculations will be inaccurate. *Figure 5.88(b)* shows a programmed curve, obtained after entry of 16 points, superimposed on the original curve. With more points, the programmed curve closely follows the original curve, and the time calculations are accurate.
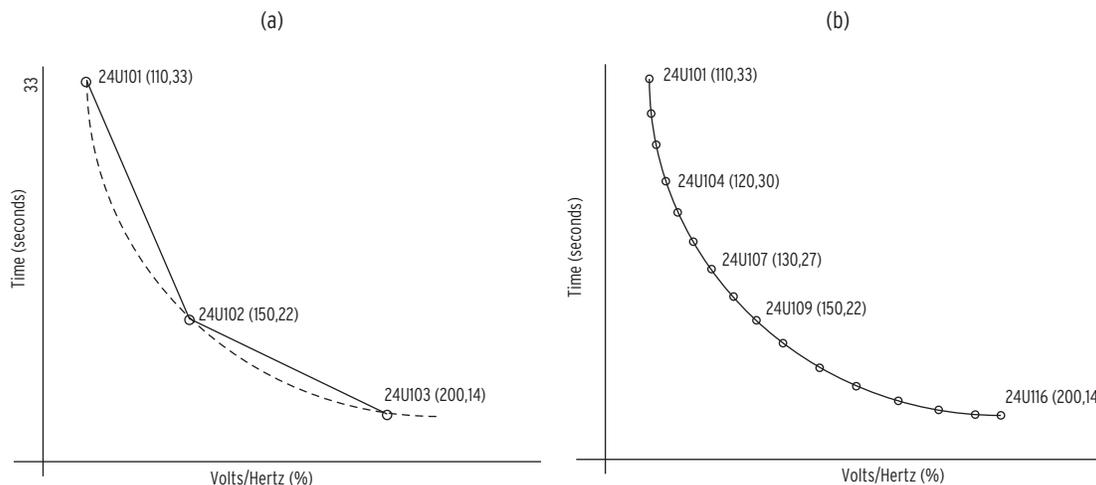
Figure 5.88   Three- and Sixteen-Point Curves

Each element has two output Relay Word bits. When the element times out, Relay Word bits 24U1T (Element 1) and 24U2T (Element 2) assert. When the elements are reset, Relay Word bits 24U1R (Element 1) and 24U2R (Element 2) assert.

Volts/Hertz Settings

24VSRC (Voltage Source for V/Hz Calculation)

⚠️**WARNING**
Make sure the estimated frequency is from the same terminal as the 24VSRC setting. See *Frequency Estimation on page 5.122* for details.

After enabling the V/Hz elements (E24 = Y), select the voltage terminal for calculating V/Hz with the 24VSRC setting. If you have enabled only one voltage terminal (using EPTTERM) then 24VSRC is forced to that terminal.

24D1P (Level 1 Overexcitation Pickup)

Set the Level 1 percentage overexcitation with the 24D1P setting. If you want to use the Level 1 element only, leave the 24CCS setting at the default value (24CCS = OFF).

24D1D (Level 1 Time Delay)

When the system V/Hz exceeds the 24D1P setting value, and if SELOGIC control equation 24TC is asserted, the V/Hz conditional timer starts timing. Set the delay (in seconds) for which the timer must run before the 24D1D setting asserts the output.

24TC (Definite-Time V/Hz Torque Control)

Use the torque-control setting to specify conditions under which the definite-time V/Hz elements must be active. This setting controls all levels of the definite-time elements. The default setting is 1, so that one input into Gates 1–3 in *Figure 5.85* is asserted permanently.

24CCS (Level 2 Composite Curve)

This setting selects which of the V/Hz elements are active, as *Table 5.14* shows.

Table 5.14   Active V/Hz Elements as a Function of the 24CCS Setting

Setting	Active V/Hz Element			
24CCS =[a]	Level 1 DD	Level 2 DD	Level 1 UD	Level 2 UD
OFF	Yes	No	No	No
DD	Yes	Yes	No	No
U1	Yes	No	Yes	No
U2	Yes	No	Yes	Yes

[a] where:
DD = Definite-time element
UD = User-defined element

Although the Level 1 DD element is active by default, you can deactivate this element with the 24TC setting.

24D2P1 (Level 2 Overexcitation Pickup)

To enable the Level 2 percentage overexcitation pickup setting, set E24 = Y and 24CSS = DD. With 24CSS = DD, both Level 1 and Level 2 definite-time V/Hz elements are active.

24D2D1 (Level 2 Time Delay)

When the system V/Hz exceeds the 24D2P1 setting value, and if SELOGIC control equation 24TC is asserted, Stair Counter 1 (*Figure 5.85*) starts timing. Set the delay (in seconds) for which the timer must run before the 24D2D1 setting asserts the output. Although the counter counts in discrete steps, for time calibration the counter is the same as for a conditional timer.

24D2P2 (Level 2 Overexcitation Pickup)

To enable the Level 2 percentage overexcitation pickup setting, set E24 = Y and 24CCS = DD. With 24CCS = DD, both Level 1 and Level 2 definite-time V/Hz elements are active.

24D2D2 (Level 2 Time Delay)

When the system V/Hz exceeds the 24D2P2 setting value, and if SELOGIC control equation 24TC is asserted, Stair Counter 2 starts timing. Set the delay (in seconds) for which the timer must run before asserting the output with the 24D2D2 setting. Although the counter counts in discrete steps, time calibration for the counter is the same as for a conditional timer.

24U1TC (User-Defined Curve 1 Torque Control)

Use the torque-control setting to specify conditions under which the user-defined V/Hz Curve 1 must be active. The default setting is 1, so one input into each of Gate 1, Gate 2, and Gate 3 in *Figure 5.85* is asserted permanently.

24U1NP (Number of Points for User-Defined Curve 1)

Form user-defined curves by entering as many as 20 points that the relay interpolates to form a particular V/Hz characteristic. Use setting 24U1NP to specify the number of points for Curve 1 (see *Figure 5.87* and *Figure 5.88*).

24U1*xx* (Data Points for User-Defined Curve 1)

Enter the data point here to form the user-defined curve. Data points must be entered in order of increasing V/Hz values. The data point format is <volts/hertz>(comma)<time> (i.e., 115,30).

The units are volts/hertz in percent and time in seconds.

24U1CR (User-Defined Curve 1 Reset Time)

Specify the Curve 1 reset time with the 24U1CR setting. This setting is only an absolute value if the element has timed out (if 24U1T has asserted). If there is interruption of the Curve 1 timing, then the reset time is proportional to the elapsed time. For example, assume there is an overexcitation condition on the system and Curve 1 starts timing. At the 60 percent mark, the system overexci-

tation condition disappears, and Curve 1 stops timing. Because the timing interruption was at the 60 percent mark, the reset time is also 60 percent of the 24U1CR setting.

24U2TC (User-Defined Curve 2 Torque Control)

Use the torque-control setting to specify conditions under which the user-defined V/Hz Curve 2 must be active. The default setting is 1, so the top input into the Curve 2 AND gate in *Figure 5.85* is asserted permanently.

24U2NP (Number of Points for User-Defined Curve 2)

Form user-defined curves by entering as many as 20 points that the relay interpolates to form a particular V/Hz characteristic. Use setting 24U2NP to specify the number of points for Curve 2 (see *Figure 5.87* and *Figure 5.88*).

24U2*xx* (Data Points for User-Defined Curve 2)

Enter the data point here to form the user-defined curve. Data points must be entered in order of increasing V/Hz values. The data point format is <volts/hertz>(comma)<time> (i.e., 115,30).

The units are volts/hertz in percent and time in seconds.

24U2CR (User-Defined Curve 2 Reset Time)

Specify the Curve 1 reset time with the 24U2CR setting. This setting is only an absolute value if the element has timed out (if 24U2T has asserted). If there is interruption of the Curve 2 timing, then the reset time is proportional to the elapsed time. For example, assume there is an overexcitation condition on the system and Curve 2 starts timing. At the 60 percent mark, the system overexcitation condition disappears and Curve 2 stops timing. Because the timing interruption was at the 60 percent mark, the reset time is also 60 percent of the 24U2CR setting.

Synchronism Check

NOTE: If the relay is using a remote data acquisition system, such as TiDL, the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

Synchronism-check elements prevent circuit breakers from closing if the corresponding phases across the open circuit breaker are excessively out-of-phase, magnitude, or frequency. The SEL-487E synchronism-check elements selectively close circuit breaker poles under the following criteria:

The systems on both sides of the open circuit breaker are in phase (within a settable voltage angle difference), and one of the following is true:

➤ The voltages on both sides of the open circuit breaker are healthy (within a settable voltage magnitude window).

➤ The difference between the voltages on both sides of the open circuit breaker is less than a set limit.

➤ The voltages on both sides are healthy and the difference voltage is less than a set limit.

You can use synchronism-check elements to program the relay to supervise circuit breaker closing; include the synchronism-check element outputs in the close SELOGIC control equations. These element outputs are Relay Word bits

25W1BK*m*, 25W2BK*m*, 25A1BK*m*, and 25A2BK*m* (*m* = S, T, U, W, or X) (see *Synchronism-Check Logic Outputs on page 5.100* and *Angle Checks and Synchronism-Check Element Outputs on page 5.107*).

An example best demonstrates the synchronism-check capability in the SEL-487E. This section presents a typical synchronism-check system.

Generalized System

The generalized system single-line drawing in *Figure 5.89* shows a partial circuit breaker-and-a-half or ring-bus substation arrangement. Assuming that both Circuit Breakers BKS and BKT are open, the system is split into three sections: Bus S, Bus T, and Line.
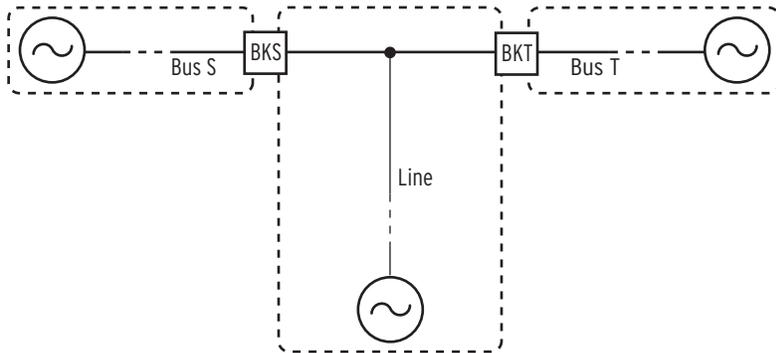
Figure 5.89   Partial Breaker-and-a-Half or Partial Ring-Bus Breaker Arrangement

Paralleled and Asynchronous Systems

Figure 5.89 shows remote sources for each section. Often, a portion of the power system is paralleled beyond the open Circuit Breakers BKS and BKT; the remote sources are really the same aggregate source. If the aggregate source is much closer to one side of the open circuit breaker than the other, there is a noticeable voltage angle difference across the system (it is not simply zero degrees). The corresponding angular separation results from load flow and the impedance of the parallel system.

You must conduct a load flow study to determine the maximum angle across the circuit breaker and consider this angle difference when setting the synchronism-check element for a paralleled system. For example, if the expected load angle because of load flow is 10 degrees, do not set the voltage angle difference setting to less than 15–20 degrees. A paralleled system does not imply a zero degree voltage angle difference at every measuring point.

Single-Phase Voltage Inputs

Figure 5.90 shows single-phase voltage transformers on Bus S and Bus T. Use these single-phase voltage sources to perform a synchronism check across the two circuit breakers.
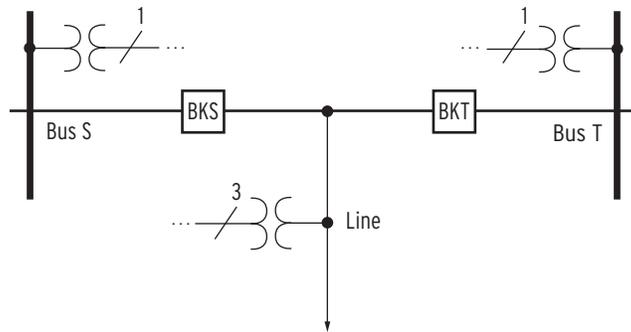
Figure 5.90   Synchronism-Check Voltages for Two Circuit Breakers

Synchronism check occurs on a single-phase voltage basis—see the single-phase potential transformers shown on each bus in *Figure 5.90*. The assumption is that if the monitored single-phase voltage inputs are in phase (within a settable voltage angle difference), and they meet the criteria of being healthy (within a settable voltage magnitude window) and/or the voltage difference is less than a set limit, the other phase-to-neutral voltages are likewise in phase and share the same voltage magnitude relationship. The line voltage source is three-phase, but you only need a single-phase bus voltage to perform a synchronism check across the corresponding circuit breaker. The relay uses the three-phase voltage from the load for other functions such as metering.

Setting 25_SCHM := Y

If setting 25_SCHM = Y, the synchronizing logic verifies that both the reference voltage and synchronizing voltage are healthy (within a settable voltage magnitude window) before enabling the synchronism-check logic.

Setting 25_SCHM := Y1

If setting 25_SCHM = Y1, the synchronizing logic verifies that the difference voltage between the reference and synchronizing voltages is less than the 25VDIF setting before enabling the synchronism-check logic.

Setting 25_SCHM := Y2

If setting 25_SCHM = Y2, the synchronizing logic verifies that both the reference and synchronizing voltages are healthy and that the difference between them is less than the 25VDIF setting before enabling the synchronism-check logic. It combines the logic that is used when 25_SCHM is set to Y or Y1.

Synchronism-Check Settings Example
E25 (Enable Synchronism Check)

Select the terminals that will be available for synchronism check. The E25 setting is hidden if the CT or PT terminals are not enabled (i.e., the setting ECTTERM = OFF or EPTTERM = OFF). The available terminals are limited to the terminals selected in the ECTTERM setting.

This example uses a two-circuit breaker arrangement (Breakers S and T) (see *Figure 5.90*). Set the synchronism-check enable settings:

E25 := **S, T** Enable Synchronism Check for Breaker S and Breaker T

Figure 5.91 shows the correspondence between the synchronism-check settings and the two-circuit breaker application example. The following sections explain these settings and include an explanation of Alternative Synchronism-Check Voltage Source T settings (see *Figure 5.105*).
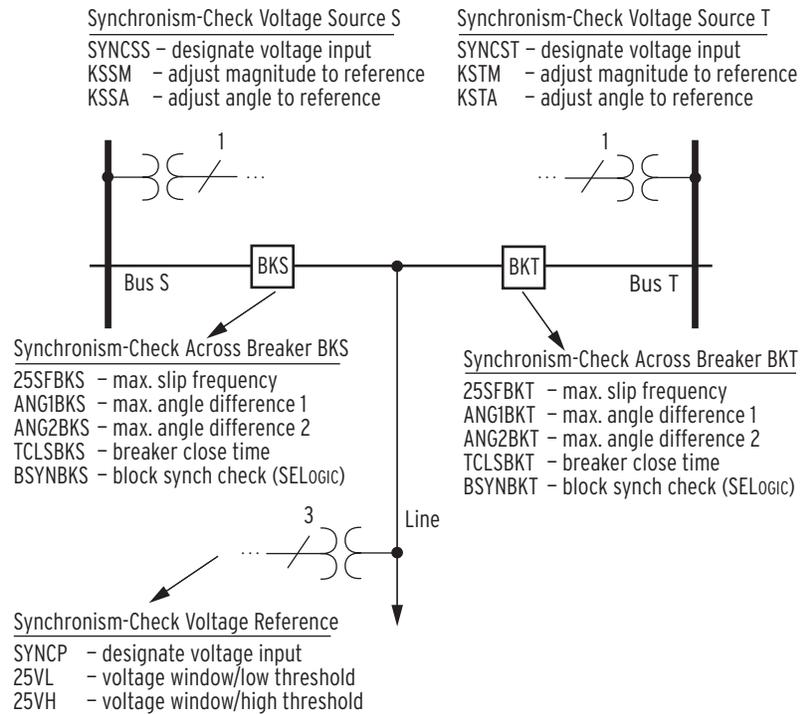
Figure 5.91   Synchronism-Check Settings

Synchronism Check (25) Voltage Reference and Breaker *m* Synchronism Source Voltage

When the E25 synchronism-check setting is enabled for terminal m, the relay checks if SYNCP (the polarizing reference voltage), and SYNCS*m* (the synchronizing source voltage), are within the voltage threshold window and the block synchronism-check equation (BSYNBK*m*) is not asserted. Note that SYNCP and SYNCS*m* need to be unique per Breaker when each of these settings are enabled. The available voltage inputs are limited to the terminals enabled by the EPTTERM setting.

Synchronism-Check Logic Outputs

Figure 5.92 shows the correspondence between synchronism-check logic outputs (Relay Word bits) and the two-circuit breaker arrangement. These Relay Word bits assert to logical 1 (e.g., 59VP equals logical 1) if true and deassert to logical 0 if false. *Table 5.15* lists these Relay Word bits.
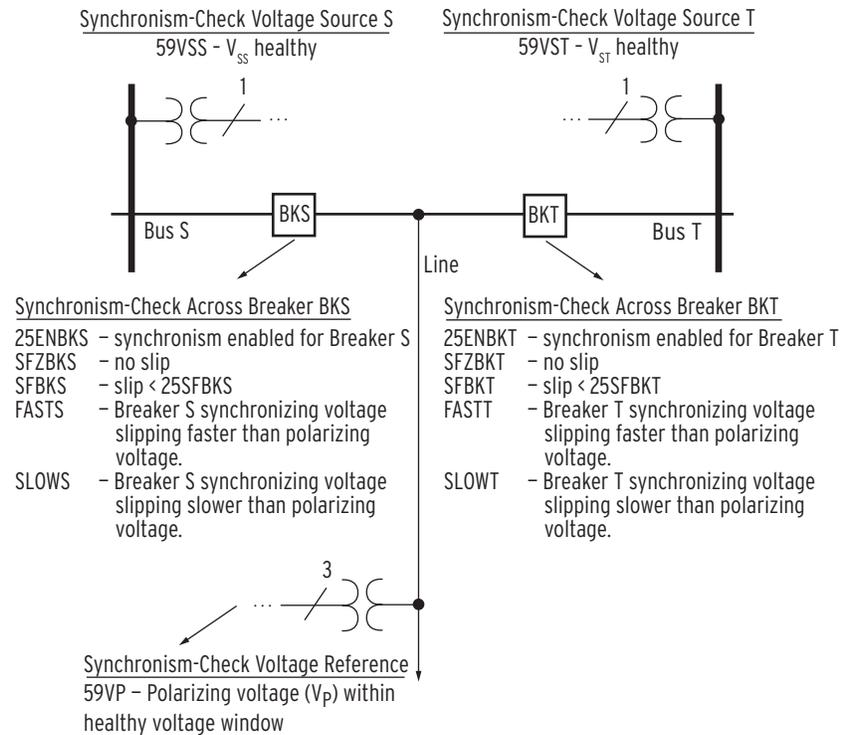
Figure 5.92 Synchronism-Check Relay Word Bits

NOTE: The polarizing voltage, VP, is often referred to as the synchronism-check voltage reference throughout the examples below. It is the user-selectable voltage associated with the Synchronism Check (25) Reference setting, SYNCP.

NOTE: f_{Sm} is the frequency of the synchronizing voltage associated with Breaker m, where m = S, T, U, W, or X.

NOTE: If the Maximum Slip Frequency setting 25SFBKm = OFF, then the Relay Word bit SFBKm = 0.

NOTE: The term uncompensated refers to the synchronism-check logic and associated Relay Word bits that do not take into consideration the breaker closing time setting (TCLSBKm) or the slip frequency (25SLIPm). If the polarizing voltage and synchronizing voltage for the breaker are not slipping (i.e., when SFZBKm = 1 or when the setting 25SFBKm = OFF), the uncompensated synchronism-check logic allows closing permission without considering the setting TCLSBKm or the analog quantity 25SLIPm. When the setting 25SFBKm = OFF, the setting TCLSBKm is disabled. The Relay Word bits associated with compensated synchronism check allow closing permission considering the breaker closing time and slip frequency.

Table 5.15 Synchronism-Check Relay Word Bits[a] (Sheet 1 of 2)

Relay Word Bit	Description
59VP	Polarizing voltage (V$_P$) within healthy voltage window.
59VPm	Breaker m polarizing voltage (V$_P$) within healthy voltage window.
59VSm	Breaker m synchronizing voltage (V$_{Sm}$) within healthy voltage window.
ALTSm	Breaker m alternate synchronizing voltage source selected.
ALTPm1	Breaker m Alternate Reference Source Selection Logic 1 (SELOGIC control equation)
ALTPm2	Breaker m Alternate Reference Source Selection Logic 2 (SELOGIC control equation)
BSYNBKm	Breaker m synchronism check blocked.
25ENBKm	Breaker m synchronism-check element enabled.
59VDIFm	The difference between the polarizing voltage magnitude, VPFM, and the Breaker m synchronizing voltage magnitude, 25VSmFM, is less than the limit set by 25VDIF (see *Figure 5.97*).
SFZBKm	Breaker m slip frequency less than 0.005 Hz ("no-slip" condition).
SFBKm	0.005 Hz ≤ Breaker m slip frequency < maximum slip frequency (25SFBKm).
25A1m	Breaker m voltage with uncompensated sync angle within ± Sync Angle 1 (ANG1BKm) window and SFZBKm is asserted (no slip).
25A2m	Breaker m voltage with uncompensated sync angle within ± Sync Angle 2 (ANG2BKm) window and SFZBKm is asserted (no slip).
25C1m	Breaker m voltage with slip-compensated sync angle is within zero degrees to ANG1BKm when FASTm is asserted. When SLOWm is asserted, it is within zero degrees to –ANG1BKm (zero-degree close attempt). 25C1m is supervised with NOT SFZBKm and maximum allowed slip-frequency setting 25SFBKm (SFBKm asserted).

Table 5.15   Synchronism-Check Relay Word Bits[a] (Sheet 2 of 2)

Relay Word Bit	Description
25WC1m	Breaker m voltage with slip-compensated sync angle is within zero degrees to ANG1BKm when FASTm is asserted. When SLOWm is asserted, it is within zero degrees to –ANG1BKm (zero-degree close attempt).
25C2m	Breaker m voltage with slip-compensated sync angle is within zero degrees to ANG2BKm when FASTm is asserted. When SLOWm is asserted, it is within zero degrees to –ANG2BKm (zero-degree close attempt). 25C2m is supervised with NOT SFZBKm and maximum allowed slip-frequency setting 25SFBKm (SFBKm asserted).
25WC2m	Breaker m voltage with slip-compensated sync angle is within zero degrees to ANG2BKm when FASTm is asserted. When SLOWm is asserted, it is within zero degrees to –ANG2BKm (zero-degree close attempt).
25W1BKm	Breaker m voltage is within the uncompensated and unsupervised Synchronism Angle 1 window.
25W2BKm	Breaker m voltage is within the uncompensated and unsupervised Synchronism Angle 1 window.
25A1BKm	Breaker m voltage is within either the uncompensated or slip-compensated Angle 1 window (25A1m OR 25C1m).
25A2BKm	Breaker m voltage is within either the uncompensated or slip-compensated Angle 2 window (25A2m OR 25C2m).
FASTm	The frequency of the voltage associated with Breaker m is greater than the frequency of the reference (polarizing) voltage ($f_{S_m} > f_P$)
SLOWm	The frequency of the voltage associated with Breaker m is less than the frequency of the reference (polarizing) voltage ($f_{S_m} < f_P$)

[a] m = S, T, U, W, or X.

If the synchronism-check element is not enabled for a particular circuit breaker, the following Relay Word bits are forced to the conditions below. In this example, the synchronism-check element is only enabled for Terminals S and T. Therefore, Terminals U, W, and X are not enabled.

E25 = S, T

25ENBK [U, W, and X] = 0

SFZBK [U, W, and X] = 0

SFBK [U, W, and X] = 0

Also, in this example, the analog quantities 25ANG [U, W, and X] = 0, 25ANGC [U, W, and X] = 0, and 25SLIP [U, W, and X] = 10,000 because synchronism check is not enabled for Terminals U, W, and X.

PT Connections

Figure 5.93 is an example of connecting PTs to the SEL-487E for two circuit breakers. The Bus S and Bus T single-phase voltages are connected to relay voltage inputs VAZ and VBZ, respectively. They could just as easily have been connected to any of the other voltage inputs. The voltage connected to voltage input VAZ (setting SYNCSS := VAZ; see *Figure 5.93*) is not necessarily from A-Phase on Bus S. Likewise, the voltage connected to voltage input VBZ (setting SYNCST := VBZ; see *Figure 5.93*) is not necessarily from B-Phase on Bus T. The connection can be from any phase-to-neutral or phase-to-phase voltage (as long as you do not exceed the relay voltage input ratings). Settings in the

SEL-487E compensate for any steady-state magnitude or angle difference with respect to a synchronism-check voltage reference, as discussed next in this example.

Three-phase line voltages are connected to relay voltage inputs VAV, VBV, and VCV (these voltage inputs are also used for loss-of-potential and directionality). Only one of these single-phase voltage inputs is designated for use in synchronism check. In this example, this voltage input is also designated the synchronism-check voltage reference (setting SYNCP := VAV; see *Figure 5.93*). As the synchronism-check voltage reference, the relay makes all steady-state magnitude and angle adjustments for the Bus S and Bus T synchronism-check voltages (connected to voltage inputs VAZ and VBZ, respectively, as discussed in the preceding paragraph) with respect to this designated reference line voltage, VAV, as discussed later in this example.
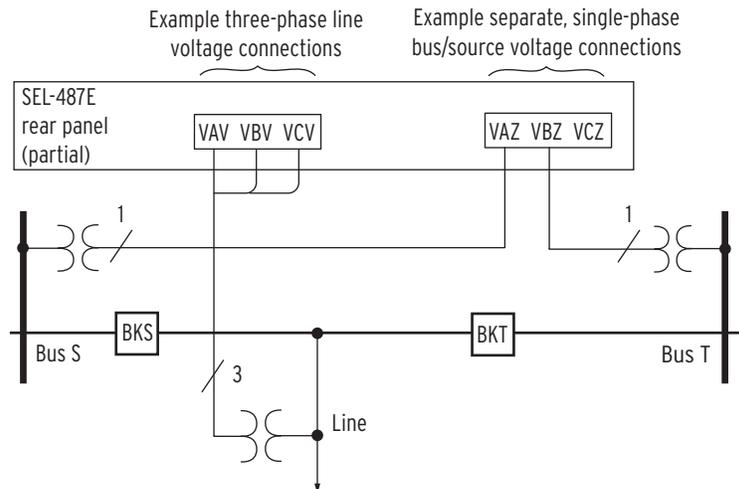
Figure 5.93   Example Synchronism-Check Voltage Connections to the SEL-487E

For a single-circuit breaker application, connect the three-phase voltage source to voltage inputs VAV, VBV, and VCV. If a single-phase voltage source is available on the other side of the circuit breaker for synchronism check, connect the source to voltage input VAZ, VBZ, or VCZ.

Voltage Magnitude and Angle Compensation

The *Figure 5.93* example continues in *Figure 5.94*. The *Figure 5.94* example demonstrates possible voltage input connections (presuming ABC phase rotation). The synchronism-check voltage reference (V_P) is from the A-Phase voltage (V_A) of the line (setting SYNCP := VAV). You can connect the voltage synchronizing source, SYNCSS, as a phase-to-phase voltage V_{BC} originating from Bus S, and connect the voltage synchronizing source, SYNCST, as a phase-to-neutral voltage V_C from Bus T. Thus, Bus S voltage V_{BC} lags synchronism-check voltage reference V_P by 90 degrees, and Bus T voltage V_C lags the synchronism-check voltage reference V_P by 240 degrees (same as –120 degrees). To compensate for these steady-state angle differences, set KSSA for Bus S and KSTA for Bus T as follows.

KSSA := **90** Synchronism Source S Angle Shift (–179.99 to 180 degrees)

KSTA := **–120** Synchronism Source T Angle Shift (–179.99 to 180 degrees)
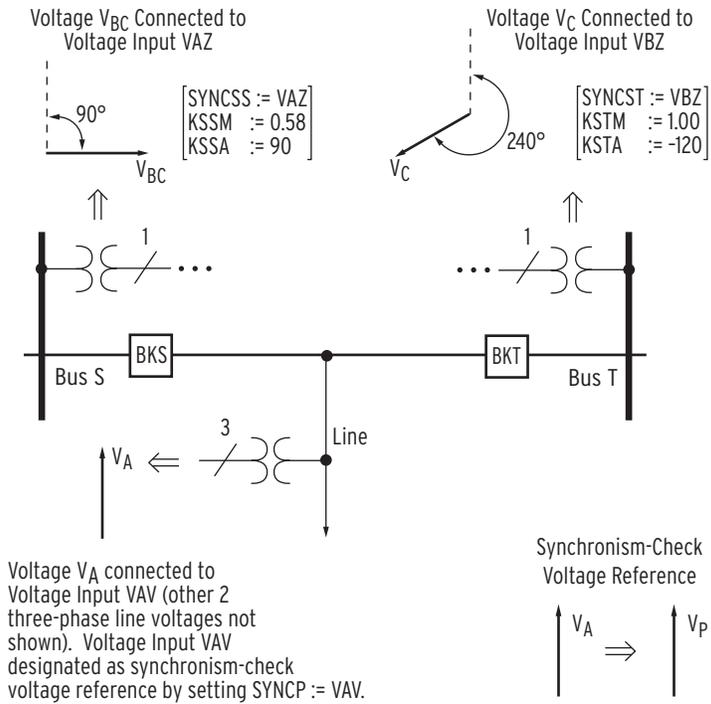
Figure 5.94   Synchronism-Check Voltage Reference

For a given secondary base voltage, phase-to-phase voltages are a factor of 1.73 ($\sqrt{3}$) times the magnitude of the phase-to-neutral voltages. In reverse, phase-to-neutral voltages are a factor of 0.58 ($1/\sqrt{3}$) times the magnitude of the phase-to-phase voltages. Therefore, you must compensate the Bus S voltage V_{BC} magnitude with setting KSSM to reference it to the synchronism-check voltage reference V_P magnitude.

> KSSM := **0.58** Synchronism Source S Ratio Factor (0.10–3.00)

You do not need special magnitude compensation for the Bus T voltage V_C to reference Synchronism Source T to the synchronism-check voltage reference V_P magnitude; these are both phase-to-neutral voltages with the same nominal rating (for example, 67 V secondary).

> KSTM := **1.00** Synchronism Source T Ratio Factor (0.10–3.00)

As another example of synchronism-source magnitude adjustment flexibility, suppose Bus S voltage V_{BC} is 201 V secondary (phase-to-phase), and the synchronism-check voltage reference V_P is 67 V secondary (phase-to-neutral). Then, the magnitude compensation setting would be as in *Equation 5.32*.

$$\text{KSSM} = \frac{67\text{ V}}{201\text{ V}} := 0.33$$

Equation 5.32

Normalized Synchronism-Check Voltage Sources VSS and VST

The *Figure 5.94* example continues in *Figure 5.95*. *Figure 5.95* graphically illustrates how the introduced settings adjust the Bus S and Bus T synchronism-check input voltages in angle and magnitude to reference to the synchronism-check voltage reference, V_P. The resultant Bus S and Bus T voltages are the normalized synchronism-check voltage sources V_{SS} and V_{ST}, respectively.

Voltages V_P, V_{SS}, and V_{ST} are used in the logic of this section to check for healthy voltage and determine voltage phase angle for synchronism-check element operation. Analog quantities 25VPFM and 25VPFA are available to monitor the polarizing voltage magnitude and angle. Similarly, the analog quantities 25VS*m*FM and 25VS*m*FA are available to monitor the normalized synchronizing voltage magnitude and angle for Breaker *m*.
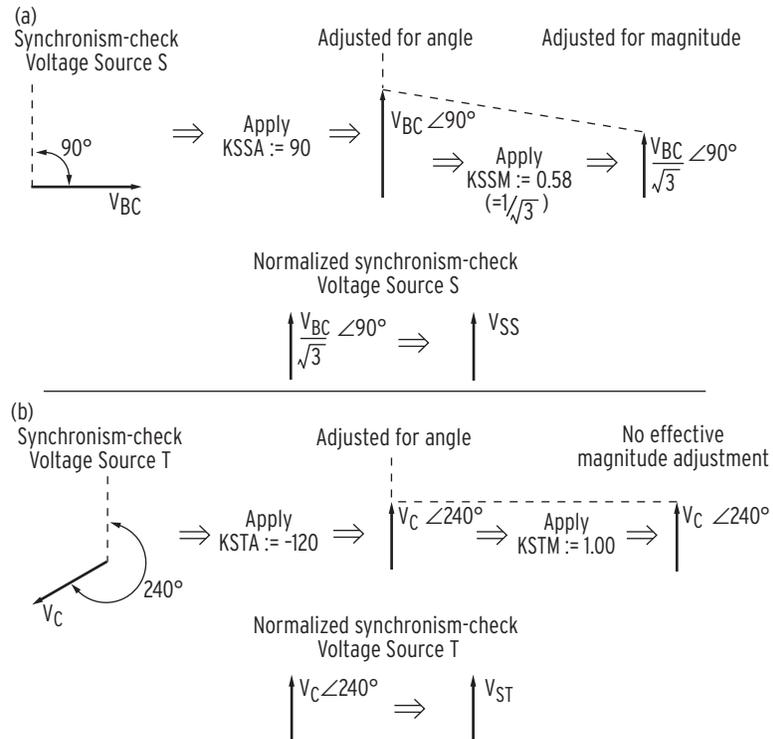
Figure 5.95   Normalized Synchronism-Check Voltage Sources V_{SS} and V_{ST}

Voltage Checks and Blocking Logic

Two conditions can cause the synchronism-check function in the SEL-487E to abort. These conditions are out-of-range synchronism-check input voltages and block synchronism-check configurations that you specify in SELOGIC control equations.

Voltage Magnitude Checks (Applicable When 25_SCHM = Y or Y2)

For synchronism check to proceed for a given circuit breaker (BKS or BKT) when 25_SCHM = Y or Y2, the voltage magnitudes of the synchronism-check voltage reference, V_P, and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker (normalized voltage V_{SS} for Circuit Breaker BKS and normalized voltage V_{ST} for Circuit Breaker BKT) must lie within a healthy voltage window, bounded by voltage threshold settings 25VH and 25VL (see *Figure 5.96*).

The relay asserts Relay Word bits 59VP, 59VSS, and 59VST to indicate healthy synchronism-check voltages V_P, V_{SS}, and V_{ST} (see *Figure 5.96*). If either of the voltage pairs (V_P and V_{SS} or V_P and V_{ST}) does not meet this healthy voltage criterion, synchronism check cannot proceed for the circuit breaker associated with the corresponding voltage pair.
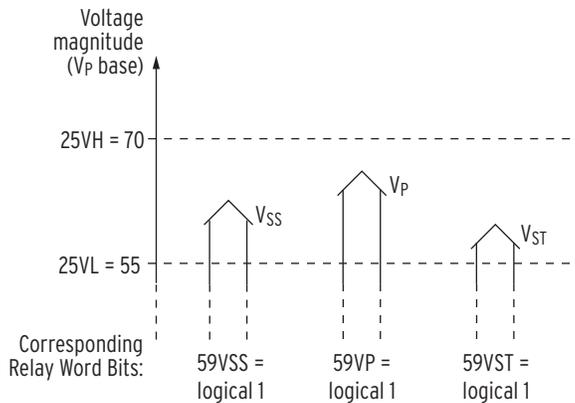
Figure 5.96   Healthy Voltage Window and Indication

Voltage Difference Checks (Applicable When 25_SCHM = Y1 or Y2)

For synchronism check to proceed for a given circuit breaker (BKm) when 25_SCHM = Y1 or Y2, the absolute value of the difference between the synchronism-check reference voltage, 25VPFM, and the corresponding normalized synchronism-check voltage source on the other side of the circuit breaker, 25VSmFM (m = S, T, U, W, X), must be less than the 25VDIF setting (see *Figure 5.97*). The logic includes a 5 V secondary check to ensure the relay does not operate on erroneous signals.

> **NOTE:** Analog quantities 25VPFM and 25VPFA are forced to zero when EISYNC := Y; analog quantities 25VPmFM and 25VPmFA are forced to zero when EISYNC :=N.
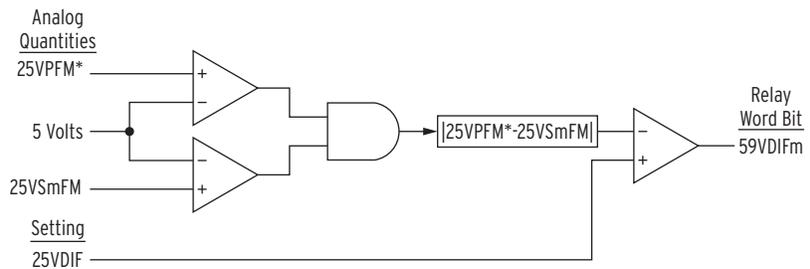
* 25VPFM is replaced with 25VPmFM when EISYNC = Y

Figure 5.97   Synchronism-Check Voltage Difference Logic

Block Synchronism Check

If the block synchronism check BSYNBKm SELOGIC control equation (where m = S, T, U, W, or X) asserts, synchronism check cannot proceed for the corresponding circuit breaker. Following is an example for Circuit Breaker BKm:

BSYNBKm := **52CLm**   Block Synchronism Check—BKm (SELOGIC Equation)

If Circuit Breaker BKm is closed, the indication back to the relay shows 52CLm equals logical 1. Thus, BSYNBKm equals logical 1, and synchronism check is blocked for Circuit Breaker BKm. There is no need to qualify or continue with the synchronism check for circuit breaker closing; the circuit breaker is already closed.

Synchronism-Check Enable Logic

The relay combines the voltage check elements and block synchronism check condition to create a synchronism-check enable condition for each circuit breaker, as shown in *Figure 5.98*. The 25_SCHM setting determines which enable logic is active.
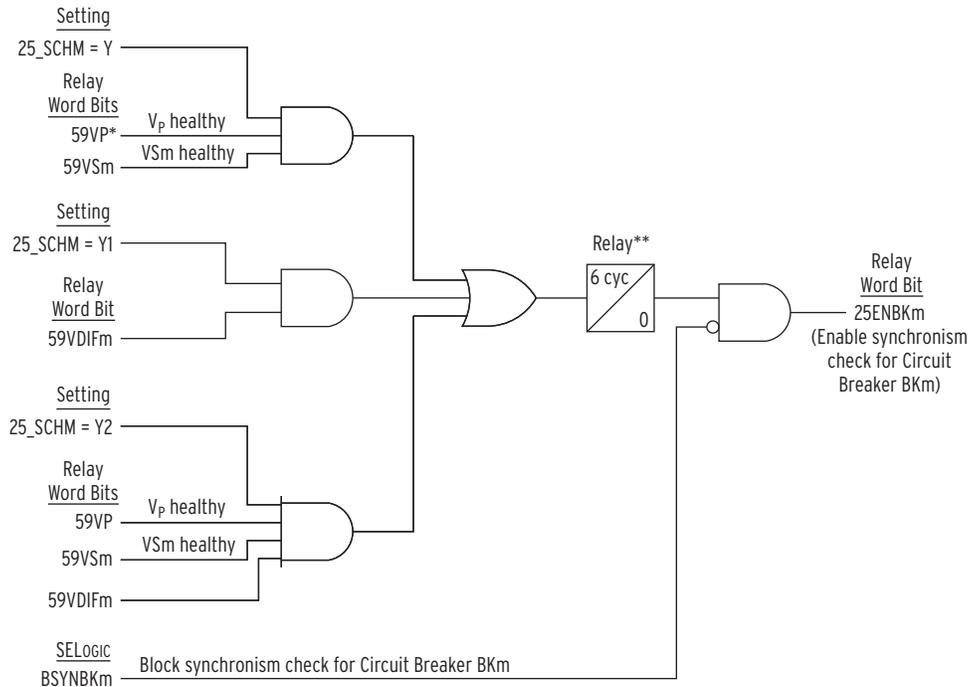
* 59VPm replaces 59VP when EISYNC = Y.
** The pickup timer resets whenever a synchronizing or polarizing voltage source changes.

Figure 5.98 Synchronism-Check Enable Logic

Angle Checks and Synchronism-Check Element Outputs

After the relay determines that it is appropriate to enable synchronism-check logic as defined in *Figure 5.98*, the relay must check voltage phase angles across the circuit breakers before a final synchronism-check element output can be available for supervising circuit breaker closing.

The following discussion/examples use Circuit Breaker BKS. Synchronism-check element output operation for Circuit Breaker BKT, U, W, or X is similar (replace BKT, U, W, or X for BKS in associated settings and Relay Word bits).

Angle Difference Settings ANG1BKS and ANG2BKS

NOTE: If the relay is using a remote data acquisition system, such as TiDL, the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

Each circuit breaker has two angle difference windows. For Circuit Breaker BKS, the maximum angle difference settings are ANG1BKS and ANG2BKS.

Slip-Frequency Element
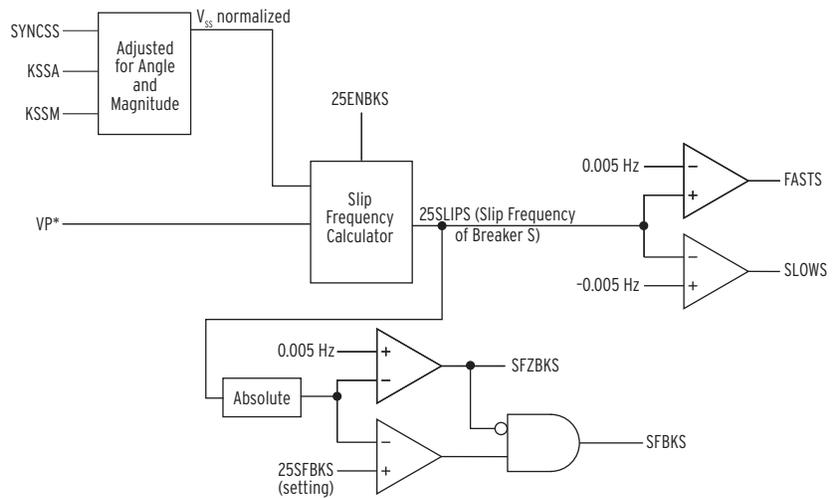
* Each breaker is assigned a polarizing voltage (VP*m*) and normalized when
EISYNC = Y. See *Independent Synchronism-Check Polarizing Voltage Selection
Settings on page 5.116* for details.

Figure 5.99   Breaker S Slip Frequency Check Logic

"No-Slip" and "Slipping" Synchronism-Check Elements

Figure 5.100 and *Figure 5.101* show the logic for static and slipping synchro-
nism-check elements. The following examples compare the operation of these
two elements under different system conditions.
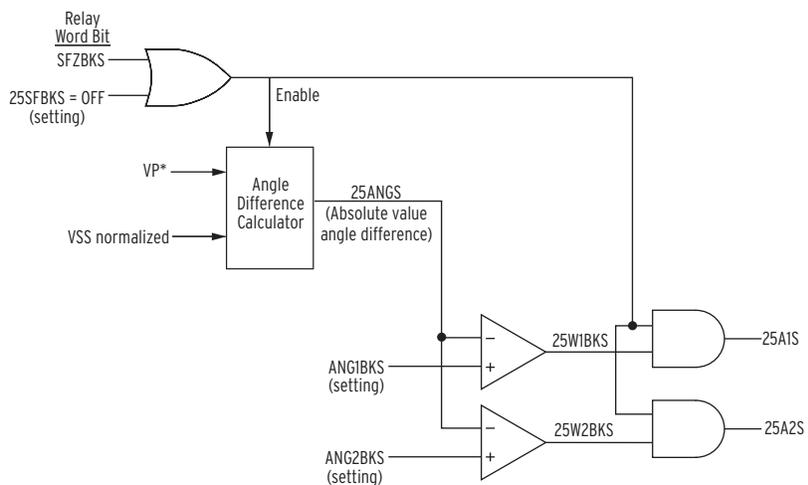
* Each breaker is assigned a polarizing voltage (VP*m*) and normalized when
EISYNC = Y. See *Independent Synchronism-Check Polarizing Voltage Selection
Settings on page 5.116* for details.

Figure 5.100   Static (Not Slipping) Synchronism-Check Elements
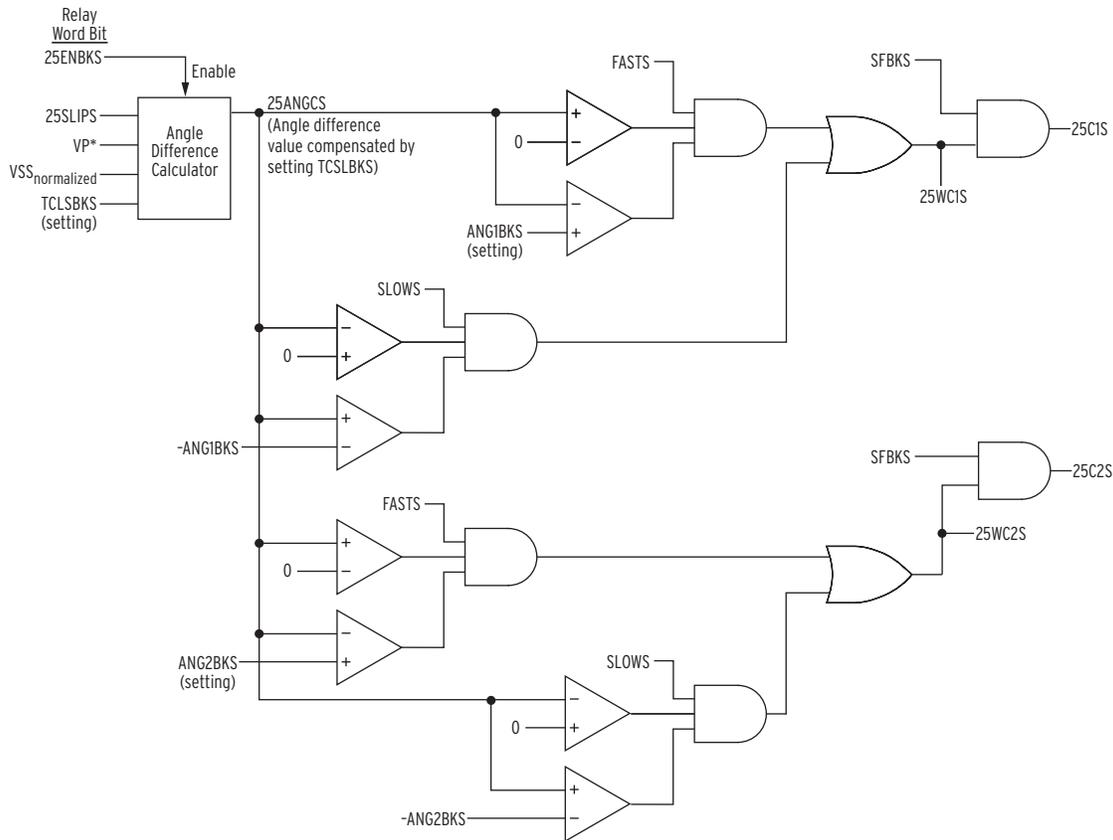
* Each breaker is assigned a polarizing voltage (VP*m*) and normalized when EISYNC = Y. See *Independent Synchronism-Check Polarizing Voltage Selection Settings on page 5.116* for details.

Figure 5.101   Slipping Synchronism-Check Elements

"No-Slip" Synchronism Check

Refer to the paralleled system beyond the open circuit breaker in *Figure 5.101*. For such a system, there is essentially no slip across the open circuit breaker (the monitored voltage phasors on each side are not moving with respect to one another). In a "no-slip" system, any voltage angle difference across the open circuit breaker remains relatively constant.

The four drawings shown in *Figure 5.102* are separate, independent cases for a "no- slip" paralleled system. If the phase angle between the synchronism-check voltage reference V_P and the normalized synchronism-check voltage source V_{SS} is less than angle setting ANG1BKS, synchronism-check element output 25A1S asserts to logical 1. The relay declares that the per-phase voltages across Circuit Breaker BKS are in synchronism. Otherwise, if the phase angle is greater than or equal to angle setting ANG1BKS, element output 25A1S deasserts to logical 0; the relay declares that the per-phase voltages across Circuit Breaker BKS are out-of-synchronism.

The out-of-synchronism phase angles in *Figure 5.102* appear dramatic for a "no-slip" paralleled system. This is for illustrative purposes; these angles are not usually this large in actual systems.
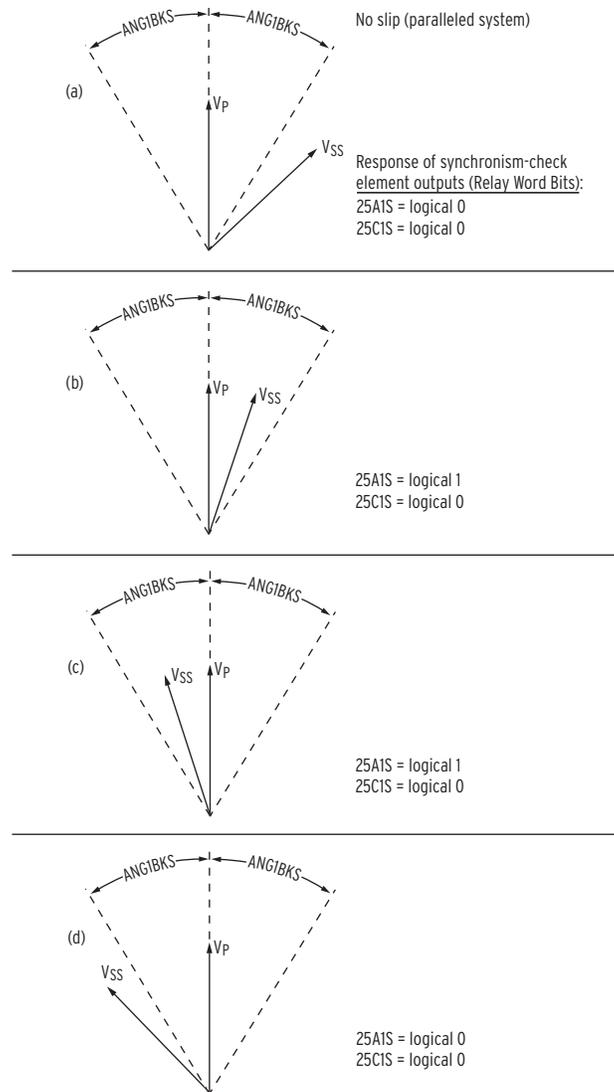
Figure 5.102   "No-Slip" System Synchronism-Check Element Output Response

Slip Frequency and SFZBKS

Relay Word bit SFZBKS (BKS Slip Frequency less than 0.005 Hz) also asserts to logical 1, indicating a "no-slip" condition across Circuit Breaker BKS. In other words, the slip frequency is less than 0.005 Hz ($|f_{SS}-f_P| < 0.005$ Hz).

Synchronism-Check Element Output Effects

Note that during a "no-slip" condition, FASTS, SLOWS, and SFBKS will all be deasserted, forcing 25C1S to logical 0.

"Slip—No Compensation" Synchronism Check

The four cases [*(a)*, *(b)*, *(c)*, and *(d)*] shown in *Figure 5.103* are "slip—no compensation" cases for asynchronous systems (not paralleled). The cases progress in time from top to bottom. The normalized synchronism-check voltage source V_{SS} slips with respect to synchronism-check voltage reference V_P. The indication

of the rotation arrow on phasor V_{SS} (and the time progression from top to bottom) shows that the system corresponding to V_{SS} has a higher system frequency f_{SS} than the system corresponding reference V_P with system frequency f_P. The slip frequency across Circuit Breaker BKS is $f_{SS}-f_P$.
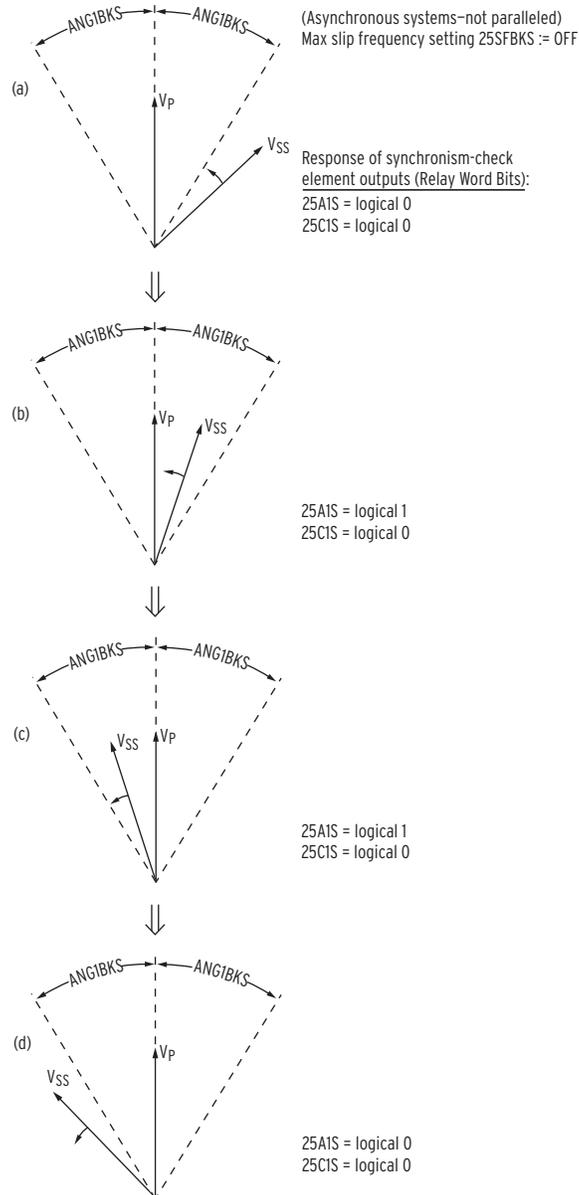
Figure 5.103   "Slip–No Compensation" Synchronism-Check Element Output Response

Positive Slip Frequency

If the slip frequency is positive, V_{SS} is slipping ahead of reference V_P (the system corresponding to V_{SS} has a higher system frequency than the system corresponding to V_P; $f_{SS} > f_P$). Positive slip frequency is the counter-clockwise rotation of V_{SS} with respect to reference V_P, as shown in *Figure 5.103*. Relay Word bit FASTS asserts to logical 1 (and Relay Word bit SLOWS deasserts to logical 0) to indicate this condition.

Negative-Slip Frequency

If the slip frequency is negative, V_{SS} is slipping behind reference V_P (the system corresponding to V_{SS} has a lower system frequency than the system corresponding to V_P; $f_{SS} < f_P$). For such a case, V_{SS} rotates clockwise with respect to reference V_P. Relay Word bit SLOWS asserts to logical 1 (and Relay Word bit FASTS deasserts to logical 0) to indicate this condition.

"No-Slip" Condition

If the absolute value of the slip is less than 0.005 Hz ($|f_{SS}-f_P| < 0.005$ Hz; a "no-slip" condition), both Relay Word bits FASTS and SLOWS deassert to logical 0 and Relay Word bit SFZBKS asserts to logical 1. A "no-slip" condition is confirmed when FASTS and SLOWS are deasserted and SFZBKS is asserted.

Synchronism-Check Element Output Effects

Compare the corresponding "slip—no compensation" cases in *Figure 5.103* to the previous "no-slip" cases in *Figure 5.102*.

With setting 25SFBKS := OFF, the relay does not compensate for the further angular travel of V_{SS} (with respect to reference V_P) during the Circuit Breaker BKS close time setting TCLSBKS. The relay measures the phase angle directly with no compensation between reference V_P and V_{SS} for synchronism-check element output 25WC1S. SFKBS will be deasserted when 25SFBKS := OFF, forcing 25C1S to logical 0.

The relay always measures the phase angle directly (without compensation) between reference V_P and V_{SS} for element output 25A1S. Setting 25SFBKS, time setting TCLSBKS, and whether system conditions are "no-slip" (*Figure 5.102*) have no effect on element output 25A1S.

"Slip—With Compensation" Synchronism Check

Figure 5.104 is derived from *Figure 5.103*, but with the maximum slip frequency setting 25SFBKS set to some value other than OFF; thus, the relay compensates for circuit breaker closing time with setting TCLSBKS. This results in a compensated normalized synchronism-check voltage source V'_{SS}.
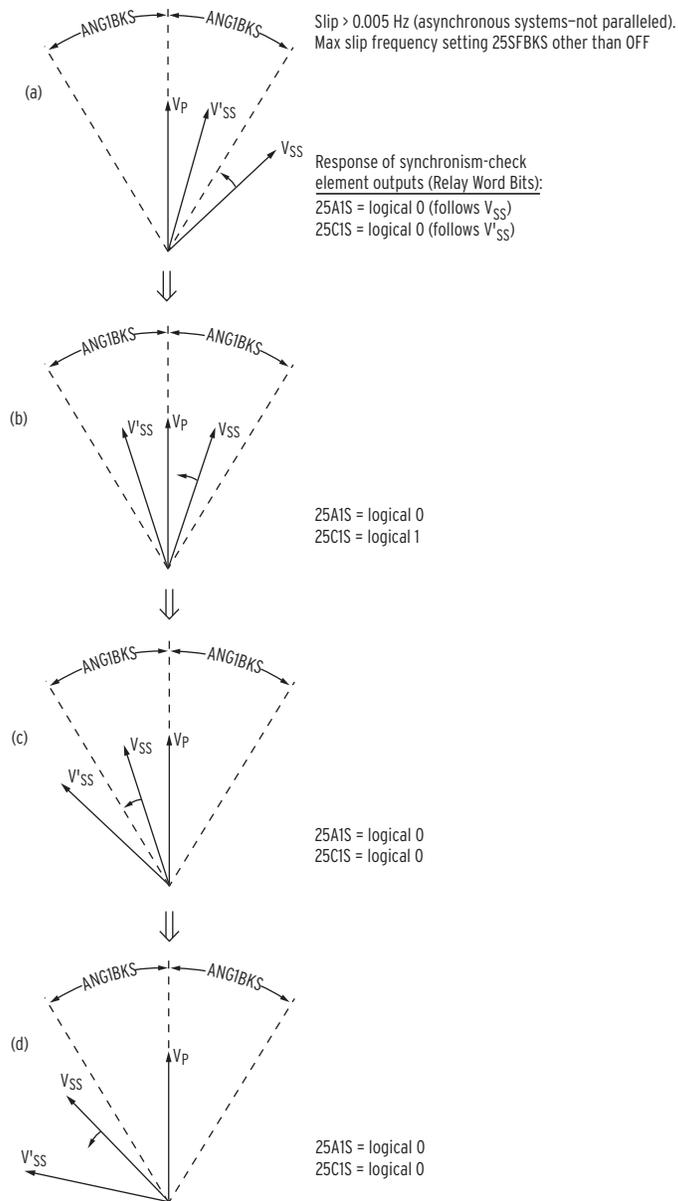
Figure 5.104   "Slip—With Compensation" Synchronism-Check Element Output Response

NOTE: If the relay is using a remote data acquisition system, such as TiDL, the operating times will be delayed by 1.5 ms. Use caution when setting the relay for synchronism check to account for this added delay.

Element 25C1S follows V'$_{SS}$. With setting 25SFBKS (maximum slip frequency) set to other than OFF, the relay calculates V'$_{SS}$ derived from V$_{SS}$. Phasor V'$_{SS}$ leads V$_{SS}$ by an angle described by *Equation 5.33*.

$$\text{angle} \ = \ \frac{(f_{SS} - f_P)\text{slip cycle}}{s \bullet \dfrac{60 \text{ cyc}}{s}} \bullet \frac{360°}{\text{slip cycle}} \bullet \text{TCLSBKS (cyc)}$$

Equation 5.33

From *Equation 5.33*, note that the angle between V$_{SS}$ and V'$_{SS}$ increases for a greater slip between V$_{SS}$ and V$_P$ (f$_{SS}$–f$_P$), a greater Circuit Breaker BKS close time setting TCLSBKS, or both in combination. For any case [*(a)*, *(b)*, *(c)*, or *(d)*] in *Figure 5.104*, the location of V'$_{SS}$ is the location of V$_{SS}$ a period later (this period is setting TCLSBKS, Circuit Breaker BKS Close Time). Consider, for example, issuing a close command to Circuit Breaker BKS. If case *(b)* in

Figure 5.104 represents the time at which the close command occurs, then V_{SS} is the normalized synchronism-check voltage source position at the instant the close is issued and V'_{SS} is the position of V_{SS} when Circuit Breaker BKS actually closes.

Slip Frequency

If the slip frequency exceeds setting 25SFBKS, synchronism check stops because element 25C1S deasserts to logical 0 for an out-of-range slip frequency condition, regardless of other synchronism-check conditions such as healthy voltage magnitudes.

Synchronism-Check Element Output Effects

A contradiction seems to result from analysis of case *(a)* in *Figure 5.104*; it appears that element output 25C1S should assert to logical 1 because V'_{SS} is within angle setting ANG1BKS. Note in this case, however, that V'_{SS} is approaching synchronism-check reference V_P. This is where element output 25C1S behaves differently than element output 25A1S, for setting 25SFBKS set to some value other than OFF. As V'_{SS} approaches V_P, 25C1S remains deasserted (equals logical 0) until the phase angle difference between reference V_P and V'_{SS} equals zero degrees.

At this zero degrees difference between V_P and V'_{SS}, element output 25CS1 asserts to logical 1. We know the systems will truly be in synchronism (0 degrees between reference V_P and V_{SS}) a period later (this period is setting TCLSBKS, Circuit Breaker BKS Close Time). Thus, if a close command occurs right at the instant that element output 25C1S asserts to logical 1, then there will be a zero-degree phase angle difference across Circuit Breaker BKS when Circuit Breaker BKS actually closes. Closing Circuit Breaker BKS at a phase angle difference of 0 degrees between reference V_P and V'_{SS} minimizes system shock when you bring two asynchronous systems together.

Element output 25C1S remains asserted to logical 1 as V'_{SS} moves away from reference V_P. When the phase angle difference between reference V_P and V'_{SS} is again greater than an angle setting ANG1BKS, element output 25C1S deasserts to logical 0.

When the slip frequency is greater than 0.005 Hz and 25SFBKS is set to other than OFF, element output 25A1S remains deasserted.

Alternative Synchronism-Check Source ALTS*m* Settings

You can program alternative input sources for the synchronism-check function in the SEL-487E. Alternative inputs give you additional flexibility to synchronize other portions of your power system.

The SELOGIC control equation ALTS*m* determines when the relay uses alternate Synchronism-Check Voltage Source *m* in place of regular Synchronism-Check Voltage Source *m*. When ALTS*m* is logical 1, the relay substitutes alternative Synchronism-Check Voltage Source *m* (ASYNCS*m*) and corresponding settings AKS*m*M and AKS*m*A for the regular Synchronism-Check Voltage Source *m* values SYNCS*m*, KS*m*M, and KS*m*A. The result is a normalized synchronism-check voltage source V_{Sm} derived from the alternative source.

Example 5.8   Setting Alternative Synchronism-Check Source T

Figure 5.105 shows an extra circuit breaker (BKU) and a generator position added to the existing example system of *Figure 5.90*. You can monitor the voltage at the generator position by connecting a single-phase voltage to remaining voltage input VCZ (see *Figure 5.93*). Make setting ASYNCST := VCZ to designate this relay voltage input as the alternate synchronism-check voltage source.

> ASYNCST := **VCZ** Alternative Synchronism Source T (VAV, VBV, VCV, VAZ, VBZ, VCZ)

For this new synchronism source voltage connection, adjust the source-to-reference magnitude ratio with setting AKSTM and the source-to-reference angle compensation with setting AKSTA, considering the settings for Voltage Magnitude and Angle Compensation.

Synchronism-Check Voltage Source T
SYNCST − designate voltage input
KSTM − adjust magnitude to reference
KSTA − adjust angle to reference

Bus S

BKS   BKT   BKU

Bus T

Switch

Line

Generator

Alternative Synchronism-Check Voltage Source T
ASYNCST − designate voltage input
AKSTM − adjust magnitude to reference
AKSTA − adjust angle to reference
ALTST − enable alternative source T
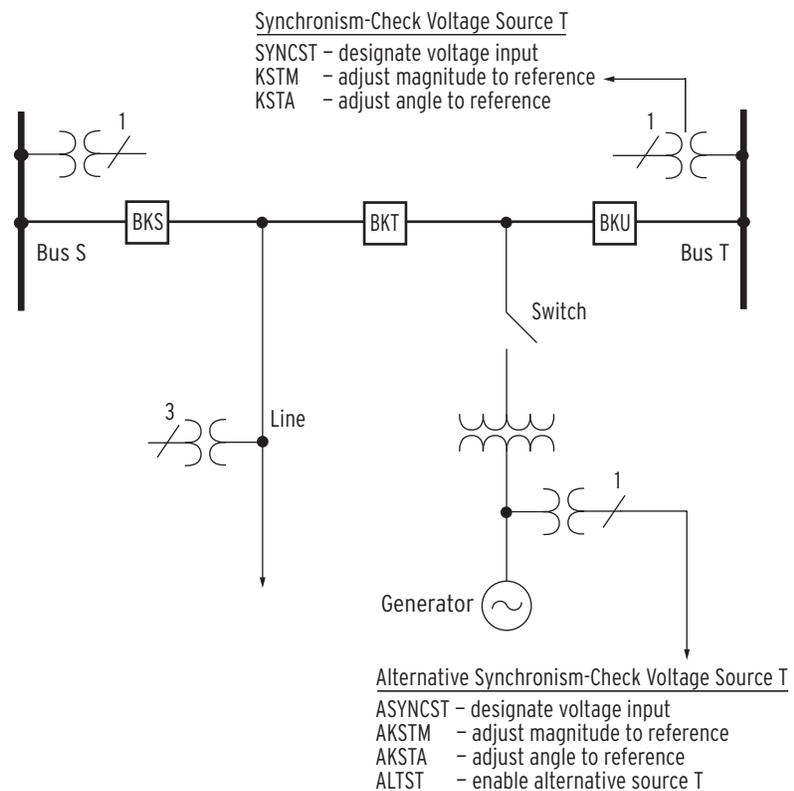
Figure 5.105   Alternative Synchronism-Check Source T Example and Settings

For example, in *Figure 5.105*, the Bus T voltage is the preferred Synchronism-Check Voltage Source T for synchronism check across Circuit Breaker BKT. However, if Circuit Breaker BKU is open and the generator switch is closed, the preferred Synchronism-Check Voltage Source T transfers to the Alternative Synchronism-Check Voltage Source T the voltage from the generator position.

Example 5.8   Setting Alternative Synchronism-Check Source T (Continued)

For circuit breaker status, make the following 52A auxiliary contact connections from the circuit breaker and switch to control inputs on the SEL-487E:

➤ Circuit Breaker BKU to IN203

➤ Generator switch to IN202

These input connections are for this application example only; use relay inputs that are appropriate for your system.

Set the ALTST SELOGIC control equation to assert when Circuit Breaker BKT is open and the generator switch is closed.

ALTST := **IN202 AND NOT IN203**   Alternative Synchronism Source T
    (SELOGIC equation)

Independent Synchronism-Check Polarizing Voltage Selection Settings

You can program independent and alternative polarizing voltages for each available breaker synchronism-check element via the enable independent synchronism check setting, EISYNC.

Setting EISYNC := Y enables dynamic reconfiguration of the polarizing sources based on changes in substation topology. With EISYNC := Y, each breaker has its own unique polarizing voltage with two alternate polarizing sources. See *Example 5.9* for a description of a practical application that uses these settings. When EISYNC := N, breakers use the same polarizing voltage (VP), and there are no alternate polarizing sources available, as described earlier in this section.

The user-programmable ALTPm1 and ALTPm2 logic settings are available while EISYNC := Y, and when combined, they determine the active polarizing voltage for breaker m (m = S, T, U, W, or X), as shown in *Figure 5.106*. The impact of the logic is then summarized in *Table 5.16*.
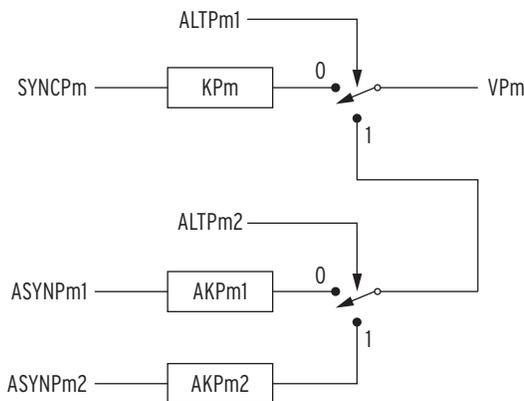
Figure 5.106   Alternate Synchronism-Check Polarizing Voltage Selection Logic

Table 5.16 shows that when ALTPm1 := 0, the status of ALTPm2 does not impact the selected polarizing voltage.

Table 5.16   Active Polarizing Voltage

ALTP*m*1	ALTP*m*2	Polarizing Voltage for Breaker *m*
0	0	SYNCP*m*
0	1	SYNCP*m*
1	0	ASYNP*m*1
1	1	ASYNP*m*2

Use the ALTP*m*1 and ALTP*m*2 settings to determine the alternate polarizing voltages and use the ALTS*m* setting to determine the alternate synchronizing voltage. See *Alternative Synchronism-Check Source ALTSm Settings on page 5.114* for additional information on alternative synchronizing voltages.

When compensating synchronism-check voltages, create an equivalent voltage base for secondary voltage magnitudes and account for any phase shifts between voltage inputs on a per-breaker basis. Typically, the polarizing voltage source of one of the breakers is used as the voltage and phase angle reference to which all other synchronism-check voltages are to be compensated. When configuring alternate sources for both polarizing and synchronizing quantities, the primary and alternate voltages need to be compensated to the same equivalent base.

Group settings KP*m*M and KP*m*A are provided when EISYNC := Y to compensate the magnitude and angle of the primary polarizing voltage input identified by the SYNCP*m* setting. The AKP*m*1M and AKP*m*1A settings compensate the magnitude and angle of the first alternate polarizing voltage input, as identified by the ASYNP*m*1 setting. The AKP*m*2M and AKP*m*2A settings compensate the magnitude and angle of the second alternate polarizing voltage input, as identified by the ASYNP*m*2 setting. These compensation settings are similar to KS*m*M and KS*m*A, which were previously discussed in *Alternative Synchronism-Check Source ALTSm Settings on page 5.114*,

The active polarizing voltage for Breaker *m* is compensated by the associated compensating factors and then assigned to the 25VP*m*FM and 25VP*m*FA analog quantities. The 25VP*m*FM quantity is compared to the synchronizing source voltage, 25VS*m*FM, and the voltage-difference setting, 25VDIF, to ensure an acceptable voltage difference between the polarizing and source voltages, as shown in *Figure 5.97*.

Whenever a synchronizing or polarizing voltage quantity changes through either the ALTS*m* or the ALTP*m*1 and ALTP*m*2 settings, the synchronism-check enable bit is reset, and there is a 6-cycle stability counter that must be satisfied prior to re-enabling the Breaker *m* synchronism-check logic (25ENBK*m* = 1). See *Figure 5.98*.

Example 5.9   Synchronism-Check Application/Settings Example (EISYNC = Y)

Figure 5.107 shows a line switch added to the existing example system of *Figure 5.105*.

The bus voltages are available to the relay unconditionally, and the line voltage measurement (VAV) is only available to the relay if the line disconnect switch, 89L1, is closed. Similarly, the generator voltage measurement (VBZ) is only available to the relay if the Line 2 disconnect switch, 89L2, is closed. Assume the normally open 89L1A and 89L2A contacts are mapped to relay digital inputs IN201 and IN202, respectively.

Example 5.9   Synchronism-Check Application/Settings Example (EISYNC = Y)

Consider the settings for the Breaker S synchronism-check element. The Bus S voltage (VAZ) acts as the synchronizing quantity for Breaker S, and no alternate value is needed. The synchronizing-voltage settings for Breaker S are SYNCSS := VAZ and ALTSS := NA.

VAV is the preferred polarizing quantity for Breaker S. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VBZ from the generator as a first alternate polarizing source for Breaker S. If disconnect switches 89L1 and 89L2 are both open, the relay uses the Bus T voltage (VCZ) as a second alternate polarizing source for Breaker S. The polarizing voltage settings for Breaker S are SYNCPS := VAV, ASYNPS1 := VBZ, ASYNPS2 := VCZ, ALTPS1 := NOT IN201, and ALTPS2 := NOT IN202.

Consider the settings for the Breaker T synchronism-check element. VAV is the preferred polarizing quantity for Breaker T. If disconnect switch 89L1 is open and this voltage is unavailable, the relay instead uses VAZ (from Bus S) as an alternate polarizing source for Breaker T. The polarizing voltage settings for Breaker T are SYNCPT := VAV, ASYNPT1 := VAZ, ALTPT1 := NOT IN201, ALTPT2 := NA.

VBZ is the preferred synchronizing quantity for Breaker T. If disconnect switch 89L2 is open and this voltage is unavailable, the relay instead uses VCZ (from Bus T) as an alternate synchronizing source for Breaker T. The synchronizing voltage settings for Breaker T are SYNCST := VBZ, ASYNCST := VCZ, and ALTST := NOT IN202.

As a final application note for EISYNC = Y, be sure to use the angle-correction factors to compensate for use of voltages from different phases (e.g., A, B, or C) and to compensate for differently connected potential transformers (e.g., delta or wye).

Example 5.9 Synchronism-Check Application/Settings Example (EISYNC = Y)

Breaker S		Breaker T	
Polarizing	Synchronizing	Polarizing	Synchronizing
SYNCPS := VAV	SYNCSS := VAZ	SYNCPT := VAV	SYNCST := VBZ
ASYNPS1 := VBZ	ALTSS := NA	ASYNPT1 := VAZ	ASYNCST := VCZ
ALTPS1 := NOT IN201		ALTPT1 := NOT IN201	ALTST := NOT IN202
ASYNPS2 := VCZ		ALTPT2 := NA	
ALTPS2 := NOT IN202			
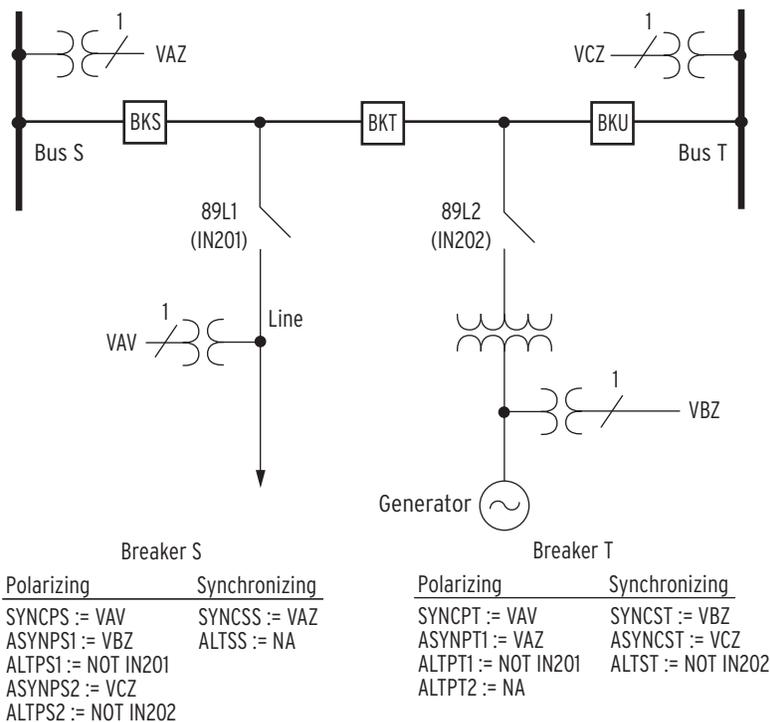
Figure 5.107 Alternate Synchronism-Check Polarizing Voltage Example System

Over- and Undervoltage Elements

The SEL-487E offers as many as five undervoltage and five overvoltage elements. Each of these 10 elements has two levels, for a total of 20 under- and overvoltage elements. *Figure 5.108* shows the undervoltage elements, and *Figure 5.109* shows the overvoltage elements.

Table 5.17 Fundamental or RMS Operating Quantities[a]

Parameter	Fundamental Quantities	RMS Quantities
Phase and Phase-to-Phase	VpkFM, VppFM, VNMINkF, VNMAXkF, VPMINkF, VPMAXkF	VpkRMS, VppRMS, VNMINkR, VNMAXkR, VPMINkR, VPMAXkR
Sequence	V1kM, 3V2kM[b], 3V0kM[b]	

[a] where:
  p = A, B, C
  pp = AB, BC, CA
  k = V, Z

[b] Not available for undervoltage elements.
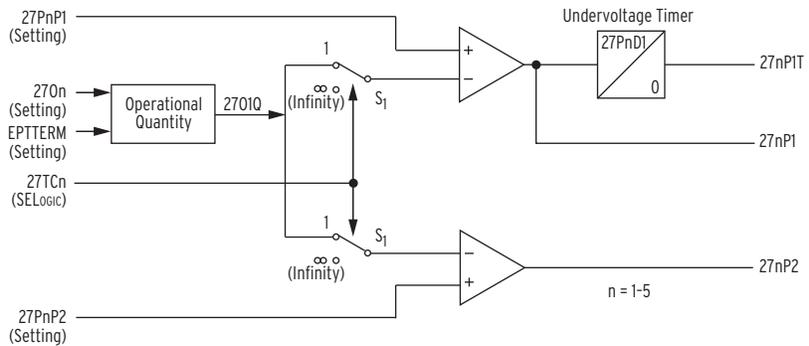
Figure 5.108   Undervoltage Elements

Although each under- and overvoltage element offers two levels, only Level 1 has a timer. If your application requires a time delay for the Level 2 elements, use a programmable timer to delay the output.
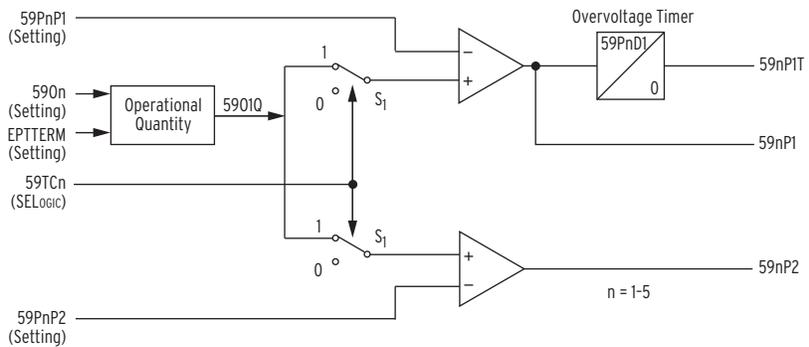
Figure 5.109   Overvoltage Elements

Select any one of the voltage elements from *Table 5.17* as an input quantity. You can select the same quantity for the undervoltage element as for an overvoltage element. Be sure that the PT terminal is enabled with the Group EPTTERM setting. For example, if EPTTERM = V, then only voltage values from the V potential transformer are available for selection.

Over- and Undervoltage Settings
E59 (Enable Overvoltage Elements)

Select the number of overvoltage elements (1–5) you require for your application. This setting is not available if EPTTERM = OFF.

E27 (Enable Undervoltage Elements)

Select the number of undervoltage elements (1–5) you require for your application. This setting is not available if EPTTERM = OFF.

270*n* (Undervoltage Element Operating Quantity)

Select the operating quantity you want for each voltage terminal from *Table 5.17*. Only voltage quantities from enabled voltage terminals are available.

27P*n*P1 (Undervoltage Level 1 Pickup)

Set pickup values for the voltage values below which you want the Level 1 undervoltage elements to assert.

The SEL-487E voltage inputs are available as 300 Vac maximum inputs or as LEA inputs. All the relay settings are on the 300 Vac base.

If LEA inputs are ordered, the voltage element pickup values must be adjusted prior to making the settings (see *Potential Transformer (PT) Ratio Settings With LEA Inputs on page 5.2*).

27P*n*P2 (Undervoltage Level 2 Pickup)

Set pickup values for the voltage values below which you want the Level 2 undervoltage elements to assert.

27TC (Undervoltage Torque Control)

Use the torque-control setting to specify conditions under which the undervoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

27P*n*D1 (Undervoltage Level 1 Time Delay)

When the system voltage falls below the undervoltage setting value, the undervoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 27P*n*D1 setting asserts the output.

590*n* (Overvoltage Element Operating Quantity)

Select from *Table 5.17* the operating quantity you want for each voltage terminal. Only voltage quantities from enabled voltage terminals (see *ECTTERM, EPT-TERM (CT and PT Terminal Enable) on page 5.24*) are available.

59P*n*P1 (Overvoltage Level 1 Pickup)

Set pickup values for the voltage values above which you want the Level 1 overvoltage elements to assert.

The SEL-487E voltage inputs are available as 300 Vac maximum inputs or as LEA inputs. All the relay settings are on the 300 Vac base.

If LEA inputs are ordered, the voltage element pickup values must be adjusted prior to making the settings (see *Potential Transformer (PT) Ratio Settings With LEA Inputs on page 5.2*).

59P*n*P2 (Overvoltage Level 2 Pickup)

Set pickup values for the voltage value above which you want the Level 2 overvoltage elements to assert.

59TC*n* (Overvoltage Torque Control)

Use the torque-control setting to specify conditions under which the overvoltage elements must be active. There is only one setting for both Level 1 and Level 2 elements. With the default setting equal to 1, both levels are active permanently.

59P*n*D1 (Overvoltage Level 1 Time Delay)

When the system voltage exceeds the overvoltage setting value, the overvoltage timer starts timing. Set the delay (in cycles) for which the timer must run before the 59P*n*D1 setting asserts the output.

Frequency Estimation

The relay uses filtered analog values related to the system frequency to calculate internal quantities such as phasor magnitudes and phase angles. When the system frequency changes, the relay measures these frequency changes and adapts the processing rate of the protection functions accordingly. Adapting the processing rate is called frequency tracking.

Note that frequency measurement is not the same as frequency tracking. The relay first measures the frequency and then tracks the frequency by changing the processing rate.

The relay measures the frequency over the 20–80 Hz range (protection frequency, see FREQP in *Table 5.19*), but only tracks the frequency over the 40–65 Hz range (see FREQ in *Table 5.19*). If the system frequency is outside the 40–65 Hz range, the relay does not track the frequency. Instead, it clamps the frequency to either limit. For frequencies below 40 Hz, the relay clamps the frequency at 40 Hz. For frequencies above 65 Hz, the relay clamps the frequency at 65 Hz.

To measure the frequency, the relay calculates the alpha component quantity and then estimates the frequency based on the zero-crossings of the alpha component. Relay Word bit FREQOK asserts when the relay measures the frequency over the range 20–80 Hz. If the frequency is below 40 Hz or above 65 Hz, FREQ reports the clamped values of either 40 Hz or 65 Hz. In this case, the relay no longer tracks the frequency. Instead, it uses either 40 Hz or 65 Hz to calculate the internal quantities.

If the frequency is in the 20–80 Hz range, but outside the 40–65 Hz range (for example, 70 Hz), FREQP shows the frequency the relay measures and FREQ shows the clamped frequency. In this case, FREQP = 70 Hz and FREQ = 65 Hz. *Table 5.18* summarizes the frequency measurement and frequency tracking ranges.

If the frequency is below 20 Hz or above 80 Hz, the relay no longer measures the frequency. Relay Word bit FREQFZ asserts and Relay Word bit FREQOK deasserts to indicate this condition. FREQ and FREQP are no longer valid, but they display the frequency at the time that the relay stopped measuring the frequency.

Table 5.18   Frequency Measurement and Frequency Tracking Ranges

Frequency Range (Hz)	Measures Frequency	Tracks Frequency	FREQOK	FREQFZ
40–65	Y	Y	1	0
20–39.99	Y	N	1	0
65.01–80	Y	N	1	0
Below 20 or above 80	N	N	0	1

The relay has six voltage inputs (VAV, VBV, VCV, VAZ, VBZ, and VCZ) that can be used as sources for estimating the frequency. Assign any of the six voltage inputs to VF01, VF02, and VF03. Note that assigning **ZERO** will set that input to zero. The relay also provides an alternate frequency source selection where you can assign any of the six voltage inputs to VF11, VF12, and VF13. The relay uses VF01, VF02, and VF03 as sources if the SELOGIC evaluation of EAFSRC is 0. The relay uses VF11, VF12, and VF13 as sources if EAFSRC is 1. The relay calculates the alpha quantity, Valpha, as shown in *Figure 5.110* using the mapped sources. Note that the alpha quantity is based on the instantaneous secondary voltage samples from the mapped resources and is an instantaneous quantity.
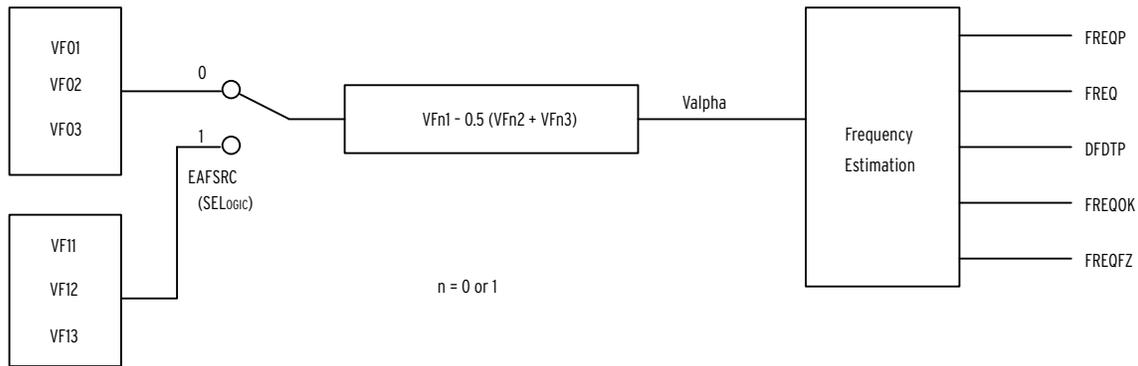
Figure 5.110   SEL-487E Alpha Quantity Calculation

Table 5.19   Frequency Estimation Outputs

Name	Description	Type
FREQ	Measured system frequency (Hz) (40–65 Hz)	Analog Quantity
FREQP	Measured frequency (Hz) (20–80 Hz)	Analog Quantity
FREQOK	Measured frequency is valid	Relay Word bit
FREQFZ	Measured frequency is frozen	Relay Word bit

Undervoltage Supervision Logic

Relay Word bit 27B81, the output of the logic in *Figure 5.111*, supervises the frequency elements for system undervoltage conditions. In the logic, the comparator compares the absolute value of the alpha component voltage (Valpha) against the 81UVSP setting value. *Equation 5.34* shows the equation for calculating Valpha.

$$\text{Valpha} = \text{VF01} - \left[\frac{\text{VF02}}{2} + \frac{\text{VF03}}{2} \right]$$

Equation 5.34

Generally, settings VF01, VF02, VF03 correlate to VA, VB, and VC.

Equation 5.35 shows the relationship between the peak amplitude of Valpha and the rms value of the system voltage phasors for three-phase voltage inputs.

$$\text{Valpha} = \sqrt{2} \bullet 1.5 \bullet \text{Vrms}$$

Equation 5.35

where Vrms is the root-mean-square value of the voltage phasor.

Relay Word bit 27B81 asserts if Valpha falls below the 81UVSP setting value for longer than a cycle.
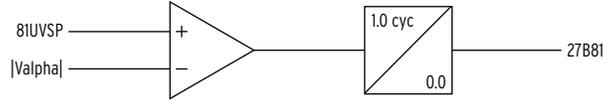
Figure 5.111   Undervoltage Supervision Logic

Calculate the 81UVSP Setting Value

Because the relay accepts voltage input from the potential transformers (PTs) in any combination, Valpha can have different values, depending on the voltage inputs. In general, the following examples use the average (60 percent) of the 50–70 percent undervoltage range that the IEEE C37.117 Guide recommends. Also, the calculations are based on an rms phase-to-neutral value of 67 V for the PT inputs, although the 81UVSP setting is a peak value and not an rms value.

Case 1: Three-Phase PT Inputs

In this case, VF01 = VA, VF02 = VB, and VF03 = VC (with default settings). Use *Equation 5.35* to calculate the nominal value of Valpha as follows:

$$\text{Valpha} = \sqrt{2} \bullet 1.5 \bullet 67 \text{ V}$$

Equation 5.36

$$\text{Valpha} = 142.13 \text{ V}$$

Equation 5.37

Set 81UVSP to 60 percent of this value:

$$\text{81UVSP} = 0.6 \bullet 142.13 \text{ V}$$

Equation 5.38

$$\text{81UVSP} = 85.28 \text{ V}$$

Equation 5.39

Case 2: Single-Phase PT Input, Connected to the A-Phase Input

In this case, VF01 = VA, VF02 = ZERO, and VF03 = ZERO.

$$\text{Valpha} = \sqrt{2} \bullet 67 \text{ V}$$

Equation 5.40

$$\text{Valpha} = 94.75 \text{ V}$$

Equation 5.41

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \bullet 94.75 \text{ V}$$

<div align="right">**Equation 5.42**</div>

$$81UVSP = 56.85 \text{ V}$$

<div align="right">**Equation 5.43**</div>

Case 3: Single-Phase PT Input, Connected to the B- or C-Phase Input

In this case, VF01 = ZERO, VF02 = VB, and VF03 = ZERO.

$$Valpha = \sqrt{2} \bullet \frac{67}{2} \text{V}$$

<div align="right">**Equation 5.44**</div>

$$Valpha = 47.37 \text{ V}$$

<div align="right">**Equation 5.45**</div>

Set 81UVSP to 60 percent of this value:

$$81UVSP = 0.6 \bullet 47.37 \text{ V}$$

<div align="right">**Equation 5.46**</div>

$$81UVSP = 28.43 \text{ V}$$

<div align="right">**Equation 5.47**</div>

Table 5.20 summarizes the results of the three cases.

Table 5.20   Summary of the Valpha and 81UVSP Calculations

Case	PT Connections	VA	VB	VC	Valpha	0.6 • Valpha
Case 1	Three-phase	$67 \angle 0°$	$67 \angle -120°$	$67 \angle 120°$	142.13	85.28
Case 2	Single-phase, VA	$67 \angle 0°$	0	0	94.75	56.85
Case 3	Single-phase, VB/VC	0	$67 \angle -120°$	0	47.38	28.43

Over- and Underfrequency Elements

Use the relay frequency elements for such abnormal frequency protection as underfrequency load shedding.

Figure 5.112 shows the logic for the six levels of over- and underfrequency elements in the relay.

Each frequency element can operate as an overfrequency or as an underfrequency element, depending on its pickup setting. If the element pickup setting (81DnP, $n = 1$–6) is less than the nominal system frequency setting, NFREQ, the element operates as an underfrequency element, picking up if measured frequency is less than the set point. If the pickup setting is greater than NFREQ, the element operates as an overfrequency element, picking up if measured frequency is greater than the set point.
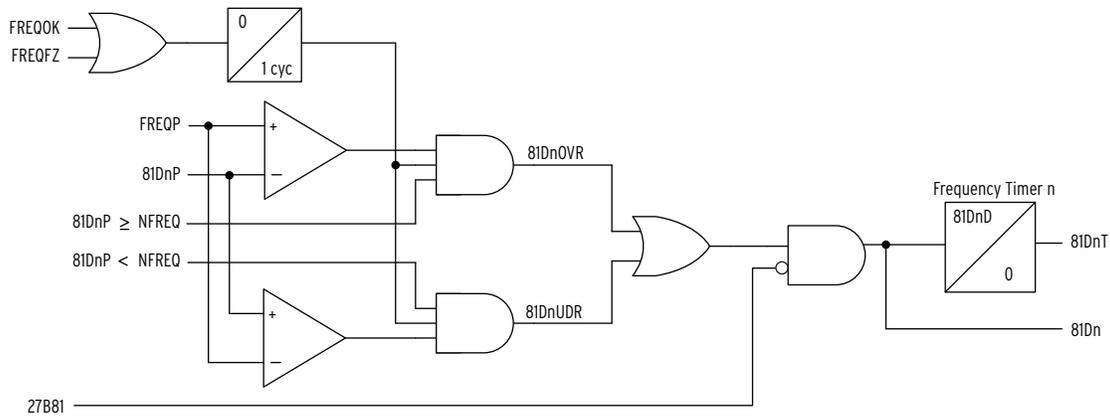
Figure 5.112   Frequency Element Logic

Note that Relay Word bit 27B81 controls all six frequency elements. This under-voltage supervision control prevents erroneous frequency element operations during system faults.

Over- and Underfrequency Element Settings
E81 (Enable 81 Elements)

Set E81 to enable as many as six over- and underfrequency elements. When E81 = N, the relay disables the frequency elements and hides corresponding settings; you do not need to enter these hidden settings.

81UVSP (81 Element Undervoltage Supervision)

This setting applies to all six frequency elements. If the instantaneous alpha voltage falls below the 81UVSP setting, all frequency elements are disabled.

81D*n*P (Level *n* Pickup)

Set the value at which you want the frequency element for each of six levels to assert. For a value of 81D*n*P less than the nominal system frequency NFREQ (50 or 60 Hz), the element operates as an underfrequency element. For a value greater than NFREQ, the element operates as an overfrequency element. Note that *n* can be one of six levels, 1–6.

81D*n*D (Level *n* Time Delay)

Select a time in seconds that you want frequency elements to wait before asserting.

IEC Thermal Elements

Thermal Element

The relay implements three independent thermal elements that conform to the IEC 60255-149 standard. Use these elements to activate a control action or issue an alarm or trip when your equipment overheats as a result of adverse operating conditions.

The relay computes the instantaneous thermal level, H, of the equipment. The thermal level is a ratio between the estimated actual temperature of the equipment and the steady-state temperature of the equipment when the equipment is operating at a maximum current value.

The relay computes the accumulated thermal level by using the following equations:

If IEQ ≥ IEQPU

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONH}{TCONH + \Delta t} \right) + \left(\frac{IEQ_t}{IMC} \right)^2 \cdot \left(\frac{\Delta t}{TCONH + \Delta t} \right) \cdot FAMB$$

Equation 5.48

If IEQ < IEQPU

$$THRL_t = THRL_{t-1} \cdot \left(\frac{TCONC}{TCONC + \Delta t} \right)$$

Equation 5.49

where:

THRL$_t$ =	The accumulated thermal level at time t
THRL$_{t-1}$ =	The accumulated thermal level from the previous processing interval
Δt =	The processing interval for the element, which is once every power system cycle (i.e., 50 or 60 Hz)
IEQ =	The equivalent heating current at time t, given in per unit
IEQPU =	The equivalent heating current pick up threshold, given in per unit
IMC =	The maximum continuous current, given in per unit
TCONH =	User-selectable equipment hot time constant that models the thermal characteristics of the equipment when it is energized. The setting is entered in minutes. The setting is converted to cycles before it is used in *Equation 5.49*.
TCONC =	User-selectable equipment cold time constant that models the thermal characteristics of the equipment when it is de-energized. The setting is entered in minutes. The setting is converted to cycles before it is used in *Equation 5.49*.
FAMB =	The ambient temperature factor

The relay calculates the equivalent heating current, IEQ, according to the following:

$$IEQ = \frac{THRO}{INOM}$$

Equation 5.50

where:

THRO = User-selectable thermal model operating current

INOM = Nominal current rating of the input associated with THRO operating current (i.e., 1 or 5 A). For combination terminals (ST, TU, UW, or WX), the INOM of the terminal with the greatest CT ratio is used.

Additionally, the relay calculates the maximum continuous current (IMC), according to the following:

$$IMC = KCONS \cdot IBAS$$

Equation 5.51

where:

KCONS = User-selectable basic current correction factor

IBAS = User-selectable basic current values in per unit

NOTE: FAMB freezes on the last calculated value if the relay loses RTD connectivity (MAMB_OK = 0).

Lastly, the relay computes the ambient temperature factor, FAMB, according to the following:

$$FAMB = \frac{TMAX - 40°C}{TMAX - MAMBT}$$

Equation 5.52

where:

TMAX = User-selectable maximum operating temperature of the equipment

MAMBT = Ambient temperature measurement from the user-selectable temperature probe

Thermal Element Logic

Figure 5.113 shows the thermal alarming and tripping logic for each of the three thermal elements (*n* = 1, 2, and 3).
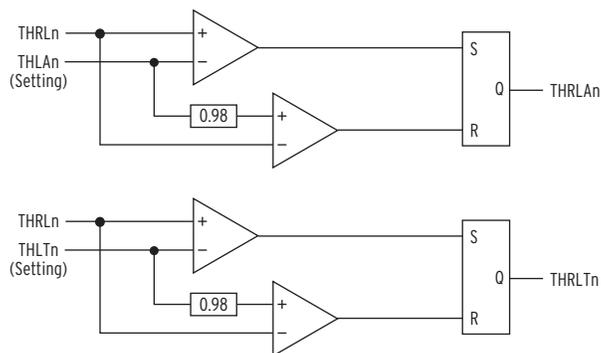
Figure 5.113   Thermal Alarming and Tripping Logic

When considering settings levels for the thermal elements alarming and tripping functions, note from *Equation 5.53* that the relay calculates the instantaneous thermal level, H, as follows:

$$H = \left(\frac{IEQ_t}{IMC}\right)^2 \cdot FAMB$$

Equation 5.53

From this equation, the per-unit thermal level the relay computes depends on the per-unit current flowing through the equipment (IEQ) and the KCONS and IBAS settings (these two settings make up the IMC value). Given this information, one can set the thermal level alarm and tripping thresholds when considering the various operating current levels and temperature the equipment will be subjected to.

If the instantaneous thermal level H is greater than the thermal level trip limit (THLT*n*) and the accumulated tripping element has not yet asserted (THRLT*n*), the relay calculates the remaining time before the thermal element trips, as shown in *Equation 5.54*. The relay also calculates how much of the thermal capacity of the equipment is currently being used, as shown in *Equation 5.55*.

$$THTRIP n = TCONH n \bullet \ln\left(\frac{H n - THRL n}{H n - \left(\frac{THLT n}{100}\right)}\right)$$

Equation 5.54

$$THTCU n = 100 \bullet \left(\frac{THRL n}{\left(\frac{THLT n}{100}\right)}\right)$$

Equation 5.55

Thermal levels (THRL*n*), thermal element remaining time before trip (THTRIP*n*), and thermal element capacity used (THTCU*n*) are all available as analog quantities. Additionally, the three thermal level alarming RWBs, (THRLA*n*), as well as the three thermal level tripping RWBs, THRLT*n*, are available.

Settings Description
Enable IEC Thermal Element (ETHRIEC)

Enable 1, 2, or 3 independent thermal elements.

Label	Prompt	Range	Default
ETHRIEC	Enable IEC Thermal (N, 1–3)	N, 1–3	N

Thermal Model Operating Quantity (THROn)

The thermal model must use a current that includes all of the additional heating effects of the current passing through the equipment. For this reason, the operating current choices are the three individual phase RMS currents from a user-selectable terminal or the IMAXWR current, which is the maximum RMS current seen among the three phase currents.

Label	Prompt	Range	Default
THRO*n*[a]	Thermal Model *n* Operating Quantity	IA*m*RMS, IB*m*RMS, IC*m*RMS[b]	THRO1 = IASRMS THRO2 = IBSRMS THRO3 = ICSRMS

[a] *n* = 1-3.
[b] *m* = S, T, U, W, X, ST, TU, UW, or WX

Basic Current Value in Per Unit (IBASn)

This setting accounts for the specified limiting value of the current for which the relay is required not to operate at when considering steady-state conditions. The product of the Basic Current Value, IBAS*n* (*n* = 1–3), and the Basic Current Correction Factor, KCONS*n* (described below), is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
IBAS*n*[a]	Basic Current Value in PU *n* (0.1–3.0)	0.1–3	1.1

[a] *n* = 1-3.

Equivalent Heating Current Pickup Value in Per Unit (IEQPUn)

The equivalent heating current pickup value is used by the relay to switch between the hot and cold time constant thermal equations. This setting defines what the equipment considers to be insignificant operating current that results in negligible heating effects. Typically this value is very close to zero, corresponding to when the equipment is de-energized.

Label	Prompt	Range	Default
IEQPU*n*[a]	Eq. Heating Current PickUp Value in PU *n* (0.05–1)	0.05–1	0.05

[a] *n* = 1-3.

Basic Current Correction Factor (KCONSn)

This setting dictates the maximum continuous load current of the equipment. The product of the Basic Current Value, IBAS*n*, and the Basic Current Correction Factor, KCONS*n*, is the Maximum Continuous Current, IMC, used by the relay in computing the thermal level.

Label	Prompt	Range	Default
KCONS*n*[a]	Basic Current Correction Factor n (0.50-1.5)	0.05–1	1

[a] *n* = 1-3.

Heating Thermal Time Constant (TCONHn)

This setting defines the thermal characteristic of the equipment when the equipment is energized, that is when the current is above the IEQPU value.

Label	Prompt	Range	Default
TCONH*n*[a]	Heating Thermal Time Constant *n* (1–500 min)	1–500 min	60

[a] *n* = 1-3.

Cooling Thermal Time Constant (TCONCn)

This setting defines the thermal characteristic of the equipment when the equipment is de-energized, that is when the current is below the IEQPU value.

Label	Prompt	Range	Default
TCONCn[a]	Cooling Thermal Time Constant n (1-500 min)	1–500 min	60

[a] n = 1-3.

Thermal Level Alarm Limit (THLAn)

This setting specifies the per-unit thermal level when the relay will assert the thermal alarm Relay Word bit.

Label	Prompt	Range	Default
THLAn[a]	Thermal Level Alarm Limit n (1–100%)	1.0–100%	50

[a] n = 1-3.

Thermal Level Trip Limit (THLTn)

This setting specifies the per-unit thermal level when the relay will assert the thermal trip Relay Word bit.

Label	Prompt	Range	Default
THLTn[a]	Thermal Level Trip Limit n (1–100%)	1.0–100%	80

[a] n = 1-3.

Maximum Temperature of the Equipment (TMAXn)

This setting specifies the maximum operating temperature of the protected equipment. This setting is used to calculate FAMBn (see *Equation 5.52*).

Label	Prompt	Range	Default
TMAXn[a, b]	Maximum Temperature of the Equipment n (80°–300°C)	80°–300°C	155

[a] n = 1-3.
[b] Hide setting if AMB_M = NA.

Over- and Underpower Element

The SEL-487E offers 10 overpower elements and 10 underpower elements. Use Group setting E32 to enable the number of power elements you want. Typical applications of power elements are the following:

➤ Overpower and/or underpower protection/control

➤ Reverse power protection/control

➤ VAR control for capacitor banks

The SEL-487E uses the IEEE convention for power measurement, as *Figure 5.114* and *Figure 5.115* illustrate.
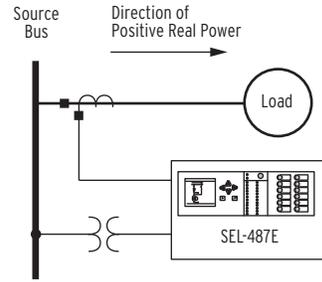
Figure 5.114   Primary Plant Connections
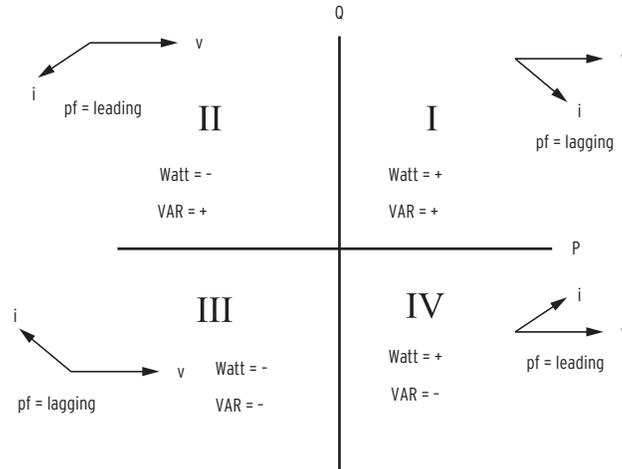
Figure 5.115   Complex Power Measurement Conventions

Figure 5.116 shows an installation with the direction of real power as indicated. CT S and CT T are the HV and LV CTs, connected in the conventional way to supply the differential elements with the correct polarity CT inputs. In this installation, be sure to specify operating quantities from CT S to comply with the IEEE convention.
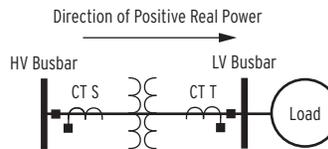
Figure 5.116   Selection of Operating Quantities

Input quantities for the 10 power elements are not fixed; make your selection from the three-phase power elements in *Table 5.21*. All analog quantities in *Table 5.21* are fundamental secondary values and include power quantities for single terminals as well as combined terminals.

Table 5.21   Power Element Operating Quantities (Secondary Values)

Analog Quantity	Description
3PmF[a]	Fundamental three-phase active power, Terminal m
3QmF	Fundamental three-phase reactive power, Terminal m
3PqpF[b]	Fundamental three-phase active power, combined Terminals qp
3QqpF	Fundamental three-phase reactive power, combined Terminals qp

[a] m = S, T, U, W, X.

[b] qp = ST, TU, UW, WX.

Figure 5.117 shows the logic for the overpower element, and *Figure 5.121* shows the logic for the underpower element. There are four conditions that must be met to enable both over- or underpower logic:

➤ ECTTERM and EPTTERM must not be set to OFF.

➤ Power calculations (EPCAL) must be enabled.

➤ Over- and underpower elements must be specified (E32).

➤ An operating quantity (32OPO*nn*) must be specified.

➤ SELOGIC control equation E32OP*nn* must be asserted.
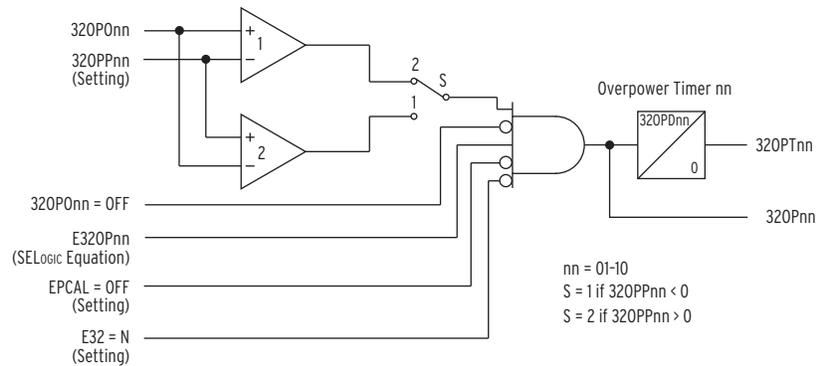
Figure 5.117 Overpower Element Logic

Input 32OPO*nn* is the power quantity (see *Table 5.21*) that the logic compares against the 32OPP*nn* setting. In general, the output of a comparator asserts to logical 1 when the (+) quantity exceeds the (–) quantity. Switch S selects the appropriate comparator as a function of the 32OPP*nn* setting. For example, if 32OPP*nn* < 0 (negative value), then Switch S is in position 1 and Comparator 2 is in use. In this case, the output of Comparator 2 asserts to logical 1 when the 32OPP*nn* setting value exceeds the 32OPO*nn* analog quantity.

Conversely, if 32OPP*nn* > 0 (positive value), then Switch S is in position 2, and Comparator 1 is in use. In this case, the output of Comparator 1 asserts to logical 1 when the 32OPO*nn* analog quantity exceeds the 32OPP*nn* setting value.

As an example, assume that you want to assert an output when the fundamental three-phase active power of Terminal S exceeds 54 VA secondary in the direction of the load flow. From *Table 5.21*, select 3PSF (fundamental three-phase active power) as the operating quantity. Using the first power element, set 32OPO01 = 3PSF. From *Figure 5.115*, the direction of the load flow is positive in the first and fourth quadrants. Therefore, set the threshold to a positive value (32OPP01 = +54). If you want to control the load in the reverse direction, then set 32OPP01 = –54. *Figure 5.118* shows a case where the control direction is towards the load, and *Figure 5.119* shows a case where the control direction is away from the load.
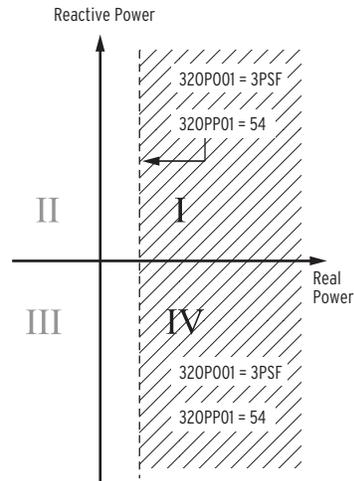
Figure 5.118   Load Flow Towards Load
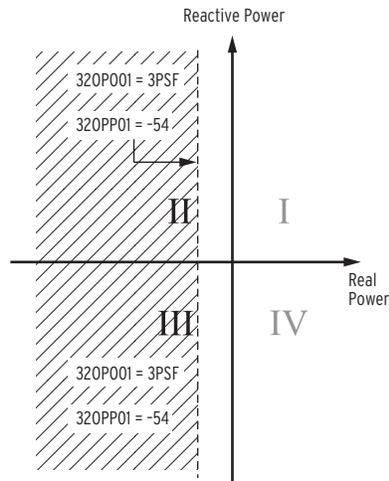
Figure 5.119   Reverse Load Flow

Use SELOGIC control equation E32OP*nn* to state the conditions when the power elements must be active. Output 32OP*nn* is the instantaneous output when the AND gate turns on, and 32OPT*nn* is the time-delayed output.

The sign of the pickup setting also determines the directional control for the reactive power element. In *Figure 5.120*, the top shaded area shows a case where the direction of the fundamental three-phase reactive power (3QPSF) is towards the load. The bottom shaded area shows a case where the flow is in the reverse direction.
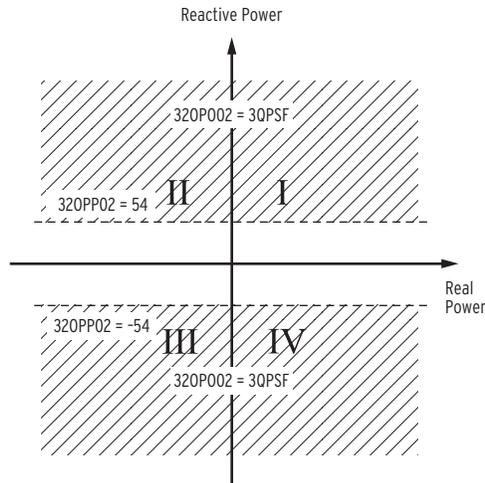
Figure 5.120   Reactive Power Characteristic

Figure 5.121 shows the logic for the underpower element. This element is the same as the overpower element.
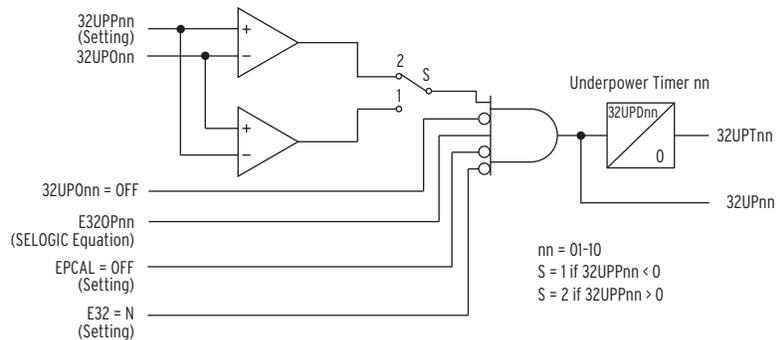
Figure 5.121   Underpower Element Logic

Over- and Underpower Element Settings
E32 (Enable Over/Underpower)

Set E32 to the number of power elements for the specific terminals in your application. The E32 setting considers for selection only terminals that you include in the ECTTERM and the EPCAL settings.

32OPO*gg* (Overpower Operating Quantities)

Select the analog quantity (see *Table 5.21*) for each of the enabled (E32 setting) power elements. The 32OPO*gg* setting considers for selection only terminals that you include in the ECTTERM setting and the EPCAL setting.

32OPP*gg* (Overpower Pickup)

The 32OPP*gg* setting is the overpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.114* and *Figure 5.115*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.119* and *Figure 5.120*). Analog quantities in *Table 5.21* are in secondary quantities, so you do not need any conversions.

32OPD*gg* (Overpower Delay)

For each enabled overpower element, select a time in cycles that you want the element(s) to wait before asserting.

E32OP*gg* (Torque Control)

Use the torque-control setting to specify conditions under which the overpower elements must be active. With the default setting of NA, the element is switched off.

32UPO*gg* (Underpower Operating Quantities)

Select the analog quantity (see *Table 5.21*) for each of the enabled (set in the E32 setting) power elements. The 32UPO*gg* setting considers for selection only terminals that you include in the ECTTERM setting and the EPCAL setting.

32UPP*gg* (Underpower Pickup)

The 32UPP*gg* setting is the underpower pickup and directional control setting for each of the enabled overpower elements in secondary VA. In general, a setting with a positive sign controls power in the direction of the load (see *Figure 5.114* and *Figure 5.115*), and a setting with a negative sign controls power in the reverse direction (see *Figure 5.119* and *Figure 5.120*). Analog quantities in *Table 5.21* are in secondary quantities, so you do not need any conversions.

32UPD*gg* (Underpower Delay)

For each enabled underpower element, select a time in cycles that you want the element(s) to wait before asserting.

E32UP*gg* (Torque Control)

Use the torque-control setting to specify conditions under which the underpower elements must be active. With the default setting of NA, the element is switched off.

Trip Logic

To provide settings for selective tripping between unit faults and system faults, the SEL-487E includes six trip logics. Use the logic in *Figure 5.122* for transformer (unit) faults and the logic in *Figure 5.123* (one for each of the five breakers) for system faults. Although you set the input quantities separately for each of the six logics, there exists only one Minimum Trip Duration timer and only one reset setting (RSTTRGT) for all the logics.

In *Figure 5.122*, the Transformer Trip timer starts when SELOGIC control equation TRXFMR asserts for one processing interval. Assertion of this equation immediately asserts Output TRPXFMR. Output TRPXFMR remains asserted for

the Minimum Trip Duration timer (TDURD) setting regardless of the status of Input TRXFMR. When Output TRPXFMR asserts, the logic seals TRPXFMR in through the AND gate under the following conditions:

➤ SELOGIC control equation RSTTRGT is deasserted (Global setting)

➤ The target reset (TRGTR) input is deasserted

➤ The unlatch input (ULTXFMR) is deasserted

➤ The ECTTERM setting includes the terminal name

Relay Word bit TRGTR asserts for one processing interval when either you press the front-panel **TARGET RESET** pushbutton or you issue the ASCII **TAR R** command.

Once latched, TRPXFMR remains asserted until any (or all) of the following happens:

➤ SELOGIC control equation RSTTRGT asserts

➤ The target reset (TRGTR) input asserts

➤ The unlatch input (ULTXFMR) asserts
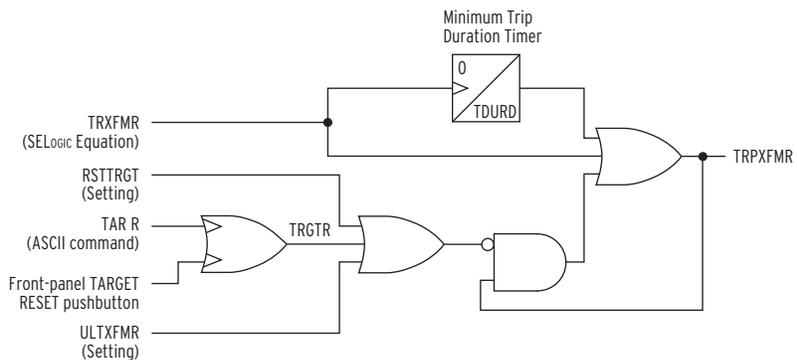
Figure 5.122   Transformer Trip Logic

Figure 5.123 shows the trip logic for each of the five circuit breakers. The logic itself is identical, but there are trip (TR*m*) and trip unlatch (ULTR*m*) equations for each of the five circuit breakers.
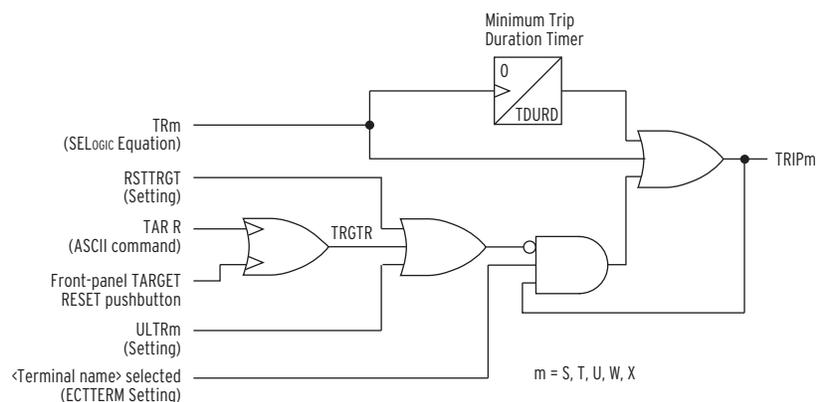
Figure 5.123   Circuit Breaker Trip Logic
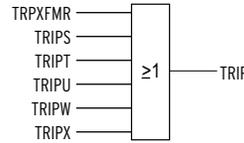
Figure 5.124   TRIP Logic

Trip-Logic Settings

TRXFMR (Trip Transformer)

Specify the conditions under which all the circuit breaker must trip with the TRXFMR setting. Default settings are the differential and restricted earth fault trip outputs.

ULTXFMR (Unlatch Trip Transformer)

Specify the conditions to unlatch the transformer trip output command (TRPXFMR). The default setting is Relay Word bit TRGTR.

TR*m* (Trip Terminal)

Specify the conditions under which each of the enabled circuit breakers must trip with the TR*m* setting. Default settings are the phase and negative-sequence overcurrent elements.

ULTR*m* (Unlatch Trip Terminal)

NOTE: Changing setting groups when the trip duration timer is running extends the duration by 3.5–4 cycles. The timer does not reset during this delay.

Specify the conditions to unlatch each of the enabled circuit breaker trip outputs with the ULTR*m* setting. The default setting is Relay Word bit TRGTR.

TDURD (Minimum Trip Duration Timer)

There is only one minimum trip duration timer for all five terminals. Set this delay (in cycles) slightly longer than the trip time of the slowest circuit breaker.

Close Logic

Figure 5.125 shows the close logic that removes the close command to the circuit breaker after a set time. If the ECTTERM setting includes the terminal name, and if the unlatch input SELOGIC control equation (ULCL*m*) is deasserted, the two bottom inputs of the AND gate are logical 1. When SELOGIC control equation CL*m* asserts, the AND gate turns on. When the gate turns on, the Close Failure timer asserts and seals itself in through the OR gate for a time equal to the CFD setting, or until ULCL*m* asserts. With the Close Failure timer sealed in, output CLS*m* is also sealed in for the CFD time setting.

The close failure timer is unaffected by a setting group change. The timer starts timing in the present setting group, continues to run for the intermediate time between setting groups, and completes timing in the new setting group.
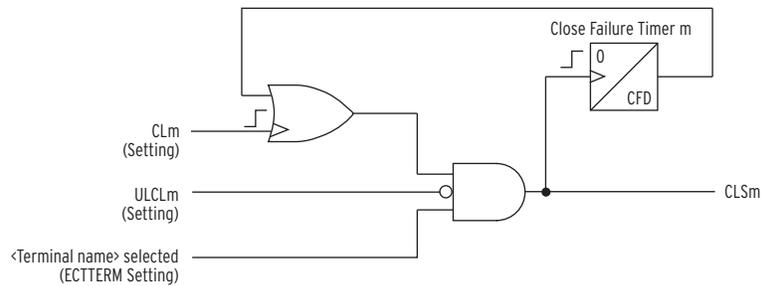
Figure 5.125 Close Logic for Breaker *m*

Close Logic Settings

CL*m* (Close SEL~OGIC~ Control Equation)

Specify the conditions under which the circuit breaker must close with the CL*m* setting. The default setting is local bit LB10, which controls close operations from the front panel. This settings category is hidden when ECTTERM = OFF.

ULCL*m* (Unlatch Close SEL~OGIC~ Control Equation)

Specify the conditions to unlatch the close output command (CLS*m*) and reset the close failure timer. The close output command and close failure timer will reset on the rising edge of the unlatch. Default settings are the 52A breaker auxiliary contacts that assert when the breakers close.

Loss-of-Potential (LOP) Logic

Directional elements are voltage-polarized, so loss of potential can cause the directional elements to misoperate. To prevent directional element misoperation, the LOP logic blocks the directional elements for a particular PT (V or Z) after detecting a blown PT fuse.

In general, the following three conditions cause a loss of potential:

➤ Incorrect operating procedures

➤ System faults

➤ Blown PT fuse(s)

Incorrect operating procedures include incidents such as energizing the relay without PT fuses after maintenance. Although the LOP logic alarms for this condition, the logic primarily detects the occurrence of blown PT fuses when the relay is in service.

To distinguish an LOP condition from a system fault condition, the LOP logic correlates the change in voltage with a change in current. Because a system fault causes a change in both voltage and current, the LOP logic compares the present values of the positive-sequence current and angle to the values of the positive-sequence current and angle of the previous cycle. In separate calculations, the LOP logic also compares the present values of the negative-sequence current to the value of the negative-sequence current of the previous cycle.

Figure 5.126 shows the logic that calculates the change in current for Terminal S; other terminals have similar logic. For each terminal included in the ECTTERM setting, the logic calculates the change in current, ImDELTA (m = S, T, U, W, X), for three possible conditions:

1. Change in positive-sequence current angle is greater than five degrees, provided that the present positive-sequence current magnitude and that of a cycle ago are greater than five percent of the nominal current (nominal current is 5 A or 1 A).

2. Change in positive-sequence current magnitude is greater than two percent of nominal current (5 A or 1 A).

3. Change in negative-sequence current magnitude is greater than six percent of nominal current (5 A or 1 A).

NOTE: The LOP logic only evaluates the change in current-for-current terminals included in the ECTTERM setting.

When any one of these three conditions is true, Relay Word bit ISDELTA asserts, causing Output IDELTA to assert. When IDELTA asserts, the IDELTA Timer maintains the output for 15 cycles. During these 15 cycles, AND Gate 2 (see *Figure 5.126*) cannot turn on, and an LOPV condition is not possible.
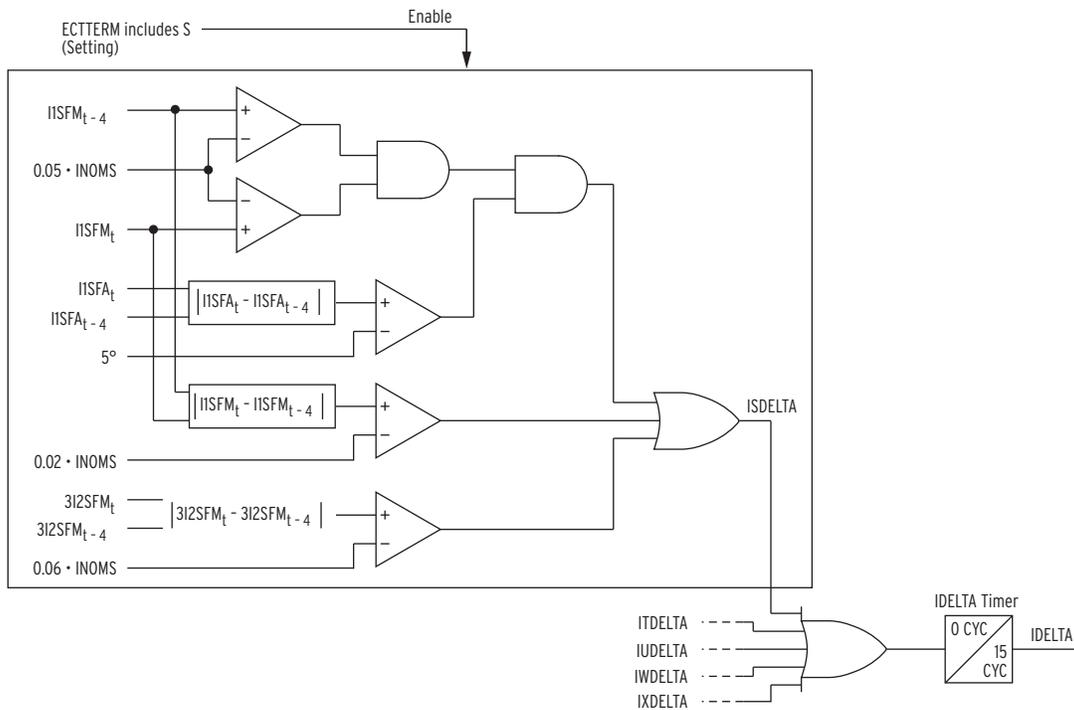
Figure 5.126   Logic that Calculates the Change in Current

Figure 5.127 shows the LOP logic for PT V; PT Z has similar logic. Whereas the delta current calculations determine the difference in current, the LOP logic calculates the ratio of the present voltage and the voltage one cycle earlier. AND Gate 1 turns on when the following three conditions are true:

➤ EPTTERM includes PT V.

➤ The ratio of the present voltage and the voltage one cycle earlier is below 0.9 (also turns AND Gate 3 off).

➤ The voltage from one cycle earlier is higher than 10 percent of the nominal voltage of PT V.
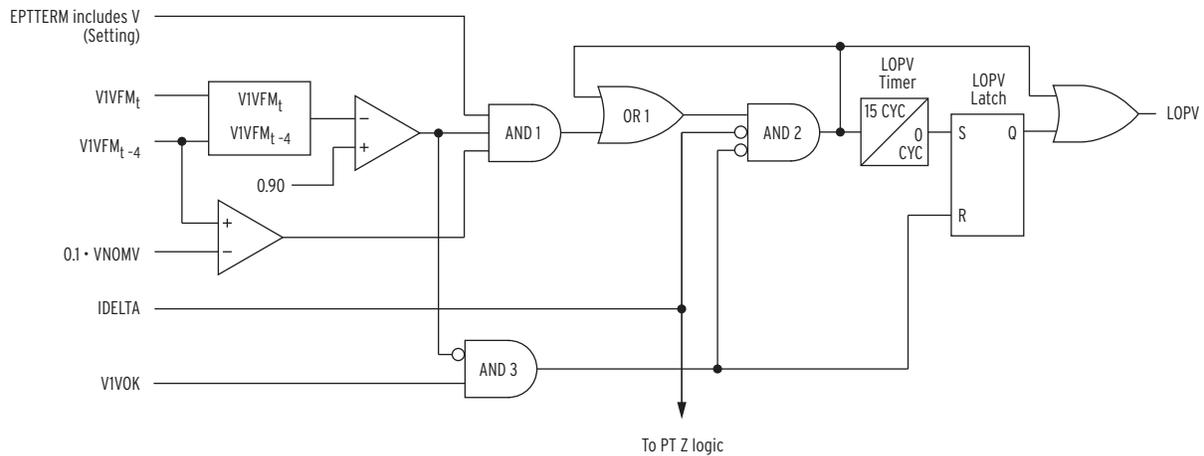
Figure 5.127   LOP Logic for Potential Transformer V

AND Gate 1 turns on when there is a drop in voltage greater than 10 percent in the positive-sequence voltage. If there is a simultaneous change in current (IDELTA asserts), then the drop is the result of a system fault, and AND Gate 2 does not turn on. However, if IDELTA does not assert, (no corresponding change in current), then the voltage drop is the result of a loss-of-potential condition. Therefore, as shown in *Figure 5.127*, the logic requires AND Gate 1 to assert, IDELTA to not assert, and the ratio of the present voltage and the one-cycle-earlier voltage to be below 0.9 (AND Gate 3 is off) in order for AND Gate 2 to assert. When AND Gate 2 asserts, the following takes place:

➤   AND Gate 2 seals itself in through OR Gate 1.

➤   Output LOPV asserts and blocks all directional elements that have PT V as reference voltage (VREF*m* settings).

➤   The 15-cycle LOPV Timer starts. If the LOP condition lasts for 15 cycles, then the LOPV Timer expires and asserts the LOPV Latch, which latches the LOPV output. The LOPV Latch resets only when AND Gate 3 turns on.

Figure 5.128 shows the logic for detecting an abnormal voltage condition when the transformer is energized, or when a particular winding picks up load. When the circuit breaker is open, the open-phase detection (OPH*m*) asserts. Closing the circuit breaker does not necessarily cause OPH*m* to deassert; OPH*m* deasserts only when current flows. On the falling edge of OPH*m*, the OPH Timer asserts LD (load detected) for 130 cycles, thus asserting the bottom input into AND Gate 1. If the positive-sequence voltage is greater than 75 percent and the negative-sequence voltage (3V2) is less than 60 percent, the logic declares the condition as a possible missing or blown fuse, and it starts the PT Timer. If the condition persists for 120 cycles, then the PT Timer expires and sets the PT Latch. This setting of the PT Latch then asserts Output VALARMV. When the positive-sequence voltage is greater than 85 percent of the nominal voltage, and the ratio of negative-sequence (3V2) voltage to positive-sequence voltage is below 30 percent, the output V1VOK asserts, and the PT Latch resets.
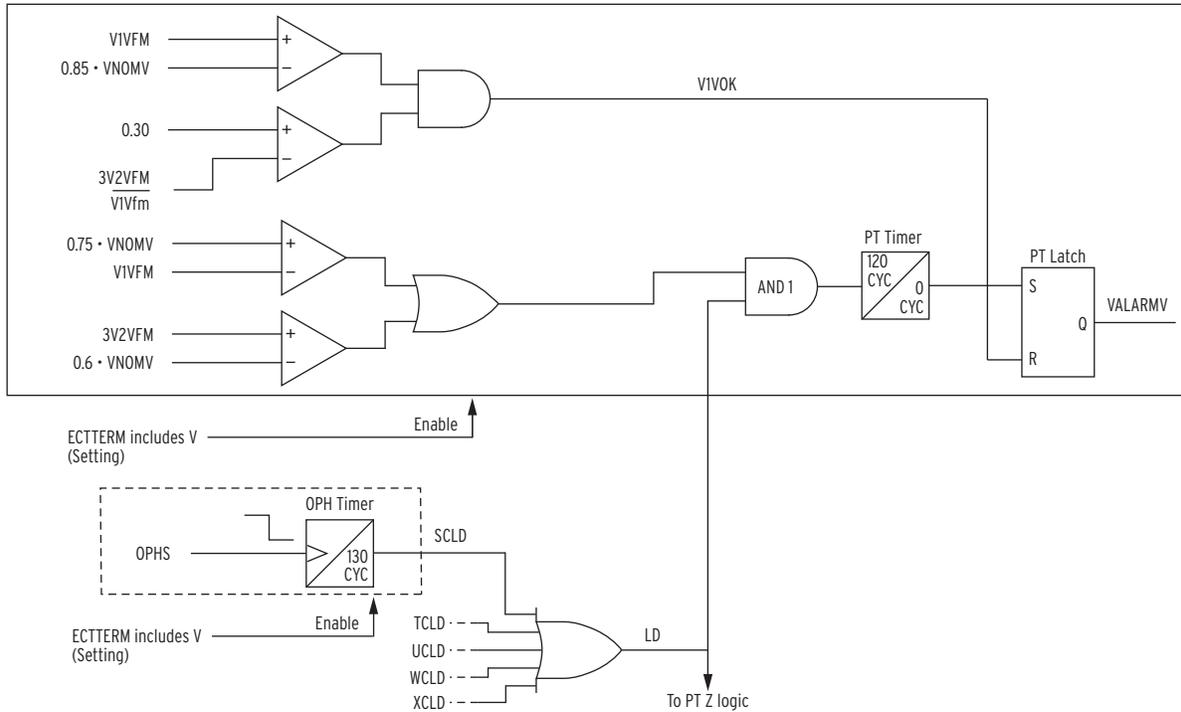
Figure 5.128   Logic to Detect Abnormal Voltage Condition

Circuit Breaker Status

Figure 5.129 shows the circuit breaker status logic, which uses the combination of breaker 52A (normally open) auxiliary contact and the open-phase detection function, OPHm (m = S, T, U, W, X). Because 52B (normally closed) contacts are not always available, and as a means to reduce the number of I/O required, the 52B contacts are not required in the logic. However, for applications where the protection philosophy requires a 52B (normally closed) contact, wire the 52B contact into the relay, but use the negated form of the 52B contact in the logic (i.e., NOT 52B (52A_m: = NOT IN101)).
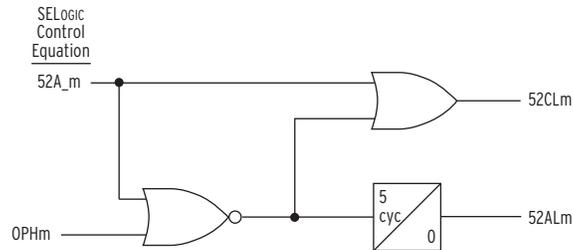
Figure 5.129   Circuit Breaker Status

Relay Word bits 52CLm assert when the breaker is closed. Open-phase detection logic (OPHm) Relay Word bits are included in the circuit breaker status logic to guard against delayed breaker status declaration resulting from possible breaker

auxiliary contact misalignment. If a discrepancy between the open-phase detection logic and the breaker auxiliary contact exists for as long as five cycles, the logic generates an alarm that indicates one of the following:

➤ Possible auxiliary contact supply voltage failure

➤ Possible failure in an auxiliary contact connection circuit

➤ Possible failure of auxiliary contact mechanism

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Protection Application Examples

This section provides instructions for setting the SEL-487E relay protection functions. Use these application examples to help familiarize yourself with the relay and assist you with your own protection settings calculations. This section is not intended to provide a complete settings guide for the relay.

Transformer Winding and CT Connection Compensation Settings Examples

NOTE: This section provides a procedure to determine and set the Terminal *m* CT connection compensation settings (T*m*CTC [where *m* = S, T, U, W, or X]).

NOTE: In this section, the term "phase rotation" is synonymous with "phase sequence". This section uses "phase rotation" to be consistent with the relay Global setting PHROT.

In electromechanical and solid-state transformer differential relays, the standard current transformer (CT) configuration is wye- connected on the delta winding of the transformer and delta connected on the wye winding of the transformer. The CT delta connection is constructed based on the power transformer delta to compensate for the phase shift that occurs on the system primary currents because of the power transformer connection. This CT configuration allows the currents entering the relay for through-load or external faults to be 180 degrees out-of-phase so that the phasor sum of the currents adds to zero (no differential current) in an electromechanical differential relay. Taps on the relay current inputs compensate for magnitude differences. Modern digital relays perform both the connection (or phase) and magnitude compensation mathematically so all CTs can be connected in wye.

The SEL-487E offers connection compensation settings, T*m*CTC, to compensate for the phase shift across the transformer. While it is not entirely accurate to refer to a phase shift across a transformer, it is a well-accepted term. Each of the connection compensation settings offer thirteen 3x3 matrices, CTC(0)–CTC(12), permitting CT connection compensation from 0 degrees to 360 degrees, in increments of 30 degrees, respectively. Refer to *Table 5.2* for each of the compensation matrices. When applied on a system with ABC phase rotation, these matrices perform phase angle correction in a counter-clockwise (CCW) direction in multiples of 30 degrees, as shown in *Table 6.1*. For systems with ACB phase rotation, the direction of correction is clockwise (CW). See *Special Cases on page 6.19* for compensation settings examples on a system with ACB phase rotation.

Table 6.1   T*m*CTC Setting: Corresponding Phase and Direction of Correction (Sheet 1 of 2)

T*m*CTC Setting[a]	Matrix	ABC System Rotation Amount and Direction of Correction	ACB System Rotation Amount and Direction of Correction
0	CTC(0)	0°	0°
1	CTC(1)	30° CCW	30° CW
2	CTC(2)	60° CCW	60° CW
3	CTC(3)	90° CCW	90° CW
4	CTC(4)	120° CCW	120° CW
5	CTC(5)	150° CCW	150° CW

Table 6.1 T*m*CTC Setting: Corresponding Phase and Direction of Correction (Sheet 2 of 2)

T*m*CTC Setting[a]	Matrix	ABC System Rotation Amount and Direction of Correction	ACB System Rotation Amount and Direction of Correction
6	CTC(6)	180° CCW	180° CW
7	CTC(7)	210° CCW	210° CW
8	CTC(8)	240° CCW	240° CW
9	CTC(9)	270° CCW	270° CW
10	CTC(10)	300° CCW	300° CW
11	CTC(11)	330° CCW	330° CW
12	CTC(12)	0° (360°) CCW	0° (360°) CW

[a] *m* = S, T, U, W, X.

As shown in *Table 5.2*, the compensation Matrix CTC(0) multiplies the currents by the identity matrix and creates no change in the currents. The compensation Matrix CTC(12) is similar to CTC(0) in that it produces no phase shift (or, more correctly, 360 degrees of shift) in a balanced set of phasors separated by 120 degrees. However, CTC(12) removes zero-sequence components from the measured current, as do all of the matrices having non-zero values.

Transformer Nameplates and System Connections

In order to determine the phase shift detected by the relay, the following information is required:

➤ Transformer phasor (vector) diagram (transformer nameplate)

➤ Three-line connection diagram showing the following:

   ➢ System phase-to-transformer bushing connections

   ➢ CT connections

   ➢ CT-to-relay connections

Figure 6.1 shows the key information from a typical nameplate for a two-winding transformer. The winding connection diagram and the phasor (vector) diagram are needed to determine the winding compensation settings in the relay.

```
KVA.....7500/10000
HV.....13800
kV BIL.  95HV/60LV
LV.....4160Y/2402
LV AMP. 1041/1388
AVG./MAX. AMB.  30/40
```
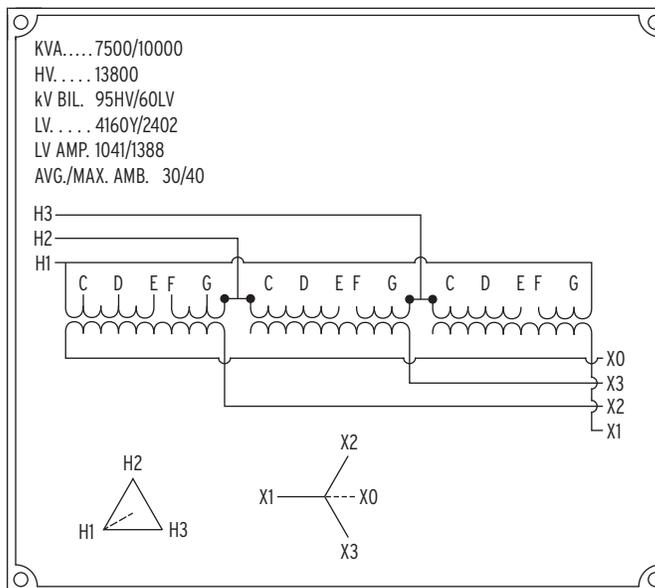
Figure 6.1   Transformer Nameplate

Note that there is no phase designation nor any phase rotation designation on the nameplate. However, the phasor diagram is representative of an H1-H2-H3 sequence. The phase shift on the power system depends on the transformer winding connections, the system phase-to-transformer bushing connections, and the system phase rotation.

Figure 6.2 shows a three-line connection diagram with the transformer of *Figure 6.1* with what this guideline refers to as standard connections. Standard phase-to-bushing connections are A-Phase to H1, B-Phase to H2, C-Phase to H3, a-phase to X1, b-phase to X2, and c-phase to X3. Standard CT connections include wye-connected CTs with polarity marks of both CTs away from the transformer or towards the transformer. *Figure 6.2* shows both H-side and X-side CTs connected in wye and the polarity marks away from the transformer. A CT-to-relay connection is considered to be standard when the polarity of the CT is connected to the polarity of the relay analog current input and the primary system phase current is connected to the same phase input on the relay (e.g., IA system to IAS). Unless otherwise noted, an ABC phase rotation is assumed for the following discussion.
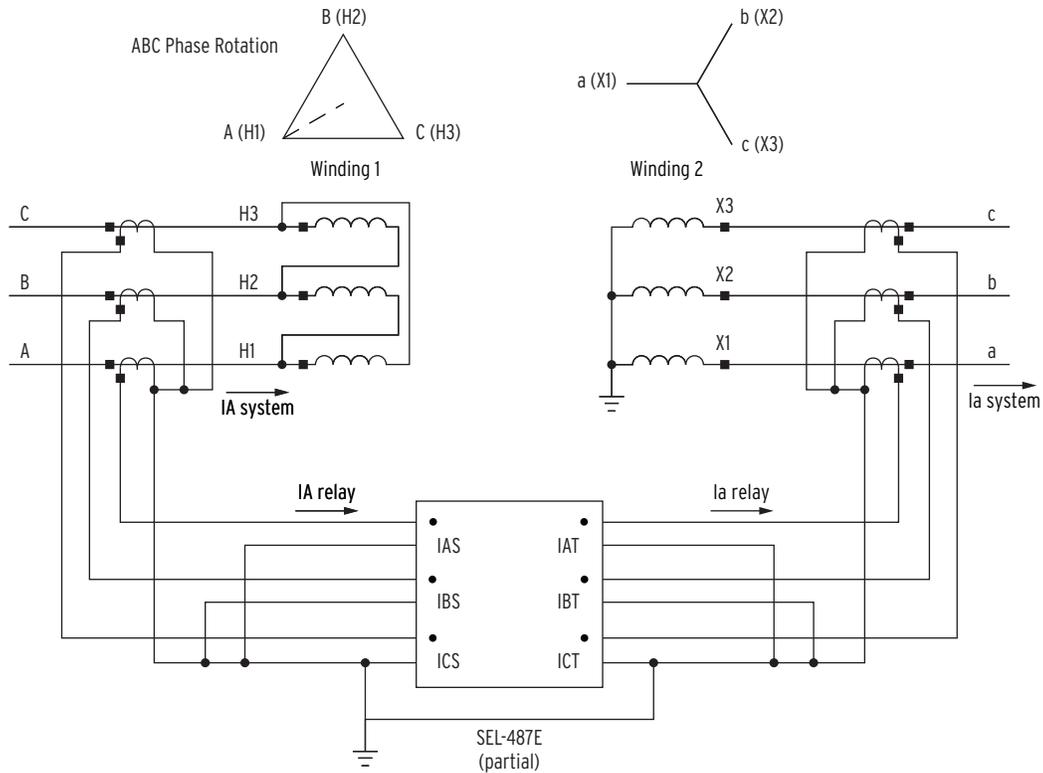
Figure 6.2   Three-Line Diagram Showing System Phase-to-Transformer Bushing, CT, and CT-to-Relay Connections

If all the connections are standard as shown in *Figure 6.2*, under a through-load condition the phase relationship between the system primary currents (Ia system and IA system) and corresponding secondary currents as seen by the relay (IAT and IAS) will look like as shown in *Figure 6.3* (Ia lags IA by 30 degrees) and *Figure 6.4* (IAT lags IAS by 210 degrees), respectively. The goal of the compensation settings is to compensate IAT to bring IAT_compensated 180 degrees out-of-phase with IAS.
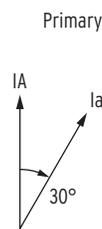
Figure 6.3   Primary Current Phasors
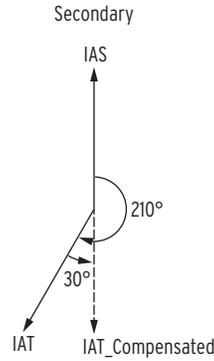
Figure 6.4   Current at the Relay Terminals

Many applications do not conform to the standard connections so the compensation settings are adaptable to fit the application. The subsequent sections outlines the procedure to determine the phase shift and current transformer compensation settings along with discussing what to do with non-standard phase-to-bushing, CT, and CT-to-relay connections.

Steps to Determine the Compensation Settings (T*m*CTC)

Use the following guidelines to determine compensation settings for each application.

Step 1.   Determine the phase shift as seen by the relay.

a.   Determine the phase shift in the primary load current.

b.   Determine if there are non-standard CT connections.

Step 2.   Select the reference winding and associated relay terminal.

a.   If a delta winding exists and is wired into the relay, choose it as the reference winding. Select Matrix CTC(0) for the compensation of the delta winding. If a zig-zag grounding transformer exists on the delta side of the transformer and is within the zone of protection, select Matrix CTC(12).

b.   If a delta winding does not exist, select one of the wye windings as the reference and choose Matrix CTC(11) for the compensation.

Step 3.   Once the reference winding is selected, determine the required compensation setting for all other windings. Select Matrix CTC(0) for delta windings. Use odd matrices for compensating wye-windings. Avoid the use of even matrices when possible.

There may be applications that require the guidelines to be violated, but they should be followed when possible.

The rest of this section discusses each of the guidelines in detail. Examples and special cases are provided to illustrate the application of the guidelines in determining the compensation settings.

Step 1. Determine the Phase Shift as Seen by the Relay

Determine the Phase Shift in the Primary Load Current

NOTE: Unless otherwise stated, this discussion assumes an ABC system phase rotation.

The first step in selecting the compensation setting in the relay is to determine the phase shift in the primary load current.

Standard System Phase-to-Transformer Bushing Connections

Consider the transformer in *Figure 6.1* and the phase-to-bushing connection of *Figure 6.2*. Assume balanced X-side (wye-winding), three-phase currents Ia, Ib, and Ic, as shown in *Figure 6.5*. The currents in the H-side (delta-winding) of the transformer are Ia/N, Ib/N, and Ic/N where N is the turns ratio of the transformer. Because the discussion focuses on the phase shift and not the magnitude, one can assume N = 1 for this discussion.
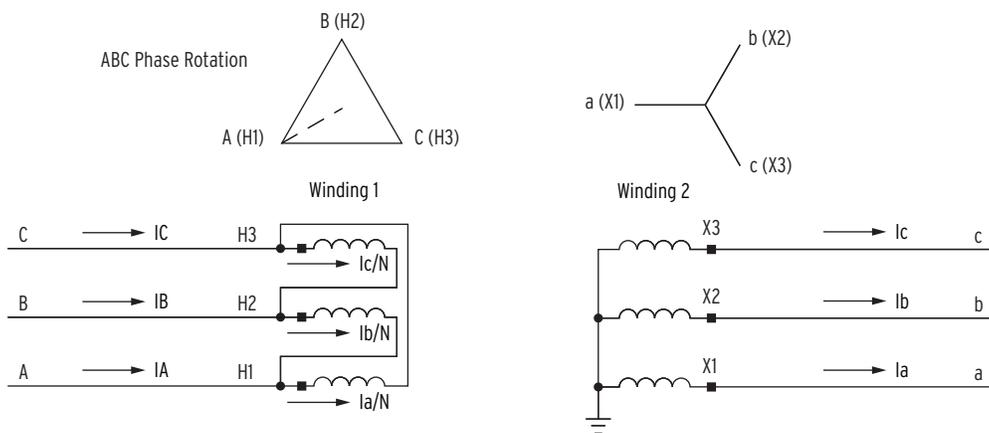
Figure 6.5   Standard System Phase-to-Transformer Bushing Connections

Kirchhoff's Current Law is used at each H node to determine the primary phase currents on the H-side of the system:

$$IA = Ia - Ib$$

$$IB = Ib - Ic$$

$$IC = Ic - Ia$$

In the following examples start with the currents on the wye-side of the transformer to graphically derive the currents on the delta side of the transformer. *Figure 6.6* shows that system primary current Ia (X-side) lags the system primary current IA (H-side) by 30 degrees.
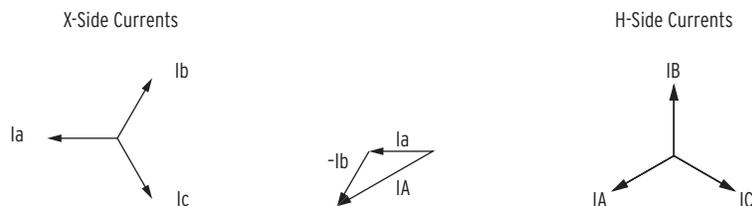
Figure 6.6   X- and H-Side Current Phasors for *Figure 6.5*

The primary load phase shift determined in *Figure 6.6* applies for the phase-to-bushing connections shown in *Table 6.2*. In each of these phase-to-bushing connections, the order of the phases (A, B, C) matches the order of the bushings (H1, H2, H3).

Table 6.2   (A, B, C) to (H1, H2, H3) Phase-to-Bushing Connections

	Bushing					
	H1	**H2**	**H3**	**X1**	**X2**	**X3**
System Phase	A	B	C	a	b	c
	B	C	A	b	c	a
	C	A	B	c	a	b

Non-Standard Phase-to-Bushing Connections

Consider the transformer connections of *Figure 6.7*. This is the same transformer discussed in *Figure 6.5*, but with different phase-to-bushing connections: A-Phase to H3, B-Phase to H2, C-Phase to H1, a-phase to X3, b-phase to X2, and c-phase to X1.
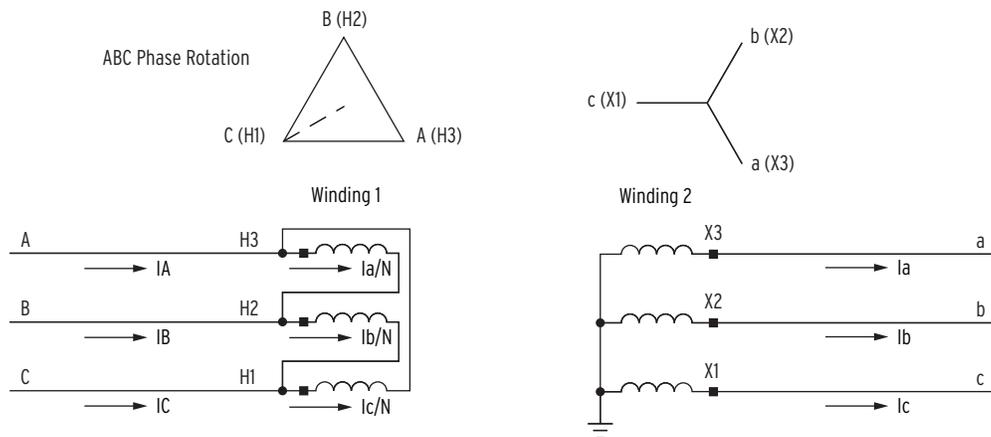
Figure 6.7   Non-Standard System Phase-to-Transformer Bushing Connections

Assume balanced X-side (wye-winding), three-phase currents Ia, Ib, and Ic. Kirchhoff's Current Law is used at each H node to determine the primary phase currents on the H-side of the system:

IA = Ia – Ic

IB = Ib – Ia

IC = Ic – Ib

Figure 6.8 shows that system primary current Ia (X-side) leads the system primary current IA (H-side) by 30 degrees.
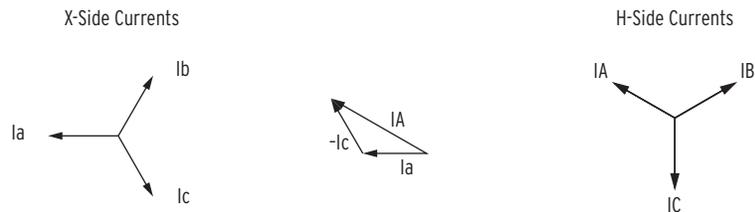
Figure 6.8   X- and H-Side Current Phasors for *Figure 6.7*

The primary load phase shift determined in *Figure 6.8* applies for the phase-to-bushing connections shown in *Table 6.3*. In each of these phase-to-bushing connections, the order of the phase connections (A, C, B) is opposite the order of the bushings (H1, H2, H3).

Table 6.3 (A, C, B) to (H1, H2, H3) Phase-to-Bushing Connections

	Bushing					
	H1	**H2**	**H3**	**X1**	**X2**	**X3**
System Phase	C	B	A	c	b	a
	B	A	C	b	a	c
	A	C	B	a	c	b

The system phase-to-transformer bushing connection diagrams in *Figure 6.5* and *Figure 6.7* are on the same transformer, but with a different order of the phases connected to the transformer bushings. As a result, the X-side primary current shifts 30 degrees in opposite directions in the two systems.

Combination of Standard and Non-Standard Phase-to-Bushing Connections

Consider the transformer connections shown in *Figure 6.9*. The transformer is the same as in previous examples. However, in this example, the H-side phase-to-bushing connections are standard: A-Phase to H1, B-Phase to H2, and C-Phase to H3. The X-side connections are non-standard: a-phase to X2, b-phase to X3, and c-phase to X1.
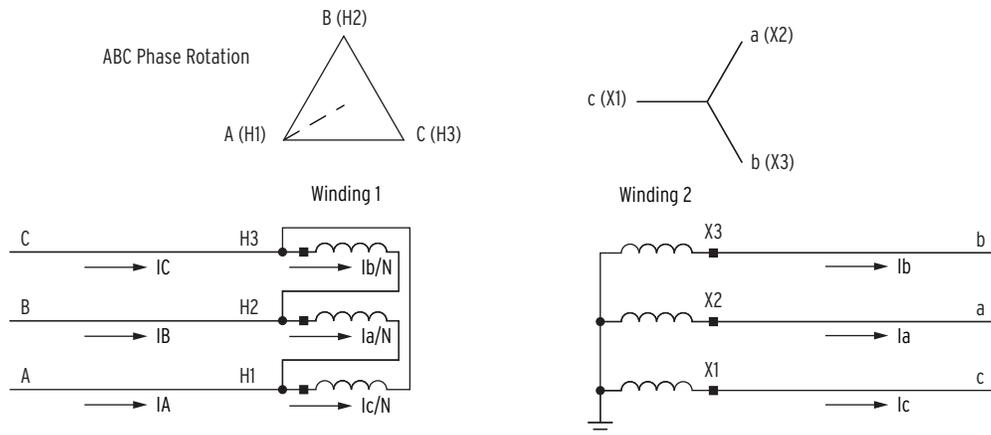
Figure 6.9 Combination of Standard and Non-Standard Phase-to-Bushing Connection Diagram

Assume balanced X-side (wye-winding), three-phase currents Ia, Ib, and Ic. Kirchhoff's Current Law is used at each H node to determine the primary phase currents on the H-side of the system:

IA = Ic – Ia

IB = Ia – Ib

IC = Ib – Ic

Figure 6.10 shows that system primary current Ia (X-side) lags the system primary current IA (H-side) by 150 degrees.

X-Side Currents
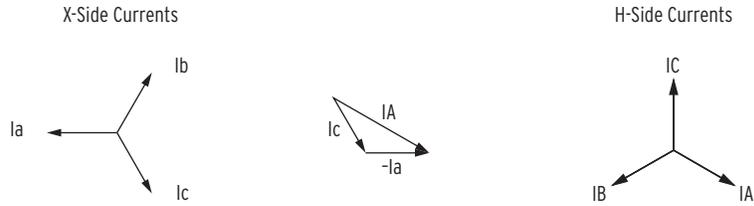
H-Side Currents

Figure 6.10   X- and H-Side Current Phasors for *Figure 6.9*

These three examples show that the same transformer winding connections can produce different phase shifts in the system primary-load current based on the phase-to-bushing connections.

Determine if There Are Non-Standard CT Connections

Figure 6.11 shows the transformer of *Figure 6.2* with standard current transformer configuration; that is, both the H-side and X-side CTs are connected in wye and the polarity marks are away from the power transformer.
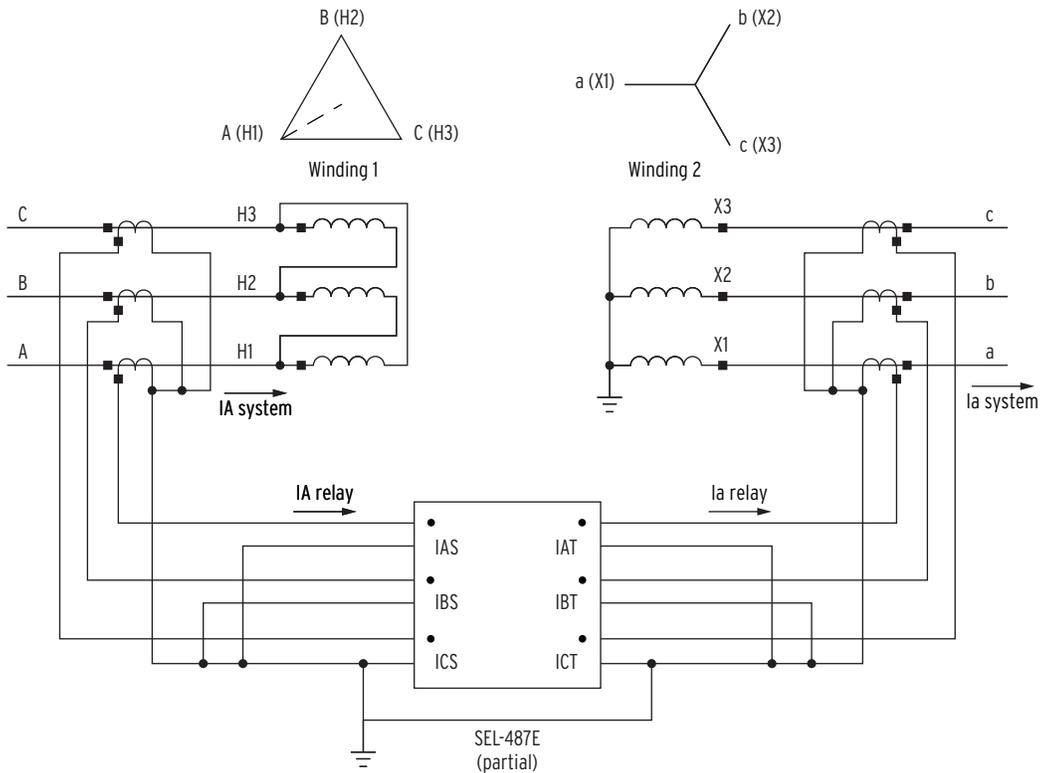
Figure 6.11   Standard CT Connections

Standard CT Connections

In *Figure 6.11*, the polarity of the CT connects to the polarity of the relay analog current input, and the primary system phase current connects to the same phase input on the relay (e.g., IA system to IAS relay input). While the H-side currents connect to the S-Terminal and the X-side currents connect to the T-Terminal, they could be connected to any two sets of current inputs on the relay. *Figure 6.11* represents the standard connections for the transformer, CTs, and relay.

Figure 6.11 also shows the primary system currents (IA system, Ia system) and the CT secondary currents seen by the relay (IA relay, Ia relay) based on the currents of *Figure 6.6*. For these connections, with power flow from the H-side to

X-side of the transformer, currents enter the relay at the polarity mark on the H-side, and leave the relay at the polarity mark on the X-side. Thus, on the primary system, Ia lags IA by 30 degrees but at the relay IAT leads IAS by 150 degrees, as shown in *Figure 6.12*. B- and C-Phases follow this relationship. Only A-Phase is discussed for simplicity, but the concept is the same.
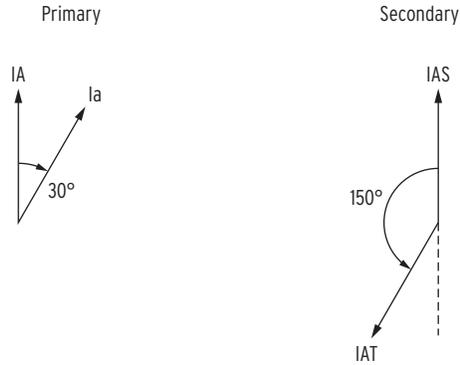
Figure 6.12   Primary System Current and Current as Seen by the Relay

Non-Standard CT Connections: Reversed CT Polarity

Figure 6.13 shows the X-side CT polarity marks toward the transformer. However, because the connections to the relay remain the same, the relay currents flow the same, as in *Figure 6.12*. No additional adjustments need to be made because of this type of non-standard CT connection.
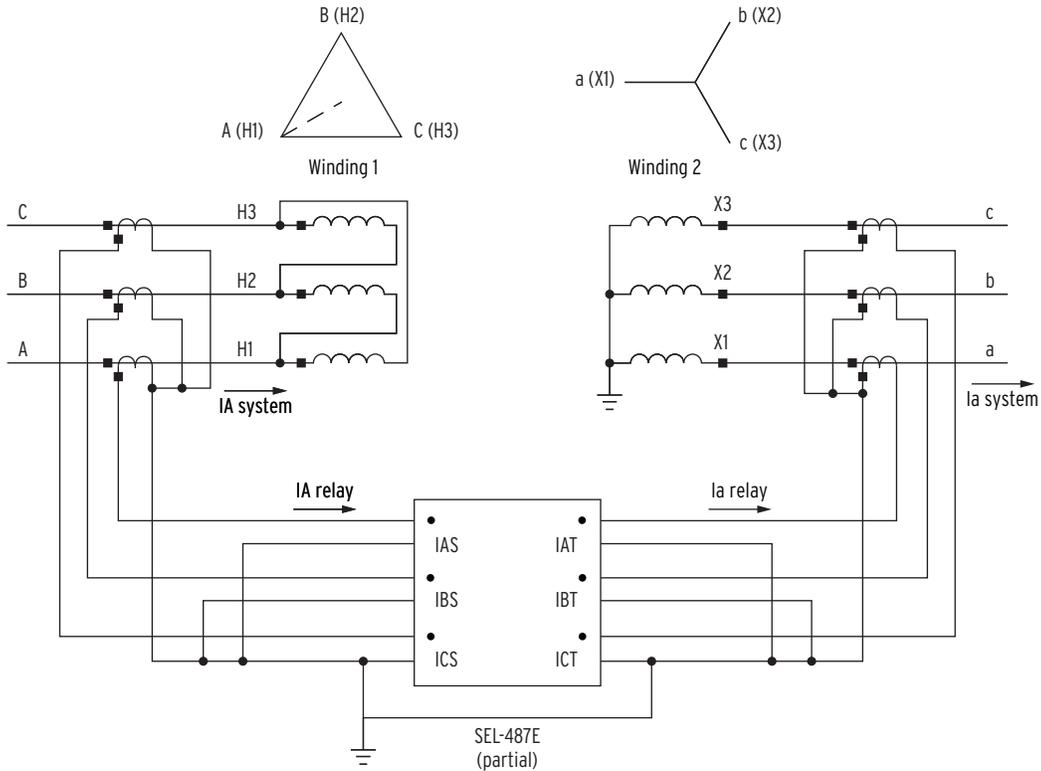
Figure 6.13   Current Flow With Reversed X-Side CT Polarity

Non-Standard CT Connections: Reversed CT Polarity and Reversed Connections

In *Figure 6.14*, the polarity marks of the X-side CTs are toward the transformer, as in *Figure 6.13*, but the neutral sides of the CTs are away from the transformer. With these connections, the H-side and X-side currents are both entering the relay at the relay polarity mark.
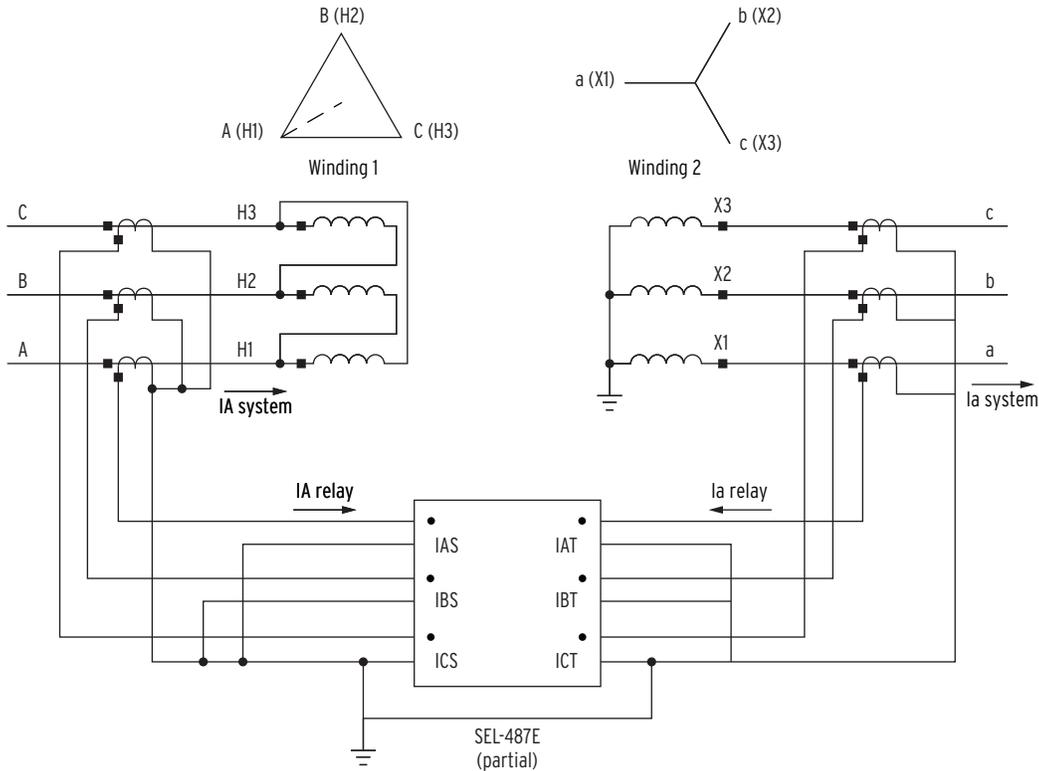
Figure 6.14   Current Flow With Reversed X-Side CT Polarity and Reversed Connections

As shown in *Figure 6.15*, the resulting IAT current measured by the relay is now shifted 180 degrees as compared to the previous example.
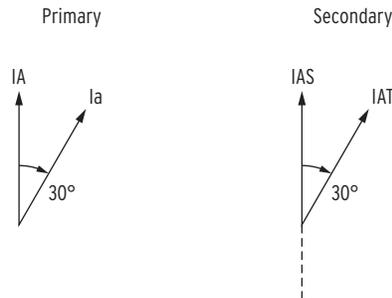
Figure 6.15   Results of Reversed X-Side CT Polarity and Reversed Connections

One method to correct this is to reverse the current connections at the relay. Connect the non-polarity terminal of the CT to the polarity terminal of the relay analog current input and the polarity terminal of the CT to the non-polarity terminal of the relay analog current input. These changes result in the connections shown in *Figure 6.13*.

An alternate method corrects the phase shift with the CT compensation setting, T*m*CTC. As shown in *Table 6.1*, each CTC setting results in a counter-clockwise phase shift that is a multiple of 30 degrees for an ABC system phase rotation. Selecting a compensation setting of 6 effectively shifts the current by 180 degrees (6 • 30 degrees = 180 degrees). Further explanation of selecting the final settings for non-standard CT connections is provided in *Example 6.3*.

Step 2. Select the Reference Winding and Associated Relay Terminal

If there is a delta winding on the power transformer, the delta winding should be selected as the reference winding regardless of whether it is the high- or low-voltage winding. The reference winding can be associated with any analog current measurement terminal on the relay. For example, if the delta winding current is measured by the S-Terminal inputs on the relay, TSCTC is the setting that corresponds to the reference winding.

The compensation for the delta winding should be set to Matrix CTC(0) (T*m*CTC = 0) unless there is a grounding bank on the delta winding within the differential zone. Grounding banks are a source of zero-sequence current and this current needs to be filtered to avoid operation of the differential element for external ground faults. If there is a grounding bank within the differential zone, use T*m*CTC = 12. Both T*m*CTC = 0 and T*m*CTC = 12 result in no phase shift, but T*m*CTC = 12 additionally removes zero-sequence current from the differential calculation.

If there is no delta winding, select one of the wye windings as the reference and set the compensation to 11 (T*m*CTC = 11) for the reference winding.

Step 3. Determine the Remaining Compensation Settings for All Other Windings

Use the following guidelines for choosing the remaining CT compensation settings.

1. Compensate delta windings with Matrix CTC(0).

2. Compensate wye windings with odd matrices.

3. Avoid the use of even matrices.

There may be applications that require one or more of the guidelines to be violated, but they should be followed when possible. The following examples will illustrate the steps required to determine the compensation settings for the remaining windings.

Application Examples

Example 6.1   Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation

Consider the system shown in *Figure 6.16*. The primary current phase shift for these connections was determined in *Figure 6.6*. The system primary current Ia (X-side) lags the system primary current IA (H-side) by 30 degrees. The CT connections are standard, which results in IAT leading IAS by 150 degrees.

Example 6.1   Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation (Continued)
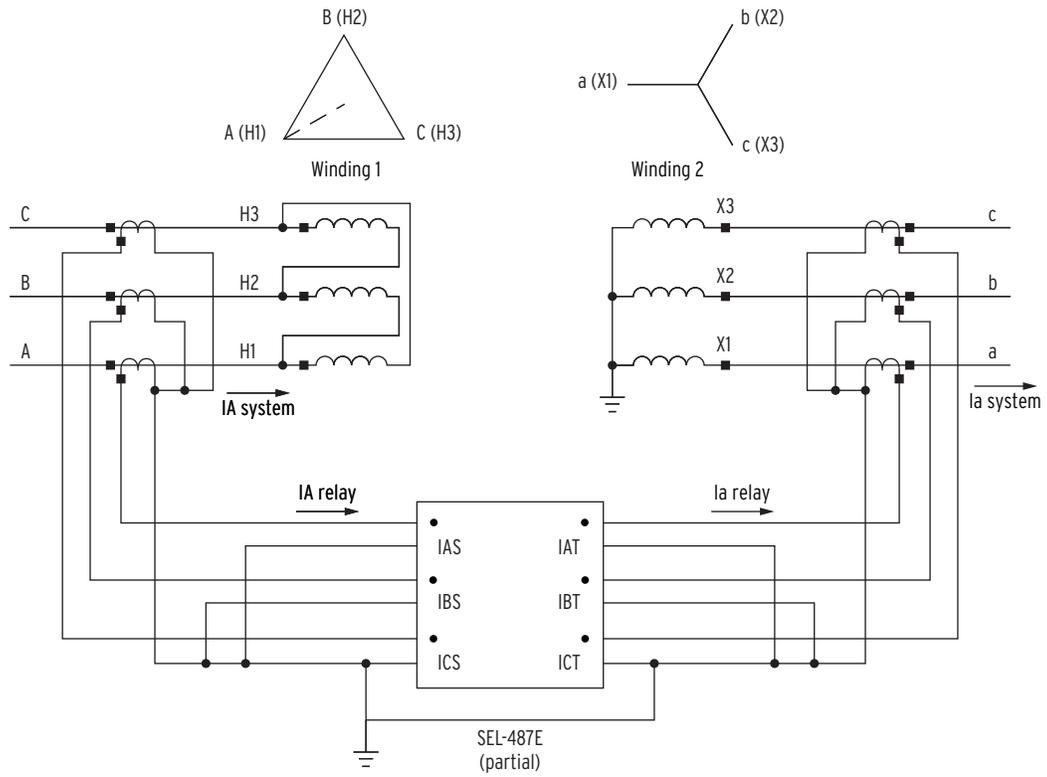
Figure 6.16   Delta-Wye Transformer With Standard Phase-to-Bushing Connections

Select the delta winding as the reference winding. The H-side delta current is connected to Terminal S of the SEL-487E Relay. Therefore, set TSCTC = 0. The X-side currents are connected to Terminal T of the SEL-487E Relay, so TTCTC must be determined. *Figure 6.17* shows the phase relationship of both the primary system phase currents and the secondary phase currents as seen by the relay.
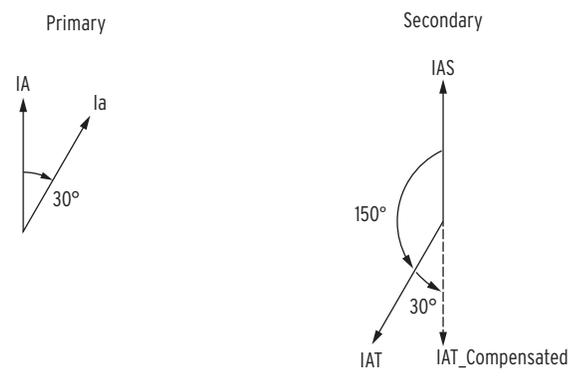
Figure 6.17   Differential Current Measured by the Relay

IAT must be rotated 30 degrees (1 multiple of 30 degrees) in the counter-clockwise direction for systems with ABC phase rotation to be 180 degrees out-of-phase with IAS. Therefore, set TTCTC = 1. The resulting compensation settings for *Example 6.1* are TSCTC = 0 and TTCTC = 1.

Example 6.2   Delta-Wye Transformer With Non-Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation

This example uses the transformer and relay connections of *Figure 6.18*. This is the same transformer as in *Example 6.1*, but with non-standard phase-to-bushing connections. *Figure 6.8* shows that for this connection, the system current Ia (X-side) leads the system current IA (H-side) by 30 degrees, or lags by 330 degrees. The CT connections are standard, which results in IAT lagging IAS by 150 degrees.
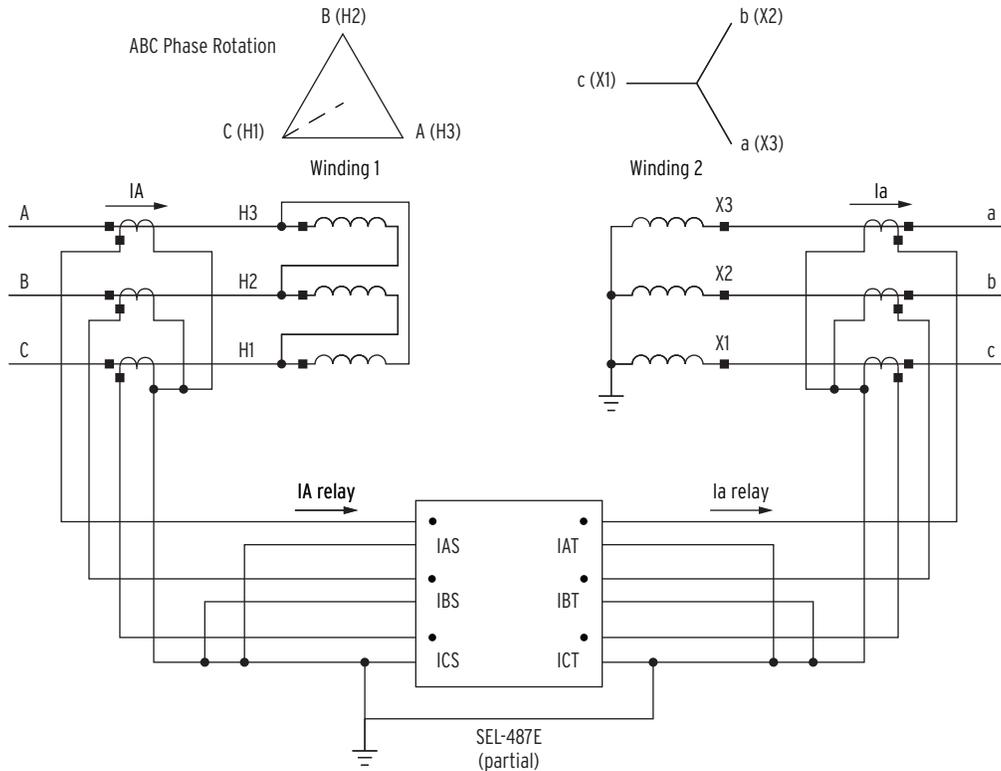
Figure 6.18   Delta-Wye Transformer With Non-Standard Phase-to-Bushing Connections for *Example 6.2*

Select the delta winding as the reference winding. The H-side delta current is connected to Terminal S of the SEL-487E Relay. Therefore, set TSCTC = 0. The X-side currents are connected to Terminal T, so TTCTC must be determined. *Figure 6.19* shows the phase relationship of both the primary system phase currents and the secondary phase currents as seen by the relay.
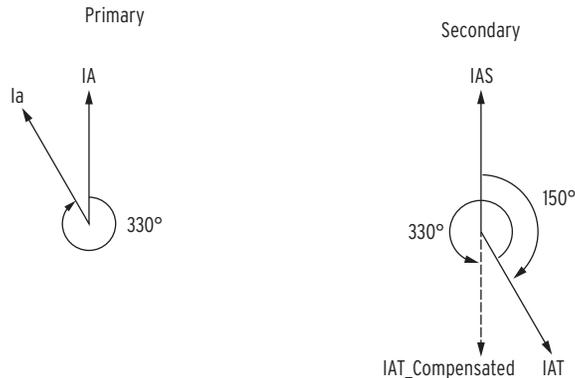
Figure 6.19   IAS and IAT for *Example 6.2*

Example 6.2   Delta-Wye Transformer With Non-Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation (Continued)

IAT must be rotated 330 degrees (11 multiples of 30 degrees) in the counter-clockwise direction for a system with an ABC phase rotation to be 180 degrees out-of-phase with IAS. Therefore, set TTCTC = 11. The resulting compensation settings for *Example 6.2* are TSCTC = 0 and TTCTC = 11. Although the same transformer is used in *Example 6.1* and *Example 6.2*, notice that the non-standard phase-to-bushing connections affect the compensation settings in both examples.

Example 6.3   Delta-Wye Transformer With Standard Phase-to-Bushing Connections, X-Side Non-Standard CT Connections, and ABC System Phase Rotation

This example uses standard phase-to-bushing connections, as shown in *Figure 6.20*. Notice the X-side CT connections are non-standard. This example differs from the previous examples because the wye winding is now on the high side. The method to solve for the compensation settings is the same.
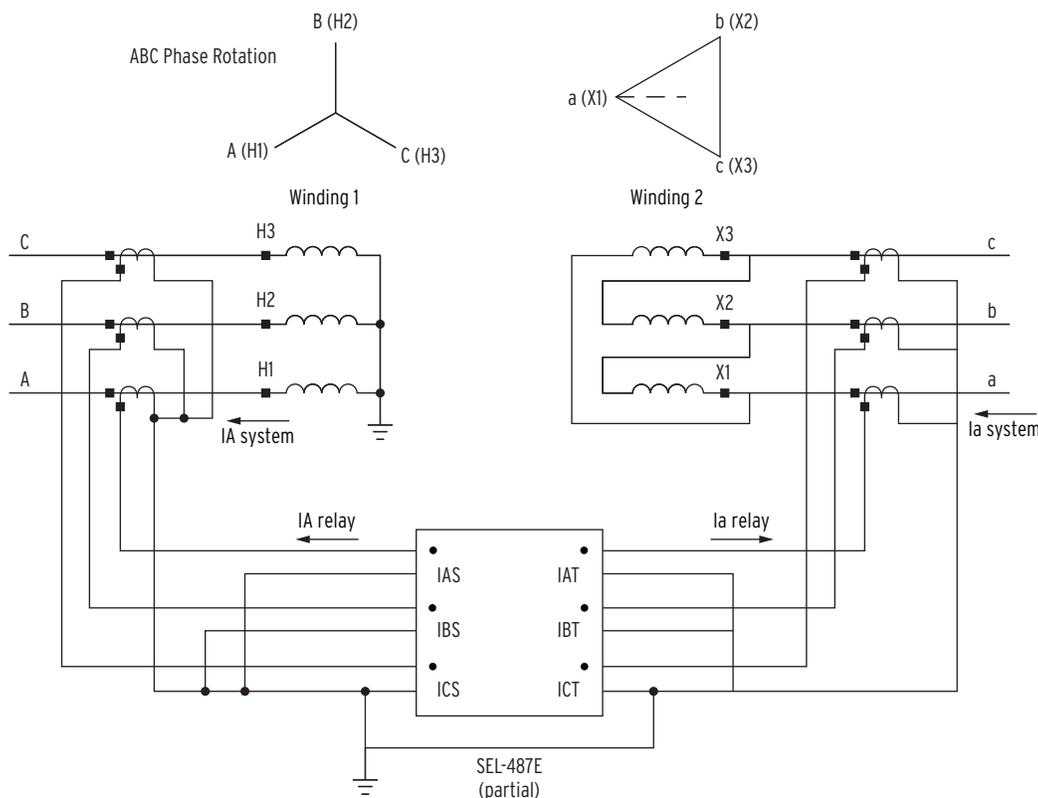
Figure 6.20   Wye-Delta Transformer With Non-Standard CT Connections on X-Side

Assume balanced three-phase currents on the wye side of the transformer. In this example, the wye side is associated with the H-side of the transformer. The phase currents on the X-side are:

$$Ia = IA - IC$$

$$Ib = IB - IA$$

$$Ic = IC - IB$$

Example 6.3   Delta-Wye Transformer With Standard Phase-to-Bushing Connections, X-Side Non-Standard CT Connections, and ABC System Phase Rotation (Continued)

Figure 6.21 selects IA on the wye side of the transformer as the reference to derive the phasor diagram of the delta-side currents. The system primary current Ia (X-side) lags the system primary current IA (H-side) by 30 degrees.
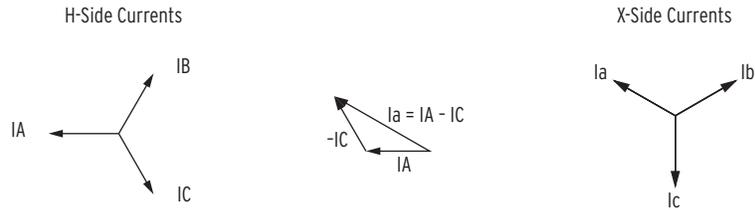
Figure 6.21   System Currents on H-Side (Wye) and X-Side (Delta) of the Transformer

With the reversed CT polarity on the X-side, the current is leaving Terminal T at the polarity mark instead of entering the polarity mark, which makes the current seen by the relay 180 degrees out-of-phase compared to a standard CT connection. In *Non-Standard CT Connections: Reversed CT Polarity and Reversed Connections on page 6.11*, two methods were proposed to correct the phase shift for reverse polarity CTs. The first is to rewire the current inputs on the relay so that they match the standard connections. The second is to use the compensation setting by adding or subtracting 6 from the setting. This example explores the latter method.

Following the settings guidelines, select the delta side as the reference. The delta side of the transformer is connected to relay Terminal T, therefore, TTCTC = 0 and is used as the reference. *Figure 6.22* compares the current phasors if the X-side CT connections used standard connections vs. non-standard connections. On the left side of *Figure 6.22*, standard CT connections and ABC phase rotation require IAS to rotate 330 degrees (11 multiples of 30 degrees) counter-clockwise to be 180 degrees out-of-phase with IAT. Therefore, if the X-side CTs had standard connections, set TSCTC = 11. The resulting compensation settings with standard CT connections are TTCTC = 0 and TSCTC = 11.
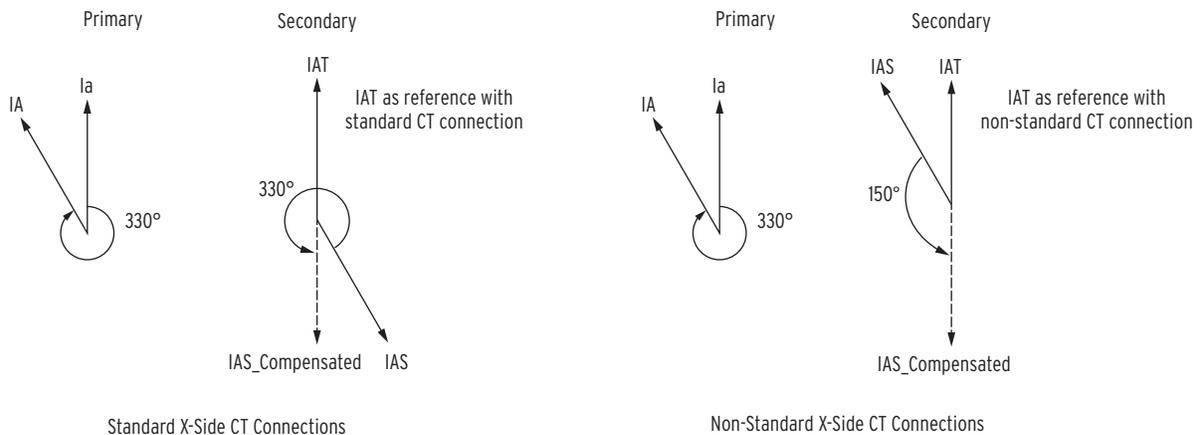
Figure 6.22   Comparison of Standard and Non-CT Connections on X-Side of Transformer

Example 6.3   Delta-Wye Transformer With Standard Phase-to-Bushing Connections, X-Side Non-Standard CT Connections, and ABC System Phase Rotation (Continued)

However, in this example, non-standard CT connections are used on the delta winding which results in IAS leading IAT by 30 degrees. IAS needs to rotate 150 degrees (5 multiples of 30 degrees) counter-clockwise for a system with an ABC phase rotation to be 180 degrees out-of-phase with IAT. Therefore, set TSCTC = 5. The resulting compensation settings for *Example 6.3* with non-standard CT connections on the X-side are TTCTC = 0 and TSCTC = 5.

Example 6.4   Autotransformer, Standard Phase-to-Bushing Connections, Standard CT Connections, and an ABC System Phase Rotation

Consider the autotransformer shown in *Figure 6.23*. The delta tertiary exists but is buried and not brought out to the relay. The primary current phase shift for these connections is shown in *Figure 6.24*. The system primary current Ia (X-side) is in phase with the system primary current IA (H-side). The CT connections are standard, which results in IAT 180 degrees out-of-phase with IAS.

Per the guidelines, because there is no delta winding connected to the relay, choose any one of the wye windings, say H-side, as the reference winding and choose matrix CTC(11) for the compensation. The H-side currents are connected to Terminal S of the SEL-487E Relay. Therefore, set TSCTC = 11. The X-side currents are connected to Terminal T, so TTCTC must be determined. *Figure 6.24* shows the phase relationship of both the primary system phase currents and the secondary phase currents as seen by the relay. Because Matrix 11 is applied to Winding 1, this will shift IAS 11 multiples of 30 degrees in the counterclockwise direction. To keep Winding 2 current, IAT 180 degrees out-of-phase with IAS, you must also shift IAT by 11 multiples of 30 degrees in the counterclockwise direction. The resulting compensation settings are TSCTC = 11 and TTCTC = 11.

Example 6.4 Autotransformer, Standard Phase-to-Bushing Connections, Standard CT Connections, and an ABC System Phase Rotation (Continued)
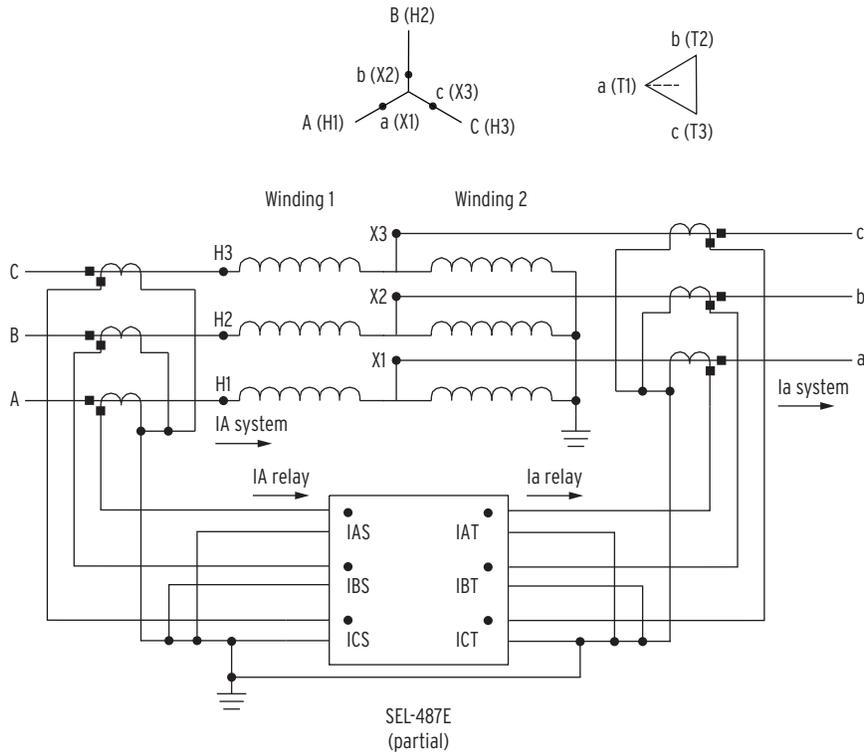
Figure 6.23 Autotransformer With Standard Phase-to-Bushing Connections
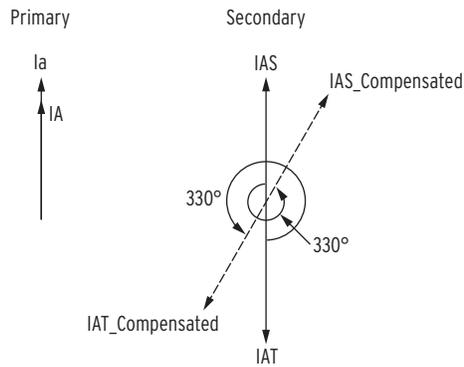
Figure 6.24 Primary Currents and Secondary Currents as Measured by the Relay

Special Cases

Example 6.5   Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ACB System Phase Rotation

Consider the application in *Figure 6.25* with standard phase-to-bushing connections, standard CT connections, and ACB system phase rotation.
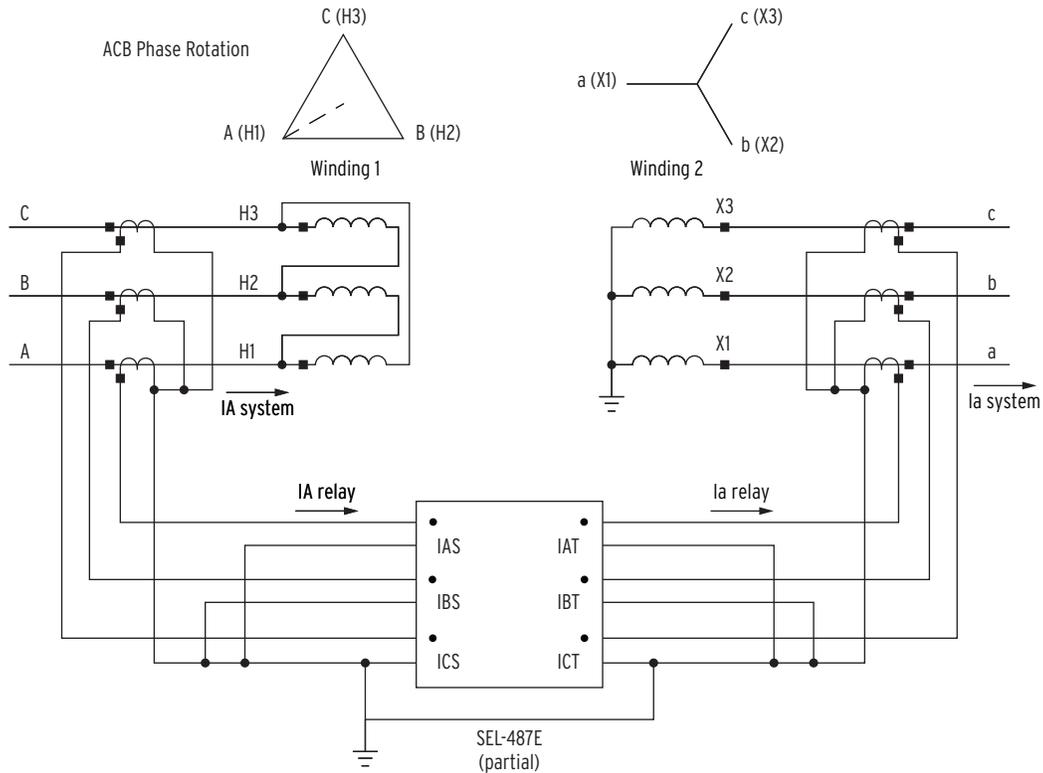
Figure 6.25   Delta-Wye Transformer With Standard Phase-to-Bushing Connections With an ACB Phase Rotation

The H-side currents are:

$IA = Ia - Ib$

$IB = Ib - Ic$

$IC = Ic - Ia$

Figure 6.26 uses a balanced set of three phase currents with ACB phase sequence on the wye winding as a reference to derive the delta winding (H-side) currents. When compared to *Example 6.1*, even with the same transformer and the same connections, *Figure 6.26* shows that Ia (X-side) now leads IA (H-side) by 30 degrees because of the system phase rotation. Note that in *Example 6.1*, Ia (X-side) lags IA (H-side) by 30 degrees.

Example 6.5   Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ACB System Phase Rotation (Continued)

X-Side Currents   H-Side Currents
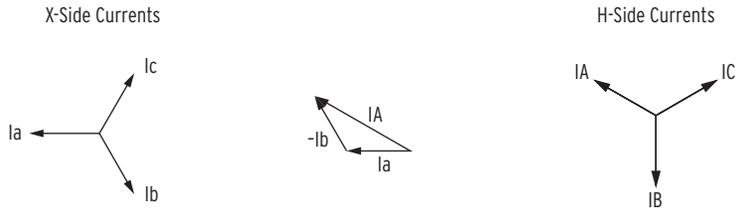
Figure 6.26   X- and H-Side Current Phasors for *Figure 6.25*

A common misconception is that a different compensation setting is required depending on the system phase rotation. However, closer inspection of the compensation matrices and the direction of correction in *Table 6.1* indicates that the matrix will cause the compensated currents to rotate in the opposite direction depending on the system phase rotation.
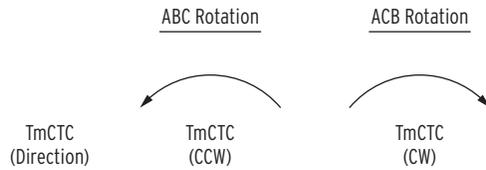
Thus, the compensation settings required for *Example 6.1* and *Example 6.5* are the same. Following the settings guideline, the delta side of the transformer is selected as the reference, so TSCTC = 0. *Figure 6.27* shows IAT needs to rotate 30 degrees (1 multiple of 30 degrees) clockwise for a system with an ACB phase rotation to be 180 degrees out-of-phase with IAS. Therefore, set TTCTC = 1. The resulting compensation settings for *Example 6.5* are TSCTC = 0 and TTCTC = 1.
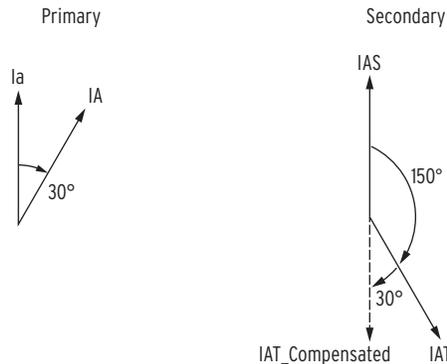
Primary   Secondary

Figure 6.27   Primary Currents and Secondary Currents as Measured by the Relay

If the relay is set assuming an ABC phase rotation, but the actual system phase sequence is ACB, the relay compensation settings do not need to be changed. However, the calculated positive- and negative-sequence currents will be incorrect unless the Global setting for phase rotation, PHROT, matches the system phase sequence. PHROT does not affect the compensation settings or differential protection.

Example 6.6   Delta-Wye Transformer With Standard Phase-to-Bushing Connections, Standard CT Connections, and ABC System Phase Rotation With Zig-Zag Grounding Bank on a Delta Transformer Winding Inside the Differential Zone

This example uses the same transformer and CT connections as in *Example 6.1*, except that it includes a zig-zag grounding transformer on the delta side of the transformer within the differential zone. Zig-zag transformers are typically used for grounding purposes and act as a source of zero-sequence current. If the zig-zag transformer is located outside of the differential zone on the delta side, it can be ignored, and the compensation settings will remain the same as in *Example 6.1*. The same is true if the zig-zag transformer is present on the wye side, be it inside or outside the differential zone. If the zig-zag transformer is within the differential zone on the delta side, then it has to be accounted for when determining the compensation settings.

The resulting compensation settings in *Example 6.1* were TSCTC = 0 for the delta winding (reference winding) and TTCTC = 1 for the wye winding. When a ground current source is within the differential zone on the delta side, the recommended compensation setting of TSCTC = 0 cannot be used. The zero-sequence current needs to be filtered to avoid operation of the differential element for external ground faults. Therefore, set TSCTC = 12. Matrix CTC(12) has no phase shift but removes zero-sequence current from the differential calculation.

Quick Settings Guide for Standard Connections

Figure 6.28 shows examples of common transformer connections. *Table 6.4* is a quick settings guide to be used when all standard phase-to-bushing, CT, and relay connections are present. *Table 6.4* is applicable to both ABC and ACB system phase rotations.
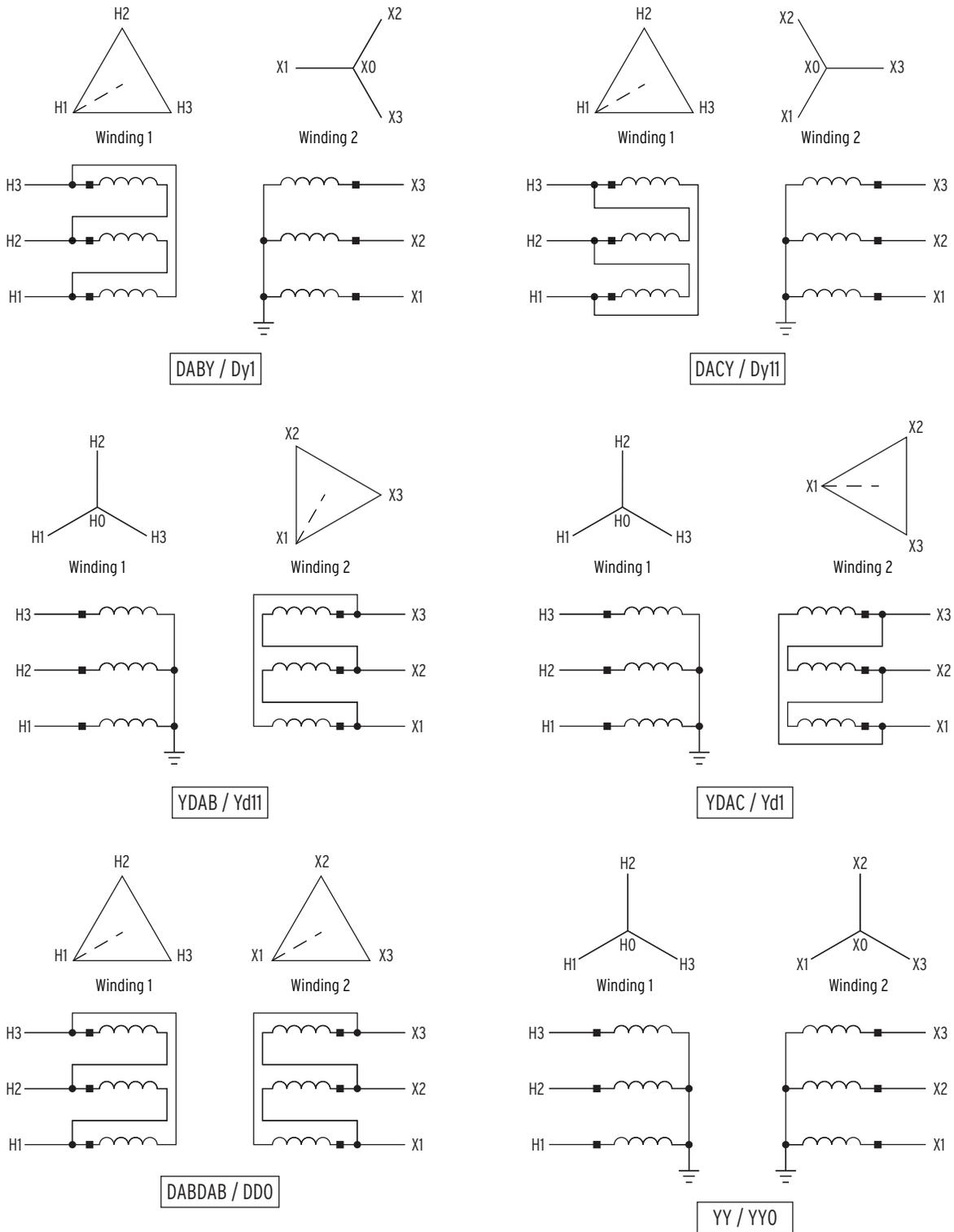
Figure 6.28   Common Transformer Connections

Table 6.4   Quick Settings Guide for Common Transformer Configurations and Standard Connections

XFMR Designation		TSCTC (Winding 1)	TTCTC (Winding 2)
Connection	**IEC**		
DABY	Dy1	0	1
DACY	Dy11	0	11
YDAC	Yd1	11	0
YDAB	Yd11	1	0
DABDAB DACDAC	Dd0	0	0
YY	Yy0	11	11

The compensation settings of *Table 6.4* assume that the Winding 1 side of the transformer is connected to relay Terminal S and the Winding 2 side of the transformer is connected to relay Terminal T. These settings apply for all standard phase-to-bushing connections shown in *Table 6.2*. In each of these phase-to-bushing connections, the order of the phase connections (A, B, C) matches the order of the bushings (H1, H2, H3).

References

Further discussion on selecting transformer compensations settings can be found in the technical paper *Beyond the Nameplate – Selecting Transformer Compensation Settings for Secure Differential Protection* by Barker Edwards, David G. Williams, Ariana Hargrave, Matthew Watkins, and Vinod K. Yedidi (available at selinc.com).

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SECTION 7

Metering, Monitoring, and Reporting

The SEL-487E relay provides extensive capabilities for metering important power system parameters, monitoring transformer components, and reporting on system operation. The relay provides the following useful features:

- ➤ *Metering on page 7.1*
- ➤ *Circuit Breaker Monitor on page 7.13*
- ➤ *Station DC Battery System Monitor on page 7.14*
- ➤ *Thermal Monitor on page 7.14*
- ➤ *Through-Fault Monitor on page 7.34*
- ➤ *Analog Signal Profiling on page 7.39*
- ➤ *Reporting on page 7.40*

See *Section 7: Metering, Section 8: Monitoring, and Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for general information. This section contains details specific to the SEL-487E.

Metering

The SEL-487E provides one-cycle average metering for measuring power system conditions and differential protection values. Each SEL-487E processes 18 currents, six voltages, and one battery monitor.

Table 7.1 shows all the **MET** commands available in the relay.

Table 7.1   MET Command (Sheet 1 of 2)

Command	Description
MET RMS *w n*[a, b]	Display root-mean-square (rms) metering quantities (current and voltage only)
MET F *w n*	Display fundamental metering quantities
MET F N *n*	Display neutral current fundamental metering quantities
MET F Y *n*	Display Y-terminal fundamental metering quantities
MET SEC *w n*	Display secondary metering quantities
MET D *n*	Display demand and peak demand metering quantities
MET RD	Reset demand meter data
MET RP	Reset peak demand data
MET DIF *n*	Display differential data
MET E *n*	Display energy import and export metering quantities
MET RE	Reset energy data
MET PM *n*	Display synchrophasor data
MET PM	Triggers a synchrophasor measurement

Table 7.1   MET Command (Sheet 2 of 2)

Command	Description
MET RTD *n*	SEL-2600 temperature quantities
MET PMV *n*	Display protection math variables
MET AMV *n*	Display automation math variables
MET BAT *n*	Display battery data
MET RBM	Reset station battery max/min measurements
MET ANA *n*	Display analog values from MIRRORED BITS analog, and remote analogs

[a]   *w* = S, T, U, W, X, ST, TU, UW, WX.

[b]   *n* = the number of times the relay repeats the response.

Because of the large number of analog channels, not all analog channels are required for every application. Furthermore, when the Torque-Control settings (of those analog quantities that have Torque-Control settings) deassert, those analog quantities are not shown in the meter report.

There are thus two different instances for not displaying analog quantities in the meter report: you either did not select the analog quantity, or the analog quantity is temporarily not calculated when the Torque-Control equation de-asserts. To distinguish between these two conditions, the relay display dashes (-----) when the analog quantity was not selected, and zeros (000.00) when the Torque-Control equation deasserts.

Instantaneous Metering
Fundamental Meter

Use the **MET** (**F**) *w* command (*w* = S, T, U, W, X, ST, TU, UW, WX) to view the fundamental (60 or 50 Hz) metering values. When you type **MET** without an argument, the report defaults to Winding S. For each winding, the fundamental meter report provides the quantities shown in *Table 7.3*.

Table 7.2 shows the order of valid reference quantities that the relay uses to display the angular relationship among the metering values.

Table 7.2   Valid Reference Quantities

Reference Quantity	Source	Valid Value
Positive-sequence voltage	PT V	Positive-sequence voltage > 0.1 • VNOMV
Positive-sequence voltage	PT Z	Positive-sequence voltage > 0.1 • VNOMZ
Positive-sequence current	Winding S	Positive-sequence current > 0.05 • INOMS
Positive-sequence current	Winding T	Positive-sequence current > 0.05 • INOMT
Positive-sequence current	Winding U	Positive-sequence current > 0.05 • INOMU
Positive-sequence current	Winding W	Positive-sequence current > 0.05 • INOMW
Positive-sequence current	Winding X	Positive-sequence current > 0.05 • INOMX

For example, the positive-sequence voltage calculated from the PT V voltage inputs is reference for all metering quantities, provided that this positive-sequence voltage exceeds 10 percent of the VNOMV setting. If PT V is not available, then the positive-sequence voltage calculated from the PT Z voltage inputs

is reference for all metering quantities, provided that this positive-sequence voltage exceeds 10 percent of the VNOMV settings. This sequence continues for all other reference quantities.

Table 7.3   Quantities in the Fundamental Meter Report

Quantity	Description
IA, IB, IC	Winding *w* A-Phase, B-Phase, and C-Phase primary current. The reference is independent of the VREF*k* settings (*k* = S, T, U, W, X), and is determined as follows: 1. A-Phase of PT V (if available) 2. A-Phase of PT Z (if available, and PT V is not available) 3. A-Phase of Winding *w* current (if no PTs are available). If *w* is a combination of terminals, such as ST, the reference is selected as the first current terminal in the pair.
I1, 3I2, 3I0	Positive-, negative-, and zero-sequence components for Winding *w*. 3I0 is not available when the CTs are connected in delta (CTCON = D).
VA, VB, VC	Primary voltage of the PT specified in the VREF*k* setting (A-Phase as reference). The PTRV and PTRZ settings are entered in an adjusted fashion when Low-Energy Analog (LEA) inputs are present, as described in *Potential Transformer (PT) Ratio Settings With LEA Inputs on page 5.2*. If LEA inputs are in use, the actual primary to secondary ratio of the voltage divider must be scaled down before entry as the PTRV or PTRZ setting.
V1, 3V2, 3V0	Positive-, negative-, and zero-sequence components of the PT specified in the VREF*k* setting. 3V0 is not available when the PTs are connected in delta (PTCON = D).
PA, PB, PC, 3P	A-Phase, B-Phase, C-Phase, and three-phase active (real) power for Winding *w*. Only three-phase real power is available when either CTs or PTs (or both) are delta-connected. Not calculated if setting VREF*k* does not include a reference PT and/or setting EPCAL does not include the winding.
QA, QB, QC, 3Q	A-Phase, B-Phase, C-Phase, and three-phase reactive power for Winding *w*. Only three-phase reactive power is available when either CTs or PTs (or both) are delta-connected. Not calculated if setting VREF*k* does not include a reference PT and/or setting EPCAL does not include the winding.
SA, SB, SC, 3S	A-Phase, B-Phase, C-Phase, and three-phase apparent power for Winding *w* Only three-phase power apparent is available when either CTs or PTs (or both) are delta-connected. Not calculated if setting VREF*k* does not include the winding and/or setting EPCAL does not include the winding.
Power factor	A-Phase, B-Phase, C-Phase, and three-phase power factor for Winding *w* Not calculated if setting VREF*k* does not include a reference PT and/or setting EPCAL does not include the winding.
VAB, VBC, CA	AB, BC, and CA line-to-line voltages for PT V
VAB, VBC, CA	AB, BC, and CA line-to-line voltages for PT Z
Frequency	Measured system frequency
Frequency Tracking	When the relay tracks the frequency, the report display "Y", and "N" when the relay does not track the frequency.
Battery Voltage	Measured battery voltage
Volts/Hertz	Percentage V/Hz

Enable current, voltage, and power meter quantities with the following settings:

➤ Current: include the Winding(s) in the ECTTERM Group setting

➤ Voltage: include the PT in the EPTTERM Group setting

➤ Power (fundamental power only):

➢ In addition to being included in the EPTTERM setting, also
select the reference PT for each winding (VREF*k*) setting.
Table 7.4 summarizes the settings for Winding S and PT V.

➢ Include Winding S in the EPCAL setting

Table 7.4 Report Settings Summary

I in Report	V in Report	S, P, Q in Report
ECTTERM = S	EPTTERM = V	VREFS = V, EPCAL = S

Figure 7.1 shows the report with the following settings:

➤ ECTTERM: includes S (ECTTERM = S,…)

➤ EPTTERM: does not includes V or Z (EPTTERM = OFF)

➤ VREFS: no reference voltage specified (VREFS = OFF)

➤ EPCAL = OFF

➤ E24 = N

With these settings, the report shows only the current values for Winding S.
Notice that there is no indication of the reference PT in the `Phase Voltages - PT -`
heading (VREFS = OFF). Also, the A-Phase current is the reference because
there is no PT available.

```
=>>MET <Enter>

Relay 1                                      Date: 04/20/2008  Time: 02:03:30.014
Station A                                    Serial Number: 2008030645

Fundamental Meter: Winding S

              Phase Currents                    Sequence Currents
          IA        IB        IC           I1         3I2        3I0
MAG(A,pri) 219.26    219.47    219.96       219.55      1.52       1.92
ANG(deg)    -0.13   -120.14    120.28         0.00    -51.86    -170.31

              Phase Voltages - PT -             Sequence Voltages
          VA        VB        VC           V1         3V2        3V0
MAG (kV)  -------   -------   -------      -------    -------    -------
ANG(deg)  ------    ------    ------       ------     ------     ------

Power Quantities
Active Power P (MW,pri)
    PA        PB        PC        3P
------    ------    ------    ------

Reactive Power Q (MVAr,pri)
    QA        QB        QC        3Q
------    ------    ------    ------

Apparent Power  S (MVA,pri)
    SA        SB        SC        3S
------    ------    ------    ------

Power factor
 Phase A    Phase B    Phase C    3-Phase
 ----       ----       ----       ----

Line-to-Line Voltage
           PT - V                         PT - Z
          VAB       VBC       VCA         VAB       VBC       VCA
MAG (kV)  -------   -------   -------     -------   -------   -------
ANG(deg)  ------    ------    ------      ------    ------    ------

FREQ (Hz) 59.991         Frequency Tracking = Y
VDC (V)   115.81         V/Hz     -----%

=>>
```

Figure 7.1   Fundamental Quantities Report With VREFS = OFF and EPTTERM = OFF

In the report shown in *Figure 7.1*, the EPTTERM includes both V and Z PTs, but
PT Z is connected to a dead busbar.

Figure 7.2 shows the report with the following settings:

➤ ECTTERM: includes S (ECTTERM = S,....)

➤ EPTTERM: includes both V or Z (EPTTERM = V, Z), but PT Z is de-energized

➤ VREFS: no reference voltage specified (VREFS = OFF)

➤ EPCAL = OFF

➤ E24 = N

With these settings, Winding S current is available, as well as the two PTs. Although there is no reference voltage selected (VREFS = OFF), the phase currents are referenced to the A-Phase of PT V.

```
=>>MET <Enter>

Relay 1                                  Date: 04/20/2008  Time: 02:08:46.920
Station A                                Serial Number: 2008030645



Fundamental Meter: Winding S

              Phase Currents                 Sequence Currents
          IA      IB       IC          I1       3I2       3I0
MAG(A,pri)  219.81  219.28   219.23      219.44      1.20      1.39
ANG(deg)   -16.17  -135.86   104.10      -15.97    -85.85    -76.74

              Phase Voltages - PT -          Sequence Voltages
          VA      VB       VC          V1       3V2       3V0
MAG (kV)  ------- -------  -------     ------- -------   -------
ANG(deg)  ------  ------   ------      ------   ------    ------

Power Quantities
Active Power P (MW,pri)
    PA        PB        PC        3P
------    ------    ------    ------

Reactive Power Q (MVAr,pri)
    QA        QB        QC        3Q
------    ------    ------    ------

Apparent Power  S (MVA,pri)
    SA        SB        SC        3S
------    ------    ------    ------

Power factor
 Phase A    Phase B    Phase C    3-Phase
 ----        ----        ----        ----

Line-to-Line Voltage
          PT - V                      PT - Z
          VAB     VBC      VCA          VAB      VBC       VCA
MAG (kV)  217.888 217.704  218.330      0.005    0.007     0.005
ANG(deg)  29.89   -89.93   150.02      -166.32   61.99    -75.31

FREQ (Hz) 59.991            Frequency Tracking = Y
VDC (V)   115.82            V/Hz      -----%

=>>
```

Figure 7.2 Fundamental Quantities Report With VREFS = OFF and EPTTERM = V, Z

In the report shown in *Figure 7.3*, the EPTTERM includes both V and Z PTs (PT Z is hot), and the VREFS setting include Winding S. The Phase Voltages heading now indicates the reference PT (V), and the voltage values are shown. Because EPCAL = OFF there are no power values shown in the report.

Figure 7.3 shows the report with the following settings:

- ➤ ECTTERM: includes S (ECTTERM = S,…)
- ➤ EPTTERM: includes both V or Z (EPTTERM = V, Z)
- ➤ VREFS: PT V as reference voltage (VREFS = S…)
- ➤ EPCAL = OFF
- ➤ E24 = Y

```
=>>MET S <Enter>

Relay 1                                    Date: 04/20/2008  Time: 02:23:31.610
Station A                                  Serial Number: 2008030645



Fundamental Meter: Winding S

              Phase Currents                     Sequence Currents
          IA        IB        IC          I1        3I2        3I0
MAG(A,pri) 219.56    219.68    219.24      219.49      0.96       1.60
ANG(deg)   -16.16   -135.90    104.21      -15.95    -77.23    -117.62

              Phase Voltages - PT V              Sequence Voltages
          VA        VB        VC          V1        3V2        3V0
MAG (kV)  125.839   125.873   125.853     125.854    0.647      0.710
ANG(deg)   -0.14   -120.06    120.21       0.00     -41.95    -138.62

Power Quantities
Active Power P (MW,pri)
    PA        PB        PC        3P
------    ------    ------    ------

Reactive Power Q (MVAr,pri)
    QA        QB        QC        3Q
------    ------    ------    ------

Apparent Power  S (MVA,pri)
    SA        SB        SC        3S
------    ------    ------    ------

Power factor
 Phase A    Phase B    Phase C    3-Phase
 ----       ----       ----       ----

Line-to-Line Voltage
                PT - V                          PT - Z
          VAB       VBC       VCA          VAB       VBC       VCA
MAG (kV)  217.911   217.710   218.363      130.809   130.743   130.966
ANG(deg)   29.90    -89.93    150.03        29.96    -89.95    150.03

FREQ (Hz) 59.992           Frequency Tracking = Y
VDC (V)   115.81           V/Hz       99.87%

=>>
```

Figure 7.3 Fundamental Quantities With EPCAL = OFF

In the report shown in *Figure 7.4*, the EPTTERM includes both V and Z PTs, and the EPCAL setting include Winding S.

Figure 7.4 shows the report with the following settings:

- ➤ ECTTERM: includes S (ECTTERM = S,…)
- ➤ EPTTERM: includes both V or Z (EPTTERM = V, Z)
- ➤ VREFS: PT V as reference voltage (VREFS = V….)
- ➤ EPCAL: includes Winding S (EPCAL = S….)
- ➤ E24 = Y

With these settings, all functions are enabled and all values are shown.

```
=>>MET <Enter>

Relay 1                                      Date: 04/20/2008  Time: 05:28:37.595
Station A                                    Serial Number: 2008030645

Fundamental Meter: Winding S

             Phase Currents                    Sequence Currents
          IA       IB       IC            I1        3I2       3I0
MAG(A,pri) 219.78   219.58   219.29        219.54     1.19      1.37
ANG(deg)   -16.15   -135.94  104.22        -15.96    -59.31   -112.78

             Phase Voltages - PT V             Sequence Voltages
          VA       VB       VC            V1        3V2       3V0
MAG (kV)  125.845  125.866  125.852       125.854    0.662     0.703
ANG(deg)   -0.14   -120.07  120.21          0.00    -41.11   -139.10

Power Quantities
Active Power P (MW,pri)
     PA        PB        PC        3P
    26.58     26.58     26.53     79.70

Reactive Power Q (MVAr,pri)
     QA        QB        QC        3Q
     7.63      7.56      7.60     22.79

Apparent Power  S (MVA,pri)
     SA        SB        SC        3S
    27.66     27.64     27.60     82.89

Power factor
Phase A    Phase B    Phase C    3-Phase
 0.96 Lag   0.96 Lag   0.96 Lag   0.96 Lag

Line-to-Line Voltage
                PT - V                         PT - Z
          VAB      VBC      VCA           VAB      VBC      VCA
MAG (kV)  217.912  217.694  218.347       130.807  130.728  130.953
ANG(deg)   29.90   -89.93   150.03         29.96   -89.95   150.03

FREQ (Hz) 59.991           Frequency Tracking = Y
VDC (V)   115.21           V/Hz      99.01%

=>>
```

Figure 7.4   Fundamental Quantities Report

Power

Table 7.3 shows the power quantities that the relay measures. The instantaneous power measurements are derived from 1-cycle averages that the SEL-487E reports by using the generator condition of the positive power flow convention; for example, real and reactive power flowing out (export) is positive, and real and reactive power flowing in (import) is negative (see *Table 7.5*). For power factor, LAG and LEAD refer to whether the current lags or leads the applied voltage. The reactive power Q is positive when the voltage angle is greater than the current angle ($\theta_V > \theta_I$), which is the case for inductive loads where the current lags the applied voltage. Conversely, Q is negative when the voltage angle is less than the current angle ($\theta_V < \theta_I$); this is when the current leads the voltage, as in the case of capacitive loads.
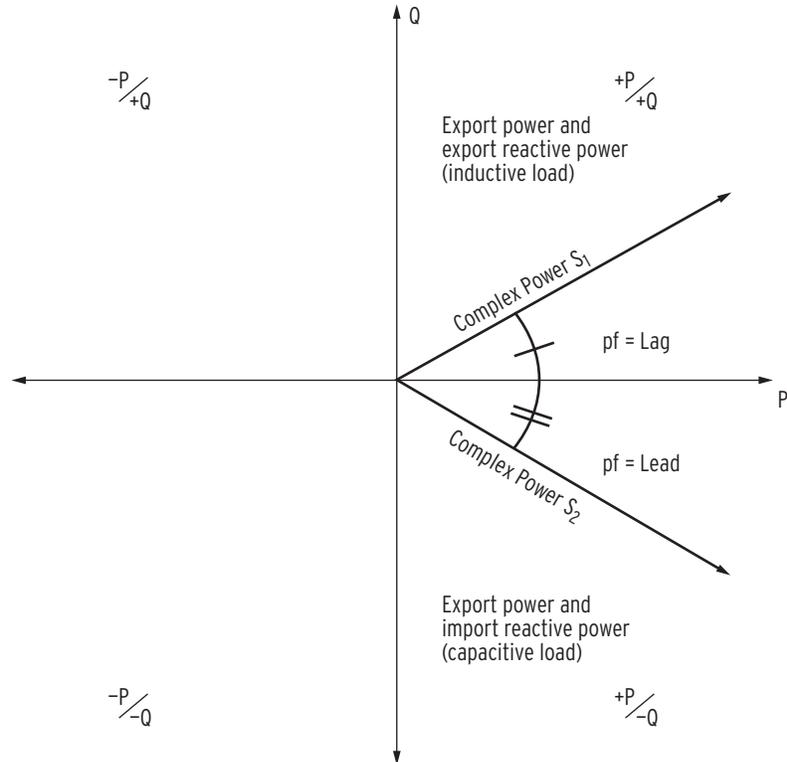
Figure 7.5   Complex Power (P/Q) Plane

The SEL-487E includes Relay Word bits to indicate the leading or lagging power factor (see *Section 11: Relay Word Bits*). In the case of a unity power factor or loss of phase or potential condition, the resulting power factor angle would be on this axis of the complex power (P/Q) plane shown in *Figure 7.5*. This would cause the power factor Relay Word bits to rapidly change state (chatter). Be aware of expected system conditions when monitoring the power factor Relay Word bits. It is not recommended to use chattering Relay Word bits in the SER or anything that will trigger an event.

RMS Meter

Use the **MET RMS *w*** command (*w* = S, T, U, W, X, ST, TU, UW, WX) to view the root-mean-square (rms) current and voltage values; the relay does not calculate rms power values. Setting conditions (EPCAL, VREFk, EPTTERM, and ECTTERM) are the same for rms metering as for fundamental metering. *Table 7.5* shows the quantities in the rms report.

Table 7.5   Quantities in the RMS Meter Report (Sheet 1 of 2)

Quantity	Description
IA, IB, IC	Winding *w* A-Phase, B-Phase, and C-Phase primary current. The reference is independent of the VREF*k* settings, and is determined as follows: 1. A-Phase of PT V (if available) 2. A-Phase of PT Z (if available, and PT V is not available) 3. A-Phase of Winding *w* current (if no PTs are available)
VA, VB, VC	Primary voltage of the PT specified in the VREF*k* setting (A-Phase as reference)
VAB, VBC, CA	Primary voltage AB, BC, and CA line-to-line voltages for PT V

Table 7.5   Quantities in the RMS Meter Report (Sheet 2 of 2)

Quantity	Description
VAB, VBC, CA	Primary voltage AB, BC, and CA line-to-line voltages for PT Z
Frequency	Measured system frequency
Frequency Tracking	When the relay tracks the frequency, the report display "Y", and "N" when the relay does not track the frequency
Battery Voltage	Measured battery voltage
Volts/Hertz	Percentage V/Hz

Figure 7.6 shows an rms report for Winding S; other windings have similar reports.

```
=>>MET RMS <Enter>

Relay 1                                 Date: 04/20/2008  Time: 06:21:32.214
Station A                               Serial Number: 2008030645

        RMS Meter: Winding S

Phase Currents, I (A,pri)
IA        IB        IC
 219.73    218.97    219.79

Phase Voltages (kV,pri)  - PT V
VA        VB        VC
125.841   125.847   125.855

Line-to-Line Voltage V (kV,pri)
PT - V                          PT - Z
VAB       VBC       VCA         VAB       VBC       VCA
217.889   217.696   218.336     130.796   130.731   130.945

FREQ (Hz) 59.991           Frequency Tracking = Y
VDC (V)   115.81           V/Hz     99.78%

=>>
```

Figure 7.6   RMS Report for Winding S

Secondary Meter

Use the **MET SEC** command to see the secondary fundamental current and voltage values. Setting conditions (EPCAL, VREF*k*, EPTTER, and ECTTERM) are the same for rms metering as for fundamental metering. *Figure 7.7* shows the report for Winding T; other windings have similar reports. *Table 7.6* shows the quantities in the secondary quantities report.

Table 7.6   Quantities in the MET SEC Report (Sheet 1 of 2)

Quantity	Description

IA, IB, IC	Winding *w* A-Phase, B-Phase, and C-Phase in secondary current. The reference is independent of the VREF*k* settings, and is determined as follows:
	
	    1. A-Phase of PT V (if available)
	    2. A-Phase of PT Z (if available, and PT V is not available)
	    3. A-Phase of Winding *w* current (if no PTs are available)

VA, VB, VC	Secondary voltage of the PT specified in the VREF*k* setting (A-phase as reference)
VAB, VBC, CA	Secondary voltage AB, BC, and CA line-to-line voltages for PT V
VAB, VBC, CA	Secondary voltage AB, BC, and CA line-to-line voltages for PT Z
Frequency	Measured system frequency
Frequency Tracking	When the relay tracks the frequency, the report display "Y", and "N" when the relay does not track the frequency.

Table 7.6   Quantities in the MET SEC Report (Sheet 2 of 2)

Quantity	Description
Battery Voltage	Measured battery voltage
Volts/Hertz	Percentage V/Hz

```
=>>MET SEC T <Enter>

Relay 1                                Date: 04/20/2008  Time: 06:47:23.494
Station A                              Serial Number: 2008030645

  Secondary Meter: Winding T

             Phase Currents                  Sequence Currents
          IA        IB        IC          I1        3I2        3I0
MAG(A,sec)  4.37      4.37      4.36        4.37       0.01       0.01
ANG(deg)  164.23     44.32    -75.60      164.32     118.41      63.71

             Phase Voltages - PT V           Sequence Voltages
          VA        VB        VC          V1        3V2        3V0
MAG(V,sec) 62.922    62.937    62.924      62.928      0.324      0.353
ANG(deg)   -0.13   -120.07    120.19        0.00     -40.24    -138.95

Line-to-Line Voltage
                 PT - V                          PT - Z
          VAB       VBC       VCA         VAB       VBC        VCA
Mag(V,sec) 108.962   108.850   109.171     109.014   108.946    109.126
ANG(deg)    29.89    -89.94    150.03       29.95    -89.95     150.03

FREQ (Hz) 59.991           Frequency Tracking = Y
VDC (V)   115.81           V/Hz      99.56%

=>>
```

Figure 7.7   MET SEC Report for Winding T

Demand Meter

Figure 7.8 shows the Demand report with four of the available ten elements enabled (see *Thermal Demand and Rolling Demand on page 7.6 in the SEL-400 Series Relays Instruction Manual* for more information). *Table 7.7* shows the quantities in the demand metering report. See *Table 7.8* for a list of quantities that may be included in the demand metering report. See *Section 7: Metering in the SEL-400 Series Relays Instruction Manual* for a complete description of how demand metering works.

Table 7.7   Quantities in the Demand Metering Report

Quantity	Description
DM01–DM04	Four of the available ten elements (DM01–DM10 available)
Op_Qty	Displays the analog quantities selected for each enabled element (see *Table 7.8* for a list of available analog quantities)
Type	Displays the selected type (rolling demand or thermal) of demand meter for each element (see *Thermal Demand and Rolling Demand on page 7.6 in the SEL-400 Series Relays Instruction Manual* for more information)
Demand	Displays the accumulated demand and the time and date of the recording
Peak	Displays the peak demand and the time and date of the recording

Table 7.8   Demand Metering Operating Quantities (Sheet 1 of 2)

Analog Quantity	Description
IϕmRS[a, b]	1-second average rms current ϕ phase, Terminal m
IϕqpRS[b, c]	1-second average rms current f phase, combined Terminal qp
IMXmRS[a]	1-second average rms maximum phase current, Terminal m

Table 7.8   Demand Metering Operating Quantities (Sheet 2 of 2)

Analog Quantity	Description
IMXqpRS[c]	1-second average rms maximum phase current, combined Terminal qp
3I2mMS[a]	1-second average negative-sequence current angle, Terminal m
3I0mMS[a]	1-second average zero-sequence current angle, Terminal m
3I2qpMS[c]	1-second average negative-sequence current, combined Terminals qp
3I0qpMS[c]	1-second average zero-sequence current, combined Terminals qp

[a] m = S, T, U, W, X.

[b] ϕ = A, B, C.

[c] qp = ST, TU, UW, WX.

```
=>>MET D <Enter>

Relay 1                                  Date: 04/20/2008  Time: 20:30:08.674
Station A                                Serial Number: 2008030645

        Op_Qty     Type    Demand     Peak    Date       Time

DM01    IMXSRS     THERM    1.864     2.580 04/18/2008 23:17:10.635
DM02    IMXTRS     ROLL     2.184     2.184 04/20/2008 20:29:14.898
DM03    IMXURS     THERM    0.004     7.664 01/02/1792 03:32:27.834
DM04    IMXXRS     THERM    3.243     3.243 04/20/2008 20:30:08.536

LAST DEMAND RESET: 04/20/2008 20:24:14.615
LAST MAX DEMAND RESET: 04/15/2008 22:51:50.456

=>>
```

Figure 7.8   Demand Report With Four Elements Enabled

Synchrophasor Meter

Use the **MET PM** command to display the synchrophasor values, as shown in *Figure 7.9* (see *Synchrophasors on page 10.66* for more information).

```
=>>MET PM <Enter>

Relay 1                               Date: 05/28/2008  Time: 12:29:09.000
Station A                             Serial Number: 0000000000

Time Quality   Maximum time synchronization error: >999.999 (ms)  TSOK = 0

Synchrophasors
                    VV Phase Voltages          Pos. Sequence Voltage
               VA       VB       VC                  V1
MAG (kV)       0.003    0.007    0.010               0.005
ANG (DEG)    -84.721  147.645  125.695             -42.686

                    VZ Phase Voltages          Pos. Sequence Voltage
               VA       VB       VC                  V1
MAG (kV)       0.000    0.000    0.000               0.000
ANG (DEG)      0.000    0.000    0.000               0.000

                    IS Phase Currents          IS Pos. Sequence Current
               IA       IB       IC                  I1S
MAG (A)        0.178    0.371    0.462               0.042
ANG (DEG)    150.260  116.837  136.352             -47.019

                    IT Phase Currents          IT Pos. Sequence Current
               IA       IB       IC                  I1T
MAG (A)        0.000    0.000    0.000               0.000
ANG (DEG)      0.000    0.000    0.000               0.000

                    IU Phase Currents          IU Pos. Sequence Current
               IA       IB       IC                  I1U
MAG (A)        0.000    0.000    0.000               0.000
ANG (DEG)      0.000    0.000    0.000               0.000

                    IW Phase Currents          IW Pos. Sequence Current
               IA       IB       IC                  I1W
MAG (A)        0.000    0.000    0.000               0.000
ANG (DEG)      0.000    0.000    0.000               0.000

                    IX Phase Currents          IX Pos. Sequence Current
               IA       IB       IC                  I1X
MAG (A)        0.000    0.000    0.000               0.000
ANG (DEG)      0.000    0.000    0.000               0.000

                    IY Phase Currents          IY Pos. Sequence Current
               IA       IB       IC                  I1X
MAG (A)        0.000    0.000    0.000               0.000
ANG (DEG)    0.000    0.000    0.000             0.000

FREQ (Hz) 60.000        Frequency Tracking = N
Rate-of-change of FREQ (Hz/s)    0.00

Digitals

PSV08  PSV07  PSV06  PSV05  PSV04  PSV03  PSV02  PSV01
  0      0      0      0      0      0      0      0
PSV16  PSV15  PSV14  PSV13  PSV12  PSV11  PSV10  PSV09
  0      0      0      0      0      0      0      0
PSV24  PSV23  PSV22  PSV21  PSV20  PSV19  PSV18  PSV17
  0      0      0      0      0      0      0      0
PSV32  PSV31  PSV30  PSV29  PSV28  PSV27  PSV26  PSV25
  0      0      0      0      0      0      0      0
PSV40  PSV39  PSV38  PSV37  PSV36  PSV35  PSV34  PSV33
  0      0      0      0      0      0      0      0
PSV48  PSV47  PSV46  PSV45  PSV44  PSV43  PSV42  PSV41
  0      0      0      0      0      0      0      0
PSV56  PSV55  PSV54  PSV53  PSV52  PSV51  PSV50  PSV49
  0      0      0      0      0      0      0      0
PSV64  PSV63  PSV62  PSV61  PSV60  PSV59  PSV58  PSV57
  0      0      0      0      0      0      0      0

Analogs

PMV49      0.000  PMV50      0.000  PMV51      0.000  PMV52      0.000
PMV53      0.000  PMV54      0.000  PMV55      0.000  PMV56      0.000
PMV57      0.000  PMV58      0.000  PMV59      0.000  PMV60      0.000
PMV61      0.000  PMV62      0.000  PMV63      0.000  PMV64      0.000

=>>
```

Figure 7.9   Synchrophasor Report

Differential Meter

Use the **MET DIF** command to see the differential operate, restraint and percentage harmonic values. *Table 7.9* summarizes the quantities in the differential report, and *Figure 7.10* shows the differential element report.

Table 7.9   Quantities in the MET SEC Report

Quantity	Description
IOPA, IOPB, IOPC	Per-unit operating current for Differential Element A, Differential Element B, and Differential Element C
IRTA, IRTB, IRTC	Per-unit restraint current for Differential Element A, Differential Element B, and Differential Element C
IOPAF2, IOPBF2, IOPCF2	Second-harmonic currents, expressed as a percentage of the operating current.
IOPAF4, IOPBF4, IOPCF4	Fourth-harmonic currents, expressed as a percentage of the operating current.
IOPAF5, IOPBF5, IOPCF5	Fifth-harmonic currents, expressed as a percentage of the operating current.
Enabled Windings	Displays the windings included in the differential calculations (based on the E87T setting)

```
=>>MET DIF <Enter>

Relay 1                              Date: 04/12/2008  Time: 06:06:31.366
Station A                            Serial Number: 2008030645


Operate Currents (per unit)       Restraint Currents (per unit)
IOPA      IOPB      IOPC          IRTA      IRTB      IRTC
 1.32      1.32      1.32          3.91      3.91      3.91

2nd Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF2    IOPBF2    IOPCF2
 0.08      0.09      0.01

4th Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF4    IOPBF4    IOPCF4
 0.05      0.10      0.06

5th Harmonic Currents (percentage of IOPA, IOPB, IOPC)
IOPAF5    IOPBF5    IOPCF5
 0.06      0.11      0.04

Enabled Windings:  S, T


=>>
```

Figure 7.10   Differential-Element Report

Circuit Breaker Monitor

The SEL-487E features advanced circuit breaker monitoring. The general features of the circuit breaker monitor are described in *Section 8: Monitoring in the SEL-400 Series Relays Instruction Manual*. The SEL-487E supports monitoring five three-pole breakers, designated S, T, U, W, and X.

Station DC Battery System Monitor

The SEL-487E automatically monitors one station battery system health by measuring the dc voltage, ac ripple, and voltage between each battery terminal and ground. See *Section 8: Monitoring in the SEL-400 Series Relays Instruction Manual* for a complete description of the battery monitor.

Thermal Monitor

The SEL-487E provides a thermal element based on IEEE Std C57.91-1995, IEEE Guide for Loading Mineral-Oil-Immersed Transformers. Use this element to activate a control action or issue a warning or alarm when your transformer overheats or is in danger of excessive insulation aging or loss of life. Capture current hourly or daily data about your transformer using the thermal event report. The data acquisition interval is one minute, which constitutes the maximum element timing error. This very short time interval makes the element suitable for both thermal protection and control functions.

Operating Characteristic

The SEL-487E thermal element compares top-oil, Θ_{TO}, and winding hot-spot, Θ_H, temperatures against thresholds beyond which a Relay Word bit asserts. You can use these bits to alarm for overheating of the transformer. Top-oil temperature is a calculation of the transformer oil temperature, while hot-spot temperature is a calculation of the hottest point on the transformer winding. The thermal element uses top-oil temperature and hot-spot temperature to calculate the insulation aging acceleration factor, FAA, daily rate of loss of life, RLOL, and total loss of life, TLOL. For each of these quantities you can set a threshold beyond which a Relay Word bit will assert.

The thermal element operates in one of three modes, depending upon the presence or lack of measured temperature inputs:

➤ Measured ambient and top-oil temperature inputs

➤ Measured ambient temperature only

➤ No measured temperature inputs

If the relay receives measured ambient and top-oil temperatures, the thermal element calculates hot-spot temperature (*Figure 7.11(a)*). When the relay receives a measured ambient temperature but not a measured top-oil temperature, the thermal element calculates the top-oil temperature and hot-spot temperature (*Figure 7.11(b)*). In the absence of any measured ambient or top-oil temperatures, the thermal element uses a default ambient temperature setting (D_AMB) that you select and calculates the top-oil and hot-spot temperatures (*Figure 7.11(c)*). Regardless of the available measuring inputs, the relay always calculates the top-oil temperature for use in the cooling system efficiency element.

The SEL-487E is capable of supporting temperature inputs from 12 RTD inputs or from Remote Analog inputs received via IEC 61850 GOOSE messaging. The 12 RTD inputs will be obtained via an EIA-232 communications port connected to an SEL-2600. The Fast Message protocol will be used to transmit data from the SEL-2600 to the relay.

Θ_H = Calculated hot-spot temperature
using $\Delta\Theta_H$

Θ_{TO} = Measured top oil temperature

Θ_H = Calculated hot-spot temperature
using $\Delta\Theta_H$ and Θ_{TO}

Θ_{TO} = Calculated top oil temperature
using $\Delta\Theta_{TO}$

Θ_A = Measured ambient oil temperature

Θ_H = Calculated hot-spot temperature
using $\Delta\Theta_H$ and Θ_{TO}

Θ_{TO} = Calculated top oil temperature
using $\Delta\Theta_{TO}$

Θ_A = From D_AMB setting
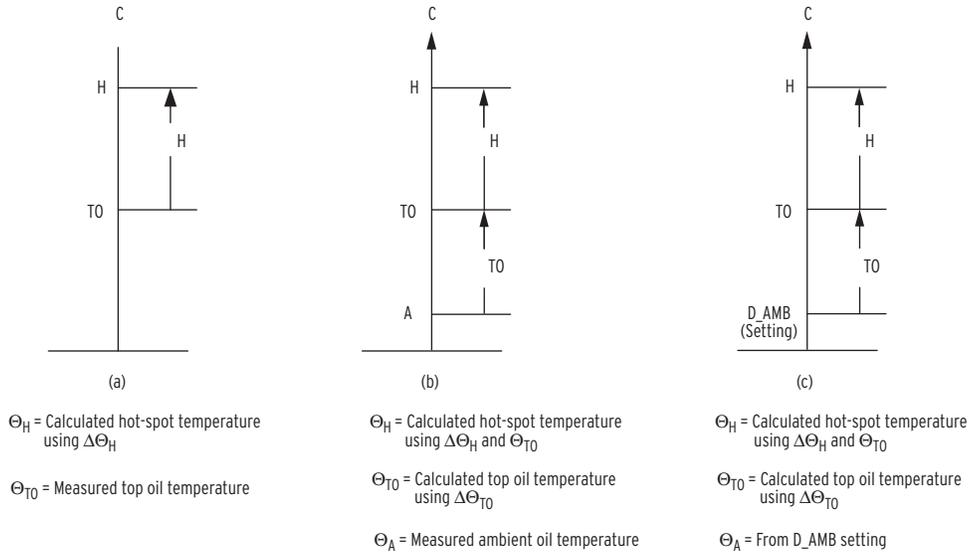
Figure 7.11   Top-Oil and Hot-Spot Temperatures

Thermal Element
Thermal Element With Ambient and Top-Oil Temperature Inputs

In this case the relay receives measured ambient and top-oil temperature inputs and uses the top-oil temperature to calculate the hot-spot temperature. Because the ambient temperature is available, the thermal event reports show the ambient temperature. For a single tank, three-phase transformer, there are as many as two thermal inputs: the ambient temperature input and the top-oil input. For independent, single-phase transformers, there normally are as many as four thermal inputs: one ambient temperature input and a top-oil input for each of the three tanks. During a fixed time interval, $\Delta t = 1$ minute, the relay calculates the winding hot-spot temperature at the end of the interval, according to *Equation 7.1*.

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

Equation 7.1

where:

Θ_H = winding hot-spot temperature, °C

Θ_{TO} = top-oil temperature, °C

$\Delta\Theta_H$ = winding hot-spot rise over top-oil temperature, °C

The relay calculates winding hot-spot rise over top-oil temperature, $\Delta\Theta_H$, according to *Equation 7.2*:

$$\Delta\Theta_H = (\Delta\Theta_{H,U} - \Delta\Theta_{H,i}) \bullet \left(1 - e^{\frac{-\Delta t}{60 \bullet THS}} \right) + \Delta\Theta_{H,i} \, °C$$

Equation 7.2

where:

$\Delta\Theta_{H,U}$ = the ultimate hot-spot rise over top-oil temperature for any load, °C

$\Delta\Theta_{H,i}$ = initial hot-spot rise over top-oil temperature at the start time of the interval, °C

THS = thermal time constant of hot spot, in hours (set from *Table 7.10*)

Δt = one-minute temperature data acquisition interval

$$\Delta\Theta_{H,U} = K^2 \cdot EXPM \cdot THGR \, °C$$

Equation 7.3

where:

K = load expressed in per unit of transformer nameplate rating according to the cooling system in service (phase rms current divided by the nominal current)

EXPM = winding exponent (set from *Table 7.10*)

THGR = rated winding hot-spot rise over top-oil at rated load, °C (set from *Table 7.10*)

Table 7.10   Default Transformer Constants

IEEE	Setting	THWR = 55°			THWR = 65°		
		NUMCS = 1	NUMCS = 2	NUMCS = 3	NUMCS = 1	NUMCS = 2	NUMCS = 3
$\Delta\Theta_{TO,R}$	THOR (°C)	45°	40°	37°	55°	50°	45°
$\Delta\Theta_{H,R}$	THGR (°C)	20°	25°	28°	25°	30°	35°
R	RATL	3.0	3.5	5.0	3.2	4.5	6.5
n	EXPN	0.8	0.9	1.0	0.8	0.9	1.0
$\tau_{TO,R}$	OTR	3.0	2.0	1.25	3.0	2.0	1.25
m	EXPM	0.8	0.8	1.0	0.8	0.8	1.0
τ_H	THS	0.08					

Thermal Element With Ambient Temperature Input Only

In this case the relay receives a measured ambient temperature input and uses this input to calculate top-oil and hot-spot temperatures.

Where the relay has a measured ambient temperature input without a top-oil temperature input, you have one thermal input (for ambient temperature) regardless of whether you have a single three-phase transformer or independent single-phase transformers. The relay calculates winding hot-spot temperature, Θ_H, according to *Equation 7.1*.

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

Equation 7.4

and calculates top-oil temperature, Θ_{TO}, according to *Equation 7.5*:

$$\Theta_{TO} = \Theta_A + \Delta\Theta_{TO}$$

Equation 7.5

where:

Θ_A = ambient temperature, °C

$\Delta\Theta_{TO}$ = top-oil rise over ambient temperature, °C

The relay calculates top-oil rise over ambient temperature according to *Equation 7.6*:

$$\Delta\Theta_{TO} := (\Delta\Theta_{TO,U} - \Delta\Theta_{TO,i}) \bullet \left(1 - e^{\frac{-\Delta T}{60 \bullet T_o}}\right) + \Delta\Theta_{TO,i} {}^{\circ}C$$

<div align="right">**Equation 7.6**</div>

where:

$\Delta\Theta_{TO,U} =$ the ultimate top-oil rise over ambient temperature for any load, °C, and is a function of load and the values in *Table 7.10*

$\Delta\Theta_{TO,i} =$ initial top-oil rise over ambient temperature at the start time of the interval, °C ($\Delta\Theta_{TO,i}$)

$T_o =$ thermal top-oil time constant of transformer, in hours

$$T_o := OTR \bullet \left[\frac{\dfrac{\Delta\Theta_{TO,U}}{THOR} - \dfrac{\Delta\Theta_{TO,i}}{THOR}}{\left(\dfrac{\Delta\Theta_{TO,U}}{THOR}\right)^{\frac{1}{EXPN}} - \left(\dfrac{\Delta\Theta_{TO,i}}{THOR}\right)^{\frac{1}{EXPN}}} \right]$$

<div align="right">**Equation 7.7**</div>

where:

$OTR =$ thermal time constant in hours at rated load with initial top-oil temperature equal to ambient temperature (set from *Table 7.10*)

$THOR =$ top-oil rise over ambient temperature at rated load, °C (set from *Table 7.10*)

$EXPN =$ oil exponent (set from *Table 7.10*)

The relay calculates the ultimate top-oil rise over ambient temperature, $\Delta\Theta_{TO,U}$, according to *Equation 7.8*:

$$\Delta\Theta_{TO,U} = \left(\frac{(K^2 \bullet RATL + 1)}{(RATL + 1)}\right)^{EXPN} \bullet THOR {}^{\circ}C$$

<div align="right">**Equation 7.8**</div>

where:

$RATL =$ ratio of load loss at rated load to no-load loss (set from *Table 7.10*)

Thermal Element With No Measured Temperature Inputs

In this case, the relay uses a default ambient temperature value (D_AMB setting) that you select and calculates a hot-spot temperature and top-oil temperature. The relay calculates hot-spot temperature according to *Equation 7.9*:

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

<div align="right">**Equation 7.9**</div>

and the top-oil temperature according to *Equation 7.10*:

$$\Theta_{TO} = \Theta_A + \Delta\Theta_{TO}$$

<div align="right">**Equation 7.10**</div>

The relay has no measured ambient temperature input, so you must select an ambient temperature setting (D_AMB) for the thermal element calculation of top-oil temperature as shown in *Equation 7.11*:

$$\Theta_{TO} = D\_AMB + \Delta\Theta_{TO}$$

<div align="right">**Equation 7.11**</div>

where:

$D\_AMB =$ user-selectable default ambient temperature

Top-Oil Temperature Comparison to Indicate Cooling System Efficiency

Figure 7.12 shows the logic the relay uses to calculate the difference between the measured top-oil temperature and the calculated top-oil temperature for Transformer 1. If all probes are in order and all coefficients have been correctly chosen, you can use the element to verify the integrity of both the cooling system and the measuring devices.

Relay Word bits CSE_x (x = 1, 2, or 3) asserts when the measured top-oil temperature is greater than the calculated top-oil temperature, indicating that the cooling system (fans and/or pumps) operates below the expected efficiency.

Conversely, when the measured top-oil temperature is lower than the calculated top-oil temperature, then Relay Word bits CSCM_x assert, indicating wrong RTD probe selection or incorrect cooling coefficients settings.

Relay Word bit CSCM is the OR combination of the CSCM_x Relay Word bits, and Relay Word bit CSE is the OR combination of the CSE_x Relay Word bits.
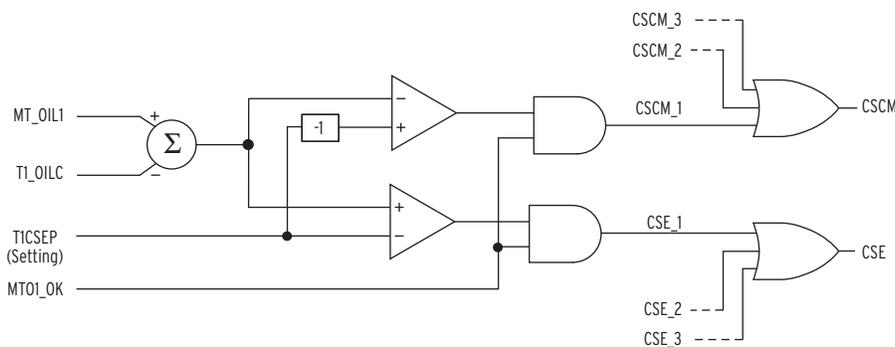
Figure 7.12   Cooling System Efficiency Logic

where:[a]

$TxCSEP =$ Cooling System Efficiency Pickup setting, °C
$MT\_OILx =$ measured oil temperature
$Tx\_OILC =$ calculated oil temperature
$MT0x\_OK =$ RTD assigned to the top-oil measurement is healthy

[a] x = 1 if TRTYPE = 1; x = 1, 2, 3 if TRTYPE = 3.

SEL-2600 Status Monitoring

The SEL-2600 message contains 2 bytes of data that report the status of the SEL-2600. One status bit reports a power supply failure, and a second bit reports a ram failure within the SEL-2600. The relay decodes the status information from the data package and asserts Relay Word bit RTDFL when either failure occurs. If the relay does not receive data from the SEL-2600 for 1.25 seconds, the relay asserts the communications failure Relay Word bit RTDCOMF. If either of these two Relay Word bits assert, the relay deasserts all RTD*mm*OK Relay Word bits.

Insulation Loss of Life
Insulation Aging Acceleration Factor

The relay thermal element uses the hot-spot temperature to calculate an insulation aging acceleration factor, FAA, which indicates how fast the transformer insulation is aging. The relay calculates the insulation aging acceleration factor, FAA, for each time interval, Δt, as shown in *Equation 7.12*:

$$\text{FAA} := e^{\left(\frac{\text{BFFA}}{\Theta_{H,R} + 273} - \frac{\text{BFFA}}{\Theta_{H} + 273} \right)}$$

Equation 7.12

where:

$\quad$ FAA = insulation aging acceleration factor

$\quad$ BFFA = a design constant, typically 15000 (set from *Table 7.10*)

$\quad \Theta_{H,R}$ = winding hot-spot temperature at rated load
$\qquad$ (95°C if THWR = 55°C, 110°C if THWR = 65°C)

$\quad$ THWR = average winding rise over ambient at rated load (setting)

Daily Rate of Loss of Life

The relay calculates daily rate of loss of life (RLOL, percent loss of life per day) for a 24-hour period as shown in *Equation 7.13*:

$$\text{RLOL} := \frac{\text{FEQA} \bullet 24}{\text{ILIFE}} \bullet 100$$

Equation 7.13

where:

$\quad$ RLOL = rate of loss of life in percent per day

$\quad$ ILIFE = expected normal insulation life in hours (set from *Table 7.10*)

The relay stores the RLOL value at midnight each day to provide the user with trend information on the loss of insulation life. *Equation 7.14* shows the equivalent life at the reference hot-spot temperature (95ºC or 110ºC) that will be consumed in a given time period for a given temperature cycle.

$$FEQA := \frac{\sum_{n=1}^{N} FAA_n \bullet \Delta t_n}{\sum_{n=1}^{N} \Delta t_n}$$

Equation 7.14

where:

$FEQA$ = equivalent insulation aging factor for a total time period

n = index of the time interval

N = total number of time intervals for the time period

FAA = insulation aging acceleration factor for the time interval, Δt_n

Δt = time interval (fixed at 1 minute)

$$N = \frac{24}{\left(\frac{\Delta t}{60}\right)} = \frac{1440}{\Delta t}$$

Equation 7.15

where:

Δt = time interval (fixed at 1 minute)

Because the time intervals and the total time period used in the thermal model will be constant, we can simplify the calculation of FEQA to the following:

$$FEQA := \frac{\sum_{n=1}^{N} FAA_n}{N}$$

Equation 7.16

Total Accumulated Loss of Life

The relay estimates the total accumulated loss of insulation life in percentage of normal insulation life by summing all of the daily RLOL values.

$$TLOL_d := (RLOL_d + TLOL_{d-1})$$

Equation 7.17

where:

$TLOL_d$ = total accumulated loss of life, TLOL

$RLOL_d$ = most recent daily calculation

$TLOL_{d-1}$ = previous TLOL

The relay stores the TLOL value at midnight each day. You can use the **THE P** command to load an initial value of TLOL into the relay.

Estimated Time to Assert TLL Alarm

Estimated time to assert TLL bit:

$$TTLt = \frac{TLOLL - TLOL}{RLOL} \bullet 24$$

Equation 7.18

where:

$$
\begin{aligned}
TLLt &= \text{estimated time to assert total loss-of-life alarm, in hours} \\
TLOLL &= \text{total loss-of-life limit setting} \\
TLOL &= \text{total accumulated loss of life, TLOL} \\
RLOL &= \text{most recent daily rate of loss-of-life calculation}
\end{aligned}
$$

Setting Descriptions

See *Monitor Settings on page 8.9* for the prompts and defaults for these settings.

Number of Transformers (TRTYPE)

A three-phase transformer can consist of one three-phase core and coil assembly in one physical enclosure or three physically separate single-phase transformers connected externally. Set TRTYPE to either 1 for a three-phase unit, or 3 for three single-phase units.

Transformer Winding Connections (TRWCON)

If the power transformer winding associated with the thermal element (see Transformer Winding Selection (*TRWSEL*)) is delta connected OR if the current transformers associated with this winding are delta connected, set TRWCON = D (delta). Set TRWCON = Y (wye) only if both the power transformer winding AND current transformers are wye-connected.

With TRWCON = Y, the relay uses the measured currents for each phase in the thermal element calculations. This means for three single-phase power transformers (TRTYPE = 3), the thermal element outputs may vary between phases because the phase currents may be different. With TRWCON = D, the relay selects the highest magnitude phase current and sets the other two phase currents to that value to force a balanced condition. In this case, the thermal element outputs for three single-phase transformers will be the same, assuming that each is operating at the same cooling stage and the thermal constants are set identically.

Transformer Winding Selection (TRWSEL)

The TRWSEL setting determines which power transformer winding corresponds with the measured currents the thermal element uses for calculations. The measured currents the thermal element uses must represent either the total current in or the total current out of the power transformer (not both). TRWSEL allows selection of Windings enabled with the ECTTERM setting (S, T, U, W, X, ST [two currents added together], TU, UW, or WX) to be the current for the thermal element calculations. Also see *Delta-Connected CTs on page 5.40*.

For a two-winding power transformer, current transformers located on either the high-voltage or low-voltage side would provide the correct current values. You can apply the thermal element on a three-, four- or five- winding power transformer, provided that the TRWSEL setting represents the total current in or out of the power transformer (not both).

Nominal Winding Voltage (TRWNOM)

Set TRWNOM to the rated line-to-line voltage for the winding you select in the TRWSEL setting. The relay uses TRWNOM and the power transformer MVA rating (see *Cooling Stage MVA Rating (MVAcCSb) on page 7.24*) to calculate rated current. The relay then divides measured current by the rated current to determine the per-unit load current, which the relay uses in thermal element calculations.

Enable Default Transformer (EDFTC)

By setting EDFTC = Y, the relay uses the default settings shown in *Table 7.10* for the thermal calculations. When using the default settings, the following settings become unavailable: T*c*THOR*b*, T*c*HGR*b*, T*c*RATL*b*, T*c*OTR*b*, T*c*EXPN*b*, T*c*EXPM*b*, and T*c*THS ($b = c = 1–3$).

Winding Temp/Ambient Temp (THWR)

Rated winding rise over ambient temperature is the difference in degrees Celsius of the winding temperature of a transformer above the ambient temperature. The actual winding temperature will be between the top-oil and hot-spot temperature.

Most power transformers manufactured in 1977 and later are rated for a 65°C rise over ambient. Power transformers manufactured prior to 1977 can be rated for a 55°C rise over ambient. Set THWR for either 55 or 65, based on the rating of the power transformer. This setting determines which set of default transformer constants from *Table 7.10* the relay will use if EDFTC = Y.

Number of Cooling Stages (NUMCS)

Power transformers generally have a self-cooled rating and one or two stages of forced cooling. Set NUMCS to the maximum number of cooling stages associated with the monitored power transformer.

Transformer De-Energized (TRDE)

Transformer heating consists of heating resulting from transformer losses and heating resulting from load. IEEE C57.91-1995 assumes the transformer is energized and calculates an increase in oil and winding temperatures resulting from transformer losses.

Relay Word TRDE provides the thermal element a way to distinguish between the de-energized (no magnetizing current flowing) and energized stages (magnetizing current flowing). To achieve this, wire, for example, a 52b (normally closed) circuit breaker auxiliary contact to input IN101 and enter the SELOGIC control equation TRDE = IN101. When IN101 asserts (circuit breaker main contacts open and the 52b auxiliary contacts closed), the thermal element considers the transformer de-energized (no magnetizing current flowing) and the ambient, top-oil, and hot-spot temperatures all have the same value.

Be sure to make up an "effective external contact" from one or more 52a or 52b contacts (from one or more breakers) indicating that all the "source" breakers are open. Failing to assign a properly configured digital input to TRDE causes the relay to consider the transformer as energized, and the top-oil and hot-spot temperatures will increase over the ambient temperature even when the power transformer is actually de-energized (in accordance with the IEEE model).

Default Ambient Temperature (D_AMB)

If the ambient temperature input is unavailable on relay power up, the thermal element calculates the required temperatures using the D_AMB setting. Therefore, select a reasonable value for D_AMB, even if your data acquisition system provides measurement of the ambient temperature (near the power transformer). If your data acquisition system cannot measure ambient temperature, then the thermal element calculations always use the D_AMB value. The D_AMB setting units are degrees Celsius.

Number of RTD Inputs From the SEL-2600 (RTDNUM)

This setting is under the Port Setting category, but is also included here for the sake of completeness. Connect the temperature devices (ambient and transformer temperatures) to an SEL-2600, and connect the SEL-2600 in turn to any one of the EIA-232 ports of the SEL-487E. The maximum number of thermal inputs is 12.

RTD Type (RTD*xx*TY)

These settings are under the Port Setting Category, but are also included here for the sake of completeness. Specify the type of RTD metal for each of the ($xx = 1$–12) RTD inputs.

Ambient Temperature Input (AMB_M)

Use this setting to assign one of the selected RTD or Remote Analog temperature inputs to the ambient temperature variable in the SEL-487E thermal model.

Top-Oil Temperature Input (T*a*_OILM)

Use this setting to assign the selected temperature input to the top-oil temperature variables ($a = 1$–3) in the SEL-487E thermal model.

Default Ambient Temperature if RTD Fails (AMBRTDF)

Since Remote Analog values could be coming from non-SEL devices monitoring transformer temperatures, a setting is provided to deassert the Measured Ambient and Top-Oil Temperature OK status bits (MAMB_OK and MTOn_OK) using a programmable (SELOGIC) setting. The settings AMB_F and TnOIL_F are provided for this purpose. Additionally, it is verified that the incoming Remote Analog values are within acceptable ranges. The ranges from RTD temperature measurement devices must be no lower than –50°C and no higher than +250°C, and so a check is made to ensure that the Remote Analog values fall within this same range. If either condition (Failure Booleans are true, or range is exceeded) exists while Remote Analogs are being used, the respective OK status bit (MAMB_OK or MTOn_OK) will deassert.

In most cases, an RTD communication failure is temporary in nature or can be rectified quickly. In general, the thermal element updates the ambient temperature value once a minute, and stores this value in a buffer until the next update. If you set AMBRTDF to BUFF, then the relay uses the stored value in the buffer instead of the D_AMB setting. Because the ambient temperature changes slowly, the temperature calculations will be accurate if the RTD communication is restored quickly. When setting AMBRTDF to SET, the relay uses D_AMB setting instead of the buffered value in the thermal calculations. This setting is not available if AMB_M is set to NA, in which case AMBRTDF = SET.

Transformer Cooling Stage Activation (T*a*CS*b*)

The thermal element uses the output of SELOGIC control equations to determine which cooling stage is active, so that thermal element calculations use the correct transformer constants. Settings TRTYPE and NUMCS determine the number of SELOGIC control equations for which the relay prompts the user.

NOTE: *a* designates the transformer number and *b* designates the cooling stage.

Because the maximum number of cooling stages is three, the relay evaluates a maximum of two SELOGIC control equations to determine the particular cooling stage. Use auxiliary contacts from the fan control devices as inputs to the SEL-487E with the T*x*CS*y* SELOGIC control equations set to the corresponding digital input. For example, for a single transformer (TRTYPE = 1) with three cooling stages (NUMCS = 3), the relay prompts you to set settings T1CS2S and T1CS3S.

Assume the input from Stage 2 is connected to IN101 and the input from Stage 3 is connected to IN102. Set the two SELOGIC control equations as follows:

T1CS2S := **IN101**

T1CS3S := **IN102**

To determine the cooling stage, the relay first evaluates T1CS2S, and then T1CS3S. *Table 7.11* shows the results of the evaluation.

Table 7.11   T1CS2S and T1CS23 Evaluation

Cooling Stage	T1CS2S	T1CS3S
1	0	0
2	1	0
3	1	1

Therefore, the relay uses the values for cooling Stage 1 when both inputs are deasserted, the values for cooling Stage 2 when T1CS2S is asserted, but T1CS3S is deasserted, and the values for cooling Stage 3 when both inputs are asserted. Be sure to use contacts that assert in the correct order; if T1CS23 asserts and T1CS2S is not asserted, the relay asserts the CSALRM bit and uses cooling Stage 1 values in the thermal calculations.

Cooling Stage MVA Rating (MVA*c*CS*b*)

Range: 0.2–5000 MVA, in 0.1-MVA steps

The MVA rating for all types of transformers (TRTYPE = 1 or 3) is taken as the nameplate MVA (MVA) rating and the line-to-line kilovolt (kV) values.

Cooling Stage Constants

Top-Oil Rise Over Ambient Temperature T*c*THOR*b*

Top-oil rise over ambient temperature is the difference in degrees Celsius of the top-oil temperature of a transformer above the ambient temperature. The default values listed in *Table 7.10* are from IEEE C57.92-1981. If specific values for a particular transformer are known, you can enter values from within a range of 0° to 100°C.

Hot-Spot Conductor Rise Over Top-Oil Temperature (T*c*THGR*b*)

Range: 0.01° to 100°C, in 0.1°C steps

Hot-spot rise over top-oil temperature is the difference in degrees Celsius of the temperature of the hottest spot on the conductor winding over the top-oil temperature. If not provided, THGR can be calculated from *Equation 7.19*:

$$THGR = THWR + \Theta_{hswr} - THOR$$

Equation 7.19

where:

THWR =	average winding rise over ambient at rated load (55°C or 65°C)	
Θ_{hswr} =	hot-spot winding rise over average winding rise	
=	(10°C if THWR = 55 or 15°C if THWR = 65)	

Ratio Losses (T*c*RATL*b*)

RATL is the ratio of load loss at rated load to no-load loss. The default values listed in *Table 7.10* are from IEEE C57.92-1981, Tables 2 and 4. If specific values for a particular transformer are known, you can enter values from within a range of 0.1 to 100.

Oil Thermal Time Constant (T*c*OTR*b*)

The oil thermal time constant is the time it takes the top-oil temperature rise over ambient temperature to reach 63.2 percent of the difference between final rise and initial rise during a load change. If not provided, T*c*OTR can be calculated from *Equation 7.20*:

$$TcOTR = C \bullet \left[\frac{THOR}{P_r} \right]$$

Equation 7.20

where:

C = transformer thermal capacity (watt-hours/degree)

= 0.06 • (weight of core and coil assembly in pounds)
+ 0.04 • (weight of tank and fitting in pounds)
+ 1.33 • (gallons of oil)

or C = 0.0272 • (weight of core and coil assembly in kilograms)
+ 0.01814 • (weight of tank and fitting in kilograms)
+ 5.034 • (liters of oil)

P_r = total loss at rated load (watts)

THOR = top-oil rise over ambient at rated load

1 kilogram = 2.2046 pounds

1 gallon = 3.785 liters

Oil Exponent (T*c*EXPN*b*)

This exponent is a constant that the thermal element uses in calculating ultimate top-oil rise over ambient temperature ($\Delta\Theta_{TO}$). The default values listed in *Table 7.10* are from IEEE C57.92-1981, Tables 2 and 4. If specific values for a particular transformer are known, you can enter values from within a range of 0.1 to 5.

Winding Exponent (T*c*EXPM*b*)

This exponent is a constant that the thermal unit uses in calculating ultimate hot-spot conductor rise over top-oil temperature ($\Delta\Theta_H$). The default values listed in *Table 7.10* are from IEEE C57.92-1981, Tables 2 and 4. If specific values for a particular transformer are known, you can enter values from within a range of 0.1 to 5.

Hot-Spot Thermal Time Constant (T*c*THS)

IEEE C57.91-1995 section 7.2.6 states that the winding time constant, τH (THS), is the time it takes the winding-temperature rise over oil-temperature rise to reach 63.2 percent of the difference between final rise and initial rise during a load change. The winding time constant may be estimated from the resistance cooling curve during thermal tests or calculated by the manufacturer using the mass of the conductor materials.

Normal Insulation Life (TRLIFE)

IEEE C57.91-1995 suggests that normal transformer insulation life is 20.55 years or 180000 hours. You can select other values within a range of 1000–999999 hours.

Constant to Calculate FAA (T*d*BFFA)

IEEE C57.91-1995 section 5.2 states that B (T*d*BFFA) is an empirical constant equal to 15000. You can select other values from within a range of 0 to 100000. The thermal element uses this constant to calculate the transformer insulation aging acceleration factor (FAA).

Top-Oil Temperature Limit (TOT1, TOT2)

One of the outputs the thermal element provides is top-oil temperature. TOT1 and TOT2 determine limits for top-oil temperature. If the top-oil temperature exceeds either limit, the corresponding TOT1 or TOT2 bit asserts. Using SEL*OGIC* control equations, you can configure the TOT*x* (*x* = 1 or 2) bits to close alarm contacts. When measured temperature inputs are available, the relay compares the TOT1 and TOT2 settings against the measured value. Should the measured value not be available (communications failure or lack of instrumentation), the relay compares the TOT1 and TOT2 settings against the calculated top-oil value.

With TRTYPE = 3 and top-oil temperatures being measured or calculated for each of the three single-phase transformers, the TOT1 or TOT2 bits assert when any of the three values exceeds a limit, as shown in *Figure 7.13*. The thermal report shows which transformer exceeded the limits.
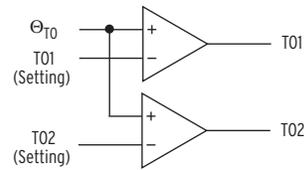
Figure 7.13   Oil Temperature Logic

Hot-Spot Temperature Limit (HST1, HST2)

One of the outputs the thermal element provides is hot-spot temperature. HST1 and HST2 determine limits for hot-spot temperature. If the hot-spot temperature exceeds one of these limits, the corresponding HS1 or HS2 bit asserts, as shown in *Figure 7.14*. Using SELOGIC control equations, you can configure these bits to close alarm contacts.

With TRTYPE = 3 and hot-spot temperatures being calculated for each of the three single-phase transformers, the HST1 or HST2 bits assert when any of the three values exceeds the limits. The thermal report shows which transformer exceeded the limits. *Figure 7.14* shows the oil temperature and hot-spot logic.
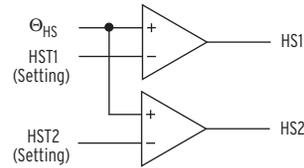
Figure 7.14   Hot-Spot Logic

Aging Acceleration Factor Limits (FAAL1, FAAL2)

The insulation of a transformer operating at temperatures higher than the rated temperature ages faster than the same transformer operating at or below rated temperature. One of the outputs the thermal element provides is a transformer insulation aging acceleration factor, which, when multiplied by elapsed time, provides an indication of the how fast the insulation is aging at the present load and temperature. Should load and temperature be greater than normal, this factor is greater than 1. Should load and temperature be less than normal, the factor is less than 1. FAAL1 and FAAL2 determine limits for the aging acceleration factor. If the aging acceleration factor exceeds the limits, the FAA1 or FAA2 bit asserts, as shown in *Figure 7.15*. Using SELOGIC control equations, you can configure these bits to close alarm contacts.

With TRTYPE = 3 and aging acceleration factors being calculated for each of the three single-phase transformers, the FAA1 or FAA2 bit asserts when any of the three values exceeds the limits. The thermal report will show which transformer was above the limits.
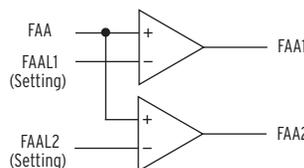
Figure 7.15   Aging Acceleration Factors Logic

Daily Rate of Loss-of-Life Limit (RLOLL)

One of the outputs the thermal element provides is daily rate of loss of life. This output is a measure, in percent, of the life lost from the transformer during a 24-hour period. RLOLL determines a limit for daily rate of loss of life. If the daily rate of loss of life exceeds the limit, the RLLOL bit asserts, as shown in *Figure 7.16*. Using SELOGIC control equations, you can configure the RLOLL bit to close an alarm contact. With TRTYPE = 3 and daily rate of loss of life being calculated for each of the three single-phase transformers, the RLL bit asserts when any of the three values exceeds the limit. The thermal report will show which transformer exceeded the limit.
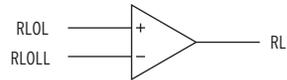
Figure 7.16   Daily Rate of Loss-of-Life Logic

Total Loss-of-Life Limit (TLOLL)

Range: 0.00–99.99%, in 0.01% steps

One of the outputs the thermal element provides is total loss of life, which is an estimate of the accumulated loss of transformer insulation life as a percentage of normal expected transformer insulation life. TLOLL determines a limit for total loss of life. If the total loss of life exceeds the limit, a TLL bit asserts, as shown in *Figure 7.17*. Using SELOGIC control equations, you can configure the TLL bit to close an alarm contact. With TRTYPE = 3 and aging acceleration factors being calculated for each of the three single-phase transformers, the TLL bit asserts when any of the three values exceeds the limit. The thermal report will show which transformer exceeded the limit.
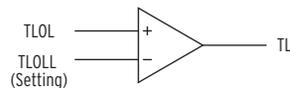
Figure 7.17   Total Loss-of-Life Logic

Preload Total Loss-of-Life Limit (TxTLOL)

Because many transformers have been in service for many years, use the preload setting to set an estimated loss-of-life value. This value is usually difficult to estimate because the operating conditions (load current and ambient temperature) for the preload time period are not recorded. Do not use current alone as a guideline; temperature as well as current affects insulation aging.

Cooling System Efficiency Pickup (TxCSEP)

When a measured top-oil temperature is available via the serial port, measured currents are used to determine a calculated top-oil temperature. If the measured top-oil temperature is greater than the calculated top-oil temperature by the value of setting TxCSEP (x = 1–3), then a Cooling System Efficiency, TxCSEP, asserts. Using SELOGIC control equations, the TxCSEP bit can be configured to any of the relay outputs to perform alarm or tripping functions. Assertion of the TxCSEP bit indicates that the cooling system (fans and/or pumps) is operating below expected efficiency and may require maintenance. With TRTYPE = 3 and cooling system efficiency being calculated for each of the three single-phase transformers, the CSE bit is set when any of the three values exceeds the limit. The thermal report will show which transformer was above the setting.

Thermal Element Condition

Figure 7.18 shows the logic that reports on the overall thermal health of the transformer by generating four status messages in relation to Normal, Warning 1, Warning 2, and Warning 3. These four messages are composed from various Thermal Element Conditions (TEC), and grouped into three alarm categories, in relation to Level 1, Level 2, and Level 3 alarms. *Figure 7.18* shows the reporting process for Transformer 1 (similar logic for Transformers 2 and 3), starting with the three alarm levels, the assessment of these levels, and the generation of the warning messages (see *Table 7.12*).
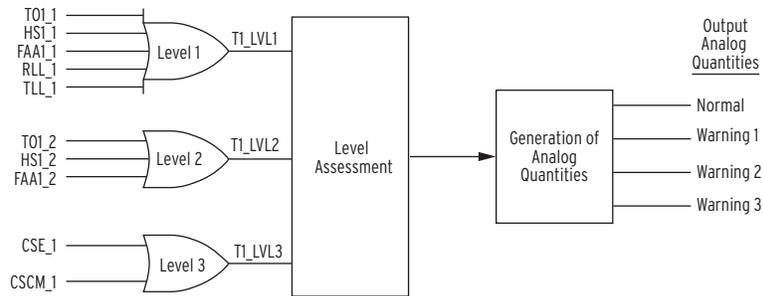
Figure 7.18   Thermal Condition (TEC) Logic for Transformer 1

Table 7.12 shows values for analog quantity TEC_1 for various combinations of the three input levels. If all three levels are deasserted, then the TEC_1 value is 1, and the message is "Normal". If any of the Level 1 alarms assert and no alarms from either Level 2 or Level 3 assert, then the value of TEC_1 is 2, and the message is "Warning 1". Likewise, if only Level 2 alarm(s) assert, TEC_1 has a value of 4, and the message is "Warning 2", and if only Level 3 alarm(s) assert, TEC_1 has a value of 8, and the message is "Warning 3". Should Level 1 and Level 2 alarms assert at the same time, Warning 2 has preference over Warning 1; if Level 2 and Level 3 alarms assert at the same time, then Warning 3 has preference over Warning 2.

Table 7.12   Default Transformer Constants

Level 3	Level 2	Level 1	TEC_1	Message
0	0	0	1	Normal
0	0	1	2	Warning 1
0	1	0	4	Warning 2
0	1	1	4	Warning 2
1	0	0	8	Warning 3
1	0	1	8	Warning 3
1	1	0	8	Warning 3
1	1	1	8	Warning 3

While the SEL-487E Relays can communicate directly with the SEL-2600A for gathering temperature readings, some applications may use the SEL-2030 communications processor for retrieving the temperature data from the SEL-2600A.

The SEL-487E obtains temperature information via one of its serial ports. The relay may receive data from as many as four temperature transducers: a single ambient temperature transducer and one transducer for top-oil temperature from each of three single-phase transformers. These data could come from an SEL-2032 or an SEL-2030 Communications Processor, which receives the temperature data from either an SEL-2600A RTD Module or a PLC (see

Figure 7.19). The SEL communications processor must receive the temperature data in Modbus, SEL Fast Messaging, or ASCII protocol. The SEL communications processor passes these data on to the SEL-487E in the form of an SEL Fast Message. While the SEL-487E can receive temperature data at any rate, the thermal element uses these data only once a minute.

Please refer to SEL Application Guide AG2000-07, *Connection and Configuration of an SEL Communications Processor and an SEL-2600A to Obtain Measured Ambient and Top-Oil Temperatures for the SEL-387-6 Relay Thermal Element*, and Application Guide AG2006-05, *SEL Communications Processor and an SEL-2410 I/O Processor to Obtain Measured Ambient and Top-Oil Temperatures for the SEL-387-6 Relay Thermal Element*, for information about how to set the SEL communications processor to communicate with the SEL-2600A RTD Module and the SEL-487E.
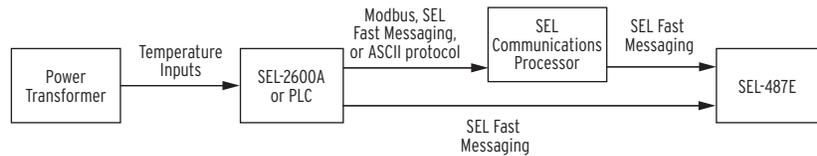
Figure 7.19   Example System Block Diagram

Thermal Monitor Report

The **THERM** or **THE** command, with no additional parameters, displays the present thermal status of the transformer(s) monitored by the relay. If an alarm condition is detected (one or more of the thermal Relay Word bits are set), the relay saves a snapshot of the thermal status of the transformer to EEPROM. The format for the **THE** report is as follows:

```
=>>THE <Enter>

Relay 1                                    Date: 03/28/2008  Time: 02:12:44.594
Station A                                  Serial Number: 2008030645

                                Transformer 1 Transformer 2 Transformer 3
        Thermal Element Condition : NORMAL        NORMAL        NORMAL
                 Load(Per Unit) :0.81          0.83          0.81
            In Service Cooling Stage :1             1             1
                   Ambient (deg. C) :20.0          20.0          20.0
        Calculated Top Oil (deg. C) :25.4          26.1          25.7
          Measured Top Oil (deg. C) :46.6          46.9          46.1
          Winding Hot Spot (deg. C) :55.4          56.8          55.1
   Aging Acceleration Factor, FAA :0.00           0.00          0.00
               Rate of LOL (%/day) :0.00           0.00          0.00
          Total Accumulated LOL (%) :0.00           0.00          0.00
             Time-Assert TLL (hrs) :0.00           0.00          0.00
=>>
```

Thermal Event Report Quantities
Thermal Element Conditions

The load condition value can be Normal, Warning 1, Warning 2, or Warning 3. See *Table 7.12* for more information.

Load Current

The load current is reported as a per-unit value based on transformer rating.

In-Service Cooling Stage

The active cooling system value is 1 for Cooling Stage 1, 2 for Cooling Stage 2, and 3 for Cooling Stage 3. Only one of the cooling stages can be active at a time (see *Transformer Cooling Stage Activation (TaCSb) on page 7.24* for more information).

Ambient Temperature

The value displayed (in degrees Celsius) is either the actual ambient temperature received from the serial port or a stored value (see *Default Ambient Temperature (D_AMB) on page 7.23* and *Default Ambient Temperature if RTD Fails (AMBRTDF) on page 7.23* for more information).

Calculated Top-Oil Temperature

The value displayed (in degrees Celsius) is the top-oil temperature of the transformer computed using the load current.

Measured Top-Oil Temperature

The value displayed (in degrees Celsius) is the top-oil temperature of the transformer received from the serial port. If no data (or invalid data) are received from the serial port, the value displayed is `-0-`.

Winding Hot-Spot Temperature

The value displayed (in degrees Celsius) is the computed value of the winding hot-spot temperature using the actual ambient and top-oil temperatures or the load current.

Aging Acceleration Factor

The value displayed is the active insulation aging acceleration factor (FAA). The maximum value of FAA is limited to 9999.0.

Rate of Loss of Life

The value displayed is the computed daily rate of loss of life (percent) accumulated in a 24-hour period. This value is updated at midnight daily.

Total Loss of Life

The value displayed represents the total accumulated loss of life (percent) since last reset.

Time to Assert TLL

The value displayed represents the estimated time (in hours) to assert the total loss-of-life alarm (TLL Relay Word bit).

Thermal Event Report (THE *n* Command)

Whenever a thermal alarm condition is set (load conditions are Warning 1, Warning 2, or Warning 3), the SEL-487E saves a snapshot of the thermal status of the transformer(s) in EEPROM. The five most recent thermal events are saved. If the command for retrieving the *n*th saved thermal event report is **THE *n*** (where

$n = 1$–5), **THE 1** will display the most recent event report while **THE 5** will display the oldest thermal event report. The format and data for the **THE n** report are the same as for the **THE** report.

Thermal Profile Data Report (THE H and THE D Commands)

The SEL-487E stores two types of trend data: one set on an hourly basis for the last 24 hours, and one set on a daily basis for the last 31 days. The format of the retrieved data report is suitable for display in Microsoft Excel.

Hourly Profile Data Report (THE H Command)

NOTE: When the thermal model is applied on one three-phase transformer (TRTYPE = 1), the SEL-487E displays only the values for Transformer 1. When the thermal model is applied on a set of three single-phase transformers (TRTYPE = 3), the SEL-487E displays the values for Transformer 1, Transformer 2, and Transformer 3.

The SEL-487E stores the following data on an hourly basis for the last 24 hours. The data are stored at the beginning of each hour.

➤ One-hour average ambient temperature

➤ One-hour average calculated top-oil temperature

➤ One-hour average measured top-oil temperature

➤ One-hour average winding hot-spot temperature

➤ One-hour average per-unit load current

➤ One-hour average insulation aging acceleration factor (FAA)

The format for the **THE H** report is as follows:

```
=>>THE H <Enter>

Relay 1                          Date: 03/28/2008  Time: 02:36:09.634
Station A                        Serial Number: 2008030645

Transformer 1
             Ambient   Calc     Measured             Load
Date    Time Temp      Top Oil  Top Oil  Hot Spot    Current   FAA
03/16/2008 2300  0.0   25.2     25.0     25.2         0.80     0.99
03/15/2008 2200  0.0   25.1     25.0     25.1         0.70     0.99

Transformer 2
             Ambient   Calc     Measured             Load
Date    Time Temp      Top Oil  Top Oil  Hot Spot    Current   FAA
03/16/2008 2300  0.0   24.2     25.6     25.2         0.80     0.99
03/15/2008 2200  0.0   24.1     25.6     25.1         0.70     0.99

Transformer 3
             Ambient   Calc     Measured             Load
Date    Time Temp      Top Oil  Top Oil  Hot Spot    Current   FAA
03/16/2008 2300  0.0   24.8     25.2     25.2         0.80     0.99
03/15/2008 2200  0.0   24.9     25.3     25.1         0.70     0.99

=>>
```

Daily Profile Data Report Function (THE D Command)

The relay stores the following on a daily basis (at midnight) for the last 30 days:

➤ Maximum ambient temperature

➤ Maximum calculated top-oil temperature

➤ Maximum measured top-oil temperature

➤ Maximum winding hot-spot temperature

➤ Maximum per-unit load

➤ Maximum insulation aging acceleration factor (FAA)

➤ Daily 24-hour accumulated loss of life (value of accumulated 24-hour loss of life at midnight)

➤ Total accumulated loss of life (sum of the daily 24-hour accumulated loss of life values)

The format for the **THE D** report is as follows:

```
=>>THE D <Enter>

Relay 1                              Date: 03/28/2008  Time: 02:43:48.623
Station A                            Serial Number: 2008030645

Transformer 1
          Max     Max Calc Max Msd  Max
Date      Ambient Top Oil  Top Oil  Hot Spot  Max Load  Max FAA  RLOL   TLOL
03/28/2008 15.0   25.3     26.7     45.3      0.60      0.99     0.00   0.00

Transformer 2
          Max     Max Calc Max Msd  Max
Date      Ambient Top Oil  Top Oil  Hot Spot  Max Load  Max FAA  RLOL   TLOL
03/28/2008 15.0   25.9     27.7     44.3      0.60      0.99     0.00   0.00

Transformer 3
          Max     Max Calc Max Msd  Max
Date      Ambient Top Oil  Top Oil  Hot Spot  Max Load  Max FAA  RLOL   TLOL
03/28/2008 15.0   25.7     26.5     43.4      0.60      0.99     0.00   0.00

=>>
```

Retrieving Thermal Data Reports

Thermal data reports are accessed with the **THE** command as shown in *Table 7.13*.

Table 7.13   Using the THE Command to Access Data Reports

Example THE Serial Port Commands	Format
THE	Enter **THE** command with no additional parameters to display the present status of the monitored transformer.
THE 1	Enter **THE** command followed by a number (1 in this example) to display the latest archived thermal event report.
THE D	Enter **THE** command followed by **D** and no additional parameters to display all available daily profile data records.
THE H	Enter **THE** command followed by an **H** but with no additional parameters to display all available hourly profile data records. The chronological progression through the report is down the page and in descending order.
THE H (or **D**) **3/30/00**	Enter **THE H** (or **D**) followed by the date (**3/30/00** in this example) to display all records (if they exist) starting with that date and ending with the present date. The records display with the latest record at the beginning (top) of the report and the oldest record at the end (bottom) of the report. Chronological progression through the report is down the page and in descending order.
THE D (or **H**) **2/17/00 3/07/00**	Enter **THE D** (or **H**) followed by two dates (**2/17/00** chronologically *precedes* **3/07/00** in this example) to display all the records (if they exist) among (and including) those dates. The records display with the latest record (3/07/00) at the beginning (top) of the report and the oldest record (2/17/00) at the end (bottom) of the report.
THE D 3/07/00 2/17/00	Enter **THE D** (or **H**) followed by two dates (**3/07/00** chronologically *follows* date **2/17/00** in this example) to display all records (if they exist) among (and including) those dates. The records display with the latest record (3/07/00) at the beginning (top) of the report and the oldest record (2/17/00) at the end (bottom) of the report.

The date entries in the examples for the **THE H** and **THE D** commands are dependent on the Date Format setting DATE_F. If setting DATE_F = MDY, enter the dates as in the above examples (Month/Day/Year). If setting DATE_F = YMD, enter the dates Year/Month/Day.

If the requested **THE** hourly or daily profile records do not exist, the relay responds: Invalid Record. If there are no data in the hourly or daily profile buffers, the relay responds: `No Data Available`.

Thermal Monitor Reset (THE R and THE P Commands)

The **THE R** (Reset Thermal Function) command clears all the thermal archives (daily profile data, hourly profile data, and thermal event data) and resets the total accumulated loss-of-life value to its preset value (if it exists) or zero. Using the **THE P _n_** (Load Preset Value of Total Loss of Life) command, the user can preset the initial loss-of-life values for each phase of the monitored transformer. The command must be followed by a value between zero and 100 percent. This command initializes the total loss-of-life value to the preset value entered by the user, clears all the thermal archive data, and restarts the thermal element.

Through-Fault Monitor

Operating Characteristic

Figure 7.20 shows a through-fault, which is a fault that occurs outside the area of unit protection of the transformer. Through-fault damage to the transformer is cumulative and results from both thermal and mechanical effects, with mechanical stress being much more damaging than thermal stress to transformer insulation for sustained or frequent faults. To this end, the through-fault element calculates the cumulative stress on the transformer, taking into account both mechanical and thermal effects.
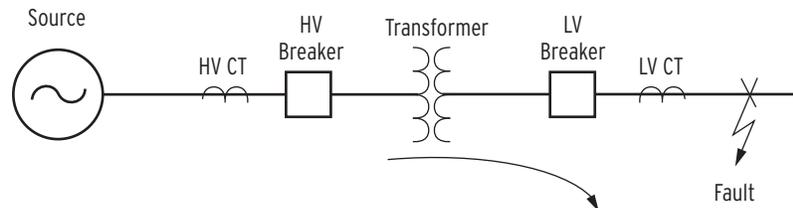
Figure 7.20   Transformer Bank Subjected to Through Fault

Figure 7.21 shows through-fault curves for Category IV transformers as published in IEEE C57 (1994 edition). These curves apply to transformers that are covered by the IEEE standard or, in general, to transformers that were built beginning in the early 1970s. For transformers built prior to 1970, consult the manufacturer to obtain the transformer short-circuit withstand capabilities.
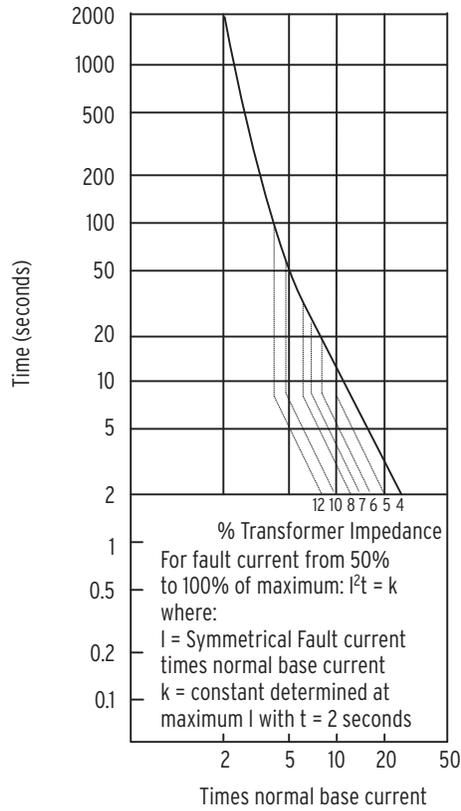
Figure 7.21   Category IV Transformers Through-Fault Protection Curves

The curves in *Figure 7.21* are a function of the transformer short-circuit imped-
ance, and are keyed to the maximum I^2t of the worst-case mechanical duty (max-
imum fault current for 2 seconds). *Equation 7.21* through *Equation 7.23* show
how the element uses the measured current and nameplate data to set parameters
for the accumulator shown in *Figure 7.22*. To convert the secondary current to
primary current, the element multiplies the secondary current by the CT ratio of
the particular winding. For combined windings, the element uses the highest CT
ratio of the two windings (see *Delta-Connected CTs on page 5.40*).

$$I_{RMS\_PU} = \frac{I_{RMS} \bullet \sqrt{3} \bullet kV_{LL}}{MVA}$$

Equation 7.21

$$I_{MAX\_PU} = \frac{100}{Z_{PU}}$$

Equation 7.22

$$K =$$

$$1250 \text{ if: } I_{RMS\_PU} \leq 0.5 \bullet I_{MAX\_PU}$$

$$2 \bullet (I_{MAX\_PU})^2 \text{ if: } I_{RMS\_PU} > 0.5 \bullet I_{MAX\_PU}$$

Equation 7.23

where:

I_{RMS} = Measured current

MVA = Transformer MVA rating (MVA)

kV_{LL} = Line-to-line voltage setting, VTERM*m*

Z_{PU} = Transformer per-unit impedance setting, TRFRZ

There are only five settings to set the through-fault element, all under the Monitor category (see *Table 8.25*). Enable the element by setting the SELOGIC control equation ETHRFLT for the conditions under which you want to enable the element. Use setting THFLTD to select the terminal that you want the element to use when calculating the through-fault current. (Switch S1 in *Figure 7.22* selects one of S, T, U, W, X, ST, TU, UW, or WX.) Be sure to select a winding that is included in the ECTTERM setting. Set the through-fault alarm pickup (THFLTPU) to the desired value, and enter the transformer percentage impedance (in percent) at the TRFRZ setting.

NOTE: Prior to firmware version R316, a through-fault condition was qualified when the ratio of measured terminal rms current to transformer full-load current exceeded 4.75.

Set the through-fault current pickup setting (TFLTIPU) based on the ratio of measured rms current of the THFLTD terminal to transformer full-load current that is required to qualify a through-fault condition. The relay automatically calculates the transformer full-load current for the selected terminal by using the nominal terminal voltage and transformer MVA (established by the VTERM*m* and MVA settings, respectively). When the ETHRFLT SELOGIC control equation evaluates as logical 1 and the ratio of the measured rms current to transformer full-load current exceeds the TFLTIPU setting, the relay begins running the through-fault logic. The through-fault logic stops running when the rms current falls below 0.95 • TFLTIPU times the full-load current.

Figure 7.22 shows a functional diagram of the through-fault element for the A-Phase of Terminal S (THFLTD = S), the B-Phase and C-Phase elements having identical diagrams. When SELOGIC control equation ETHRFLT asserts and the A-Phase current exceeds TFLTIPU times the transformer full-load current, Enable asserts and the 10-cycle Timer starts. When Enable asserts, the following occur:

➤ The through-fault element advances the A-Phase fault counter by 1 count

➤ The through-fault element advances the total fault counter by 1 count

➤ The through-fault element records the time when the fault starts (rising edge of Enable)

➤ The process to determine the maximum through-fault current for the fault duration starts

➤ The integration process starts, whereby the element sums the values calculated each processing interval (1/8 of a power system cycle)
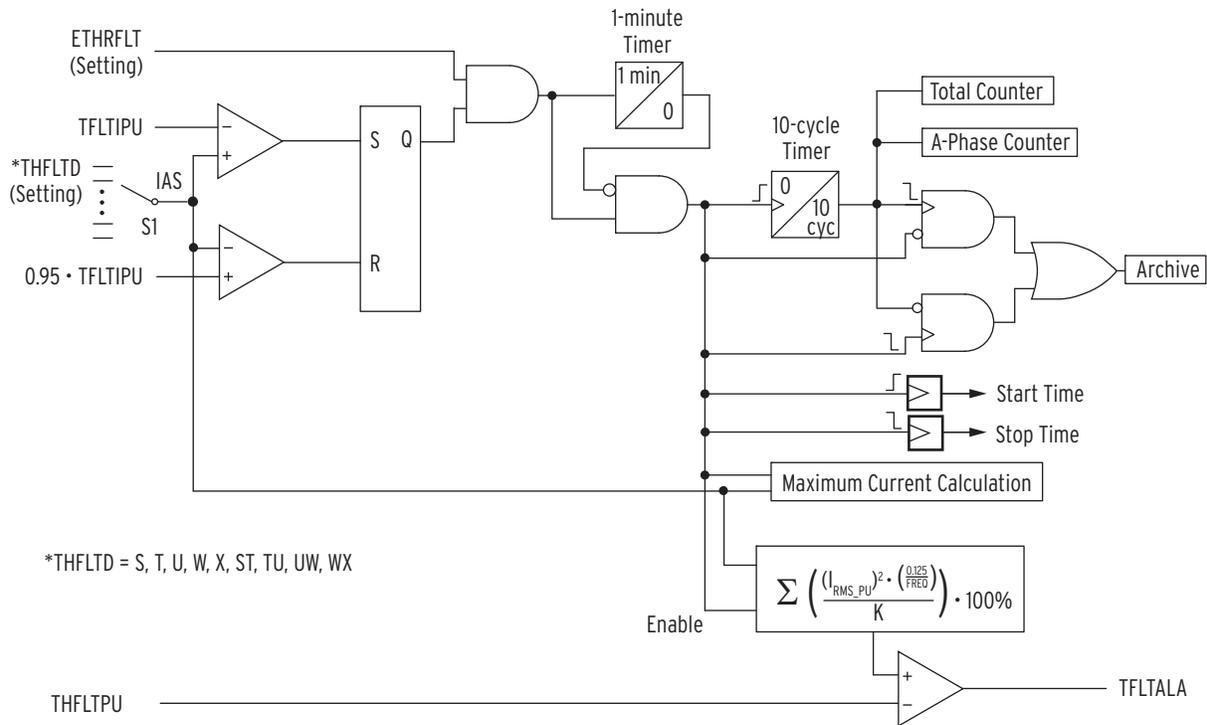
Figure 7.22 Through-Fault Diagram

The 10-cycle Timer avoids the inadvertent increment of the counters or archiving of the data if the fault current momentarily drops below the lower threshold level.

Setting threshold THFLTPU would usually be set to alarm for excessive, cumulative transformer bank stress. When the integration exceeds the value as specified by the THFLTPU setting, Relay Word bit TFLTALA asserts. Assign output Relay Word bit TFLTALA to an output for annunciation or control action such as to modify distribution feeder autoreclosing (e.g., to reduce the number of reclosures from 3 to 2).

When the fault current falls below 0.95 • TFLTIPU times the full-load level, the element deasserts and the following occur:

➤ The through-fault element records the stop time, then calculates (and records) the fault duration.

➤ The through-fault element records the maximum value of the fault current during the fault.

➤ The integration process stops.

The relay can store (archive) the data of 1200 through faults in a first-in-first-out (FIFO) buffer. The element automatically archives the data when one of the following conditions is true:

➤ The 10-cycle timer deasserts and the enable signal is deasserted.

➤ The 10-cycle timer is deasserted and the enable signal deasserts.

Through-Fault Monitor Reports

The format of the **TFE** command is as follows: **TFE *nnnn* A|P|C**

where:

nnnn =	Specifies number of through faults to display
A =	The relay displays all the Through Fault Records in the memory
P =	Use to specify preloading
C =	Sets the accumulated values to 0 and deletes the history

Figure 7.23 displays the relay response to the **TFE** (no other parameters) command. Notice that Winding S is the winding whose current inputs the element uses in the calculations (THFLTD = S). The **TFE** command lists as many as 20 of the most recent through faults. "Total Number of Transformer Through Faults" is the sum of the detected through faults of all three phases since the last reset, with a maximum of 65,535. "Number of *n* Phase Through Faults" (*n* = A, B, C) refers to the through faults detected for that particular phase since the last reset, also with a maximum of 65,535. The through-fault alarm state is either a 1 (indicating an alarm state) or a 0 (indicating a normal state).

```
=>TFE <Enter>

Winding S
Total Number of Transformer Through Faults:   5
Total Number of A Phase Through Faults:        3
Total Number of B Phase Through Faults:        1
Total Number of C Phase Through Faults:        1

Total Accumulated Percentage of Through Fault Capability:
                               A-Phase      B-Phase      C-Phase
                               26.45        12.34        11.78
Through Fault Alarm:   <O>        <O>          <O>

Last Reset: 11/12/07 12:15:23

#    Date         Time               Duration    IA     IB     IC      A     B     C       Alarm
                                     (seconds) (max primary kA)     (Increment %)
xxxx mm/dd/yy hh:mm:ss.sss   sss.sss+   xxx.xx xxx.xx xxx.xx    xxx.x xxx.x xxx.x    <alarm>
xxxx mm/dd/yy hh:mm:ss.sss   sss.sss+   xxx.xx xxx.xx xxx.xx    xxx.x xxx.x xxx.x    <alarm>
xxxx mm/dd/yy hh:mm:ss.sss   sss.sss+   xxx.xx xxx.xx xxx.xx    xxx.x xxx.x xxx.x    <alarm>
xxxx mm/dd/yy hh:mm:ss.sss   sss.sss+   xxx.xx xxx.xx xxx.xx    xxx.x xxx.x xxx.x    <alarm>
```

Figure 7.23   Result of the TFE Command

Following is a description of each column (#, Date, Time, etc.) of the event report. Through-fault events are numbered (# column) from 1 (the most recent event, at the top) to a maximum of 1200 through-fault events.

Under the date and time columns, the event shows the date of occurrence and the start time of each event (the date format is dependent upon the DATE_F setting).

Although the element processes all values each cycle, event duration (the Duration column) is reported in seconds with processing-interval resolution (if the event duration is equal to or greater than 136 seconds [60 Hz] or 163 seconds [50 Hz], the element appends a "+" to the time value).

IA, IB, and IC show the maximum primary current for each phase, with a maximum of 100,000 A primary.

A, B, and C show the amount (percent increase) of the present fault for each phase. Alarm shows those phase(s) that were in the alarm state at the end of the through-fault event.

Table 7.14 shows events report messages and the reason why these messages may appear in the events report.

Table 7.14   Through-Fault Events Report Messages

Message	Cause
Invalid Data	The accumulated data are corrupt.
Through Fault Event Monitor Disabled	ETHFLTM = N, ETHRFLT = NA, ETHRFLT evaluates to 0, or MVA = OFF.
Too many events—Data Lost	The memory is full.
Through Fault Event Buffer Empty	There are no event records in the nonvolatile memory.
Memory resources are low; check for activity on other ports	There is insufficient memory to display the event records.

Use the **TFE A** command to list all the stored through-fault events (not only the last 20 events) since the monitor was last reset. To list a particular number of through-fault events, enter the **TFE _n_** command (_n_ = 1 to 1200).

To clear event accumulated data, and all event records, use the **TFE C** command. Note that when you change the ETHRFLT setting, the relay also clears the data and records; i.e., it has the same effect as the **TFE C** command.

Use the **TFE P** command to preload or change the values of the through-fault event accumulated data, as shown in *Figure 7.24*. Enter these values in percent for each phase, up to a maximum value of 100.0 percent.

```
Winding S Total Accumulated Percentage of Through Fault Capability:
A-Phase = xxx.x? yyy.y
B-Phase = xxx.x? yyy.y
C-Phase = xxx.x? yyy.y
```

Figure 7.24   Preload the Values of the Accumulated Data

Analog Signal Profiling

Use the analog signal profiling function to record and track values of as many as 20 analog quantities. This function provides data in CASCII that is compatible to import directly into applications like spreadsheets. Specify the specific analog quantities for profiling with the SPAQ Report settings.

At the data acquisition rate of 5 minutes, the SEL-487E stores at least 10 days of all analog signals selected for profiling in nonvolatile memory. The report includes the time of acquisitions and the magnitude of each selected analog quantity. By defining conditions in the signal profiling enable SELOGIC variable setting (SPEN), you can record analog values at particular periods or conditions of interest.

SPAQgg (Analog Quantities for Signal Profiling)

Enter any analog quantity available in the relay from the Analog Quantity list (see *Section 12: Analog Quantities*) in this freeform setting.

SPAR (Signal Profile Acquisition Rate)

Although you can select as many as 20 analog quantities, the signal acquisition rate is the same for all analog quantities. Select an acquisition rate of 1, 5, 15, 30, or 60 minutes.

SPEN (Signal Profile Enable)

Use this SELOGIC control equation to specify conditions under which the profiling must take place. If there are no conditions, be sure to set SPEN = 1, else no data are recorded (default value of NA disables the function).

Use the compressed ASCII **CPR** command to view the profile data, as shown in *Figure 7.25*.

```
=>>CPR <Enter>
"#","DATE","TIME","VA_MAG","VB_MAG","VC_MAG","AI301","AI302","AI303","AI304","AI
305","AI306","13D7"
1,"03/17/2005","04:20:51.603",20.000,25.769,15.811,0.020,0.027,0.032,0.034,0.054
,0.045,"1066"

=>>
```

Figure 7.25   Compressed ASCII Data Display

Because the data are optimally formatted for machine-to-machine compatibility, use software such as Excel to display the profile data. *Figure 7.26* shows the data from *Figure 7.25* after importing the data (comma-delimited) into an Excel spreadsheet.

	J17	▼	=										
	A	B	C	D	E	F	G	H	I	J	K	L	M
1													
2	☐"#"	DATE	TIME	VA_MAG	VB_MAG	VC_MAG	AI301	AI302	AI303	AI304	AI305	AI306	13D7
3	1	3/17/2005	10:51.6	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045	1000
4	2	3/17/2005	05:51.6	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045	100C
5	3	3/17/2005	00:51.7	9.52	10	2.795	0.02	0.028	0.032	0.034	0.054	0.045	1005
6	☐												
7	☐=>>☐												

Figure 7.26   Profile Data in Excel Spreadsheet

Use the **PRO C**(lear) command to clear all profile data, as shown in *Figure 7.27*.

```
=>>PRO C <Enter>
Reset All Profile Data (Y,N)? Y <Enter>
Reset Complete

=>>
```

Figure 7.27   Profile Data Reset

Reporting

The SEL-487E features comprehensive power system data analysis capabilities. These are described in *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual*. This section describes reporting characteristics that are unique to the SEL-487E.

Duration of Data Captures and Event Reports

The SEL-487E stores high-resolution raw data and filtered data. The number of stored high-resolution raw data captures and event reports is a function of the amount of data contained in each capture.

Table 7.15 lists the maximum number of data captures/event reports the relay stores in nonvolatile memory when ERDIG = S for various report lengths and sample rates. The relay automatically overwrites the oldest events with the newest events when the nonvolatile storage capacity is exceeded.

The relay stores high-resolution raw and filtered event data in nonvolatile memory. *Table 7.15* lists the storage capability of the SEL-487E for common event reports.

The lower rows of *Table 7.15* show the number of event reports the relay stores at the maximum data capture times for each SRATE sampling rate setting. Table entries are the maximum number of stored events; these can vary by 10 percent according to relay memory usage.

NOTE: Consider the total capture time when choosing a value for setting LER at the SRATE := 8 kHz. At LER := 3.0, the relay records at least 12 data captures when ERDIG = S. These and smaller LER settings are sufficient for most power system disturbances.

Table 7.15   Event Report Nonvolatile Storage Capability When ERDIG = S

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	111	143	166	194
0.5 seconds	65	87	104	127
1.0 seconds	35	48	60	75
3.0 seconds	12	17	22	28
6.0 seconds	N/A	9	11	14
12.0 seconds	N/A	N/A	5	7
24.0 seconds	N/A	N/A	N/A	3

When the event report digital setting is set to include all Relay Word bits in the event report (ERDIG = A), the maximum number of stored reports is reduced, as shown in *Table 7.16*.

Table 7.16   Event Report Nonvolatile Storage Capability When ERDIG = A

Event Report Length	Maximum Number of Stored Reports			
	8 kHz	4 kHz	2 kHz	1 kHz
0.25 seconds	91	111	124	140
0.50 seconds	51	64	73	85
1.0 seconds	N/A	34	40	47
3.0 seconds	N/A	N/A	13	17
6.0 seconds	N/A	N/A	N/A	8
12.0 seconds	N/A	N/A	N/A	N/A
24.0 seconds	N/A	N/A	N/A	N/A

Event Reports, Event Summaries, and Event Histories

See *Section 9: Reporting in the SEL-400 Series Relays Instruction Manual* for an overview of event reports, event summaries, and event histories. This section describes the characteristics of these that are unique to the SEL-487E.

Base Set of Relay Word Bits

The following Relay Word bits are always included in COMTRADE and compressed event reports: TLED_1, TLED_2, TLED_3, TLED_4, TLED_5, TLED_6, TLED_7, TLED_8, TLED_9, TLED_10, TLED_11, TLED_12, TLED_13, TLED_14, TLED_15, TLED_16, TLED_17, TLED_18, TLED_19, TLED_20, TLED_21, TLED_22, TLED_23, TLED_24, 87RA, 87RB, 87RC, RMBnA, TMBnA, RMBnB, TMBnB, ROKA, RBADA, CBADA, LBOKA, ROKB, RBADB, CBADB, LBOKB, TRS, TRT, TRU, TRW, TRX, CLS, CLT, CLU, CLW, CLX, 52CLS, 52CLT, 52CLU, 52CLW, 52CLX.

Event Reports

Report Header Section of the Event Report

The first portion of an event report is the report header. See *Figure 7.28* for the location of items included in a sample fixed analog section of an event report.

The report header is the standard SEL-487E header listing the relay identifiers, date, and time. Report headers help you organize report data. Each event report begins with information about the relay and the event, such as the RID setting (Relay ID), the SID setting (Station ID), and the firmware checksum (CID). The FID string identifies the relay model, flash firmware version, and the date code of the firmware. See *Firmware on page A.1* for a description of the FID string. To complete the header, the relay reports a date and time stamp to indicate the internal clock time when the relay triggered the event.

Fixed Analog Section of the Event Report

The fixed analog section follows the header section and starts with column labels. The data underneath the analog column labels contain samples of power system voltages and currents in primary kilovolts and primary amperes, respectively. These quantities are instantaneous values scaled by $\sqrt{2}/2$ (0.707). Although you may not use all 24 channels of the SEL-487E in your application, all 24 channels are always displayed in the event report. To display all 24 channels, the event report consists of three groups. Current channels IAS through ICU are in the first group as shown in *Figure 7.28*. Current channels IAW–IY3 are shown in the second group, and voltage channels VAV–VCZ are shown in the third group.

Figure 7.28 contains selected data from the analog section of a 4-samples/cycle event report for a transformer fault. The bracketed numbers at the left of the report (for example, [11]) indicate the cycle number; *Figure 7.28* presents 11 cycles of 4-samples/cycle data. The trigger row includes a > character to indicate the trigger point. This is the dividing point between the prefault or PRE time and the fault or remainder of the data capture.

```
Relay 1                              Date: 04/21/2015  Time: 02:03:38.102    Header
Station A                            Serial Number: 1132490016
FID=SEL-487E-3-R311-V0-Z105101-D20150513  Event Number = 10020    CID=0x5EB8
```
Firmware ID

```
              Currents (Pri. Amps)
    IAS    IBS    ICS    IAT    IBT    ICT    IAU    IBU    ICU
 [1]
    190    -39   -150   -416     84    331      0      0      0
    -64    195   -132    141   -431    289      0      0      0      One cycle of data
   -190     39    150    416    -84   -331      0      0      0
     63   -195    132   -141    431   -289      0      0      0

 [2]
    190    -39   -150   -416     84    331      0      0      0
    -63    195   -132    141   -432    289      0      0      0
   -190     39    150    416    -84   -331      0      0      0
     64   -195    132   -141    431   -289      0      0      0
 [3]
    190    -39   -150   -416     84    331      0      0      0
    -64    195   -132    141   -431    289      0      0      0
   -190     39    150    416    -84   -331      0      0      0
     63   -195    132   -141    431   -289      0      0      0
 [4]
    190    -39   -150   -416     84    331      0      0      0
    -63    195   -132    141   -431    289      0      0      0
   -190     39    150    416    -84   -331      0      0      0
     63   -195    132   -141    432   -289      0      0      0
 [5]
    189    -39   -150   -416     84    331      0      0      0
    -63    195   -132    141   -432    289      0      0      0
   -190     39    150    416    -84   -331      0      0      0
     85   -195    132   -135    427   -285      0      0      0
 [6]
    561    -39   -150   -319     77    327      0      0      0
   -291    195   -132     81   -408    272      0      0      0
  -1177     39    150    158    -73   -312      0      0      0
    475   -195    132    -32    392   -263      0      0      0
 [7]
   1422    -39   -150    -94     77    301      0      0      0>     Trigger

   -475    195   -132     32   -393    263      0      0      0
  -1422     39    150     94    -77   -301      0      0      0
    534   -195    132    -37    392   -263      0      0      0
 [8]
   2421    -39   -150   -180     77    301      0      0      0

  -1088    195   -132     85   -392    263      0      0      0*    125 Cycles after trigger (to Event Summary)

  -4079     39    150    322    -77   -301      0      0      0
   1583   -195    132   -128    392   -263      0      0      0
 [9]
   4740    -39   -150   -378     77    301      0      0      0
  -1583    195   -132    128   -392    263      0      0      0
  -4740     39    150    378    -77   -301      0      0      0
   1583   -195    132   -128    392   -263      0      0      0
 [10]
   4739    -39   -150   -378     77    301      0      0      0
  -1583    195   -132    128   -392    263      0      0      0
  -4739     39    150    378    -77   -301      0      0      0
   1517   -185    125   -123    372   -248      0      0      0
 [11]
   3308      1   -133   -264     -3    266      0      0      0
   -726     87    -58     59   -175    116      0      0      0
   -939    -20     58     75     42   -115      0      0      0

      0      1      0      0     -1      1      0      0      0      Circuit breaker open
```

Figure 7.28   Analog Section of the Event Report

Table 7.17   Event Report Analog Quantities (Sheet 1 of 2)

Quantity	Description
IAS, IBS, ICS	Winding S, filtered phase current vector
IAT, IBT, ICT	Winding T, filtered phase current vector
IAU, IBU, ICU	Winding U, filtered phase current vector
IAW, IBW, ICW	Winding W, filtered phase current vector
IAX, IBX, ICX	Winding X, filtered phase current vector

Table 7.17 Event Report Analog Quantities (Sheet 2 of 2)

Quantity	Description
IY1, IY2, IY3	Windings Y1, Y2, and Y3, filtered phase current vectors
VAV, VBV, VCV	Voltage V, filtered phase voltage vector
VAZ, VBZ, VCZ	Voltage Z, filtered phase voltage vector

Fixed Analog Differential Report

The differential report is not a part of the event report. Use the **EVE DIF**[**F**] command (add **DIF**[**F**] to the **EVE** command) to retrieve the most recent differential report. The analog differential report follows the header section. The analog differential report displays operate and restraint quantities for each differential element, and the percentage second-, fourth-, and fifth-harmonic currents in each element, as shown in *Figure 7.29*.

```
Relay 1                            Date: 04/21/2015  Time: 02:03:38.102
Station A                          Serial Number: 1132490016
FID=SEL-487-3-R311-V0-Z105101-D20150513  Event Number = 10020   CID=0x5EB8

  Differential Quantities      2nd Harmonic   4th Harmonic   5th Harmonic
 IOPA  IRTA  IOPB  IRTB  IOPC  IRTC  IAH2 IBH2 ICH2 IAH4 IBH4 ICH4 IAH5 IBH5 ICH5

[1]
 0.05  1.96  0.06  1.95  0.05  1.96    2    2    1    1    0    1    1    1    1
 0.05  1.96  0.06  1.95  0.05  1.96    2    2    2    2    1    1    1    1    1
 0.05  1.96  0.06  1.95  0.05  1.96    2    2    2    1    1    1    1    1    2
 0.05  1.96  0.06  1.95  0.05  1.96    2    2    2    1    1    1    1    1    2
[2]
 0.05  1.96  0.06  1.95  0.05  1.96    2    2    2    1    1    1    1    2    1
 0.05  1.96  0.06  1.95  0.05  1.96    2    2    2    1    1    0    1    2    2
 0.05  1.96  0.06  1.95  0.05  1.96    2    2    1    2    2    1    1    2    2
 0.05  1.96  0.06  1.95  0.05  1.96    3    2    1    2    2    1    1    2    2
[3]
 0.05  1.96  0.06  1.95  0.05  1.96    1    2    2    2    2    1    1    1    2
 0.05  1.96  0.06  1.95  0.05  1.96    1    3    2    1    2    1    1    1    1
 0.05  1.96  0.06  1.95  0.05  1.96    1    1    2    2    2    1    0    1    1
 0.05  1.96  0.06  1.95  0.05  1.96    1    1    2    1    1    1    1    1    2
[4]
 0.05  1.96  0.06  1.95  0.05  1.96    1    3    1    1    0    0    1    0    2
 0.05  1.96  0.06  1.95  0.05  1.96    1    1    2    1    1    0    1    1    2
 0.05  1.96  0.06  1.95  0.05  1.96    1    1    2    1    1    0    1    2    2
 0.05  1.96  0.05  1.95  0.05  1.96    2    3    1    1    1    1    1    1    2
[5]
 0.05  1.96  0.05  1.95  0.05  1.96    0    0    0    1    0    0    1    1    2
 0.05  1.96  0.06  1.95  0.05  1.96    0    2    1    1    1    1    1    1    1
 0.05  1.96  0.06  1.95  0.05  1.96    2    2    1    1    2    1    0    1    1
 0.07  1.98  0.01  1.97  0.08  1.93    2    3    1    1    1    1    1    1    2
[6]
 1.29  2.97  0.67  2.22  0.62  2.38    1    2    3    1    1    1    1    1    1
 1.51  3.14  0.78  2.40  0.74  2.28    1    3    3    1    1    0    0    1    0
 3.59  4.74  1.81  3.07  1.79  3.15    1    2    3    1    1    1    1    1    1
 3.79  4.90  1.92  3.19  1.88  3.15    0    0    0    0    0    0    1    6    8
[7]
 4.62  5.53  2.31  3.49  2.31  3.50    0    0    0    0    0    0    0    0    0
 4.62  5.53  2.31  3.49  2.31  3.50    0    0    0    0    0    0    0    0    0
 4.62  5.53  2.31  3.49  2.31  3.50    0    0    0    0    0    0    0    0    0
 4.68  5.60  2.34  3.55  2.34  3.49    0    0    1    1    1    0    0    0    1
[8]
 7.60  8.77  3.80  4.92  3.80  5.12    1    2    3    1    1    1    1    1    1
 8.14  9.35  4.07  5.39  4.06  5.20    1    2    3    1    1    1    1    1    1
12.91 14.53  6.46  7.73  6.45  7.87    1    2    3    1    1    1    1    1    1
13.38 15.04  6.69  8.09  6.68  8.00    1    2    3    1    1    1    1    1    1
[9]
15.27 17.10  7.64  9.04  7.63  9.05    0    0    0    0    0    0    0    0    0
15.27 17.10  7.64  9.04  7.63  9.05    0    0    0    0    0    0    0    0    0
15.27 17.10  7.64  9.04  7.63  9.05    0    0    0    0    0    0    0    0    0
15.27 17.10  7.64  9.04  7.63  9.05    0    0    0    0    0    0    0    0    0
[10]
15.27 17.10  7.64  9.04  7.63  9.05    0    0    0    0    0    0    0    0    0
15.27 17.10  7.64  9.04  7.63  9.05    0    0    0    0    0    0    0    0    0
15.27 17.09  7.64  9.04  7.63  9.05    0    0    0    0    0    0    0    0    0
15.21 17.02  7.61  8.94  7.60  9.01    1    1    1    1    1    1    1    0    1
[11]
11.12 12.45  5.56  6.82  5.56  6.76    1    2    3    1    1    1    1    1    1
10.35 11.59  5.17  5.66  5.18  6.40    0    0    1    1    1    0    0    0    1
 3.63  4.06  1.82  2.43  1.81  2.27    0    0    1    1    1    0    0    0    1
 2.87  3.21  1.43  1.43  1.44  1.97    0    0    1    1    1    0    0    0    1
[12]
 0.00  0.00  0.00  0.00  0.00  0.00    0    0    0    0    0    0    0    0   02
```

Figure 7.29   Differential Report

Digital Section of the Event Report

The next portion of an event report is the digital section. Inspect the digital data to evaluate relay element response during an event. See *Figure 7.30* for the locations of items in a sample event report digital section. If you want to view only the digital portion of an event report, use the **EVE D** command (see *EVENT on page 14.31 in the SEL-400 Series Relays Instruction Manual* and *Section 9: ASCII Command Reference* for details). In the digital portion of the event report, the relay indicates deasserted elements with a period (.) and asserted elements with an asterisk (*) character.

The element and digital information labels are single character columns. Read these columns from top to bottom. The trigger row includes a > character following immediately after the last digital element column to indicate the trigger point. The relay marks the row used to report the maximum fault current with an asterisk (*) character at the right of the last digital element column. Event reports that are 4-samples/cycle reports show the OR combination of digital elements in the two 8-samples/cycle rows to make the quarter-cycle entry.

The digital report arranges the event report digital settings into 79 column pages. For every 79 columns, the relay generates a new report that follows the previous report. The report displays the digital label header for each column in a vertical fashion, aligned on the last character. For example, if the first digital section elements are TRPXFMR, TRIPS, TRIPT, TRIPU, TRIPW, TRIPX, #, and 87RA, the header appears as in *Figure 7.31*. If the Relay Word bits included in the header were assigned aliases, the alias names appear in the report.

```
 T

 R                                                         OOOOOO
 PTTTTT      RRRRRR VV   SSSSSS TTTTTT UUUUUU WWWWWW XXXXXX      IIIIIII UUUUUU
 XRRRRR 888  EEEEEE PPLL FRFRFR FRFRFR FRFRFR FRFRFR FRFRFR FFFFF NNNNNNN TTTTTT    Digital Column Labels
 FIIIII 7778 FFFFFF OOOO 333333 333333 333333 333333 333333 BBBBB 1111111 111111
 MPPPPP RRR7 FFFRRR LLPP 222222 222222 222222 222222 222222 FFFFF 0000000 000000
 RSTUWX ABCQ 123123 VZVZ PPQQGG PPQQGG PPQQGG PPQQGG PPQQGG STUWX 1234567 123456

 [1]

 ...... .... ...... .... ...... ...... ...... ...... ...... ..... ....... ......
 ...... .... ...... .... ...... ...... ...... ...... ...... ..... ....... ......   One Cycle of Data
 ...... .... ...... .... ...... ...... ...... ...... ...... ..... ....... ......
 ...... .... ...... .... ...... ...... ...... ...... ...... ..... ....... ......
 .
 .
 .
 [7]
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....>   Trigger

 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 [8]
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....*
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 [9]
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
 *..... *... ...... .... ...... ...... ...... ...... ...... ..... ....... *.....
```

Figure 7.30   Digital Section of the Event Report

```
                        ┌──────────── Transformer Trip
                        │┌─────────── Winding S Trip
                        ││┌────────── Winding T Trip
                        │││┌───────── Winding U Trip
                        ││││┌──────── Winding W Trip
                        │││││┌─────── Winding X Trip
                        ││││││┌────── # (space)
                        │││││││┌───── Restraint Differential A
         T              │││││││
         R              │││││││
         PTTTTT         │││││││
         XRRRRR 8
         FIIIII 7
         MPPPPP R
         RSTUWX A
         ...... .
         ***... *
         ***... *
```

Figure 7.31   Sample Digital Portion of the Event Report

Event Summary Section of the Event Report

The next portion of an event report is the summary section. See *Figure 7.32* for the locations of items included in a sample summary section of an event report. If you want to exclude the summary portion from an event report, use the **EVE NSUM** command.

Table 7.18 shows the order of valid reference quantities that the relay uses to display the angular relationship among the metering values. Notice that the SEL-487E does not adjust the angle of the current values for delta-connected CTs.

Table 7.18   Valid Reference Quantities

Reference Quantity	Source	Y-Connected	Delta-Connected
Fundamental voltage magnitude	PT V[a]	VAVFAC	VABVFAC
Fundamental voltage magnitude	PT Z[b]	VAZFAC	VABZFAC
Positive-sequence current	Winding S[c]	IASFAC	Not calculated
Positive-sequence current	Winding T[c]	IATFAC	Not calculated
Positive-sequence current	Winding U[c]	IAUFAC	Not calculated
Positive-sequence current	Winding W[c]	IAWFAC	Not calculated
Positive-sequence current	Winding X[c]	IAXFAC	Not calculated

[a] VAVFMC >5 V.

[b] VAZFMC >5 V

[c] IA*m*FMC >0.25 A (*m* = S, T, U, W, X).

For example, the A-Phase voltage measured from the PT V voltage inputs is reference for all metering quantities provided this voltage magnitude is greater than 5 V. If PT V is not available, then the A-Phase voltage measured from the PT Z voltage inputs is reference for all metering quantities provided this voltage magnitude is greater than 5 V. This sequence continues for all other reference quantities.

The information in the summary portion of the event report is the same information in the event summary, except that the report header does not appear immediately before the event information when you view a summary in the event report.

```
Event: TRIP                                Time Source: OTHER
Event Number: 10014         Frequency: 60.003          Group: 1          Event Information
Targets: TLED_13 TLED_20

Breaker S: OPEN

Fault Analog Data

        IAS   IBS   ICS   IAT   IBT   ICT   IAU   IBU   ICU
MAG(A)  426   426   426   428   428   427    0     0     0
ANG(DEG) -1.0 -120.8 119.3 179.4  59.5 -60.5 -118.1 -90.9  29.7


        IAW   IBW   ICW   IAX   IBX   ICX   IY1   IY2   IY3
MAG(A)  426    1     0     0     0     0     0     0     0
ANG(DEG) -0.9 -122.8 -152.1 -137.8 -118.8 -169.8 -143.6 -139.8 -138.1   Fault Data

        VAV   VBV   VCV   VAZ   VBZ   VCZ
MAG(kV) 134   134   134    0     0     0
ANG(DEG) 0.0 -119.9 120.3 -136.1 -112.0 -165.2

        IOPA  IRTA  IOPB  IRTB  IOPC  IRTC
MAG(p.u) 1.05  3.01  1.05  3.00  1.05  3.01
```

Figure 7.32 Summary Section of the Event Report

Event Summary

You can retrieve a summary version of stored event reports as event summaries. These short-form reports present vital information about a triggered event. The relay generates an event in response to power system faults and other trigger events. See *Figure 7.33* for a sample event summary.

```
Relay 1                      Date: 04/24/2015  Time: 08:15:52.452
Station A                    Serial Number: 1132490016               Report Header

Event: TRIP                                Time Source: OTHER
Event Number: 10015         Frequency: 60.000          Group: 1          Event Information
Targets: TLED_13 TLED_14 TLED_15

Breaker S: OPEN                                                        Breaker Status

Fault Analog Data

        IAS   IBS   ICS   IAT   IBT   ICT   IAU   IBU   ICU
MAG(A)  629   629   629    0     0     0     0     0     0
ANG(DEG) -16.1 -135.8 104.3 -75.9 136.1 161.7 -90.1 -51.3  93.8


        IAW   IBW   ICW   IAX   IBX   ICX   IY1   IY2   IY3
MAG(A)  630    0     0     0     0     0     1     0     0
ANG(DEG) -15.9 -40.2 -63.6 -101.0 -109.8 -52.7 -74.2 -68.2 -97.0     Fault Data

        VAV   VBV   VCV   VAZ   VBZ   VCZ
MAG(kV) 126   126   126    0     0     0
ANG(DEG) 0.0 -119.9 120.3 -55.9 -52.0 -84.5

        IOPA  IRTA  IOPB  IRTB  IOPC  IRTC
MAG(p.u) 3.00  3.00  2.99  2.99  3.00  3.00
```

Figure 7.33 Sample Event Summary Report

The event summary contains the following information:

➤ Standard report header

➢ Relay and terminal identification

➢ Event date and time

➤ Event type

➤ Time source (HIRIG or OTHER)

➤ Event number

➤ System frequency

➤ Active group at trigger time

➤ Targets

➤ Circuit breaker trip and close times; and auxiliary contact(s) status

➤ Fault voltages, currents, sequence current, and operate and restraint currents (from the event report row with the largest current)

➤ MIRRORED BITS communications channel status (if enabled)

The relay derives the summary target information and circuit breaker trip and close times from the rising edge of relevant Relay Word bits during the event. If no trip or circuit breaker element asserted during the event, the relay uses the last row of the event.

The SEL-487E reports the event type and *Table 7.19* lists event types in fault reporting priority. Differential and restricted earth fault indications have reporting priority over indeterminate fault events. For example, you can trigger an event when there is no fault condition on the power system by using the **TRI** command. In this case, when there is no fault, the relay reports the event type as TRIG.

Table 7.19 Event Types

Event	Description
87RA, 87RB, 87RC, REF	Differential elements involvement for event reports generated by 87RA, 87RB, or 87RC. REF is the OR combination of REFF1, REFF2, and REFF3
TRIP	Rising edge of Relay Word bit TRIP
ER (event report trigger)	Rising edge of ER (SELOGIC control equation)
TRIG	Execution of the **TRIGGER** (**TRI**) command (manually triggered)

Event History

The event history gives you a quick look at recent relay activity. The relay labels each new event with a unique number from 10000 to 42767. (At 42767, the top of the numbering range, the relay returns to 10000 for the next event number and then continues to increment.)

The event history contains the following:

➤ Standard report header

➢ Relay and terminal identification

➢ Date and time of report

➤ Event number

➤ Event date and time

➤ Event type

➤ Active group at the trigger instant

➤ Targets

The event types in the event history are the same as the event types in the event summary (see *Table 7.19* for event types). The event history report indicates events stored in relay nonvolatile memory. The relay places a blank row in the history report output; items that are above the blank row are available for viewing (use the **EVE** and **CEV** commands). Items that are below the blank row are no longer in relay memory; these events appear in the history report to indicate past power system performance.

The relay does not ordinarily modify the numerical or time order in the history report. However, if an event report is corrupted (power was lost during storage, for example), the relay lists the history report line for this event after the blank row.

This page intentionally left blank

Settings

Section 12: Settings in the SEL-400 Series Relays Instruction Manual describes common platform settings. This section contains tables of relay settings for the SEL-487E relay.

The relay hides some settings based upon the state of other settings. For example, if you set an enable setting to OFF (disabling the function), the relay hides all settings associated with that function.

The settings prompts in this section are similar to the ASCII terminal and ACSELERATOR QuickSet SEL-5030 Software prompts. Prompts in this section are unabbreviated and show all possible setting options.

For information on using settings in protection and automation, see the examples in *Section 6: Protection Application Examples*. The section contains information on the following settings classes.

> **⚠ WARNING**
> Isolate the relay trip circuits while changing settings. When changing settings for multiple classes, it is possible to be in an intermediate state that will cause an unexpected trip.

Alias Settings

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of alias settings. *Table 8.1* lists the default alias settings for the SEL-487E.

Table 8.1   Default Alias Settings

Label	Default Value
EN	RLY_EN

Global Settings

Table 8.2   Global Setting Categories

Settings	Reference
General Global Settings	*Table 8.3*
Global Enables	*Table 8.4*
Control Inputs (Global)	*Table 8.5*
Main Board Control Inputs	*Table 8.6*
Interface Board #1 Control Inputs	*Table 8.7*
Interface Board #2 Control Inputs	*Table 8.8*
Interface Board #3 Control Inputs	*Table 8.9*
Interface Board #4 Control Inputs	*Table 8.10*
Settings Group Selection	*Table 8.11*
LEA Ratio Correction Factor	*Table 8.12*
Frequency Source Selection	*Table 8.13*
Synchronized Phasor Configuration Settings	*Table 8.14*
Time and Date Management	*Table 8.22*
Data Reset Controls	*Table 8.23*
DNP	*Table 8.24*

Table 8.3   General Global Settings

Setting	Prompt	Default Value
SID	Station Identifier (40 characters)	Station A
RID	Relay Identifier (40 characters)	Relay 1
CONAM	Company Name (5 characters)	abcde
NFREQ	Nominal System Frequency (50, 60 Hz)	60
PHROT	System Phase Rotation (ABC, ACB)	ABC

Table 8.4   Global Enables

Setting	Prompt	Default Value
EICIS	Independent Control Input Settings (Y, N)	N
EPMU	Synchronized Phasor Measurement (Y, N)	N
EINVPOL	Enable Invert Polarity (OFF or combo of terminals)[a, b]	OFF

[a] Any combination of Terminals V, Z, S, T, U, W, or X, and A-, B-, or C-Phases, or Terminal Y and Inputs 1, 2, or 3. For example, EINVPOL := SA,SB,X,Y3 inverts the polarity of the A- and B-Phases for Terminal S, all phases for Terminal X, and Input 3 for Terminal Y.

[b] Cannot set from front-panel HMI.

Make *Table 8.5* settings when Global enable setting EICIS := N.

Table 8.5   Control Inputs

Setting	Prompt	Default Value	Increment
IN1XXD[a]	Mainboard Debounce Time (0.0–30 ms)	2.0	0.5
IN2XXD[b]	Int Board #1 Debounce Time (0.0–30 ms)	2.0	0.5
IN3XXD[c]	Int Board #2 Debounce Time (0.0–30 ms)	2.0	0.5
IN4XXD[d]	Int Board #3 Debounce Time (0.0–30 ms)	2.0	0.5
IN5XXD[e]	Int Board #4 Debounce Time (0.0–30 ms)	2.0	0.5

[a] Setting applies to all the main board input contacts.

[b] Setting applies to all the Interface Board #1 input contacts.

[c] Setting applies to all the Interface Board #2 input contacts.

[d] Setting applies to all the Interface Board #3 input contacts.

[e] Setting applies to all the Interface Board #4 input contacts.

Make *Table 8.6* settings when Global enable setting EICIS := Y.

Table 8.6   Main Board Control Inputs

Setting	Prompt	Default Value	Increment
IN101PU	Input IN101 Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN101DO	Input IN101 Dropout Delay (0.0–30 ms)	2.0[a]	0.5
•	•	•	•
•	•	•	•
•	•	•	•
IN107PU	Input IN107 Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN107DO	Input IN107 Dropout Delay (0.0–30 ms)	2.0[a]	0.5

[a] Set to Global setting IN1XXD when EICIS := N.

Make *Table 8.7* settings for Interface Board #1 when Global enable setting EICIS := Y.

Table 8.7   Interface Board #1 Control Inputs

Setting	Prompt	Default Value	Increment
IN201PU	Input IN201 Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN201DO	Input IN201 Dropout Delay (0.0–30 ms)	2.0[a]	0.5
•	•	•	•
•	•	•	•
•	•	•	•
IN2*mm*PU[b]	Input IN2*mm* Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN2*mm*DO[b]	Input IN2*mm* Dropout Delay (0.0–30 ms)	2.0[a]	0.5

[a] Set to Global setting IN2XXD when EICIS := N.

[b] *mm* is the number of available input contacts on the interface board.

Make *Table 8.8* settings for Interface Board #2 when Global enable setting EICIS := Y.

Table 8.8   Interface Board #2 Control Inputs

Setting	Prompt	Default Value	Increment
IN301PU	Input IN301 Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN301DO	Input IN301 Dropout Delay (0.0–30 ms)	2.0[a]	0.5
• • •	• • •	• • •	• • •
IN3*mm*PU[b]	Input IN3*mm* Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN3*mm*DO[b]	Input IN3*mm* Dropout Delay (0.0–30 ms)	2.0[a]	0.5

[a] Set to Global setting IN3XXD when EICIS := N.
[b] *mm* is the number of available input contacts on the interface board.

Make *Table 8.9* settings for Interface Board #3 when Global enable setting EICIS := Y.

Table 8.9   Interface Board #3 Control Inputs

Setting	Prompt	Default Value	Increment
IN401PU	Input IN401 Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN401DO	Input IN401 Dropout Delay (0.0–30 ms)	2.0[a]	0.5
• • •	• • •	• • •	• • •
IN4*mm*PU[b]	Input IN4*mm* Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN4*mm*DO[b]	Input IN4*mm* Dropout Delay (0.0–30 ms)	2.0[a]	0.5

[a] Set to Global setting IN4XXD when EICIS := N.
[b] *mm* is the number of available input contacts on the interface board.

Make *Table 8.10* settings for Interface Board #4 when Global enable setting EICIS := Y.

Table 8.10   Interface Board #4 Control Inputs

Setting	Prompt	Default Value	Increment
IN501PU	Input IN501 Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN501DO	Input IN501 Dropout Delay (0.0–30 ms)	2.0[a]	0.5
• • •	• • •	• • •	• • •
IN5*mm*PU[b]	Input IN5*mm* Pickup Delay (0.0–30 ms)	2.0[a]	0.5
IN5*mm*DO[b]	Input IN5*mm* Dropout Delay (0.0–30 ms)	2.0[a]	0.5

[a] Set to Global setting IN5XXD when EICIS := N.
[b] *mm* is the number of available input contacts on the interface board.

Table 8.11   Settings Group Selection

Setting	Prompt	Default Value
SS1	Select Setting Group 1 (SELOGIC Equation)	NA
SS2	Select Setting Group 2 (SELOGIC Equation)	NA
SS3	Select Setting Group 3 (SELOGIC Equation)	NA
SS4	Select Setting Group 4 (SELOGIC Equation)	NA
SS5	Select Setting Group 5 (SELOGIC Equation)	NA
SS6	Select Setting Group 6 (SELOGIC Equation)	NA
TGR	Group Change Delay (1–54000 cycles)	180

Make *Table 8.12* settings if the SEL-487E has low-energy analog (LEA) voltage inputs.

Table 8.12   LEA Ratio Correction Factor

Setting	Prompt	Default Value	Increment
VAVRCF	VAV Ratio Correction Factor (0.500–1.500)	1.000	0.001
VBVRCF	VBV Ratio Correction Factor (0.500–1.500)	1.000	0.001
VCVRCF	VCV Ratio Correction Factor (0.500–1.500)	1.000	0.001
VAZRCF	VAZ Ratio Correction Factor (0.500–1.500)	1.000	0.001
VBZRCF	VBZ Ratio Correction Factor (0.500–1.500)	1.000	0.001
VCZRCF	VCZ Ratio Correction Factor (0.500–1.500)	1.000	0.001

Table 8.13   Frequency Source Selection

Setting	Prompt	Default Value
FRQST	Primary Frequency Source Terminal (OFF, V, Z, ADV)	V
EAFSRC	Alternate Frequency Source (SELOGIC Equation)	NA
VF01	Local Frequency Source 1 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	VAV
VF02	Local Frequency Source 2 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	VBV
VF03	Local Frequency Source 3 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	VCV
VF11	Alternate Frequency Source 1 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	ZERO
VF12	Alternate Frequency Source 2 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	ZERO
VF13	Alternate Frequency Source 3 (ZERO, VAV, VBV, VCV, VAZ, VBZ, VCZ)	ZERO

Table 8.14   Synchronized Phasor Configuration Settings (Sheet 1 of 2)

Setting	Prompt[a]	Default Value
MFRMT	Message Format (C37.118, FM)	C37.118
MRATE[b]	Messages per Second (1, 2, 4, 5, 10, 12, 15, 20, 30, 60)[c]	2
PMAPP	PMU Application (F, N, 1)[d]	N
PMLEGCY	Synchrophasor Legacy Settings (Y, N, N1)	N1
NUMPHDC[b, e]	Number of Data Configurations (1–5)	1
PMSTN*q*[b, f]	Station Name (16 characters)	STATION A
PMID*q*[f]	PMU Hardware ID (1–65534)[g]	1

Table 8.14 Synchronized Phasor Configuration Settings (Sheet 2 of 2)

Setting	Prompt[a]	Default Value
PHVOLT[h]	Include Voltage Terminal (combo of V, Z)	V
PHDATAV[h]	Phasor Data Set, Voltages (V1, PH, ALL, NA)	V1
PHCURR[h]	Include Current Terminal (combo of S, T, U, W, X, Y)	S
PHDATAI[h]	Phasor Data Set, Currents (I1, PH, ALL, NA)	NA

[a] "Combo" means "combination"; enter these "combo "settings delimited with either commas or spaces.

[b] Only available if MFRMT = C37.118.

[c] If NFREQ = 50, then the range is 1, 2, 5, 10, 25, 50.

[d] Option 1 is available only if MRATE = 60.

[e] Only available if PMLEGCY = N or N1.

[f] q = 1–5 (determined by NUMPHDC). If PMLEGCY = Y, then these two settings become PMSTN and PMID.

[g] If MFRMT = FM, range is 0–4294967295.

[h] Only available if PMLEGCY = Y.

Phasors Included in the Data q
Terminal Name, Relay Word Bit, Alternate Terminal Name

Specify the terminal for synchrophasor measurement and transmission in the synchrophasor data stream q.

This is a freeform setting category for enabling the terminals for synchrophasor measurement and transmission. This freeform setting has three arguments. Specify the terminal name (any one of S, T, U, V, W, Y, or Z) for the first argument. Specify any Relay Word bit for the second argument. Specify the alternate terminal name (any one of S, T, U, V, W, X, Y, or Z) for the third argument.

The second and third arguments are optional unless switching between terminals is required. Whenever the Relay Word bit in the second argument is asserted the terminal synchrophasor data are replaced by the alternate terminal data.

Table 8.15 Phasors Included in the Data q

Setting[a]	Prompt	Default Value
PHDVq	Phasor Data Set, Voltages (V1, PH, ALL)[b, c]	V1
PHDIq	Phasor Data Set, Currents (I1, PH, ALL)[b, d]	ALL
PHNRq	Phasor Num. Representation (I = Integer, F = Float)[e]	I
PHFMTq	Phasor Format (R = Rectangular, P = Polar)[f]	R
FNRq	Freq. Num. Representation (I = Integer, F = Float)[e]	I

[a] q = 1–5 (determined by NUMPHDC setting).

[b] When MFRMT = FM, then range is (V1, ALL).

[c] Hidden and forced to PHDATAV if PMLEGCY = Y.

[d] Hidden and forced to PHDATAI if PMLEGCY = Y.

[e] Forced to F when MFRMT = FM and EPMU = Y.

[f] Forced to P when MFRMT = FM and EPMU = Y.

Phasor Aliases in Data Configuration q
Phasor Name, Alias

This is a freeform setting category with two arguments. Specify the phasor name and an optional 16-character alias to be included in the synchrophasor data stream q. See *Table 10.25* and *Table 10.26* for a list of phasor names that the PMU supports. The PMU can be configured for as many as 32 unique phasors for each PMU configuration.

Table 8.16   Phasor Aliases in Data Configuration _q_

Setting	Prompt	Default Value
PMSP*qee*[a, b]	Name of the Synchrophasor (Default Name of Any Synchrophasor)	(blank)
PMSA*qee*[a, b]	Alias of the Synchrophasor (16 characters)	(blank)

[a] _q_ = 1–5 (determined by NUMPHDC setting).

[b] _ee_ = 1-32.

From a terminal emulation program, the setting name is now shown and a freeform settings line appears after a prompt. In QuickSet, the setting name is shown and a field is available to enter the setting.

Synchrophasor Analog Quantities in Data Configuration _q_
Analog Quantity Name, Alias Name

This is a freeform setting category with two arguments. Specify the analog quantity name or its alias to be included in the synchrophasor data stream _q_ (see _Section 12: Analog Quantities_ for a list of analog quantities that the PMU supports). Optionally provide an alias name to use in the synchrophasor configuration message. The PMU can be configured for as many as 16 unique analog quantities for each data configuration _q_. The analog quantities are floating-point values, so each analog quantity the PMU includes will take four bytes.

Table 8.17   Number of Digital Status Words to Include in Stream _q_

Setting	Prompt	Default Value
NUM*ANq*	Number of Analog Quantities (0–16)	0
PMAQ*qcc*[a, b]	Any Analog Quantity (Name of Any Analog Quantity)	(blank)
PMAA*qcc*[a, b]	Alias Name for the Analog Quantity (16 characters)	(blank)

[a] _q_ = 1–5 (determined by NUMPHDC setting).

[b] _cc_ = 1-16.

From a terminal emulation program, the setting name is not shown and a freeform settings line appears after a prompt. In QuickSet, the setting name is shown and a field is available to enter the setting.

Synchrophasor Digitals in Data Configuration _q_
Digital Name, Alias Name

This is a freeform setting category with two arguments. Specify the Relay Word bit name or its alias that you need to include in the synchrophasor data stream _q_ (see _Section 11: Relay Word Bits_ for a list of Relay Word bits that the PMU supports). Optionally, include an alias name as the second parameter to use the synchrophasor configuration message. You can configure the PMU for as many as 64 unique digitals for each data configuration _q_.

Table 8.18   Synchrophasor Digitals in Data Configuration _q_

Setting	Prompt	Default Value
NUM*DWa*	Number of 16-bit Digital Status Words (0, 1, 2, 3, 4)	1
PMDG*qdd*[a, b]	Any Relay Word bit (Name of Any Relay Word Bit)	(blank)
PMDA*qdd*[a, b]	Alias Name for the Analog Quantity (16 characters)	(blank)

[a] _q_ = 1–5 (determined by NUMPHDC setting).

[b] _dd_ = 1-16.

From a terminal emulation program, the setting name is not shown and a freeform settings line appears after a prompt. In QuickSet, the setting name is shown and a field is available to enter the setting.

Table 8.19   Synchronized Phasor Configuration Settings Part 2

Setting	Prompt	Default Value	Increment
TREA[4]	Trigger Reason Bit [4] (SELOGIC Equation)	NA	
PMTRIG	Trigger (SELOGIC Equation)	NA	
PMTEST	PMU in Test Mode (SELOGIC Equation)	NA	
VkCOMP[a]	Comp. Angle Terminal k (–179.99° to 180°)	0.00	0.01
InCOMP[b]	Comp. Angle Terminal n (–179.99° to 180°)	0.00	0.01
PMFRQST	PMU Primary Frequency Source Terminal (V, Z)	V	
PMFRQA	PMU Frequency Application (F, S)	S	
PHCOMP	Freq. Based Phasor Compensation (Y, N)	Y	

[a] k = V and Z.

[b] n = S, T, U, W, X, Y.

Table 8.20   Synchronized Phasor Recorder Settings

Setting	Prompt	Default Value
EPMDR	Enable PMU Data Recording (Y, N)	N
SPMDR	Select Data Configuration for PMU Recording (1–NUMPHDC)	1
PMLER	Length of PMU Triggered Data (2–120 s)	30
PMPRE	Length of PMU Pre-Triggered Data (1–20 s)	5

Table 8.21   Synchronized Phasor Real-Time Control

Setting	Prompt	Default Value	Increment

RTCRATE	Remote Messages Per Second
	    (1, 2, 5, 10, or 50 When NFREQ := 50)
	    (1, 2, 4, 5, 10, 12, 15, 20, 30, or 60 When NFREQ := 60)
		2	

MRTCDLY	Maximum RTC Synchrophasor Packet Delay (20–1000 ms)	500	1

Table 8.22   Time and Date Management (Sheet 1 of 2)

Setting	Prompt	Default Value
DATE_F	Date Format (MDY, YMD, DMY)	MDY
IRIGC[a]	IRIG-B Control Bits Definition (None, C37.118)	None
UTCOFF[b]	Offset From UTC to Local Time (–15.5 to 15.5)	–8.0

Table 8.22   Time and Date Management (Sheet 2 of 2)

Setting	Prompt	Default Value
BEG_DST[c]	Begin DST (hh, n, d, mm, or OFF)	"2, 2, 1, 3"
END_DST	End DST (hh, n, d, mm)	"2, 1, 1, 11"

[a] When EPMU = Y and MFRMT = C37.118, IRIGC is forced to C37.118.

[b] All data, reports, and commands from the relay are stored and displayed in local time, referenced to an internal UTC master clock. Use the UTCOFF setting to specify the time offset from UTC time reference with respect to the relay location. (The only data still displayed in UTC time is streaming synchrophasor and IEC 61850 data.)

[c] The BEG_DST (and END_DST) daylight-saving time setting consists of four fields or OFF:
hh = local time hour (0–23); defines when daylight-saving time begins.
n = the week of the month when daylight-saving time begins (1–3, L); occurs in either the first, second, third, or last week of the month.
d = day of week (1–7); Sunday is the first day of the week.
mm = month (1–12).
OFF = hides the daylight-saving time settings.

Table 8.23   Data Reset Control

Setting	Prompt	Default Value
RST_DEM	Reset Demand Metering (SELOGIC Equation)	NA
RST_PDM	Reset Peak Demand Metering (SELOGIC Equation)	NA
RST_ENE	Reset Energy Metering (SELOGIC Equation)	NA
RSTTRGT	Target Reset (SELOGIC Equation)	NA
RSTDNPE	Reset DNP Fault Summary Data (SELOGIC Equation)	TRGTR
RST_HAL	Reset Warning Alarm Pulsing (SELOGIC Equation)	NA

Table 8.24   DNP

Setting	Prompt	Default Value
EVELOCK	Event Summary Lock Period (0–1000 s)	0
DNPSRC	DNP Session Time Base (LOCAL, UTC)	UTC

Monitor Settings

Table 8.25   Monitor Setting Categories (Sheet 1 of 2)

Settings	Reference
Enables	*Table 8.26*
Station DC Monitor	*Table 8.27*
Breaker Monitor Settings	*Table 8.28*
Through-Fault Monitoring	*Table 8.29*
Thermal Model Configuration	*Table 8.30*
Thermal Probe Selection	*Table 8.31*
Cooling Stage Constants for Transformers	*Table 8.32*
Default Transformer Constants (When EDFTC = Y)	*Table 8.33*
Thermal Loss-of-Life	*Table 8.34*
Thermal Alarm Limits	*Table 8.35*

Table 8.25 Monitor Setting Categories (Sheet 2 of 2)

Settings	Reference
IEC Thermal (49) Elements	*Table 8.36*
Thermal Ambient Compensation	*Table 8.37*

Table 8.26 Enables

Setting	Prompt	Default Value
EDCMON	Station DC Battery Monitor (Y, N)	N
BK_SEL	Breaker Selection (OFF or combo of S, T, U, W, X)[a]	S,T
EBMON	Enable BK Monitoring (OFF or combo of S, T, U, W, X)[a]	OFF
ETHFLTM	Enable Through Fault Monitoring (Y, N)	N
ETHERM	Enable Transformer Thermal Element (Y, N)	N
ETHRIEC	Enable IEC Thermal Element (N, 1–3)	N

[a] "Combo" means "combination of"; enter these "combo" settings delimited with either commas or spaces.

Make the settings in *Table 8.27* if EDCMON = Y.

Table 8.27 Station DC Monitor

Setting	Prompt	Default Value	Increment
DCLFP	Low Level Fail Pickup (OFF, 15–300 Vdc)	100	1
DCLWP	Low Level Warn Pickup (OFF, 15–300 Vdc)	127	1
DCHWP	High Level Warn Pickup (OFF, 15–300 Vdc)	137	1
DCHFP	High Level Fail Pickup (OFF, 15–300 Vdc)	142	1
DCRP	Peak-to-Peak AC Ripple Pickup (1–300 Vac)	9	1
DCGF	Ground Detection Factor (1.00–5.00)	1.05	0.01
RST_BAT	Reset Battery Monitoring (SELOGIC Equation)	NA	

Table 8.28 Breaker Monitor Settings (Sheet 1 of 2)

Setting[a]	Prompt	Default Value	Increment
Bm_ID	Breaker m Identifier (40 characters)	Breaker m	
52A_m	NO Contact Input—BKm (SELOGIC Equation)	IN10n[b]	
BMmTRP	Breaker Monitor Trip—BKm (SELOGIC Equation)	TRIPm	
BMmCLS	Breaker Monitor Close—BKm (SELOGIC Equation)	CLSm	
BmCOSP1	Close/Open Set Point 1—BKm (1–65000 Operations)	1000	1
BmCOSP2	Close/Open Set Point 2—BKm (1–65000 Operations)	100	1
BmCOSP3	Close/Open Set Point 3—BKm (1–65000 Operations)	10	1
BmKASP1[c]	kA Interrupted Set Point 1—BKm (1.0–999 kA)	20.0	0.1
BmKASP2	kA Interrupted Set Point 2—BKm (1.0–999 kA)	60.0	0.1
BmKASP3[c]	kA Interrupted Set Point 3—BKm (1.0–999 kA)	100.0	0.1
BmBCWAT	Contact Wear Alarm Threshold—BKm (0–100%)	90	0.1
BmESTRT	Electrical Slow Trip Alarm Threshold—BKm (1–999 ms)	50	1

Table 8.28   Breaker Monitor Settings (Sheet 2 of 2)

Setting[a]	Prompt	Default Value	Increment
B*m*ESCLT	Electrical Slow Close Alarm Threshold—BK*m* (1–999 ms)	120	1
B*m*MSTRT	Mechanical Slow Trip Alarm Threshold—BK*m* (1–999 ms)	50	1
B*m*MSCLT	Mechanical Slow Close Alarm Threshold—BK*m* (1–999 ms)	120	1
B*m*ITAT	Inactivity Time Alarm Threshold—BK*m* (N, 1–9999 days)	365	1
B*m*MRTIN	Motor Run Time Contact Input—BK*m* (SELOGIC Equation)	NA	
B*m*MRTAT	Motor Run Time Alarm Threshold—BK*m* (1–999 s)	25	1
B*m*KAIAT	kA Interrupt Capacity Alarm Threshold—BK*m* (N, 1–100%)	90	0.1
B*m*MKAI	Maximum kA Interrupt Rating—BK*m* (1–999 kA)	50	1
RST_BK*m*	Reset Monitoring Breaker *m* (SELOGIC Equation)	PLT04	

[a] *m* = S, T, U, W, X.

[b] *n* = 1 if *m* = S; *n* = 2 if *m* = T; *n* = 3 if *m* = U, etc.

[c] The ratio of settings B*m*KASP3/B*m*KASP1 must be in the range: 5 ≤B*m*KASP3/B*m*KASP1 ≤100.

Make *Table 8.29* settings if ETHFLTM := Y.

Table 8.29   Through-Fault Monitoring

Setting	Prompt	Default Value
ETHRFLT	Through-Fault Monitor Enable Condition (SELOGIC Equation)	NA
THFLTD	Through-Fault Terminal (S, T, U, W, X, ST, TU, UW, WX)	S
TFLTIPU	Through-Fault Rated Current Pickup (1.05–20 p.u.)	4.75
THFLTPU	Through-Fault Alarm Pickup (50.0–900.0%)	100.0
TRFRZ	Percentage Transformer Impedance (2.0–40.0%)	10.0

Table 8.30   Thermal Model Configuration

Setting	Prompt	Default Value
TRTYPE	Number of Transformers (1, 3)	1
TRWCON	Transformer Winding Connection (Y, D)	Y
TRWSEL	Transformer Winding Selection (S, T, ..., ST, ..., WX)	S
TRWNOM	Nominal Winding Voltage in kVLL (1.00–1000.00)	132.00
EDFTC	Enable Default Transformer Constants (Y, N)	Y
THWR	TRFR Rated Wdg Temp Rise Over Ambient (55°, 65°C)	65
NUMCS	Number of Cooling Stages (1–3)	1
TRDE	Transformer De-energized (SELOGIC Equation)	NA
D_AMB	Default Ambient Temperature (–50.00° to 100.0°C)	25.0

Table 8.31   Thermal Probe Selection

Setting	Prompt	Default Value
AMB_M	Ambient Temp. Meas. Probe (NA, RTD01–RTD12, RA001–RA256)	NA
AMB_F	Ambient Temp. Fault Condition (SELOGIC Equation)	NA
Ta_OILM[a]	TRFR a Top-Oil Temp. Probe (NA, RTD01–RTD12, RA001–RA256)	NA
TaOIL_F[a]	Ta Oil Temp. Fault Condition (SELOGIC Equation)	NA
AMBRTDF	Default Temp if Amb Temp RTD Fails (BUFF, SET)	SET

[a] a = 1-3.

Table 8.32   Cooling Stage Constants for Transformers

Setting[a]	Prompt	Default Value
TcCSb	TRFR c Cooling Stage b Activation (SELOGIC Equation)	NA
MVAcCSb	TRFR c MVA Rating Cooling Stage b (1.0–1000.0 MVA)	100
TcTHORb	Top-Oil Rise/Amb (0.1°–100.0°C)	See *Table 7.10*
TcTHGRb	Hot-Spot Cond. Rise/Top Oil (0.1°–100.0°C)	See *Table 7.10*
TcRATLb	Ratio Losses (0.1–100.0)	See *Table 7.10*
TcOTRb	Oil Thermal Time Constant (0.10–20.00 hrs)	See *Table 7.10*
TcEXPNb	Oil Exponent (0.1–5.0)	See *Table 7.10*
TcEXPMb	Winding Exponent (0.1–5.0)	See *Table 7.10*
TcTHS	Hot-Spot Thermal Time Constant (0.01–20.00 hr)	See *Table 7.10*

[a] b = c = 1-3 (b is the cooling stage; c is the transformer number).

Table 8.33   Default Transformer Constants (When EDFTC = Y)

IEEE	Cooling Stage Setting	THWR = 55°			THWR = 65°		
		CS=1	CS=2	CS=3	CS=1	CS=2	CS=3
$\Delta\Theta_{TO,R}$	THOR (°C)	45°	40°	37°	55°	50°	45°
$\Delta\Theta_{H,R}$	THGR (°C)	20°	25°	28°	25°	30°	35°
R	RATL	3.0	3.5	5.0	3.2	4.5	6.5
n	EXPN	0.8	0.9	1.0	0.8	0.9	1.0
$\tau_{TO,R}$	OTR	3.0	2.0	1.25	3.0	2.0	1.25
m	EXPM	0.8	0.8	1.0	0.8	0.8	1.0
τH	THS	0.08	0.08	0.08	0.08	0.08	0.08

Table 8.34   Thermal Loss-of-Life

Setting	Prompt	Default Value	Increment
TRLIFE	Nominal Insulation Life (1000–999999 hrs)	180000	1
TdBFFA[a]	Constant to Calc. FAA for TRFR d (0–100000)	0	1

[a] d = 1-3.

Table 8.35   Thermal Alarm Limits

Setting	Prompt	Default Value	Increment
TOT*x*[a]	Top-Oil Temp. Limit *x* (50°–150°C)	95	1
HST*x*[a]	Hot-Spot Limit *x* (80°–300°C)	100	1
T*d*CSEP[b]	TRFR *d* Cooling System Efficiency (5°–100°C)	15	1
FAAL*x*[a]	Aging Acceleration Factor Limit *x* (0.00–599.99)	100.00	0.01
RLOLL	Daily Loss-of-Life Limit (0.00–99.99%)	0.00	0.01
TLOLL	Total Loss-of-Life Limit (0.00–99.99%)	0.00	0.01

[a] *x* = 1 or 2.

[b] *d* = 1-3.

Make the settings in *Table 8.36* if ETHRIEC := 1, 2, or 3.

Table 8.36   IEC Thermal (49) Elements

Setting	Prompt	Default Value
THRO1	Thermal Model 1 Operating Quantity	IASRMS
THRO2	Thermal Model 2 Operating Quantity	IBSRMS
THRO3	Thermal Model 3 Operating Quantity	ICSRMS
IBAS1	Basic Current Value in PU 1 (0.1–3)	1.1
IBAS2	Basic Current Value in PU 2 (0.1–3)	1.1
IBAS3	Basic Current Value in PU 3 (0.1–3)	1.1
IEQPU1	Eq. Heating Current Pick Up Value in PU 1 (0.05–1)	0.05
IEQPU2	Eq. Heating Current Pick Up Value in PU 2 (0.05–1)	0.05
IEQPU3	Eq. Heating Current Pick Up Value in PU 3 (0.05–1)	0.05
KCONS1	Basic Current Correction Factor 1 (0.50–1.5)	1
KCONS2	Basic Current Correction Factor 2 (0.50–1.5)	1
KCONS3	Basic Current Correction Factor 3 (0.50–1.5)	1
TCONH1	Heating Thermal Time Constant 1 (1–500 min)	60
TCONH2	Heating Thermal Time Constant 2 (1–500 min)	60
TCONH3	Heating Thermal Time Constant 3 (1–500 min)	60
TCONC1	Cooling Thermal Time Constant 1 (1–500 min)	60
TCONC2	Cooling Thermal Time Constant 2 (1–500 min)	60
TCONC3	Cooling Thermal Time Constant 3 (1–500 min)	60
THLA1	Thermal Level Alarm Limit 1 (1.00–100%)	50
THLA2	Thermal Level Alarm Limit 2 (1.00–100%)	50
THLA3	Thermal Level Alarm Limit 3 (1.00–100%)	50
THLT1	Thermal Level Trip Limit 1 (1.00–100%)	80
THLT2	Thermal Level Trip Limit 2 (1.00–100%)	80
THLT3	Thermal Level Trip Limit 3 (1.00–100%)	80

Table 8.37   Thermal Ambient Compensation

Setting	Prompt	Default Value
TMAX1	Maximum Temperature of the Equipment 1 (80–300 C)	155
TMAX2	Maximum Temperature of the Equipment 2 (80–300 C)	155
TMAX3	Maximum Temperature of the Equipment 3 (80–300 C)	155

Group Settings

Table 8.38   Group Setting Categories

Settings	Reference
Relay Configuration	*Table 8.39*
Current Transformer Data	*Table 8.40*
Potential Transformer Data	*Table 8.41*
Voltage Reference Terminal Selection	*Table 8.42*
Differential-Element Configuration and Data	*Table 8.43*
Restricted Earth Fault Element	*Table 8.44*
Overcurrent Elements for Terminals	*Table 8.45*
Terminal *m* Phase Overcurrent Level *a*[a, b]	*Table 8.46*
Terminal *m* Negative-Sequence Overcurrent Element Levels[a]	*Table 8.47*
Terminal *m* Zero-Sequence Overcurrent Element Levels[a]	*Table 8.48*
Directional Element Blocking	*Table 8.49*
Inverse-Time Overcurrent Elements	*Table 8.50*
Terminal Current Unbalance Elements	*Table 8.51*
Volts Per Hertz Elements	*Table 8.52*
Volts Per Hertz Level 2 Definite Time	*Table 8.53*
Volts Per Hertz Level 2, User-Defined Curve *h*[c]	*Table 8.54*
Synchronism-Check (25) Elements	*Table 8.55*
Undervoltage (27) Elements	*Table 8.56*
Overvoltage (59) Elements	*Table 8.57*
Frequency (81) Elements	*Table 8.58*
Breaker Failure Logic	*Table 8.59*
Overpower (32) Elements	*Table 8.60*
Underpower (32) Elements	*Table 8.61*
Demand Metering Elements	*Table 8.62*
Trip Logic	*Table 8.63*
Close Logic	*Table 8.64*

[a] *m* = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

[b] *a* = 1–3.

[c] *h* = 1 or 2.

Table 8.39   Relay Configuration

Setting	Prompt[a]	Default Value
ECTTERM	Enable Current Terminals (OFF or combo of S, T, U, W, X)	S, T
EPTTERM	Enable Voltage Terminals (OFF or combo of V, Z)	OFF
E87	Enable Differential Terminals (OFF or combo of S, T, U, W, X)	S, T
EREF	Enable Restricted Earth Fault Element (N, 1–3)	N
E50[b]	Enable 50 Elements (OFF or combo of S, T, U, W, X, ST, TU, UW, WX)	OFF
E51	Enable Inverse Time Overcurrent Elements (N, 1–10)	N
E46	Enable Current Unbalance (OFF or combo of S, T, U, W, X)	OFF
E59	Enable Over Voltage Elements (N, 1–5)	N
E27	Enable Under Voltage Elements (N, 1–5)	N
E81	Enable Frequency Elements (N, 1–6)	N
E24	Enable Volts per Hertz Element (Y, N)	N
E25	Enable Synchronization Check (OFF or combo of S, T, U, W, X)	OFF
EBFL	Enable Bkr Failure Protection (OFF or combo of S, T, U, W, X)	OFF
BF_SCHM	Breaker Failure Scheme (Y, Y1)	Y
EPCAL	Enable Power Calculation Terminals (OFF or combo of S, T, U, W, X)	OFF
E32	Enable Over/Under Power Elements (N, 1–10)	N
EDEM	Enable Demand Metering (N, 1–10)	N

[a] "Combo" means "combination"; enter these "combo" settings delimited with either commas or spaces.

[b] Combination terminals are only available for channels with the same nominal current rating, same CT connection (CTCON), same current transformer ratio (CTR), and same voltage reference (VREF).

Table 8.40   Current Transformer Data

Setting	Prompt	Default Value	Increment
CTRm[a]	Current Trans. Ratio Terminal m (1–50000)	100	1
CTCONm[a]	Current Trans. Connection Terminal m (Y, D)	Y	
CTRYØ[b]	Current Trans. Ratio Terminal YØ (1–50000)	100	1

[a] m = S, T, U, W, X.

[b] Ø = 1, 2, 3.

Table 8.41   Potential Transformer Data

Setting[a]	Prompt	Default Value	Increment
PTRk	Potential Trans. Ratio Terminal k (1.0–10000.0)	2000.0	0.1
PTCONk	Potential Trans. Connection Terminal k (Y, D)	Y	
PTCOMPk	PT Comp. Angle Terminal k (–179.99 to 180 deg)	0.00	0.01
VNOMk	PT Nominal Voltage (L-L) Term. k (30–300 V, sec)	110	1

[a] k = V, Z.

Table 8.42   Voltage Reference Terminal Selection

Setting	Prompt	Default Value
VREF*m*[a]	Voltage Reference For Terminal *m* (OFF, V, Z)	OFF

[a] *m* = S, T, U, W, X.

Table 8.43   Differential-Element Configuration and Data

Setting	Prompt	Default Value	Increment
E87T*m*[a]	Terminal *m* included in 87 Element (SELOGIC Equation)	1	
ICOM	Internal CT Conn. Compensation Enabled (Y, N)	Y	
T*m*CTC[a]	Terminal *m* CT Conn. Compensation (0–12)	12	1
MVA	Transformer Max. Power Capacity (OFF, 1–5000 MVA)	OFF	1
VTERM*m*[a]	Terminal *m* Line-to-Line Voltage (1.00–1000 kV)	275.00	0.01
TAP*m*[a]	Terminal *m* Current Tap (0.5–175 A, secondary)[b]	1.0	0.01
O87P	Differential Element Oper. Current PU (0.10–4)	0.50	0.01
SLP1	Slope 1 Percentage (5.00–90%)	35.00	0.01
SLP2	Slope 2 Percentage (5.00–90%)	75.00	0.01
E87U	Enable Unres. Diff. Elem. (OFF or combo of F, R, W)[c]	F	
U87P	Unrestrained Element Current PU (1.00–20)	8.00	0.01
DIOPR	Incr. Operate Current Threshold PU (0.10–10)	1.20	0.01
DIRTR	Incr. Restraint Current Threshold PU (0.10–10)	1.20	0.01
E87HB	Enable Harmonic Blocked Diff. Element (Y, E, N)	N	
E87HR	Enable Harmonic Restrained Diff. Element (Y, W, N)	Y	
E87Q	Enable Neg. Seq. Diff. Element (Y, E, N)	Y	
E87UNB	Enable Waveshape Unblocking Logic (Y, N)	N	
PCT2	Second-Harmonic Percentage (OFF, 5–100%)	15	1
PCT4	Fourth-Harmonic Percentage (OFF, 5–100%)	15	1
PCT5	Fifth-Harmonic Percentage (OFF, 5–100%)	35	1
TH5P	Fifth-Harmonic Alarm Threshold PU (OFF, 0.2–3.2)	OFF	0.1
TH5D	Fifth-Harmonic Alarm Delay (0.000–8000 cyc)	30.000	0.125
87CORE	XFMR Core Type, Three Legs or Single Cores (T, S)	T	
87QP	Neg. Seq. Differential Op current (0.05–1 pu)	0.30	0.01
SLPQ1	Neg. Seq. Differential Slope (5–100%)	25	1
87QD	Neg. Seq. Differential Element Delay (2.000–9999 cyc)	10.000	0.125

[a] *m* = S, T, U, W, X.

[b] Range is 0.10–35.00 A, sec if the Terminal *m* uses a 1 A nominal CT.

[c] "Combo" means "combination"; enter these "combo" settings delimited with either commas or spaces.

Table 8.44   Restricted Earth Fault Element

Setting[a]	Prompt	Default Value	Increment
REFRF*a*	Restraint Qty REF Elem. *a* (OFF or combo of S, T, U, W, X)[b]	OFF	
REF50G*a*	Residual Current Sensitivity Pickup (0.05–3 pu)	0.25	0.01
TCREF*a*	Torque Control REF Element *a* (SEL$_{\text{OGIC}}$ Equation)	1	
REF50P*a*	REF Op. Current Inst O/C *a* Pickup (OFF, 0.25–100 A, sec)[c]	OFF	0.01
REF50D*a*	REF Inst O/C *a* Delay (0.00–16000 cyc)	10.00	0.25
REF51P*a*	REF Inv. Time O/C *a* P/U (OFF, 0.25–16 A, sec)[d]	OFF	0.01
REF51C*a*	REF Inv. Time O/C *a* Curve (U1–U5, C1–C5)	U1	
RF51TD*a*	REF Inv. Time O/C *a* Time Dial (0.50–15)	0.50	0.01
RF51RS*a*	REF Inv. Time O/C *a* EM Reset (Y, N)	N	
RF51TC*a*	REF Inv. Time O/C *a* Torque Cont. (SEL$_{\text{OGIC}}$ Equation)	1	

[a] *a* = 1–3, as determined by the EREF setting.

[b] "Combo" means "combination"; enter these "combo" settings delimited with either commas or spaces.

[c] Range is 0.05–20.00 if the terminal uses 1 A nominal CTs.

[d] Range is 0.05–3.20 if the selected terminal, REFRF*a*, uses 1 A nominal CTs.

Table 8.45   Overcurrent Elements for Terminals

Setting[a]	Prompt	Default Value	Increment
E50*m*	Type of O/C Elements Enabled Terminal *m* (Combo of P, Q, G)[b]	P	
E67*m*	Enable Directional Elements Terminal *m* (Y, N)	N	
CTP*m*	Current Transformer Polarity Terminal *m* (P, N)	P	
Z1ANG*m*	Pos.-Seq. Line Impedance Angle (5.00–90 deg)	89.00	0.01
Z0ANG*m*	Zero-Seq. Line Impedance Angle (5.00–90.00)	85.00	0.01
EADVS	Enable Advanced Settings Terminal *n* (Y, N)	N	
50FP*m*	Forward Dir. O/C Pickup (0.25–5.0 A, sec)[c]	0.60	0.01
50RP*m*	Reverse Dir. O/C Pickup (0.25–5.00 A, sec)[c]	0.40	0.01
Z2F*m*	Forward Dir. Z2 Threshold (–64.00 to 64.00 ohms, sec)[d]	–0.10[e]	0.01
Z2R*m*	Reverse Dir. Z2 Threshold (–64.00 to 64.00 ohms, sec)	0.10[f]	0.01
A2*m*	Pos.-Seq. Restraint Factor, I2/I1 (0.02–0.50)	0.10	0.01
ORDER*m*	Ground Dir. Element Priority (Q, V, QV, VQ)	QV	
K2*m*	Zero-Seq. Restraint Factor, I2/I0 (0.10–1.20)	0.20	0.01
Z0F*m*	Forward Dir. Z0 Threshold (–64.00 to 64.00 ohms, sec)[d]	–0.10[e]	0.01
Z0R*m*	Reverse Dir. Z0 Threshold (–64.00 to 64.00 ohms, sec)[d]	0.10[f]	0.01
A0*m*	Pos.-Seq. Restraint Factor, I0/I1 (0.02–0.50)	0.10	0.01

[a] *m* = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

[b] "Combo" means "combination"; enter these "combo" settings delimited with either commas or spaces.

[c] Range is 0.05–1.0 A, sec if Terminal *m* uses 1 A nominal CTs.

[d] Range is –320.00 to 320.00 ohms, sec if Terminal *m* uses 1 A nominal CTs.

[e] Default value is –0.5 if Terminal *m* uses 1 A nominal CTs.

[f] Default value is 0.5 if Terminal *m* uses 1 A nominal CTs.

Table 8.46   Terminal *m* Phase Overcurrent Element Level *a*

Setting[a, b]	Prompt	Default Value	Increment
50*m*P*a*P	Phase Inst O/C Pickup Level *a* (OFF, 0.25–100 A, sec)[c]		0.01
67*m*P*a*TC	Phase Inst O/C level *a* Torque Ctrl (SELOGIC Equation)	*m*F32P AND PLT03	
67*m*P*a*D	Phase Inst O/C level *a* Delay (0.00–16000 cyc)	0.00	0.25

[a] *m* = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).
[b] *a* = 1-3.
[c] Range is 0.05-20 A, sec if Terminal *m* uses 1 A nominal CTs.

Table 8.47   Terminal *m* Negative-Sequence Overcurrent Element Levels[a]

Setting[b]	Prompt	Default Value	Increment
50*m*Q*a*P	Neg-Seq Inst O/C pickup level *a* (OFF, 0.25–100 A, sec)[c]	OFF	0.01
67*m*Q*a*TC	Neg-Seq Inst O/C level *a* Torque Ctrl (SELOGIC Equation)	*m*F32Q	
67*m*Q*a*D	Neg-Seq Inst O/C level *a* Delay (0.00–16000 cyc)	0.00	0.25

[a] *m* = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).
[b] *a* = 1-3.
[c] Range is 0.05-20 A, sec if Terminal *m* uses 1 A nominal CTs.

Table 8.48   Terminal *m* Zero-Sequence Overcurrent Element Levels

Setting[a, b]	Prompt	Default Value	Increment
50*m*G*a*P	Zero-Seq Inst O/C Pickup Level *a* (OFF, 0.25–100 A, sec)[c]	OFF	0.01
67*m*G*a*TC	Zero-Seq Inst O/C Lvl *a* Torque Ctrl (SELOGIC Equation)	*m*F32G	
67*m*G*a*D	Zero-Seq Inst O/C Lvl *a* Delay (0.00–16000 cyc)		0.25

[a] *m* = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).
[b] *a* = 1-3.
[c] Range is 0.05-20 A, sec if Terminal *m* uses 1 A nominal CTs.

Table 8.49   Directional Element Blocking

Setting	Prompt	Default Value
DIRBLK*m*[a]	Block *m* Phase and Ground Dir. Elem. (SELOGIC Equation)	87QB

[a] *m* = S, T, U, W, X, 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

Table 8.50   Inverse-Time Overcurrent Elements

Setting[a]	Prompt	Default Value
51O*xx*	Inv. Time O/C *xx* Operating Quantity	IMAXSF
51P*xx*	Inv. Time O/C *xx* Pickup Value (SEL Math Equation)[b]	1.00
51C*xx*	Inv. Time O/C *xx* Curve Selection (U1–U5, C1–C5)	U1
51TD*xx*	Inv. Time O/C *xx* Time Dial (SEL Math Equation)[c]	1.00
51RS*xx*	Inv. Time O/C *xx* EM Reset (Y, N)	N
51TC*xx*	Inv. Time O/C *xx* Torque Control (SELOGIC Equation)	PLT09

[a] *xx* = 01-10.

[b] Usable range depends on the quantity selected for 51O*xx*. For a quantity on a 5 A terminal, the range is 0.25–16.0 A, sec. For a quantity on a 1 A terminal, the range is 0.05–3.2 A, sec. See *Selectable Time-Overcurrent Element (51) on page 5.57* for more details.

[c] Usable range depends on the curve selected for 51C*xx*. For curves U1–U5, the range is 0.50–15.0. For curves C1–C5, the range is 0.05–1.00. See *Selectable Time-Overcurrent Element (51) on page 5.57* for more details.

Table 8.51   Terminal Current Unbalance Elements

Setting[a]	Prompt	Default Value	Increment
46*m*PU	Terminal *m* Current Unbalance Pickup (5%–100%)	20	1
46*m*CD	Terminal *m* Close Delay (0.00–6000 cyc)	10.00	0.25
46*m*BD	Terminal *m* Current Unbalance Delay (0.00–6000 cyc)	10.00	0.25

[a] *m* = S, T, U, W, X.

Table 8.52   Volts-Per-Hertz Elements

Setting	Prompt	Default Value	Increment
24VSRC	Voltage Source for V/Hz Calculation (V, Z)	V	
24D1P	Level 1 Volts/Hertz P/U (100%–200%)	110	1
24D1D	Level 1 Time Delay (0.04–6000 s)	10.00	0.01
24TC	Volts/Hertz Torque Control (SELOGIC Equation)	1	
24CCS	Level 2 Composite Curve (OFF, DD, U1, U2)	OFF	

Table 8.53   Volts-Per-Hertz Level 2 Definite Time

Setting	Prompt	Default Value	Increment
24D2P1	Level 2 Volts/Hertz PU1 (100%–200%)	105	1
24D2D1	Level 2 Time Delay 1 (0.04–6000 s)	10.00	0.01
24D2P2	Level 2 Volts/Hertz PU2 (101%–200%)	110	1
24D2D2	Level 2 Time Delay 2 (0.04–6000 s)	5.00	0.01

Table 8.54   Volts-Per-Hertz Level 2, User-Defined Curve *h*[a]

Setting	Prompt	Default Value	Increment
24U*h*TC	User Defined Curve *h* Torque Control (SELOGIC Equation)	1	
24U*h*NP	Number of Points on User *h* Curve (3–20)	3	1
24U*hxx*[b]	User Def. Curve *h*, Point *xx* (100%–200%, 0.04–6000 s)	200, 400.00	1, 0.01
24U*h*CR	User Def. Curve *h* Reset Time (0.01–400 s)	0.01	0.01

[a] *h* = 1, 2.

[b] *xx* = 01-20.

Table 8.55   Synchronism-Check (25) Elements (Sheet 1 of 2)

Setting[a]	Prompt	Default Value	Increment
EISYNC	Enable Independent Synch Check Elements (Y, N)	N	
SYNCP	Synchronism Reference (VAV, VBV, VCV, VAZ, VBZ, VCZ)[b]	VAV	
25_SCHM	Synchronism-Check Voltage Scheme (Y, Y1, Y2)	Y	
25VL[c]	Voltage Window Low Threshold (20.0–200 V, sec)	55.0	0.1
25VH[c]	Voltage Window High Threshold (20.0–200 V, sec)	70.0	0.1
25VDIF[d]	Synchronism Voltage Difference Check (50.0–100.0 V, sec)	10.0	0.1
SYNCP*m*[e]	BK*m* Synch Reference (VAV, VBV, VCV, VAZ, VBZ, VCZ)	VAV	
KP*m*M[e]	BK*m* Ref Src Ratio Factor (0.10–3)	1.00	0.01
KP*m*A[e]	BK*m* Ref Src Angle Shift (–179.99 to 180 deg)	0.00	0.01
ALTP*m*1[e]	BK*m* Alt Ref Source Selection Logic 1 (SELOGIC Eq)	NA	
ASYNP*m*1[e]	BK*m* Alt Ref Src 1 (VAV, VBV, VCV, VAZ, VBZ, VCZ)	VCZ	
AKP*m*1M[e]	BK*m* Alt Ref Src 1 Ratio Factor (0.10–3)	1.00	0.01
AKP*m*1A[e]	BK*m* Alt Ref Src 1 Ang Shift (–179.99 to 180 deg)	0.00	0.01
ALTP*m*2[e]	BK*m* Alt Ref Source Selection Logic 2 (SELOGIC Eq)	NA	
ASYNP*m*2[e]	BK*m* Alt Ref Src 2 (VAV, VBV, VCV, VAZ, VBZ, VCZ)	VCZ	
AKP*m*2M[e]	BK*m* Alt Ref Src 2 Ratio Factor (0.10–3)	1.00	0.01
AKP*m*2A[e]	BK*m* Alt Ref Src 2 Ang Shift (–179.99 to 180 deg)	0.00	0.01
SYNCS*m*	Synchronism Source *m* (VAV, VBV, VCV, VAZ, VBZ, VCZ)[b]	VAZ	
KS*m*M	Synchronism Source *m* Ratio Factor (0.10–3)	1.00	0.01
KS*m*A	Synchronism Source *m* Angle Shift (–179.99 to +180 deg)	0.00	0.01
ALTS*m*[f]	Alternative Synchronism Source *m* (SELOGIC Equation)	NA	
ASYNCS*m*[f]	Alternative Synchronism Source *m* (VAV, VBV, VCV, VAZ, VBZ, VCZ)[b]	VBZ	
AKS*m*M[f]	Alternative Synchronism Source *m* Ratio Factor (0.10–3)	1.00	0.01

Table 8.55 Synchronism-Check (25) Elements (Sheet 2 of 2)

Setting[a]	Prompt	Default Value	Increment
AKS*m*A[f]	Alternative Synchronism Source *m* Angle Shift (–179.99 to +180 deg)	0.00	0.01
25SFBK*m*[g]	Maximum Slip Frequency BK*m* (OFF, 0.005–0.5 Hz)	0.050	0.001
ANG1BK*m*	Maximum Angle Difference 1 BK*m* (3.0–80 deg)	10.0	0.1
ANG2BK*m*	Maximum Angle Difference 2 BK*m* (3.0–80 deg)	10.0	0.1
TCLSBK*m*[g]	Breaker *m* Close Time (1.00–30 cyc)	8.00	0.25
BSYNBK*m*	Block Synchronism-Check—BK*m* (SELOGIC Equation)	NA	

[a] *m* = S, T, U, W, X.

[b] Range is determined by EPTTERM setting. SYNCP, SYNCS*m*, and ASYNCS*m* must be unique per Breaker *m*; otherwise, the following warning message is displayed: "Polarizing and synchronizing voltage sources are not unique."

[c] Hidden if 25_SCHM does not include Y or Y2.

[d] Hidden if 25_SCHM does not include Y1 or Y2.

[e] Hidden if EISYNC = N

[f] Set ALTS*m* to a value other than NA to enable the other alternative settings.

[g] When maximum slip frequency setting 25SFBK*m* = OFF, the relay implements the uncompensated synchronism-check logic and Breaker *m* close time setting (TCLSBK*m*) is hidden.

Table 8.56 Undervoltage (27) Elements

Setting[a]	Prompt	Default Value	Increment
27O*n*	U/V Element *n* Operating Quantity	VNMINVF	
27P*n*P1	U/V Element *n* Level 1 P/U (2.00–300 V, sec)[b]	20.00	0.01
27TC*n*	U/V Element *n* Torque Control (SELOGIC Equation)	1	
27P*n*P2	U/V Element *n* Level 2 P/U (2.00–300 V, sec)[b]	15.00	0.01
27P*n*D1	U/V Element *n* Level 1 Delay (0.00–16000 cyc)	10.00	0.25

[a] *n* = 1-5.

[b] Range is 4.00–520 V, sec for minimum, maximum, and phase-to-phase elements.

Table 8.57 Overvoltage (59) Elements

Setting[a]	Prompt	Default Value	Increment
59O*n*	O/V Element *n* Operating Quantity	VNMAXVF	
59P*n*P1	O/V Element *n* Level 1 P/U (2.00–300 V, sec)[b]	76.00	0.01
59TC*n*	O/V Element *n* Torque Control (SELOGIC Equation)	1	
59P*n*D1	O/V Element *n* Level 1 Delay (0.00–16000 cyc)	10.00	0.25
59P*n*P2	O/V Element *n* Level 2 P/U (2.00–300 V, sec)[b]	80.00	0.01

[a] *n* = 1-5.

[b] Range is 4.00–520 V, sec for minimum, maximum, and phase-to-phase elements.

Table 8.58 Frequency (81) Elements

Setting[a]	Prompt	Default Value	Increment
81UVSP	81 Element Under Voltage Super (20.00–200 V, sec)	85.00	0.01
81D*n*P	Level *n* Pickup (40.01–69.99 Hz)	61.00	0.01
81D*n*D	Level *n* Time Delay (0.04–400 s)	2.00	0.01

[a] n = 1-6.

Table 8.59   Breaker Failure Logic

Setting[a]	Prompt	Default Value	Increment
EXBFm	Enable External Breaker Fail—BKR m (SELOGIC Equation)	NA	
EBFPUm	Ext. Brkr Fail Init PU Delay—BKR m (0.00–6000 cyc)	6.00	0.125
50FPUm	Fault Current Pickup—BKR m (0.50–50 A, sec)[b]	10.00	0.01
BFPUm	Brkr Fail Init Pickup Delay—BKR m (0.00–6000 cyc)	6.00	0.125
RTPUm	Retrip Delay—BKR m (0.00–6000 cyc)	3.00	0.125
BFm	Breaker Fail Initiate—BKR m (SELOGIC Equation)	NA	
ATBFIm	Alt Breaker Fail Initiate—BKR m (SELOGIC Equation)	NA	
ENINBFm	Enable Neutral Breaker Failure—BKR m (SELOGIC Equation)	NA	
INFPUm	Neutral Current Pickup—BKR m (0.50–50 A, sec)[c]	0.50	0.01
EBFISm	Breaker Fail Initiate Seal-In—BKR m (Y, N)	N	
BFISPm	Brkr Fail Init Seal-In Delay—BKR m (0.00–1000 cyc)	3.00	0.125
BFIDOm	Brkr Fail Init Dropout Delay—BKR m (0.00–1000 cyc)	1.50	0.125

[a] m = S, T, U, W, X.
[b] Range is 0.10–10 A, sec if Terminal m uses 1 A nominal CTs.
[c] Range is 0.10–10.00 A, sec if Terminal m uses 1 A nominal CTs.

Table 8.60   Overpower (32) Elements

Setting[a]	Prompt	Default Value	Increment
32OPOgg	Overpower Op. Qty. Elem gg	OFF	
32OPPgg	Overpower Pickup Elem gg (–20000.00 to 20000 VA, sec)[b, c]	2000.00	0.01
32OPDgg	Overpower Delay Elem gg (0.00–16000 cyc)	10.00	0.25
E32OPgg	Enable Overpower Elem gg (SELOGIC Equation)	NA	

[a] gg = 01-10.
[b] Settings range is –20000 to –5, 5 to 20000 VA, sec.
[c] Range is –4000 to –1, 1 to 4000 VA, sec if the selected element, 32OPOgg, is on a 1 A nominal CT.

Table 8.61   Underpower (32) Elements

Setting[a]	Prompt	Default Value	Increment
32UPOgg	Underpower Op. Qty. Elem gg	OFF	
32UPPgg	Underpower Pickup Elem gg (–20000.00 to 20000 VA, sec)[b, c]	5.00	0.01
32UPDgg	Underpower Delay Elem gg (0.00–16000 cyc)	10.00	0.25
E32UPgg	Enable Underpower Elem gg (SELOGIC Equation)	NA	

[a] gg = 01-10.
[b] Settings range is –20000 to –5, 5 to 20000 VA, sec.
[c] Range is –4000.00 to 4000 VA, sec if the selected element, 32UPOgg, is on a 1 A nominal CT.

Table 8.62   Demand Metering Elements

Setting[a]	Prompt	Default Value	Increment
DMTY*gg*	Demand Met. Type Element *gg* (THM, ROL)	THM	
DMOQ*gg*	Demand Met. Op. Qty. Element *gg*	IMXSRS	
DMPU*gg*	Demand Met. P/U Element *gg* (0.05–16 A, sec)[b]	2.00	0.01
DMTC*gg*	Demand Met. Time Const. Element *gg* (5, 10, ..., 300 min)	5	5
EDM*gg*	Enable Demand Metering Element *gg* (SELOGIC Equation)	1	

[a]   *gg* = 01-10.

[b]   Range is 0.01–3.2 A, sec if the selected element, DMOQ*gg*, is on a 1 A nominal CT.

Table 8.63   Trip Logic

Setting	Prompt	Default Value	Increment
TRXFMR	Trip Transformer (SELOGIC Equation)	87R OR REFF1	
ULTXFMR	Unlatch Trip Transformer (SELOGIC Equation)	TRGTR	
TR*m*[a]	Trip Terminal *m* (SELOGIC Equation)	50*m*P1 OR 50*m*Q1	
ULTR*m*[a]	Unlatch Trip Terminal *m* (SELOGIC Equation)	TRGTR	
TDURD	Minimum Trip Duration (2.000–8000 cyc)	5.00	0.125
ER	Event Report Trigger Equation (SELOGIC Equation)	50SQ1 OR 50TQ1	
FAULT	Fault Condition Equation (SELOGIC Equation)	50SQ1 OR 50TQ1	

[a]   *m* = S, T, U, W, X.

Table 8.64   Close Logic

Setting[a]	Prompt	Default Value	Increment
CL*m*	Close Terminal *m* (SELOGIC Equation)	LB10	
ULCL*m*	Unlatch Close Terminal *m* (SELOGIC Equation)	52CL*m*	
CFD	Close Failure Delay (OFF, 2.00–99999 cyc)	4.00	0.125

[a]   *m* = S, T, U, W, X.

Protection Logic: Default Settings

The SEL-487E provides 250 lines of freeform SELOGIC control equations in each of the six settings groups. The following are the protection logic default settings.

```
1: # BREAKER S OPEN AND CLOSE CMD
2: PCT01IN := PB1 AND 52CLS #CMD TO OPEN BKR S
3: PCT01PU := 60
4: PCT01DO := 0
5: PCT02IN := PB7 AND NOT 52CLS #CMD TO CLOSE BKR S
6: PCT02PU := 60
7: PCT02DO := 0
```

8: # BREAKER T OPEN AND CLOSE CMD
9: PCT03IN := PB2 AND 52CLT #CMD TO OPEN BKR T
10: PCT03PU := 60
11: PCT03DO := 0
12: PCT04IN := PB8 AND NOT 52CLT #CMD TO CLOSE BKR T
13: PCT04PU := 60
14: PCT04DO := 0
15: PLT03S := PB3_PUL AND NOT PLT03 # DIRECTIONAL OVER-
CURRENT ENABLED
16: PLT03R := PB3_PUL AND PLT03
17: PLT04S := PB4_PUL AND NOT PLT04 # BREAKER WEAR LEVELS
RESET
18: PLT04R := (PB4_PUL AND PLT04) OR RST_BKS OR RST_BKT
19: PLT09S := PB9_PUL AND NOT PLT09 # ADAPTIVE OVERCUR-
RENT ENABLED
20: PLT09R := PB9_PUL AND PLT09

Automation Freeform SELᴏɢɪᴄ Control Equations

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a description of automation SELOGIC control equations. The SEL-487E supports 10 blocks of 100 lines.

Output Settings

Section 12: Settings in the SEL-400 Series Relays Instruction Manual contains a description of the output settings of the relay. This section describes SEL-487E specific default values.

Table 8.65   Main Board Default Values

Label	Default Value
OUT101	TRIPS OR PCT01Q
OUT102	TRIPT OR PCT03Q
OUT103	PCT02Q
OUT104	PCT04Q
OUT105	NA
OUT106	NA
OUT107	NA
OUT108	NOT (SALARM OR HALARM)

Front-Panel Settings

See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for a complete description of front-panel settings. This section lists the SEL-487E specific default settings values.

Table 8.66 Front-Panel Settings Defaults (Sheet 1 of 3)

Label	Default Value
FP_TO	15
EN_LEDC	G
TR_LEDC	R
PB1_LED	NOT 52CLS
PB1_COL	GO
PB2_LED	NOT 52CLT
PB2_COL	GO
PB3_LED	PLT03
PB3_COL	AO
PB4_LED	RST_BKS OR RST_BKT
PB4_COL	AO
PB5_LED	NA
PB5_COL	AO
PB6_LED	NA
PB6_COL	AO
PB7_LED	52CLS
PB7_COL	RO
PB8_LED	52CLT
PB8_COL	RO
PB9_LED	PLT09
PB9_COL	AO
PB10LED	NA
PB10COL	AO
PB11LED	NA
PB11COL	AO
PB12LED	NA
PB12LED	AO
T1_LED	TRIPS
T1LEDL	Y
T1LED	RO
T2_LED	TRIPT
T2LEDL	Y
T2LEDC	RO
T3_LED	87RA OR 87UA
T3LEDL	Y
T3LEDC	RO
T4_LED	87RB OR 87UB
T4LEDL	Y
T4LEDC	RO
T5_LED	87RC OR 87UC
T5LEDL	Y

Table 8.66 Front-Panel Settings Defaults (Sheet 2 of 3)

Label	Default Value
T5LEDC	RO
T6_LED	REF51T1
T6LEDL	Y
T6LEDC	RO
T7_LED	FBFS
T7LEDL	Y
T7LEDC	RO
T8_LED	FBFT
T8LEDL	Y
T8LEDC	RO
T9_LED	50TP1 OR 67TP1T OR 51T01
T9LEDL	Y
T9LEDC	RO
T10_LED	24D1T OR 24D2T OR 24U1T OR 24U2T
T10LEDL	Y
T10LEDC	RO
T11_LED	271P1T OR 591P1T
T11LEDL	Y
T11LEDC	RO
T12_LED	81D1T
T12LEDL	Y
T12LEDC	RO
T13_LED	32OPT01 OR 32UPT01
T13LEDL	Y
T13LEDC	RO
T14_LED	NA
T14LEDL	Y
T14LEDC	AO
T15_LEDC	87ABK5 OR 87BBK5 OR 87CBK5 OR 87XBK2
T15LEDL	N
T15LEDC	AO
T16_LED	VAVFM > 55 # VAV ON
T16LEDL	N
T16LEDC	AO
T17_LED	VBVFM > 55 # VBV ON
T17LEDL	N
T17LEDC	AO
T18_LED	VCVFM > 55 # VCV ON
T18LEDL	N
T18LEDC	AO
T19_LED	TFLTALA OR TFLTALB OR TFLTALC

Table 8.66   Front-Panel Settings Defaults (Sheet 3 of 3)

Label	Default Value
T19LEDL	Y
T19LEDC	AO
T20_LED	LOPV OR LOPZ
T20LEDL	Y
T20LEDC	AO
T21_LED	FAA1
T21LEDL	Y
T21LEDC	AO
T22_LED	TIRIG
T22LEDL	N
T22LEDC	AO
T23_LED	CON
T23LEDL	N
T23LEDC	AO
T24_LED	FREQOK
T24LEDL	N
T24LEDC	AO

The SEL-487E does not use the selectable screens as shown in *Section 4: Front-Panel Operations in the SEL-400 Series Relays Instruction Manual*, but instead uses a freeform settings block for listing the selected screens. The SEL-487E rotating display default (RDD) is the single screen: RMS_VLL.

Report Settings

The SEL-487E contains the Report settings described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*.

Port Settings

The SEL-487E port settings are as described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*.

The Fast Message read data access settings listed in *Table 12.8 in the SEL-400 Series Relays Instruction Manual* are all included in the SEL-487E.

Table 8.67   MIRRORED BITS Protocol Defaults (Sheet 1 of 2)

Label	Default Value
MBANA1	I1SM
MBANA2	I1TM
MBANA3	I1UM
MBANA4	I1WM

Table 8.67 MIRRORED BITS Protocol Defaults (Sheet 2 of 2)

Label	Default Value
MBANA5	I1XM
MBANA6	V1VM
MBANA7	V1ZM

DNP3 Settings–Custom Maps

The SEL-487E DNP3 custom map settings operate as described in *Section 12: Settings in the SEL-400 Series Relays Instruction Manual*. See *DNP3 Communication on page 10.9* to see the default map configuration.

Notes Settings

Use the notes settings like a text pad to leave notes about the relay in the Notes area of the relay. See *Section 12: Settings in the SEL-400 Series Relays Instruction Manual* for additional information on notes settings.

Bay Settings

Table 8.68 Bay Settings (Sheet 1 of 2)

Setting	Prompt	Default Value
MIMIC	Busbar One-line Screen Number (1–999)	1
BAYNAME	Bay Name (max 20 characters)	BAY 1
BAYLABx[a]	Bay Label x (max 40 pixels, aprox. 8 char.)	BAYLABx
BUSNAMx[a]	Busbar x Name (max 40 pixels, aprox. 8 char.)	BUSNAMx
EQPNAMn[f]	Equip. n Name (max 40 pixels, aprox. 20 char.)	EQn
BK1	Bkr 1 Assignment (NA, S, T, U, W, X)	S
BK2	Bkr 2 Assignment (NA, S, T, U, W, X)	T
BK3	Bkr 3 Assignment (NA, S, T, U, W, X)	U
BK4	Bkr 4 Assignment (NA, S, T, U, W, X)	W
BK5	Bkr 5 Assignment (NA, S, T, U, W, X)	X
ByHMINM[b]	Breaker y HMI Name (max 17 pixels, aprox. 3 char.)	BKy
ByCTLNM[b]	Breaker y Cntl. Scr. Name (max 15 characters)	Breaker y
52yCLSM[b]	Breaker y Close Status (SELOGIC Equation)	52CLy
52y_ALM[b]	Breaker y Alarm Status (SELOGIC Equation)	52ALy
52yRACK[b]	Breaker y[b] Racked Status (SELOGIC Equation)[c]	1
52yTEST[b]	Breaker y[b] Test Status (SELOGIC Equation)[c]	0
DrHMIN[d]	Disconnect m HMI Name (max 18 pixels, aprox. 4 char.)[e]	SWm

Table 8.68   Bay Settings (Sheet 2 of 2)

Setting	Prompt	Default Value
D*r*CTLN[d]	Disconnect *m* Control Scr. Name (max 15 char.)[e]	BB *m*
89AM*r*[d]	Disconnect *m* N/O Contact (SELOGIC Equation)[e]	IN103 for 89AM01, 1 for 89AM02–89AM10
89BM*r*[d]	Disconnect *m* N/C Contact (SELOGIC Equation)[e]	IN104 for 89BM01, 0 for 89BM02–89BM10
89ALP*r*[d]	Disconnect *m* Alarm Pickup Delay (1–99999 cyc)[e]	300
89CCN*r*[d]	Dis. *m* Remote Close Control (SELOGIC Equation)[e]	89CC*r*
89OCN*r*[d]	Dis. *m* Remote Open Control (SELOGIC Equation)[e]	89OC*r*
89CTL*r*[d]	Dis. *r* Front-Panel Ctl. Enable (SELOGIC Equation)[d]	1
89CST*r*[d]	Dis. *m* Close Seal-in Time (OFF, 1–99999 cyc)[e]	280
89CIT*r*[d]	Dis. *m* Close Immobility Time (OFF, 1–99999 cyc)[e]	20
89CRS*r*[d]	Disconnect *m* Close Reset (SELOGIC Equation)[e]	89CL*r* OR 89CSI*r*
89CBL*r*[d]	Disconnect *m* Close Block (SELOGIC Equation)[e]	NA
89OST*r*[d]	Dis. *m* Open Seal-in Time (OFF, 1–99999 cyc)	280
89OIT*r*[d]	Dis. *m* Open Immobility Time (OFF, 1–99999 cyc)[e]	20
89ORS*r*[d]	Disconnect *m* Open Reset (SELOGIC Equation)[e]	89OPN*r* OR 89OSI*r*
89OBL*r*[d]	Disconnect *m* Open Block (SELOGIC Equation)[e]	NA
89CIR*r*[d]	Dis. *m* Close Immob. Time Reset (SELOGIC Equation)[e]	NOT 89OPN*r*
89OIR*r*[d]	Dis. *m* Open Immob. Time Reset (SELOGIC Equation)[e]	NOT 89CL*r*
MDELE*n*[f]	Analog Quantity	<Blank>
MDNAM*x*[a]	Pre-text	<Blank>
MDSET*x*[a]	Text Formatting {w.d}	<Blank>
MDCLR*x*[a]	Post-text	
MDSCA*x*[a]	Scale Format {s}	1
LOCAL	Local Control (SELOGIC Equation)	PLT06

[a] *x* = 1-9.

[b] *y* = S, T, U, W, X.

[c] This setting only applies to rack-type breakers (see *Section 5: Control in the SEL-400 Series Relays Instruction Manual*). Non-rack-type breakers are not affected by this setting.

[d] *r* = 01-20.

[e] *m* = 1-20.

[f] *n* = 1-6.

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ASCII Command Reference

You can use a communications terminal or terminal emulation program to set and operate the relay. This section explains the commands that you send to the SEL-487E relay using SEL ASCII communications protocol. The relay responds to commands such as settings, metering, and control operations.

This section lists all the commands supported by the relay, but most are described in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*. This section provides information on commands and command options that are unique to the SEL-487E.

This section lists ASCII commands alphabetically. Commands, command options, and command variables that you enter are shown in bold. Lowercase italic letters and words in a command represent command variables that you determine based on the application (for example, Circuit Breaker number *n* = 1 or 2, Remote Bit number *nn* = 01–32, and level).

Command options appear with brief explanations about the command function. Refer to the references listed with the commands for more information on the relay function corresponding to the command or examples of the relay response to the command.

You can simplify the task of entering commands by shortening any ASCII command to the first three characters; for example, **ACCESS** becomes **ACC**. Always send a carriage return <CR> character, or a carriage return character followed by a line feed character <CR><LF>, to command the relay to process the ASCII command. Usually, most terminals and terminal programs interpret the **<Enter>** key as a <CR>. For example, to send the **ACCESS** command, type **ACC <Enter>**.

Tables in this section show the access level(s) where the command or command option is active. Access levels in the SEL-487E are Access Level 0, Access Level 1, Access Level B (breaker), Access Level P (protection), Access Level A (automation), Access Level O (output), Access Level 2, and Access Level C.

Description of Commands

Table 9.1 lists all the commands supported by the relay with the corresponding links to the descriptions in *Section 14: ASCII Command Reference in the SEL-400 Series Relays Instruction Manual*.

Command List

Table 9.1   SEL-487E List of Commands (Sheet 1 of 3)

Command	Location of Command in *Section 14: ASCII Command Reference* in the SEL-400 Series Relays Instruction Manual
2ACCESS	*2ACCESS on page 14.1*
89CLOSE *k*	*89CLOSE n on page 14.2* (The SEL-487E supports 20 disconnects.)
89OPEN *k*	*89OPEN n on page 14.2* (The SEL-487E supports 20 disconnects.)
AACCESS	*AACCESS on page 14.3*
ACCESS	*ACCESS on page 14.3*
BACCESS	*BACCESS on page 14.3*
BNAME	*BNAME on page 14.4*
BREAKER *n*	*BREAKER on page 14.4* (The SEL-487E supports five circuit breakers, designated S, T, U, W, and X.)
CAL	*CAL on page 14.5*
CASCII	*CASCII on page 14.5*
CBREAKER	*CBREAKER on page 14.6* (The SEL-487E supports five circuit breakers, designated S, T, U, W, and X.)
CEVENT	*CEVENT on page 14.6* (The SEL-487E supports an 8-samples/cycle large resolution event report. It does not support the **CEV L** option.)
CFG CTNOM *i j*	*CFG CTNOM on page 14.10* (In the SEL-487E, two digits are used to indicate the nominal CT currents. See *Table 2.8* and *Table 2.9* for a complete list of the parameter options.)
CFG NFREQ *f*	*CFG NFREQ on page 14.11*
CHISTORY	*CHISTORY on page 14.11*
CLOSE *n*	*CLOSE n on page 14.11* (The SEL-487E supports five circuit breakers, designated S, T, U, W, and X.)
COMMUNICATIONS *c*	*COMMUNICATIONS on page 14.12*
CONTROL *nn*	*COM SV on page 14.16*
COPY *m n*	*COPY on page 14.25*
CPR	*CPR on page 14.26*
CSER	*CSER on page 14.26*
CSTATUS	*CSTATUS on page 14.28*
CSUMMARY	*CSUMMARY on page 14.28*
DATE	*DATE on page 14.29*
DNAME X	*DNAME X on page 14.30*
DNP	*DNP on page 14.30*
ETHERNET	*ETHERNET on page 14.30*
EVENT	*EVENT on page 14.31* (The SEL-487E supports standard 4-samples/cycle and large resolution 8-samples/cycle event reports. It does not support the **EVE L** option.)
EVE DIF	See *EVE DIF on page 9.4* in this section.
EXIT	*EXIT on page 14.35*
FILE	*FILE on page 14.35*
GOOSE	*GOOSE on page 14.36*
GROUP	*GROUP on page 14.39*
HELP	*HELP on page 14.40*
HISTORY	*HISTORY on page 14.40*
ID	*ID on page 14.41*

Table 9.1   SEL-487E List of Commands (Sheet 2 of 3)

Command	Location of Command in *Section 14: ASCII Command Reference* in the SEL-400 Series Relays Instruction Manual
LOOPBACK	*LOOPBACK on page 14.43*
MAC	*MAC on page 14.44*
MAP	*MAP on page 14.45*
METER	*METER on page 14.45* (For all other **METER** options, see *METER on page 9.4* in this section.)
MET AMV	*MET AMV on page 14.46*
MET ANA	*MET ANA on page 14.46*
MET BAT	*MET BAT on page 14.46* (The SEL-487E provides battery metering for one battery monitor channel.)
MET D	*MET D on page 14.47*
MET DIF	See *MET DIF on page 9.5* in this section.
MET E	See *MET E on page 9.5* in this section.
MET PM	*MET PM on page 14.47*
MET PMV	*MET PMV on page 14.48*
MET RMS	See *MET RMS on page 9.5* in this section.
MET RTC	*MET RTC on page 14.49*
MET RTD	*MET T on page 14.49* (The **MET RTD** command in the SEL-487E is the same as the **MET T** command in other SEL-400 series relays.)
MET SEC	See *MET SEC on page 9.6* in this section.
OACCESS	*OACCESS on page 14.49*
OPEN *n*	*OPEN n on page 14.50* (The SEL-487E supports five circuit breakers, designated S, T, U, W, X.)
PACCESS	*PACCESS on page 14.50*
PASSWORD	*PASSWORD on page 14.50*
PING	*PING on page 14.51*
PORT	*PORT on page 14.51*
PROFILE	*PROFILE on page 14.53*
PULSE	*PULSE on page 14.53*
QUIT	*QUIT on page 14.54*
RTC	*RTC on page 14.54*
SER	*SER on page 14.54*
SET	*SET on page 14.56* (*Table 9.8* lists the class and instance options available in the SEL-487E.)
SHOW	*SHOW on page 14.58* (*Table 9.9* lists the class and instance options available in the SEL-487E.)
SNS	*SNS on page 14.58*
STATUS	*STATUS on page 14.58*
SUMMARY	*SUMMARY on page 14.60*
TARGET	*TARGET on page 14.61*
TEST DB	*TEST DB on page 14.63*
TEST DB2	*TEST DB2 on page 14.65*
TEST FM	*TEST FM on page 14.66*
TFE	See *TFE on page 9.8* in this section.
THE	See *THE on page 9.8* in this section.
TIME	*TIME on page 14.70*
TIME Q	*TIME Q on page 14.71*

Table 9.1   SEL-487E List of Commands (Sheet 3 of 3)

Command	Location of Command in *Section 14: ASCII Command Reference* in the SEL-400 Series Relays Instruction Manual
TRIGGER	*TRIGGER on page 14.72*
VECTOR	*VECTOR on page 14.72*
VERSION	*VERSION on page 14.72*
VIEW	*VIEW on page 14.73*

EVENT

EVE DIF

Use **EVE DIF** to display the differential report. You cannot use the A or D options with the **EVE DIF** command.

Table 9.2   EVE DIF Command

Command	Description	Access Level
EVE DIF	Display the differential report	1, B, P, A, O, 2

METER

The **METER** command displays reports about quantities the relay measures in the power system (voltages, currents, frequency, remote analogs, etc.) and internal relay operating quantities (math variables and analog quantities).

MET

Use the **MET** command to view fundamental metering quantities. The relay filters harmonics and subharmonics to present only measured quantities at the power system fundamental operating frequency. Meter values are displayed only for those terminals included in the ECTTERM setting, otherwise the relay displays `Winding Not Enabled For Metering`.

For combined windings, meter values are displayed only for those windings included in the ECTTERM setting that also have the same VREFw and CTCONw settings. If this is not the case, the relay displays `Winding Not Enabled For Metering`. If ECTTERM is set to OFF, then rms, fundamental, and secondary metering are not be available, and the relay displays `No Windings Enabled For Metering`.

Table 9.3   MET Command[a]

Command	Description	Access Level
MET	Display fundamental metering data	1, B, P, A, O, 2
MET [F] n	Display Terminal n fundamental metering quantities	1, B, P, A, O, 2
MET [F] n k	Display Terminal n fundamental metering quantities successively for k times	1, B, P, A, O, 2

[a] n = S, T, U, W, X, Y, ST, TU, UW, WX.

The **MET** command without options shows the fundamental metering data of the winding that appears first in the ECTTERM setting. Specify a specific terminal by using the terminal parameter command options. For example, specify **MET T** to view the fundamental metering quantities of Terminal T.

Some situations require that you repeatedly monitor the power system for a brief period; specify a number after any **MET** command to automatically repeat the command.

MET DIF

Use the **MET DIF** command to view the differential current metering data, in multiples of tap.

Table 9.4   MET DIF Command

Command	Description	Access Level
MET DIF	Displays the differential operate and restraint quantities	1, B, P, A, O, 2
MET DIF *k*	Displays the differential operate and restraint quantities successively for *k* times	1, B, P, A, O, 2

If the differential is disabled (E87 = OFF), the relay displays the message `Differential Elements Disabled`.

MET E

Use the **MET E** command to view the energy import and export quantities.

Table 9.5   MET E Command

Command	Description	Access Level
MET E	Display Line energy metering data	1, B, P, A, O, 2
MET E *k*	Display Line energy metering data successively for *k* times	1, B, P, A, O, 2
MET RE	Reset Line energy metering data	P, A, O, 2

The reset command, **MET RE**, resets the Line, BK1, and BK2 energy metering quantities. When you issue the **MET RE** command, the relay responds, `Reset Energy Metering (Y/N)?` If you answer **Y <Enter>**, the relay responds, `Energy Metering Reset`.

MET RMS

Use the **MET RMS** command to view fundamental metering quantities.

Table 9.6   MET RMS Command[a]

Command	Description	Access Level
MET RMS	Display root-mean-square (rms) metering quantities of the first enabled winding	1, B, P, A, O, 2
MET RMS *n*	Display Terminal *n* rms metering quantities	1, B, P, A, O, 2
MET RMS *n k*	Display Terminal *n* rms metering quantities successively for *k* times	1, B, P, A, O, 2

[a] *n* = S, T, U, W, X, ST, TU, UW, WX.

MET SEC

Use the **MET SEC** command to view secondary fundamental metering quantities.

Table 9.7   MET SEC Command[a]

Command	Description	Access Level
MET SEC	Display secondary metering quantities of the first enabled winding	1, B, P, A, O, 2
MET SEC *n*	Display Terminal *n* secondary metering quantities	1, B, P, A, O, 2
MET SEC *n k*	Display Terminal *n* secondary metering quantities successively for *k* times	1, B, P, A, O, 2

[a]   *n* = S, T, U, W, X, ST, TU, UW, WX.

SET

Table 9.8 lists the options specifically available in the SEL-487E.

Table 9.8   SET Command Overview (Sheet 1 of 2)

Command	Description	Access Level
SET	Set the Group relay settings, beginning at the first setting in the active group	P, 2
SET *n*[a]	Set the Group *n* relay settings, beginning at the first setting in the group	P, 2
SET A	Set the Automation SELOGIC control equation relay settings in Block 1	A, 2
SET A *m*[b]	Set the Automation SELOGIC control equation relay settings in Block *m*	A, 2
SET B	Bay control settings, beginning at the first setting in this class	P, B, 2
SET D	Set the DNP3 remapping settings, beginning at the first setting in this class for Instance 1	P, A, O, 2
SET D *instance*	Set the DNP3 remapping settings beginning at the first setting of Instance *instance*	P, A, O, 2
SET F	Set the Front-panel relay settings, beginning at the first setting in this class	P, A, O, 2
SET G	Set the Global relay settings, beginning at the first setting in this class	P, A, O, 2
SET L	Set the Protection SELOGIC control equation relay settings for the active group	P, 2
SEL L *n*[a]	Set the Protection SELOGIC relay settings for Group *n*	P, 2
SET M	Monitor settings, beginning at the first setting in this class	P, 2
SET N	Enter text using the text-edit format	P, A, O, 2
SET O	Set the Output SELOGIC control equation relay settings, beginning at OUT101	O, 2
SET P	Set the port presently in use, beginning at the first setting for this port	P, A, O, 2
SET P *p*[c]	Set the communications Port relay settings for Port *p*, beginning at the first setting for this port	P, A, O, 2

Table 9.8 SET Command Overview (Sheet 2 of 2)

Command	Description	Access Level
SET R	Set the Report relay settings, beginning at the first setting for this class	P, A, O, 2
SET T	Set the alias settings	P, A, O, 2

^a n = 1–6; representing Group 1 through Group 6.

^b m = 1–10; representing Block 1 through Block 10.

^c p = 1–3, F, or 5; corresponding to Port 1–Port 3, Port F, or Port 5.

SHOW

Table 9.9 lists the class and instance options available in the SEL-487E.

Table 9.9 SHO Command Overview

Command	Description	Access Level
SHO	Show the Group relay settings, beginning at the first setting in the active group	1, B, P, A, O, 2
SHO n^a	Show the Group n relay settings, beginning at the first setting in each instance	1, B, P, A, O, 2
SHO A	Show the Automation SELOGIC control equation relay settings in Block 1	1, B, P, A, O, 2
SHO A m^b	Show the Automation SELOGIC control equation relay settings in Block m	1, B, P, A, O, 2
SHO B	Show the Bay control settings, beginning at the first setting in this class	1, B, P, A, O, 2
SHO D	Show the DNP3 remapping settings for Instance 1	P, A, O, 2
SHO D *instance*	Show the DNP3 remapping settings for Instance *instance*	P, A, O, 2
SHO F	Show the Front-panel relay settings, beginning at the first setting in this class	1, B, P, A, O, 2
SHO G	Show the Global relay settings, beginning at the first setting in this class	1, B, P, A, O, 2
SHO L	Show the Protection SELOGIC control equation relay settings for the active group	1, B, P, A, O, 2
SHO L n^a	Show the Protection SELOGIC control equation relay settings for Group n	1, B, P, A, O, 2
SHO M	Show the Monitor relay settings, beginning at the first setting in this class	1, B, P, A, O, 2
SHO N	Show notes in the relay	1, B, P, A, O, 2
SHO O	Show the Output SELOGIC control equation relay settings, beginning at OUT101	1, B, P, A, O, 2
SHO P	Show the relay settings for the port presently in use, beginning at the first setting	1, B, P, A, O, 2
SHO P p^c	Show the communications Port relay settings for Port p, beginning at the first setting for this port	1, B, P, A, O, 2
SHO R	Show the Report relay settings beginning at the first setting for this class	1, B, P, A, O, 2
SHO T	Show the alias settings	1, B, P, A, O, 2

^a n = 1–6; representing Group 1 through Group 6.

^b m = 1–10; representing Block 1 through Block 10.

^c p = 1–3, F, and 5; which corresponds to Port 1–Port 3, Port F, and Port 5.

TFE

Use the **TFE** command to display, set, and clear through-fault data.

Table 9.10   TFE Command

Command	Description	Access Level
TFE	Displays as many as 20 of the most recent through-faults	Level 1 and higher
TFE A	Display all through-fault records	Level 1 and higher
TFE *nnnn*[a]	Displays *nnnn* through faults	Level 1 and higher
TFE P	Preloads through-fault values	Level B and higher
TFE R or **C**	Clears accumulated values and deletes the history	Level B and higher

[a] *nnnn* = 1-1200.

THE

Use the **THE *n*** (*n* = 1–5) command to display one of five saved thermal reports of the transformer(s) monitored by the relay. For example, **THE 1** displays the most recent event report while **THE 5** displays the oldest thermal event report. Reports are saved in a first-in, first-out (FIFO) type buffer where the newest event will overwrite the oldest report.

Table 9.11   THE Command

Command	Description	Access Level
THE *n*[a]	Displays thermal monitor report *n*	Level 1 and higher
THE P	Load preset value of accumulated insulation Loss of Life for transformer	Level 1 and higher
THE D *x* [*y*][b]	Retrieves daily profile data from day *x* to day *y*	Level 1 and higher
THE H	Retrieves hourly profile data	Level 1 and higher
THE R	Resets all stored thermal data archives and the value of total Loss of Life	Level B and higher
THE C	Clears all stored thermal data archives	Level B and higher

[a] *n* = 1-5.

[b] *x* and *y*:
   mm:dd:yy if setting DATE_F = MDY
   yy:mm:dd if setting DATE_F = YMD
   dd:mm:yy if setting DATE_F = DMY

Communications Interfaces

Section 15: Communications Interfaces–Section 19: Digital Secondary Systems in the SEL-400 Series Relays Instruction Manual describe the various communications interfaces and protocols used in SEL-400 series relays. This section describes aspects of the communications protocols that are unique to the SEL-487E relay. The following topics are discussed:

➤ *Virtual File Interface on page 10.1*

➤ *Communications Database on page 10.1*

➤ *DNP3 Communication on page 10.9*

➤ *IEC 61850 Communication on page 10.35*

➤ *Synchrophasors on page 10.66*

Virtual File Interface

REPORTS Directory

In addition to the files identified in *Section 15: Communications Interfaces in the SEL-400 Series Relays Instruction Manual*, the SEL-487E also supports the files listed in *Table 10.1*.

Table 10.1   REPORTS Directory Files

File	Usage: All Are Read-Only Files
TFE.TXT	ASCII Through-Fault-Event Report
THE.TXT	ASCII Thermal Report
THE_D.TXT	ASCII Daily Thermal Report
THE_H.TXT	ASCII Hourly Thermal Report

Communications Database

The SEL-487E maintains a database to describe itself to external devices via the Fast Message Data Access protocol. This database includes a variety of data within the relay that are available to devices connected in a serial or Ethernet network. The database includes the regions and data described in *Table 10.2*. Use the **MAP** and **VIEW** commands to display maps and contents of the database regions. See *Section 9: ASCII Command Reference* for more information on the **MAP** and **VIEW** commands.

Table 10.2   SEL-487E Database Regions

Region Name	Contents	Update Rate
LOCAL	Relay identification data including FID, Relay ID, Station ID, and active protection settings group	Updated on settings change and whenever monitored values change
METER	Metering and measurement data	0.5 s
DEMAND	Demand and peak demand measurement data	15 s
TARGET	Selected rows of Relay Word bit data	0.5 s
HISTORY	Relay event history records for the 10 most recent events	Within 15 s of any new event
BREAKER	Summary circuit breaker monitor data	15 s
STATUS	Self-test diagnostic status data	5 s
ANALOGS	Protection and automation math variables	0.5 s

Data within the Ethernet card regions are available for access by external devices via the SEL Fast Message protocol.

The LOCAL region contains the device FID, SID, and RID. It will also provide appropriate status points. This region is updated on settings changes and whenever monitored status points change (see *Table 10.3*).

Table 10.3   SEL-487E Database Structure—LOCAL Region

Address (Hex)	Name	Type	Description
0000	FID	char[48]	FID string
0030	BFID	char[48]	SELboot FID string
0060	SER_NUM	char[16]	Device Serial number, from factory settings
0070	PART_NUM	char[24]	Device part number, from factory settings
0088	CONFIG	char[8]	Device configuration string (as reported in ID command)
0090	SPECIAL	char[8]	Special device configuration string (as reported in ID command)
0098	DEVICE_ID	char[40]	Relay ID setting, from Global settings
00C0	NODE_ID	char[40]	Station ID from Global settings
00E8	GROUP	int	Active group
00E9	STATUS	int	Status indication: 0 for okay, 1 for failure

The METER region contains all the basic meter and energy information. This region is updated every 0.5 seconds. See *Table 10.4* for the map.

Table 10.4   SEL-487E Database Structure—METER Region (Sheet 1 of 4)

Address (Hex)	Name	Type	Description
1000	_YEAR	int	4-digit year when data were sampled
1001	DAY_OF_YEAR	int	1–366 day when data were sampled
1002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
1004	FREQ	float	System frequency (FREQ)
1006	VDC1	float	Battery voltage (VDC1)
1008	IS(A)	float[6]	Terminal S, 1-cycle average filtered phase-current magnitude and angle (IASFMC, IASFAC, IBSFMC, IBSFAC, ICSFMC, ICSFAC)

Table 10.4 SEL-487E Database Structure—METER Region (Sheet 2 of 4)

Address (Hex)	Name	Type	Description
1014	IT(A)	float[6]	Terminal T, 1-cycle average filtered phase-current magnitude and angle (IATFMC, IATFAC, IBTFMC, IBTFAC, ICTFMC, ICTFAC)
1020	IU(A)	float[6]	Terminal U, 1-cycle average filtered phase-current magnitude and angle (IAUFMC, IAUFAC, IBUFMC, IBUFAC, ICUFMC, ICUFAC)
102C	IW(A)	float[6]	Terminal W, 1-cycle average filtered phase-current magnitude and angle (IAWFMC, IAWFAC, IBWFMC, IBWFAC, ICWFMC, ICWFAC)
1038	IX(A)	float[6]	Terminal X, 1-cycle average filtered phase-current magnitude and angle (IAXFMC, IAXFAC. IBXFMC, IBXFAC, ICXFMC, ICXFAC)
1044	IY(A)	float[6]	Terminal Y, 1-cycle average filtered phase-current magnitude and angle (IY1FMC, IY1FAC, IY2FMC, IY2FAC, IY3FMC, IY3FAC)
1050	VV(V)	float[6]	Terminal V, 1-cycle average filtered phase voltage magnitude and angle (VAVFMC • 1000, VAVFAC, VBVFMC • 1000, VBVFAC, VCVFMC • 1000, VCVFAC)
105C	VZ(V)	float[6]	Terminal Z, 1-cycle average filtered phase voltage magnitude and angle (VAZFMC • 1000, VAZFAC, VBZFMC • 1000, VBZFAC, VCZFMC • 1000, VCZFAC)
1068	IST(A)	float[6]	Terminal ST, 1-cycle average filtered phase-current magnitude and angle (IASTFMC, IASTFAC, IBSTFMC, IBSTFAC, ICSTFMC, ICSTFAC)
1074	ITU(A)	float[6]	Terminal TU, 1-cycle average filtered phase-current magnitude and angle (IATUFMC, IATUFAC, IBTUFMC, IBTUFAC, ICTUFMC, ICTUFAC)
1080	IUW(A)	float[6]	Terminal UW, 1-cycle average filtered phase-current magnitude and angle (IAUWFMC, IAUWFAC, IBUWFMC, IBUWFAC, ICUWFMC, ICUWFAC)
108C	IWX(A)	float[6]	Terminal WX, 1-cycle average filtered phase-current magnitude and angle (IAWXFMC, IAWXFAC, IBWXFMC, IBWXFAC, ICWXFMC, ICWXFAC)
1098	ISEQ_S(A)	float[6]	Terminal S 1-cycle average sequence current magnitude and angle (3I0SMC/3, 3I0SAC, I1SMC, I1SAC, 3I2SMC/3, 3I2SAC)
10A4	ISEQ_T(A)	float[6]	Terminal T 1-cycle average sequence current magnitude and angle (3I0TMC/3, 3I0TAC, I1TMC, I1TAC, 3I2TMC/3, 3I2TAC)
10B0	ISEQ_U(A)	float[6]	Terminal U 1-cycle average sequence current magnitude and angle (3I0UMC/3, 3I0UAC, I1UMC, I1UAC, 3I2UMC/3, 3I2UAC)
10BC	ISEQ_W(A)	float[6]	Terminal W 1-cycle average sequence current magnitude and angle (3I0WMC/3, 3I0WAC, I1WMC, I1WAC, 3I2WMC/3, 3I2WAC)
10C8	ISEQ_X(A)	float[6]	Terminal X 1-cycle average sequence current magnitude and angle (3I0XMC/3, 3I0XAC, I1XMC, I1XAC, 3I2XMC/3, 3I2XAC)
10D4	ISEQ_ST(A)	float[6]	Terminal ST 1-cycle average sequence current magnitude and angle (3I0STMC/3, 3I0STAC, I1STMC, I1STAC, 3I2STMC/3, 3I2STAC)
10E0	ISEQ_TU(A)	float[6]	Terminal TU 1-cycle average sequence current magnitude and angle (3I0TUMC/3, 3I0TUAC, I1TUMC, I1TUAC, 3I2TUMC/3, 3I2TUAC)
10EC	ISEQ_UW(A)	float[6]	Terminal UW 1-cycle average sequence current magnitude and angle (3I0UWMC/3, 3I0UWAC, I1UWMC, I1UWAC, 3I2UWMC/3, 3I2UWAC)
10F8	ISEQ_WX(A)	float[6]	Terminal WX 1-cycle average sequence current magnitude and angle (3I0WXMC/3, 3I0WXAC, I1WXMC, I1WXAC, 3I2WXMC/3, 3I2WXAC)
1104	VV_LL(V)	float[6]	Terminal V, 1-cycle average phase-to-phase voltage magnitude and angle (VABVFMC • 1000, VABVFAC, VBCVFMC • 1000, VBCVFAC, VCAVFMC • 1000, VCAVFAC)
1110	VZ_LL(V)	float[6]	Terminal Z, 1-cycle average phase-to-phase voltage magnitude and angle (VABZFMC • 1000, VABZFAC, VBC-ZFMC • 1000, VBCZFAC, VCAZFMC • 1000, VCAZFAC)
111C	VSEQ_V(V)	float[6]	Terminal V, 1-cycle average sequence voltage magnitude and angle (3V0VMC/3 • 1000, 3V0VAC, V1VMC • 1000, V1VAC, 3V2VMC/3 • 1000, 3V2VAC)
1128	VSEQ_Z(V)	float[6]	Terminal Z, 1-cycle average sequence voltage magnitude and angle (3V0ZMC/3 • 1000, 3V0ZAC, V1ZMC • 1000, V1ZAC, 3V2ZMC/3 • 1000, 3V2ZAC)
1134	PS(W)	float[4]	Terminal S, 1-second average fundamental active power (PASFS, PBSFS, PCSFS, 3PSFS)

Table 10.4   SEL-487E Database Structure–METER Region (Sheet 3 of 4)

Address (Hex)	Name	Type	Description
113C	QS(VAR)	float[4]	Terminal S, 1-second average fundamental reactive power (QASFS, QBSFS, QCSFS, 3QSFS)
1144	SS(VA)	float[4]	Terminal S, 1-second average fundamental apparent power (SASFS, SBSFS, SCSFS, 3SSFS)
114C	PT(W)	float[4]	Terminal T, 1-second average fundamental active power (PATFS, PBTFS, PCTFS, 3PTFS)
1154	QT(VAR)	float[4]	Terminal T, 1-second average fundamental reactive power (QATFS, QBTFS, QCTFS, 3QTFS)
115C	ST(VA)	float[4]	Terminal T, 1-second average fundamental apparent power (SATFS, SBTFS, SCTFS, 3STFS)
1164	PU(W)	float[4]	Terminal U, 1-second average fundamental active power (PAUFS, PBUFS, PCUFS, 3PUFS)
116C	QU(VAR)	float[4]	Terminal U, 1-second average fundamental reactive power (QAUFS, QBUFS, QCUFS, 3QUFS)
1174	SU(VA)	float[4]	Terminal U, 1-second average fundamental apparent power (SAUFS, SBUFS, SCUFS, 3SUFS)
117C	PW(W)	float[4]	Terminal W, 1-second average fundamental active power (PAWFS, PBWFS, PCWFS, 3PWFS)
1184	QW(VAR)	float[4]	Terminal W, 1-second average fundamental reactive power (QAWFS, QBWFS, QCWFS, 3QWFS)
118C	SW(VA)	float[4]	Terminal W, 1-second average fundamental apparent power (SAWFS, SAWFS, SCWFS, 3SWFS)
1194	PX(W)	float[4]	Terminal X, 1-second average fundamental active power (PAXFS, PBXFS, PCXFS, 3PXFS)
119C	QX(VAR)	float[4]	Terminal X, 1-second average fundamental reactive power (QAXFS, QBXFS, QCXFS, 3QXFS)
11A4	SX(VA)	float[4]	Terminal X, 1-second average fundamental apparent power (SAXFS, SBXFS, SCXFS, 3SXFS)
11AC	PST(W)	float[4]	Combined Terminal ST, 1-second average fundamental active real power (PASTFS, PBSTFS, PCSTFS, 3PSTFS)
11B4	QST(VAR)	float[4]	Combined Terminal ST, 1-second average fundamental reactive power (QASTFS, QBSTFS, QCSTFS, 3QSTFS)
11BC	SST(VA)	float[4]	Combined Terminal ST, 1-second average fundamental apparent power (SASTFS, SBSTFS, SCSTFS, 3SSTFS)
11C4	PTU(W)	float[4]	Combined Terminal TU, 1-second average fundamental active power (PATUFS, PBTUFS, PCTUFS, 3PTUFS)
11CC	QTU(VAR)	float[4]	Combined Terminal TU, 1-second average fundamental reactive power (QATUFS, QBTUFS, QCTUFS, 3QTUFS)
11D4	STU(VA)	float[4]	Combined Terminal TU, 1-second average fundamental apparent power (SATUFS, SBTUFS, SCTUFS, 3STUFS)
11DC	PUW(W)	float[4]	Combined Terminal UW, 1-second average fundamental active power (PAUWFS, PBUWFS, PCUWFS, 3PUWFS)
11E4	QUW(VAR)	float[4]	Combined Terminal UW, 1-second average fundamental reactive power (QAU-WFS, QBUWFS, QCUWFS, 3QUWFS)
11EC	SUW(VA)	float[4]	Combined Terminal UW, 1-second average fundamental apparent power (SAU-WFS, SBUWFS, SCUWFS, 3SUWFS)
11F4	PWX(W)	float[4]	Combined Terminal WX, 1-second average fundamental active power (PAWXFS, PBWXFS, PCWXFS, 3PWXFS)
11FC	QWX(VAR)	float[4]	Combined Terminal WX, 1-second average fundamental reactive power (QAWXFS, QBWXFS, QCWXFS, 3QWXFS)
1204	SWX(VA)	float[4]	Combined Terminal WX, 1-second average fundamental apparent power (SAWXFS, SBWXFS, SCWXFS, 3SWXFS)
120C	PFS	float[4]	Terminal S, phase power factor (TPFAS, TPFBS, TPFCS, 3TPFS)
1214	PFT	float[4]	Terminal T, phase power factor (TPFAT, TPFBT, TPFCT, 3TPFT)
121C	PFU	float[4]	Terminal U, phase power factor (TPFAU, TPFBU, TPFCU, 3TPFU)
1224	PFW	float[4]	Terminal W, phase power factor (TPFAW, TPFBW, TPFCW, 3TPFW)
122C	PFX	float[4]	Terminal X, phase power factor (TPFAX, TPFBX, TPFCX, 3TPFX)
1234	PFST	float[4]	Combined Terminal ST, phase power factor (TPFAST, TPFBST, TPFCST, 3TPFST)

Table 10.4   SEL-487E Database Structure–METER Region (Sheet 4 of 4)

Address (Hex)	Name	Type	Description
123C	PFTU	float[4]	Combined Terminal TU, phase power factor (TPFATU, TPFBTU, TPFCTU, 3TPFTU)
1244	PFUW	float[4]	Combined Terminal UW, phase power factor (TPFAUW, TPFBUW, TPFCUW, 3TPFUW)
124C	PFWX	float[4]	Combined Terminal WX, phase power factor (TPFAWX, TPFBWX, TPFCWX, 3TPFWX)
1254	ES(kWh)	float[4]	Terminal S, three-phase active/reactive energy export/import in KWh (3PSP_MWh, 3PSN_MWh, 3QSP_Mvarh, 3QSN_Mvarh)
125C	ET(kWh)	float[4]	Terminal T, three-phase active/reactive energy export/import in KWh (3PTP_MWh, 3PTN_MWh, 3QTP_Mvarh, 3QTN_Mvarh)
1264	EU(kWh)	float[4]	Terminal U, three-phase active/reactive energy export/import in KWh (3PUP_MWh, 3PUN_MWh, 3QUP_Mvarh, 3QUN_Mvarh)
126C	EW(kWh)	float[4]	Terminal W, three-phase active/reactive energy export/import in KWh (3PWP_MWh, 3PWN_MWh, 3QWP_Mvarh, 3QWN_Mvarh)
1274	EX(kWh)	float[4]	Terminal X, three-phase active/reactive energy export/import in KWh (3PXP_MWh, 3PXN_MWh, 3QXP_Mvarh, 3QXN_Mvarh)
127C	EST(kWh)	float[4]	Combined Terminal ST, three-phase active/reactive energy export/import in KWh (3PSTP_MWh, 3PSTN_MWh, 3QSTP_Mvarh, 3QSTN_Mvarh)
1284	ETU(kWh)	float[4]	Combined Terminal TU, three-phase active/reactive energy export/import in KWh (3PTUP_MWh, 3PTUN_MWh, 3QTUP_Mvarh, 3QTUN_Mvarh)
128C	EUW(kWh)	float[4]	Combined Terminal UW, three-phase active/reactive energy export/import in KWh (3PUWP_MWh, 3PUWN_MWh, 3QUWP_Mvarh, 3QUWN_Mvarh)
1294	EWX(kWh)	float[4]	Combined Terminal WX, three-phase active/reactive energy export/import in KWh (3PWXP_MWh, 3PWXN_MWh, 3QWXP_Mvarh, 3QWXN_Mvarh)

The DEMAND region contains demand and peak demand information. This region is updated every 15 seconds. See *Table 10.5* for the map.

Table 10.5   SEL-487E Database Structure–DEMAND Region

Address (Hex)	Name	Type	Description
2000	_YEAR	int	4-digit year when data were sampled
2001	DAY_OF_YEAR	int	1–366 day when data were sampled
2002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
2004	DM	float[10]	Demand quantity (DM01–DM10)
2018	DMP	float[10]	Peak demand quantity (DMM01–DMM10)

The TARGET region contains the entire visible Relay Word plus the rows designated specifically for the TARGET region. This region is updated every 0.5 seconds. See *Table 10.6* for the map. See *Section 11: Relay Word Bits* for detailed information on the Relay Word bits.

Table 10.6   SEL-487E Database Structure–TARGET Region

Address (Hex)	Name	Type	Description
3000	_YEAR	int	4-digit year when data were sampled
3001	DAY_OF_YEAR	int	1–366 day when data were sampled
3002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
3004	TARGET	char[~551]	Entire Relay Word with bit labels

The HISTORY region contains all information available in a History report for the most recent 10 events. This region is updated within 15 seconds of any new events. See *Table 10.7* for the map.

Table 10.7 SEL-487E Database Structure–HISTORY Region

Address (Hex)	Name	Type	Description
4000	_YEAR	int	4-digit year when data were sampled
4001	DAY_OF_YEAR	int	1–366 day when data were sampled
4002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
4004	REF_NUM	int[10]	Event serial number (10000–42767)
400E	MONTH	int[10]	Month of event
4018	DAY	int[10]	Day of event
4022	YEAR	int[10]	Year of event
402C	HOUR	int[10]	Hour of event
4036	MIN	int[10]	Minute of event
4040	SEC	int[10]	Second of event
404A	MSEC	int[10]	Milliseconds of event
4054	EVENT	char[60]	Event type string
4090	GROUP	int[10]	Active group during fault
409A	FREQ	float[10]	System frequency at time of fault
40AE	TAR_SMALL	char[320]	System targets from event (32 characters per event)
41EE	TARGETS	char[1000]	System targets from event (100 characters per event)

The BREAKER region contains some of the information available in a summary Breaker report. This region is updated every 15 seconds. See *Table 10.8* for the map.

Table 10.8 SEL-487E Database Structure–BREAKER Region (Sheet 1 of 2)

Address (Hex)	Name	Type	Description
5000	_YEAR	int	4-digit year when data were sampled
5001	DAY_OF_YEAR	int	1–366 day when data were sampled
5002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
5004	BCW_S	float[3]	Breaker S phase breaker wear (%) (BSBCWPA, BSBCWPB, BSBCWPC)
500A	BCW_T	float[3]	Breaker T phase breaker wear (%) (BTBCWPA, BTBCWPB, BTBCWPC)
5010	BCW_U	float[3]	Breaker U phase breaker wear (%) (BUBCWPA, BUBCWPB, BUBCWPC)
5016	BCW_W	float[3]	Breaker W phase breaker wear (%) (BWBCWPA, BWBCWPB, BWBCWPC)
501C	BCW_X	float[3]	Breaker X phase breaker wear (%) (BXBCWPA, BXBCWPB, BXBCWPC)
5022	CUR_S	float[3]	Breaker S phase accumulated current (kA) (IASrms_TRIP_ACC, IBSrms_TRIP_ACC, ICSrms_TRIP_ACC)
5028	CUR_T	float[3]	Breaker T phase accumulated current (kA) (IATrms_TRIP_ACC, IBTrms_TRIP_ACC, ICTrms_TRIP_ACC)
502E	CUR_U	float[3]	Breaker U phase accumulated current (kA) (IAUrms_TRIP_ACC, IBUrms_TRIP_ACC, ICUrms_TRIP_ACC)

Table 10.8   SEL-487E Database Structure—BREAKER Region (Sheet 2 of 2)

Address (Hex)	Name	Type	Description
5034	CUR_W	float[3]	Breaker W phase accumulated current (kA) (IAWrms_TRIP_ACC, IBWrms_TRIP_ACC, ICWrms_TRIP_ACC)
503A	CUR_X	float[3]	Breaker X phase accumulated current (kA) (IAXrms_TRIP_ACC, IBXrms_TRIP_ACC, ICXrms_TRIP_ACC)
5040	NOP_S	long int	Breaker S number of operations (BS_TRP_CNT)
5042	NOP_T	long int	Breaker T number of operations (BT_TRP_CNT)
5044	NOP_U	long int	Breaker U number of operations (BU_TRP_CNT)
5046	NOP_W	long int	Breaker W number of operations (BW_TRP_CNT)
5048	NOP_X	long int	Breaker X number of operations (BX_TRP_CNT)

The STATUS region contains complete relay status information. This region is updated every 5 seconds. See *Table 10.9* for the map.

Table 10.9   SEL-487E Database Structure—STATUS Region

Address (Hex)	Name	Type	Description
6000	_YEAR	int	4-digit year when data were sampled
6001	DAY_OF_YEAR	int	1–366 day when data were sampled
6002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
6004	CH1_24(mV)	int[24]	Channel offsets, use 0 if not measured
601C	MOF(mV)	int	Master offset
601D	MOF2(mV)	int	Master offset 2
601E	OFF_WARN	char[8]	Offset warning string
6026	OFF_FAIL	char[8]	Offset failure string
602E	PS3(V)	float	3.3 Volt power supply voltage
6030	PS5(V)	float	5 Volt power supply voltage
6032	PS_N5(V)	float	–5 Volt regulated voltage
6034	PS15(V)	float	15 Volt power supply voltage
6036	PS_N15(V)	float	–15 Volt power supply voltage
6038	PS_WARN	char[8]	Power supply warning string
6040	PS_FAIL	char[8]	Power supply failure string
6048	HW_FAIL	char[40]	Hardware failure strings
6070	CC_STA	char[40]	Comm. card status strings
6098	PORT_STA	char[160]	Serial port status strings
6138	TIME_SRC	char[10]	Time source
6142	LOG_ERR	char[40]	SELOGIC error strings
616A	TEST_MD	char[160]	Test mode string
620A	WARN	char[32]	Warning strings for any active warnings
622A	FAIL	char[64]	Failure strings for any active failures

The ANALOGS region contains protection and automation variables. This region is updated every 0.5 seconds. See *Table 10.10* for the map.

Table 10.10   SEL-487E Database Structure—ANALOGS Region

Address (Hex)	Name	Type	Description
7000	_YEAR	int	4-digit year when data were sampled
7001	DAY_OF_YEAR	int	1–366 day when data were sampled
7002	TIME(ms)	long int	Time of day in ms when data were sampled (0–86,400,000)
7004	PMV01_64	float[64]	PMV01–PMV64
7084	AMV001_256	float[256]	AMV001–AMV256

The database is virtual device 1 in the relay. You can display the contents of a region using the **MAP 1:region** command (where region is one of the database region names listed in *Table 10.2*). An example of the **MAP** command is shown in *Figure 10.1*.

```
=>>MAP 1:meter <Enter>

Virtual Device 1, Data Region METER Map

Data Item      Starting Address    Type

_YEAR          1000h               int
DAY_OF_YEAR    1001h               int
TIME(ms)       1002h               int[2]
FREQ           1004h               float
VDC1           1006h               float
IS(A)          1008h               float[6]
IT(A)          1014h               float[6]
IU(A)          1020h               float[6]
IW(A)          102ch               float[6]
IX(A)          1038h               float[6]
IY(A)          1044h               float[6]
VV(V)          1050h               float[6]
VZ(V)          105ch               float[6]
IST(A)         1068h               float[6]
ITU(A)         1074h               float[6]
IUW(A)         1080h               float[6]
IWX(A)         108ch               float[6]
ISEQ_S(A)      1098h               float[6]
ISEQ_T(A)      10a4h               float[6]
ISEQ_U(A)      10b0h               float[6]
ISEQ_W(A)      10bch               float[6]
ISEQ_X(A)      10c8h               float[6]
ISEQ_ST(A)     10d4h               float[6]
ISEQ_TU(A)     10e0h               float[6]
ISEQ_UW(A)     10ech               float[6]
ISEQ_WX(A)     10f8h               float[6]
VV_LL(V)       1104h               float[6]
VZ_LL(V)       1110h               float[6]
VSEQ_V(V)      111ch               float[6]
VSEQ_Z(V)      1128h               float[6]
PS(W)          1134h               float[4]
QS(VAR)        113ch               float[4]
SS(VA)         1144h               float[4]
PT(W)          114ch               float[4]
QT(VAR)        1154h               float[4]
ST(VA)         115ch               float[4]
PU(W)          1164h               float[4]
QU(VAR)        116ch               float[4]
SU(VA)         1174h               float[4]
PW(W)          117ch               float[4]
QW(VAR)        1184h               float[4]
SW(VA)         118ch               float[4]
PX(W)          1194h               float[4]
QX(VAR)        119ch               float[4]
SX(VA)         11a4h               float[4]
PST(W)         11ach               float[4]
QST(VAR)       11b4h               float[4]
SST(VA)        11bch               float[4]
```

Figure 10.1   MAP 1:METER Command Example

```
PTU(W)      11c4h           float[4]
QTU(VAR)    11cch           float[4]
STU(VA)     11d4h           float[4]
PUW(W)      11dch           float[4]
QUW(VAR)    11e4h           float[4]
SUW(VA)     11ech           float[4]
PWX(W)      11f4h           float[4]
QWX(VAR)    11fch           float[4]
SWX(VA)     1204h           float[4]
PFS         120ch           float[4]
PFT         1214h           float[4]
PFU         121ch           float[4]
PFW         1224h           float[4]
PFX         122ch           float[4]
PFST        1234h           float[4]
PFTU        123ch           float[4]
PFUW        1244h           float[4]
PFWX        124ch           float[4]
ES(kWh)     1254h           float[4]
ET(kWh)     125ch           float[4]
EU(kWh)     1264h           float[4]
EW(kWh)     126ch           float[4]
EX(kWh)     1274h           float[4]
EST(kWh)    127ch           float[4]
ETU(kWh)    1284h           float[4]
EUW(kWh)    128ch           float[4]
EWX(kWh)    1294h           float[4]

=>>
```

Figure 10.1 MAP 1:METER Command Example (Continued)

DNP3 Communication

DNP3 operation is described in *Section 16: DNP3 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes aspects of DNP3 communication that are unique to the SEL-487E.

Reference Data Map

Table 10.11–Table 10.15 shows the SEL-487E DNP3 reference data maps. The reference data maps contain all of the data points available to the DNP3 protocol. You can select the default subset or use the custom DNP3 mapping functions of the SEL-487E to create or edit maps that contain the points required by your application.

Table 10.11 shows the Binary Input reference map. The entire Relay Word (see *Section 11: Relay Word Bits*) is part of the DNP3 reference map. You may include any label in the Relay Word as part of a DNP3 custom map. Note that Binary Inputs registered as SER points (SET R settings) will maintain SER-quality time stamps for DNP3 events.

Table 10.11 SEL-487E Binary Input Reference Data Map

Object	Label	Description
01, 02	RLYDIS	Relay disabled
01, 02	STFAIL	Relay diagnostic failure
01, 02	STWARN	Relay diagnostic warning
01, 02	STSET	Settings change or relay restart
01, 02	UNRDEV	New relay event available
01, 02	NUNREV	An unread event exists, newer than the event in the Event summary AIs
01, 02	Relay Word	Relay Word bit label. See *Section 11: Relay Word Bits*.

Table 10.12 shows the Binary Output reference map. See *Binary Outputs on page 10.27* for additional information.

Table 10.12   SEL-487E Binary Output Reference Data Map (Sheet 1 of 2)

Object	Label	Description
10, 12	RB01–RB32	Remote Bits RB01–RB32
10, 12	RB01:RB01 RB02:RB02 RB03:RB03 • • • RB32:RB32 RB01:RB02 RB03:RB04 RB05:RB06 • • • RB31:RB32	Remote Bit pulse operation, RB01 Remote Bit pulse operation, RB02 Remote Bit pulse operation, RB03 • • • Remote Bit pulse operation, RB32 Remote Bit pairs RB01–RB02 Remote Bit pairs RB03–RB04 Remote Bit pairs RB05–RB06 • • • Remote Bit pairs RB31–RB32
10, 12	OCS	Open Circuit Breaker S control
10, 12	CCS	Close Circuit Breaker S control
10, 12	OCT	Open Circuit Breaker T control
10, 12	CCT	Close Circuit Breaker T control
10, 12	OCU	Open Circuit Breaker U control
10, 12	CCU	Close Circuit Breaker U control
10, 12	OCW	Open Circuit Breaker W control
10, 12	CCW	Close Circuit Breaker W control
10, 12	OCX	Open Circuit Breaker X control
10, 12	CCX	Close Circuit Breaker X control
10, 12	OCS:CCS	Open/Close Circuit Breaker S control pair
10, 12	OCT:CCT	Open/Close Circuit Breaker T control pair
10, 12	OCU:CCU	Open/Close Circuit Breaker U control pair
10, 12	OCW:CCW	Open/Close Circuit Breaker W control pair
10, 12	OCX:CCX	Open/Close Circuit Breaker X control pair
10, 12	89OC01–89OC20	Open Disconnect Control 1–20
10, 12	89CC01–89CC20	Close Disconnect Control 1–20
10, 12	89OC01:89CC01 89OC02:89CC02 • • • 89OC20:89CC20	Open/Close Disconnect Control Pair 1 Open/Close Disconnect Control Pair 2 • • • Open/Close Disconnect Control Pair 20
10, 12	RST_DEM	Reset demand meter data
10, 12	RST_PDM	Reset peak demand meter data
10, 12	RST_ENE	Reset accumulated energy meter data
10, 12	RST_BKS	Reset Breaker S monitor data
10, 12	RST_BKT	Reset Breaker T monitor data

Table 10.12   SEL-487E Binary Output Reference Data Map (Sheet 2 of 2)

Object	Label	Description
10, 12	RST_BKU	Reset Breaker U monitor data
10, 12	RST_BKW	Reset Breaker W monitor data
10, 12	RST_BKX	Reset Breaker X monitor data
10, 12	RST_BAT	Reset battery monitoring
10, 12	RST_HAL	Reset alarm pulsing
10, 12	RSTTRGT	Reset targets
10, 12	RSTDNPE	Reset (clear) DNP event summary registers
10, 12	NXTEVE	Load next event into DNP event summary registers

Table 10.13 shows the Binary Counter reference map. See *Counters on page 16.23 in the SEL-400 Series Relays Instruction Manual* for additional information.

Table 10.13   SEL-487E Binary Counter Reference Data Map (Sheet 1 of 2)

Object	Label	Description
20, 22	ACTGRP	Active settings group
20, 22	BKRSOP	Number of Breaker S operations
20, 22	BKRTOP	Number of Breaker T operations
20, 22	BKRUOP	Number of Breaker U operations
20, 22	BKRWOP	Number of Breaker W operations
20, 22	BKRXOP	Number of Breaker X operations
20, 22	ACN01CV–ACN32CV	Automation SELOGIC counter values
20, 22	PCN01CV–PCN32CV	Protection SELOGIC counter values
20, 22	3PSKWHP[a]	Three-phase active energy exported (kWh), Terminal S
20, 22	3QSKVHP[a]	Three-phase reactive energy exported (kVARh), Terminal S
20, 22	3PSKWHN[a]	Three-phase active energy imported (kWh), Terminal S
20, 22	3QSKVHN[a]	Three-phase reactive energy imported (kVARh), Terminal S
20, 22	3PTKWHP[a]	Three-phase active energy exported (kWh), Terminal T
20, 22	3QTKVHP[a]	Three-phase reactive energy exported (kVARh), Terminal T
20, 22	3PTKWHN[a]	Three-phase active energy imported (kWh), Terminal T
20, 22	3QTKVHN[a]	Three-phase reactive energy imported (kVARh), Terminal T
20, 22	3PUKWHP[a]	Three-phase active energy exported (kWh), Terminal U
20, 22	3QUKVHP[a]	Three-phase reactive energy exported (kVARh), Terminal U
20, 22	3PUKWHN[a]	Three-phase active energy imported (kWh), Terminal U
20, 22	3QUKVHN[a]	Three-phase reactive energy imported (kVARh), Terminal U
20, 22	3PWKWHP[a]	Three-phase active energy exported (kWh), Terminal W
20, 22	3QWKVHP[a]	Three-phase reactive energy exported (kVARh), Terminal W
20, 22	3PWKWHN[a]	Three-phase active energy imported (kWh), Terminal W
20, 22	3QWKVHN[a]	Three-phase reactive energy imported (kVARh), Terminal W
20, 22	3PXKWHP[a]	Three-phase active energy exported (kWh), Terminal X
20, 22	3QXKVHP[a]	Three-phase reactive energy exported (kVARh), Terminal X

Table 10.13 SEL-487E Binary Counter Reference Data Map (Sheet 2 of 2)

Object	Label	Description
20, 22	3PXKWHN[a]	Three-phase active energy imported (kWh), Terminal X
20, 22	3QXKVHN[a]	Three-phase reactive energy imported (kVARh), Terminal X
20, 22	3STKWHP[a]	Three-phase active energy exported (kWh), combined Terminals ST
20, 22	3STKVHP[a]	Three-phase reactive energy exported (kVARh), combined Terminals ST
20, 22	3STKWHN[a]	Three-phase active energy imported (kWh), combined Terminals ST
20, 22	3STKVHN[a]	Three-phase reactive energy imported (kVARh), combined Terminals ST
20, 22	3TUKWHP[a]	Three-phase active energy exported (kWh), combined Terminals TU
20, 22	3TUKVHP[a]	Three-phase reactive energy exported (kVARh), combined Terminals TU
20, 22	3TUKWHN[a]	Three-phase active energy imported (kWh), combined Terminals TU
20, 22	3TUKVHN[a]	Three-phase reactive energy imported (kVARh), Combined terminals TU
20, 22	3UWKWHP[a]	Three-phase active energy exported (kWh), combined Terminals UW
20, 22	3UWKVHP[a]	Three-phase reactive energy exported (kVARh), combined Terminals UW
20, 22	3UWKWHN[a]	Three-phase active energy imported (kWh), combined Terminals UW
20, 22	3UWKVHN[a]	Three-phase reactive energy imported (kVARh), combined Terminals UW
20, 22	3WXKWHP[a]	Three-phase active energy exported (kWh), combined Terminals WX
20, 22	3WXKVHP[a]	Three-phase reactive energy exported (kVARh), combined Terminals WX
20, 22	3WXKWHN[a]	Three-phase active energy imported (kWh), combined Terminals WX
20, 22	3WXKVHN[a]	Three-phase reactive energy imported (kVARh), combined Terminals WX

[a] Converts to the absolute value and forces the counter to a positive value.

Table 10.14 shows the Analog Input reference map. The SEL-487E scales analog values by the indicated settings or fixed scaling. Analog inputs for event (fault) summary reporting use a default scale factor of 1 and dead band of ANADBM. Per-point scaling and dead band settings specified in a custom DNP3 map will override defaults.

Table 10.14 SEL-487E Analog Input Reference Data Map (Sheet 1 of 16)

Object	Label	Description
30, 32	FREQPM[a]	Frequency for synchrophasor data (Hz)
30, 32	DFDTPM[a]	Rate-of-change of frequency for synchrophasor data (Hz/s)
30, 32	VAVFMC, VAVFAC[b]	1-cycle average filtered, A-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VBVFMC, VBVFAC[b]	1-cycle average filtered, B-Phase voltage magnitude (kV) and angle, V-PT

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 2 of 16)

Object	Label	Description
30, 32	VCVFMC, VCVFAC[b]	1-cycle average filtered, C-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VAZFMC, VAZFAC[b]	1-cycle average filtered, A-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VBZFMC, VBZFAC[b]	1-cycle average filtered, B-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VCZFMC, VCZFAC[b]	1-cycle average filtered, C-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VABVFMC, VABVFAC[b]	1-cycle average filtered, AB-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VBCVFMC, VBCVFAC[b]	1-cycle average filtered, BC-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VCAVFMC, VCAVFAC[b]	1-cycle average filtered, CA-Phase voltage magnitude (kV) and angle, V-PT
30, 32	VABZFMC, VABZFAC[b]	1-cycle average filtered, AB-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VBCZFMC, VBCZFAC[b]	1-cycle average filtered, BC-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VCAZFMC, VCAZFAC[b]	1-cycle average filtered, CA-Phase voltage magnitude (kV) and angle, Z-PT
30, 32	VAVRC[c]	1-cycle average rms, A-Phase voltage magnitude (kV), V-PT
30, 32	VBVRC[c]	1-cycle average rms, B-Phase voltage magnitude (kV), V-PT
30, 32	VCVRC[c]	1-cycle average rms, C-Phase voltage magnitude (kV), V-PT
30, 32	VAZRC[c]	1-cycle average rms, A-Phase voltage magnitude (kV), Z-PT
30, 32	VBZRC[c]	1-cycle average rms, B-Phase voltage magnitude (kV), Z-PT
30, 32	VCZRC[c]	1-cycle average rms, C-Phase voltage magnitude (kV), Z-PT
30, 32	VABVRC[c]	1-cycle average rms, AB-Phase voltage magnitude (kV), V-PT
30, 32	VBCVRC[c]	1-cycle average rms, BC-Phase voltage magnitude (kV), V-PT
30, 32	VCAVRC[c]	1-cycle average rms, CA-Phase voltage magnitude (kV), V-PT
30, 32	VABZRC[c]	1-cycle average rms, AB-Phase voltage magnitude (kV), Z-PT
30, 32	VBCZRC[c]	1-cycle average rms, BC-Phase voltage magnitude (kV), Z-PT
30, 32	VCAZRC[c]	1-cycle average rms, CA-Phase voltage magnitude (kV), Z-PT
30, 32	V1VMC, V1VAC[b]	1-cycle average, positive-sequence voltage magnitude (kV) and angle, V-PT
30, 32	V1ZMC, V1ZAC[b]	1-cycle average, positive-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	3V2VMC, 3V2VAC[b]	1-cycle average, negative-sequence voltage magnitude (kV) and angle, V-PT
30, 32	3V2ZMC, 3V2ZAC[b]	1-cycle average, negative-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	3V0VMC, 3V0VAC[b]	1-cycle average, zero-sequence voltage magnitude (kV) and angle, V-PT
30, 32	3V0ZMC, 3V0ZAC[b]	1-cycle average, zero-sequence voltage magnitude (kV) and angle, Z-PT
30, 32	IASFMC, IASFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, Terminal S
30, 32	IBSFMC, IBSFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, Terminal S
30, 32	ICSFMC, ICSFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, Terminal S
30, 32	IATFMC, IATFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, Terminal T
30, 32	IBTFMC, IBTFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, Terminal T
30, 32	ICTFMC, ICTFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, Terminal T
30, 32	IAUFMC, IAUFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, Terminal U
30, 32	IBUFMC, IBUFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, Terminal U

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 3 of 16)

Object	Label	Description
30, 32	ICUFMC, ICUFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, Terminal U
30, 32	IAWFMC, IAWFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, Terminal W
30, 32	IBWFMC, IBWFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, Terminal W
30, 32	ICWFMC, ICWFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, Terminal W
30, 32	IAXFMC, IAXFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, Terminal X
30, 32	IBXFMC, IBXFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, Terminal X
30, 32	ICXFMC, ICXFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, Terminal X
30, 32	IY1FMC, IY1FAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, Channel 1, Terminal Y
30, 32	IY2FMC, IY2FAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, Channel 2, Terminal Y
30, 32	IY3FMC, IY3FAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, Channel 3, Terminal Y
30, 32	IASRC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, Terminal S
30, 32	IBSRC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, Terminal S
30, 32	ICSRC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, Terminal S
30, 32	IATRC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, Terminal T
30, 32	IBTRC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, Terminal T
30, 32	ICTRC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, Terminal T
30, 32	IAURC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, Terminal U
30, 32	IBURC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, Terminal U
30, 32	ICURC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, Terminal U
30, 32	IAWRC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, Terminal W
30, 32	IBWRC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, Terminal W
30, 32	ICWRC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, Terminal W
30, 32	IAXRC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, Terminal X
30, 32	IBXRC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, Terminal X
30, 32	ICXRC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, Terminal X
30, 32	IASTFMC, IASTFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, combined Terminals ST
30, 32	IBSTFMC, IBSTFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, combined Terminals ST
30, 32	ICSTFMC, ICSTFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, combined Terminals ST
30, 32	IATUFMC, IATUFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, combined Terminals TU
30, 32	IBTUFMC, IBTUFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, combined Terminals TU
30, 32	ICTUFMC, ICTUFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, combined Terminals TU

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 4 of 16)

Object	Label	Description
30, 32	IAUWFMC, IAUWFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, combined Terminals UW
30, 32	IBUWFMC, IBUWFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, combined Terminals UW
30, 32	ICUWFMC, ICUWFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, combined Terminals UW
30, 32	IAWXFMC, IAWXFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, A-Phase, combined Terminals WX
30, 32	IBWXFMC, IBWXFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, B-Phase, combined Terminals WX
30, 32	ICWXFMC, ICWXFAC[d]	1-cycle average filtered phase-current magnitude (amperes primary) and angle, C-Phase, combined Terminals WX
30, 32	IASTRC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, combined Terminals ST
30, 32	IBSTRC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, combined Terminals ST
30, 32	ICSTRC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, combined Terminals ST
30, 32	IATURC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, combined Terminals TU
30, 32	IBTURC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, combined Terminals TU
30, 32	ICTURC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, combined Terminals TU
30, 32	IAUWRC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, combined Terminals UW
30, 32	IBUWRC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, combined Terminals UW
30, 32	ICUWRC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, combined Terminals UW
30, 32	IAWXRC[f]	1-cycle average rms phase-current magnitude (amperes primary), A-Phase, combined Terminals WX
30, 32	IBWXRC[f]	1-cycle average rms phase-current magnitude (amperes primary), B-Phase, combined Terminals WX
30, 32	ICWXRC[f]	1-cycle average rms phase-current magnitude (amperes primary), C-Phase, combined Terminals WX
30, 32	I1SMC, I1SAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, Terminal S
30, 32	I1TMC, I1TAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, Terminal T
30, 32	I1UMC, I1UAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, Terminal U
30, 32	I1WMC, I1WAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, Terminal W
30, 32	I1XMC, I1XAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, Terminal X
30, 32	3I2SMC, 3I2SAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, Terminal S
30, 32	3I2TMC, 3I2TAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, Terminal T
30, 32	3I2UMC, 3I2UAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, Terminal U
30, 32	3I2WMC, 3I2WAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, Terminal W
30, 32	3I2XMC, 3I2XAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, Terminal X
30, 32	3I0SMC, 3I0SAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, Terminal S
30, 32	3I0TMC, 3I0TAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, Terminal T
30, 32	3I0UMC, 3I0UAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, Terminal U

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 5 of 16)

Object	Label	Description
30, 32	3I0WMC, 3I0WAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, Terminal W
30, 32	3I0XMC, 3I0XAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, Terminal X
30, 32	I1STMC, I1STAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, combined Terminals ST
30, 32	I1TUMC, I1TUAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, combined Terminals TU
30, 32	I1UWMC, I1UWAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, combined Terminals UW
30, 32	I1WXMC, I1WXAC[d]	1-cycle average positive-sequence current magnitude (amperes primary) and angle, combined Terminals WX
30, 32	3I2STMC, 3I2STAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, combined Terminals ST
30, 32	3I2TUMC, 3I2TUAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, combined Terminals TU
30, 32	3I2UWMC, 3I2UWAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, combined Terminals UW
30, 32	3I2WXMC, 3I2WXAC[d]	1-cycle average negative-sequence current magnitude (amperes primary) and angle, combined Terminals WX
30, 32	3I0STMC, 3I0STAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, combined Terminals ST
30, 32	3I0TUMC, 3I0TUAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, combined Terminals TU
30, 32	3I0UWMC, 3I0UWAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, combined Terminals UW
30, 32	3I0WXMC, 3I0WXAC[d]	1-cycle average zero-sequence current magnitude (amperes primary) and angle, combined Terminals WX
30, 32	IASRS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, Terminal S
30, 32	IBSRS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, Terminal S
30, 32	ICSRS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, Terminal S
30, 32	IATRS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, Terminal T
30, 32	IBTRS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, Terminal T
30, 32	ICTRS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, Terminal T
30, 32	IAURS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, Terminal U
30, 32	IBURS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, Terminal U
30, 32	ICURS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, Terminal U
30, 32	IAWRS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, Terminal W
30, 32	IBWRS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, Terminal W
30, 32	ICWRS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, Terminal W
30, 32	IAXRS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, Terminal X
30, 32	IBXRS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, Terminal X
30, 32	ICXRS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, Terminal X
30, 32	IASTRS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, combined Terminals ST
30, 32	IBSTRS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, combined Terminals ST
30, 32	ICSTRS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, combined Terminals ST
30, 32	IATURS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, combined Terminals TU

Table 10.14 SEL-487E Analog Input Reference Data Map (Sheet 6 of 16)

Object	Label	Description
30, 32	IBTURS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, combined Terminals TU
30, 32	ICTURS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, combined Terminals TU
30, 32	IAUWRS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, combined Terminals UW
30, 32	IBUWRS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, combined Terminals UW
30, 32	ICUWRS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, combined Terminals UW
30, 32	IAWXRS[f]	1-second average rms phase-current magnitude (amperes secondary), A-Phase, combined Terminals WX
30, 32	IBWXRS[f]	1-second average rms phase-current magnitude (amperes secondary), B-Phase, combined Terminals WX
30, 32	ICWXRS[f]	1-second average rms phase-current magnitude (amperes secondary), C-Phase, combined Terminals WX
30, 32	IMXSRS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), Terminal S
30, 32	IMXTRS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), Terminal T
30, 32	IMXURS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), Terminal U
30, 32	IMXWRS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), Terminal W
30, 32	IMXXRS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), Terminal X
30, 32	IMXSTRS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), combined Terminals ST
30, 32	IMXTURS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), combined Terminals TU
30, 32	IMXUWRS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), combined Terminals UW
30, 32	IMXWXRS[f]	1-second average maximum rms phase-current magnitude, (amperes secondary), combined Terminals WX
30, 32	3I2SMS[f]	1-second average negative-sequence current magnitude, (amperes secondary), Terminal S
30, 32	3I2TMS[f]	1-second average negative-sequence current magnitude, (amperes secondary), Terminal T
30, 32	3I2UMS[f]	1-second average negative-sequence current magnitude, (amperes secondary), Terminal U
30, 32	3I2WMS[f]	1-second average negative-sequence current magnitude, (amperes secondary), Terminal W
30, 32	3I2XMS[f]	1-second average negative-sequence current magnitude, (amperes secondary), Terminal X
30, 32	3I2STMS[f]	1-second average negative-sequence current magnitude, (amperes secondary), combined Terminals ST
30, 32	3I2TUMS[f]	1-second average negative-sequence current magnitude, (amperes secondary) combined Terminals TU
30, 32	3I2UWMS[f]	1-second average negative-sequence current magnitude, (amperes secondary), combined Terminals UW
30, 32	3I2WXMS[f]	1-second average negative-sequence current magnitude, (amperes secondary), combined Terminals WX
30, 32	3I0SMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), Terminal S
30, 32	3I0TMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), Terminal T
30, 32	3I0UMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), Terminal U
30, 32	3I0WMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), Terminal W
30, 32	3I0XMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), Terminal X
30, 32	3I0STMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), combined Terminals ST
30, 32	3I0TUMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), combined Terminals TU
30, 32	3I0UWMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), combined Terminals UW
30, 32	3I0WXMS[f]	1-second average zero-sequence current magnitude, (amperes secondary), combined Terminals WX
30, 32	PASFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal S
30, 32	PBSFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal S
30, 32	PCSFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal S

Table 10.14 SEL-487E Analog Input Reference Data Map (Sheet 7 of 16)

Object	Label	Description
30, 32	PATFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal T
30, 32	PBTFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal T
30, 32	PCTFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal T
30, 32	PAUFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal U
30, 32	PBUFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal U
30, 32	PCUFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal U
30, 32	PAWFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal W
30, 32	PBWFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal W
30, 32	PCWFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal W
30, 32	PAXFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), A-Phase, Terminal X
30, 32	PBXFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), B-Phase, Terminal X
30, 32	PCXFC[e]	1-cycle average phase fundamental active power magnitude (megawatts primary), C-Phase, Terminal X
30, 32	QASFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), A-Phase, Terminal S
30, 32	QBSFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), B-Phase, Terminal S
30, 32	QCSFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), C-Phase, Terminal S
30, 32	QATFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), A-Phase, Terminal T
30, 32	QBTFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), B-Phase, Terminal T
30, 32	QCTFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), C-Phase, Terminal T
30, 32	QAUFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), A-Phase, Terminal U
30, 32	QBUFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), B-Phase, Terminal U
30, 32	QCUFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), C-Phase, Terminal U
30, 32	QAWFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), A-Phase, Terminal W
30, 32	QBWFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), B-Phase, Terminal W
30, 32	QCWFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), C-Phase, Terminal W
30, 32	QAXFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), A-Phase, Terminal X
30, 32	QBXFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), B-Phase, Terminal X
30, 32	QCXFC[e]	1-cycle average phase fundamental reactive power magnitude (megavar primary), C-Phase, Terminal X
30, 32	SASFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), A-Phase, Terminal S
30, 32	SBSFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), B-Phase, Terminal S
30, 32	SCSFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), C-Phase, Terminal S
30, 32	SATFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), A-Phase, Terminal T
30, 32	SBTFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), B-Phase, Terminal T
30, 32	SCTFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), C-Phase, Terminal T

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 8 of 16)

Object	Label	Description
30, 32	SAUFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), A-Phase, Terminal U
30, 32	SBUFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), B-Phase, Terminal U
30, 32	SCUFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), C-Phase, Terminal U
30, 32	SAWFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), A-Phase, Terminal W
30, 32	SBWFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), B-Phase, Terminal W
30, 32	SCWFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), C-Phase, Terminal W
30, 32	SAXFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), A-Phase, Terminal X
30, 32	SBXFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), B-Phase, Terminal X
30, 32	SCXFC[e]	1-cycle average phase fundamental apparent power magnitude (megavoltamp primary), C-Phase, Terminal X
30, 32	3PSFC[e]	1-cycle average three-phase fundamental active power magnitude, (megawatts primary), Terminal S
30, 32	3PTFC[e]	1-cycle average three-phase fundamental active power magnitude, (megawatts primary), Terminal T
30, 32	3PUFC[e]	1-cycle average three-phase fundamental active power magnitude, (megawatts primary), Terminal U
30, 32	3PWFC[e]	1-cycle average three-phase fundamental active power magnitude, (megawatts primary), Terminal W
30, 32	3PXFC[e]	1-cycle average three-phase fundamental active power magnitude, (megawatts primary), Terminal X
30, 32	3QSFC[e]	1-cycle average three-phase fundamental reactive power magnitude, (megavars primary), Terminal S
30, 32	3QTFC[e]	1-cycle average three-phase fundamental reactive power magnitude, (megavars primary), Terminal T
30, 32	3QUFC[e]	1-cycle average three-phase fundamental reactive power magnitude, (megavars primary), Terminal U
30, 32	3QWFC[e]	1-cycle average three-phase fundamental reactive power magnitude, (megavars primary), Terminal W
30, 32	3QXFC[e]	1-cycle average three-phase fundamental apparent power magnitude, (megavars primary), Terminal X
30, 32	3SSFC[e]	1-cycle average three-phase fundamental apparent power magnitude, (megavoltamp primary), Terminal S
30, 32	3STFC[e]	1-cycle average three-phase fundamental apparent power magnitude, (megavoltamp primary), Terminal T
30, 32	3SUFC[e]	1-cycle average three-phase fundamental apparent power magnitude, (megavoltamp primary), Terminal U
30, 32	3SWFC[e]	1-cycle average three-phase fundamental apparent power magnitude, (megavoltamp primary), Terminal W
30, 32	3SXFC[e]	1-cycle average three-phase fundamental apparent power magnitude, (megavoltamp primary), Terminal X
30, 32	PASTFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, A-Phase, combined Terminals ST
30, 32	PBSTFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, B-Phase, combined Terminals ST
30, 32	PCSTFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, C-Phase, combined Terminals ST
30, 32	PATUFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, A-Phase, combined Terminals TU
30, 32	PBTUFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, B-Phase, combined Terminals TU
30, 32	PCTUFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, C-Phase, combined Terminals TU
30, 32	PAUWFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, A-Phase, combined Terminals UW

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 9 of 16)

Object	Label	Description
30, 32	PBUWFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, B-Phase, combined Terminals UW
30, 32	PCUWFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, C-Phase, combined Terminals UW
30, 32	PAWXFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, A-Phase, combined Terminals WX
30, 32	PBWXFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, B-Phase, combined Terminals WX
30, 32	PCWXFC[e]	1-cycle average phase fundamental active power magnitude, megawatts primary, C-Phase, combined Terminals WX
30, 32	QASTFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, A-Phase, combined Terminals ST
30, 32	QBSTFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, B-Phase, combined Terminals ST
30, 32	QCSTFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, C-Phase, combined Terminals ST
30, 32	QATUFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, A-Phase, combined Terminals TU
30, 32	QBTUFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, B-Phase, combined Terminals TU
30, 32	QCTUFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, C-Phase, combined Terminals TU
30, 32	QAUWFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, A-Phase, combined Terminals UW
30, 32	QBUWFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, B-Phase, combined Terminals UW
30, 32	QCUWFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, C-Phase, combined Terminals UW
30, 32	QAWXFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, A-Phase, combined Terminals WX
30, 32	QBWXFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, B-Phase, combined Terminals WX
30, 32	QCWXFC[e]	1-cycle average phase fundamental reactive power magnitude, megavars primary, C-Phase, combined Terminals WX
30, 32	SASTFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, A-Phase, combined Terminals ST
30, 32	SBSTFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, B-Phase, combined Terminals ST
30, 32	SCSTFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, C-Phase, combined Terminals ST
30, 32	SATUFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, A-Phase, combined Terminals TU
30, 32	SBTUFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, B-Phase, combined Terminals TU
30, 32	SCTUFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, C-Phase, combined Terminals TU
30, 32	SAUWFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, A-Phase, combined Terminals UW
30, 32	SBUWFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, B-Phase, combined Terminals UW

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 10 of 16)

Object	Label	Description
30, 32	SCUWFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, C-Phase, combined Terminals UW
30, 32	SAWXFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, A-Phase, combined Terminals WX
30, 32	SBWXFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, B-Phase, combined Terminals WX
30, 32	SCWXFC[e]	1-cycle average phase fundamental apparent power magnitude, megavoltamps primary, C-Phase, combined Terminals WX
30, 32	3PSTFC[e]	1-cycle average three-phase fundamental active power magnitude, megawatts primary, combined Terminals ST
30, 32	3PTUFC[e]	1-cycle average three-phase fundamental active power magnitude, megawatts primary, combined Terminals TU
30, 32	3PUWFC[e]	1-cycle average three-phase fundamental active power magnitude, megawatts primary, combined Terminals UW
30, 32	3PWXFC[e]	1-cycle average three-phase fundamental active power magnitude, megawatts primary, combined Terminals WX
30, 32	3QSTFC[e]	1-cycle average three-phase fundamental reactive power magnitude, megavars primary, combined Terminals ST
30, 32	3QTUFC[e]	1-cycle average three-phase fundamental reactive power magnitude, megavars primary, combined Terminals TU
30, 32	3QUWFC[e]	1-cycle average three-phase fundamental reactive power magnitude, megavars primary, combined Terminals UW
30, 32	3QWXFC[e]	1-cycle average three-phase fundamental reactive power magnitude, megavars primary, combined Terminals WX
30, 32	3SSTFC[e]	1-cycle average three-phase fundamental apparent power magnitude, megavoltamps primary, combined Terminals ST
30, 32	3STUFC[e]	1-cycle average three-phase fundamental apparent power magnitude, megavoltamps primary, combined Terminals TU
30, 32	3SUWFC[e]	1-cycle average three-phase fundamental apparent power magnitude, megavoltamps primary, combined Terminals UW
30, 32	3SWXFC[e]	1-cycle average three-phase fundamental apparent power magnitude, megavoltamps primary, combined Terminals WX
30, 32	DPFAS[e]	Phase displacement power factor, A-Phase, Terminal S
30, 32	DPFBS[e]	Phase displacement power factor, B-Phase, Terminal S
30, 32	DPFCS[e]	Phase displacement power factor, C-Phase, Terminal S
30, 32	DPFAT[e]	Phase displacement power factor, A-Phase, Terminal T
30, 32	DPFBT[e]	Phase displacement power factor, B-Phase, Terminal T
30, 32	DPFCT[e]	Phase displacement power factor, C-Phase, Terminal T
30, 32	DPFAU[e]	Phase displacement power factor, A-Phase, Terminal U
30, 32	DPFBU[e]	Phase displacement power factor, B-Phase, Terminal U
30, 32	DPFCU[e]	Phase displacement power factor, C-Phase, Terminal U
30, 32	DPFAW[e]	Phase displacement power factor, A-Phase, Terminal W
30, 32	DPFBW[e]	Phase displacement power factor, B-Phase, Terminal W
30, 32	DPFCW[e]	Phase displacement power factor, C-Phase, Terminal W
30, 32	DPFAX[e]	Phase displacement power factor, A-Phase, Terminal X
30, 32	DPFBX[e]	Phase displacement power factor, B-Phase, Terminal X
30, 32	DPFCX[e]	Phase displacement power factor, C-Phase, Terminal X

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 11 of 16)

Object	Label	Description
30, 32	3DPFS[e]	Three-phase displacement power factor, Terminal S
30, 32	3DPFT[e]	Three-phase displacement power factor, Terminal T
30, 32	3DPFU[e]	Three-phase displacement power factor, Terminal U
30, 32	3DPFW[e]	Three-phase displacement power factor, Terminal W
30, 32	3DPFX[e]	Three-phase displacement power factor, Terminal X
30, 32	DPFAST[e]	Phase displacement power factor, A-Phase, combined Terminals ST
30, 32	DPFBST[e]	Phase displacement power factor, B-Phase, combined Terminals ST
30, 32	DPFCST[e]	Phase displacement power factor, C-Phase, combined Terminals ST
30, 32	DPFATU[e]	Phase displacement power factor, A-Phase, combined Terminals TU
30, 32	DPFBTU[e]	Phase displacement power factor, B-Phase, combined Terminals TU
30, 32	DPFCTU[e]	Phase displacement power factor, C-Phase, combined Terminals TU
30, 32	DPFAUW[e]	Phase displacement power factor, A-Phase, combined Terminals UW
30, 32	DPFBUW[e]	Phase displacement power factor, B-Phase, combined Terminals UW
30, 32	DPFCUW[e]	Phase displacement power factor, C-Phase, combined Terminals UW
30, 32	DPFAWX[e]	Phase displacement power factor, A-Phase, combined Terminals WX
30, 32	DPFBWX[e]	Phase displacement power factor, B-Phase, combined Terminals WX
30, 32	DPFCWX[e]	Phase displacement power factor, C-Phase, combined Terminals WX
30, 32	3DPFST[e]	Three-phase displacement power factor, combined Terminals ST
30, 32	3DPFTU[e]	Three-phase displacement power factor, combined Terminals TU
30, 32	3DPFUW[e]	Three-phase displacement power factor, combined Terminals UW
30, 32	3DPFWX[e]	Three-phase displacement power factor, combined Terminals WX
30, 32	87IOPAC[f]	1-cycle average differential element operating current (per unit), A-Phase
30, 32	87IOPBC[f]	1-cycle average differential element restraint current (per unit), B-Phase
30, 32	87IOPCC[f]	1-cycle average differential element restraint current (per unit), C-Phase
30, 32	87IRTAC[f]	1-cycle average differential element restraint current (per unit), A-Phase
30, 32	87IRTBC[f]	1-cycle average differential element restraint current (per unit), B-Phase
30, 32	87IRTCC[f]	1-cycle average differential element restraint current (per unit), C-Phase
30, 32	DM01	Demand metering Element 1 value, amperes secondary
30, 32	DM02	Demand metering Element 2 value, amperes secondary
30, 32	DM03	Demand metering Element 3 value, amperes secondary
30, 32	DM04	Demand metering Element 4 value, amperes secondary
30, 32	DM05	Demand metering Element 5 value, amperes secondary
30, 32	DM06	Demand metering Element 6 value, amperes secondary
30, 32	DM07	Demand metering Element 7 value, amperes secondary
30, 32	DM08	Demand metering Element 8 value, amperes secondary
30, 32	DM09	Demand metering Element 9 value, amperes secondary
30, 32	DM10	Demand metering Element 10 value, amperes secondary
30, 32	DMM01	Demand metering Element 1 maximum value, amperes secondary
30, 32	DMM02	Demand metering Element 2 maximum value, amperes secondary
30, 32	DMM03	Demand metering Element 3 maximum value, amperes secondary
30, 32	DMM04	Demand metering Element 4 maximum value, amperes secondary

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 12 of 16)

Object	Label	Description
30, 32	DMM05	Demand metering Element 5 maximum value, amperes secondary
30, 32	DMM06	Demand metering Element 6 maximum value, amperes secondary
30, 32	DMM07	Demand metering Element 7 maximum value, amperes secondary
30, 32	DMM08	Demand metering Element 8 maximum value, amperes secondary
30, 32	DMM09	Demand metering Element 9 maximum value, amperes secondary
30, 32	DMM10	Demand metering Element 10 maximum value, amperes secondary
30, 32	RTD01TV	RTD temperature value in degrees C, RTD01
30, 32	RTD02TV	RTD temperature value in degrees C, RTD02
30, 32	RTD03TV	RTD temperature value in degrees C, RTD03
30, 32	RTD04TV	RTD temperature value in degrees C, RTD04
30, 32	RTD05TV	RTD temperature value in degrees C, RTD05
30, 32	RTD06TV	RTD temperature value in degrees C, RTD06
30, 32	RTD07TV	RTD temperature value in degrees C, RTD07
30, 32	RTD08TV	RTD temperature value in degrees C, RTD08
30, 32	RTD09TV	RTD temperature value in degrees C, RTD09
30, 32	RTD10TV	RTD temperature value in degrees C, RTD10
30, 32	RTD11TV	RTD temperature value in degrees C, RTD11
30, 32	RTD12TV	RTD temperature value in degrees C, RTD12
30, 32	3PSMWHP[e]	Three-phase active energy exported, Terminal S (megawatt hours, primary)
30, 32	3PTMWHP[e]	Three-phase active energy exported, Terminal T (megawatt hours, primary)
30, 32	3PUMWHP[e]	Three-phase active energy exported, Terminal U (megawatt hours, primary)
30, 32	3PWMWHP[e]	Three-phase active energy exported, Terminal W (megawatt hours, primary)
30, 32	3PXMWHP[e]	Three-phase active energy exported, Terminal X (megawatt hours, primary)
30, 32	3QSMVHP[e]	Three-phase reactive energy exported, Terminal S (megavar hours, primary)
30, 32	3QTMVHP[e]	Three-phase reactive energy exported, Terminal T (megavar hours, primary)
30, 32	3QUMVHP[e]	Three-phase reactive energy exported, Terminal U (megavar hours, primary)
30, 32	3QWMVHP[e]	Three-phase reactive energy exported, Terminal W (megavar hours, primary)
30, 32	3QXMVHP[e]	Three-phase reactive energy exported, Terminal X (megavar hours, primary)
30, 32	3PSMWHN[e]	Three-phase active energy imported, Terminal S (megawatt hours, primary)
30, 32	3PTMWHN[e]	Three-phase active energy imported, Terminal T (megawatt hours, primary)
30, 32	3PUMWHN[e]	Three-phase active energy imported, Terminal U (megawatt hours, primary)
30, 32	3PWMWHN[e]	Three-phase active energy imported, Terminal W (megawatt hours, primary)
30, 32	3PXMWHN[e]	Three-phase active energy imported, Terminal X (megawatt hours, primary)
30, 32	3QSMVHN[e]	Three-phase reactive energy imported, Terminal S (megavar hours, primary)
30, 32	3QTMVHN[e]	Three-phase reactive energy imported, Terminal T (megavar hours, primary)
30, 32	3QUMVHN[e]	Three-phase reactive energy imported, Terminal U (megavar hours, primary)
30, 32	3QWMVHN[e]	Three-phase reactive energy imported, Terminal W (megavar hours, primary)
30, 32	3QXMVHN[e]	Three-phase reactive energy imported, Terminal X (megavar hours, primary)
30, 32	3PSMWHT[e]	Total three-phase active energy, Terminal S (megawatt hours, primary)
30, 32	3PTMWHT[e]	Total three-phase active energy, Terminal T (megawatt hours, primary)

Table 10.14 SEL-487E Analog Input Reference Data Map (Sheet 13 of 16)

Object	Label	Description
30, 32	3PUMWHT[e]	Total three-phase active energy, Terminal U (megawatt hours, primary)
30, 32	3PWMWHT[e]	Total three-phase active energy, Terminal W (megawatt hours, primary)
30, 32	3PXMWHT[e]	Total three-phase active energy, Terminal X (megawatt hours, primary)
30, 32	3QSMVHT[e]	Total three-phase reactive energy, Terminal S (megavar hours, primary)
30, 32	3QTMVHT[e]	Total three-phase reactive energy, Terminal T (megavar hours, primary)
30, 32	3QUMVHT[e]	Total three-phase reactive energy, Terminal U (megavar hours, primary)
30, 32	3QWMVHT[e]	Total three-phase reactive energy, Terminal W (megavar hours, primary)
30, 32	3QXMVHT[e]	Total three-phase reactive energy, Terminal X (megavar hours, primary)
30, 32	3PSTWHP[e]	Three-phase active energy exported, combined Terminals ST (megawatt hours, primary)
30, 32	3PTUWHP[e]	Three-phase active energy exported, combined Terminals TU (megawatt hours, primary)
30, 32	3PUWWHP[e]	Three-phase active energy exported, combined Terminals UW (megawatt hours, primary)
30, 32	3PWXWHP[e]	Three-phase active energy exported, combined Terminals WX (megawatt hours, primary)
30, 32	3QSTVHP[e]	Three-phase reactive energy exported, combined Terminals ST (megavar hours, primary)
30, 32	3QTUVHP[e]	Three-phase reactive energy exported, combined Terminals TU (megavar hours, primary)
30, 32	3QUWVHP[e]	Three-phase reactive energy exported, combined Terminals UW (megavar hours, primary)
30, 32	3QWXVHP[e]	Three-phase reactive energy exported, combined Terminals WX (megavar hours, primary)
30, 32	3PSTWHN[e]	Three-phase active energy imported, combined Terminals ST (megawatt hours, primary)
30, 32	3PTUWHN[e]	Three-phase active energy imported, combined Terminals TU (megawatt hours, primary)
30, 32	3PUWWHN[e]	Three-phase active energy imported, combined Terminals UW (megawatt hours, primary)
30, 32	3PWXWHN[e]	Three-phase active energy imported, combined Terminals WX (megawatt hours, primary)
30, 32	3QSTVHN[e]	Three-phase reactive energy imported, combined Terminals ST (megavar hours, primary)
30, 32	3QTUVHN[e]	Three-phase reactive energy imported, combined Terminals TU (megavar hours, primary)
30, 32	3QUWVHN[e]	Three-phase reactive energy imported, combined Terminals UW (megavar hours, primary)
30, 32	3QWXVHN[e]	Three-phase reactive energy imported, combined Terminals WX (megavar hours, primary)
30, 32	3PSTWHT[e]	Total three-phase active energy, combined Terminals ST (megawatt hours, primary)
30, 32	3PTUWHT[e]	Total three-phase active energy, combined Terminals TU (megawatt hours, primary)
30, 32	3PUWWHT[e]	Total three-phase active energy, combined Terminals UW (megawatt hours, primary)
30, 32	3PWXWHT[e]	Total three-phase active energy, combined Terminals WX (megawatt hours, primary)
30, 32	3QSTVHT[e]	Total three-phase reactive energy, combined Terminals ST (megawatt hours, primary)
30, 32	3QTUVHT[e]	Total three-phase reactive energy, combined Terminals TU (megawatt hours, primary)
30, 32	3QUWVHT[e]	Total three-phase reactive energy, combined Terminals UW (megawatt hours, primary)
30, 32	3QWXVHT[e]	Total three-phase reactive energy, combined Terminals WX (megawatt hours, primary)
30, 32	FREQ[a]	Frequency used for frequency tracking (Hz)
30, 32	FREQP[a]	Frequency used for under- and overfrequency elements (Hz)
30, 32	DFDTP[a]	Rate-of-change of frequency (Hz)
30, 32	VDC	Station battery DC voltage (V)
30, 32	DCPO	Average positive to ground DC voltage (V)
30, 32	DCNE	Average negative to ground DC voltage (V)
30, 32	DCRI	AC ripple of DC voltage (V)
30, 32	DCMIN	Minimum DC voltage (V)

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 14 of 16)

Object	Label	Description
30, 32	DCMAX	Maximum DC voltage (V)
30, 32	PMV01–PMV64[g]	Protection SELOGIC math variable
30, 32	AMV001–AMV256[g]	Automation SELOGIC math variable
30, 32	PCN01CV–PCN32CV[g]	Protection SELOGIC counter current value
30, 32	ACN01CV–ACN32CV[g]	Automation SELOGIC counter current value
30, 32	ACTGRP[g]	Active group setting
30, 32	TODMS[g]	UTC time of day in milliseconds (0–86400000)
30, 32	THR[g]	UTC time, hour (0–23)
30, 32	TMIN[g]	UTC time, minute (0–59)
30, 32	TSEC[g]	UTC time, seconds (0–59)
30, 32	TMSEC[g]	UTC time, milliseconds (0–999)
30, 32	DDOW[g]	UTC date, day of the week (1–SU, ..., 7–SA)
30, 32	DDOM[g]	UTC date, day of the month (1–31)
30, 32	DDOY[g]	UTC date, day of the year (1–366)
30, 32	DMON[g]	UTC date, month (1–12)
30, 32	DYEAR[g]	UTC date, year (2000–2200)
30, 32	TLODMS[g]	Local time of day in milliseconds (0–86400000)
30, 32	TLHR[g]	Local time, hour (0–23)
30, 32	TLMIN[g]	Local time, minute (0–59)
30, 32	TLSEC[g]	Local time, seconds (0–59)
30, 32	TLMSEC[g]	Local time, milliseconds (0–999)
30, 32	TLNSEC[g]	Local time, nanoseconds (0–999999)
30, 32	DLDOW[g]	Local date, day of the week (1-SU,.., 7-SA)
30, 32	DLDOM[g]	Local date, day of the month (1–31)
30, 32	DLDOY[g]	Local date, day of the year (1–366)
30, 32	DLMON[g]	Local date, month (1–12)
30, 32	DLYEAR[g]	Local date, year (2000–2200)
30, 32	TUTC[g]	Offset from IRIG-B time to UTC time
30, 32	TQUAL[g]	Worst case IRIG-B clock time error
30, 32	RA001–RA256[g]	Remote analogs
30, 32	RLYTEMP[g]	Relay temperature (temperature of the box, degrees C)
30, 32	RAO01–RAO64[g]	Remote analog output
30, 32	BSBCWPA[g]	Breaker S contact wear for Pole A (%)
30, 32	BSBCWPB[g]	Breaker S contact wear for Pole B (%)
30, 32	BSBCWPC[g]	Breaker S contact wear for Pole C (%)
30, 32	BTBCWPA[g]	Breaker T contact wear for Pole A (%)
30, 32	BTBCWPB[g]	Breaker T contact wear for Pole B (%)
30, 32	BTBCWPC[g]	Breaker T contact wear for Pole C (%)
30, 32	BUBCWPA[g]	Breaker U contact wear for Pole A (%)
30, 32	BUBCWPB[g]	Breaker U contact wear for Pole B (%)

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 15 of 16)

Object	Label	Description
30, 32	BUBCWPC[g]	Breaker U contact wear for Pole C (%)
30, 32	BWBCWPA[g]	Breaker W contact wear for Pole A (%)
30, 32	BWBCWPB[g]	Breaker W contact wear for Pole B (%)
30, 32	BWBCWPC[g]	Breaker W contact wear for Pole C (%)
30, 32	BXBCWPA[g]	Breaker X contact wear for Pole A (%)
30, 32	BXBCWPB[g]	Breaker X contact wear for Pole B (%)
30, 32	BXBCWPC[g]	Breaker X contact wear for Pole C (%)
30, 32	25VPFM, 25VPFA[b]	25 Synchronism-check polarizing voltage magnitude, (volts secondary) and angle
30, 32	25VSSFM, 25VSSFA[b]	25 Synchronism-check synchronizing voltage magnitude for Breaker S (volts secondary) and angle
30, 32	25VSTFM, 25VSTFA[b]	25 Synchronism-check synchronizing voltage magnitude for Breaker T (volts secondary) and angle
30, 32	25VSUFM, 25VSUFA[b]	25 Synchronism-check synchronizing voltage magnitude for Breaker U (volts secondary) and angle
30, 32	25VSWFM, 25VSWFA[b]	25 Synchronism-check synchronizing voltage magnitude for Breaker W (volts secondary) and angle
30, 32	25VSXFM, 25VSXFA[b]	25 Synchronism-check synchronizing voltage magnitude for Breaker X (volts secondary) and angle
30, 32	25ANGS[a]	25 Synchronism-check angle difference for Breaker S
30, 32	25ANGT[a]	25 Synchronism-check angle difference for Breaker T
30, 32	25ANGU[a]	25 Synchronism-check angle difference for Breaker U
30, 32	25ANGW[a]	25 Synchronism-check angle difference for Breaker W
30, 32	25ANGX[a]	25 Synchronism-check angle difference for Breaker X
30, 32	25ANGCS[a]	25 Synchronism-check compensated angle difference for Breaker S
30, 32	25ANGCT[a]	25 Synchronism-check compensated angle difference for Breaker T
30, 32	25ANGCU[a]	25 Synchronism-check compensated angle difference for Breaker U
30, 32	25ANGCW[a]	25 Synchronism-check compensated angle difference for Breaker W
30, 32	25ANGCX[a]	25 Synchronism-check compensated angle difference for Breaker X
30, 32	25SLIPS[a]	25 Synchronism-check slip frequency for Breaker S (Hz)
30, 32	25SLIPT[a]	25 Synchronism-check slip frequency for Breaker T (Hz)
30, 32	25SLIPU[a]	25 Synchronism-check slip frequency for Breaker U (Hz)
30, 32	25SLIPW[a]	25 Synchronism-check slip frequency for Breaker W (Hz)
30, 32	25SLIPX[a]	25 Synchronism-check slip frequency for Breaker X (Hz)
Event Summary Analog Inputs[h, i]		
30, 32	FTYPE	Fault type
30, 32	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	FFREQ[j]	Fault frequency
30, 32	FGRP	Fault active settings group (1–6)
30, 32	FTIMEH	Fault time (local) in DNP format, high 16 bits
30, 32	FTIMEM	Fault time (local) in DNP format, middle 16 bits
30, 32	FTIMEL	Fault time (local) in DNP format, low 16 bits
30, 32	FTIMEUH	Fault time (UTC) in DNP format, high 16 bits
30, 32	FTIMEUM	Fault time (UTC) in DNP format, middle 16 bits

Table 10.14   SEL-487E Analog Input Reference Data Map (Sheet 16 of 16)

Object	Label	Description
30, 32	FTIMEUL	Fault time (UTC) in DNP format, low 16 bits
30, 32	FUNR	Number of unread fault summary reports

[a] Default scale factor is 100 and dead band ANADBM.

[b] Default voltage scaling DECPLV on magnitudes and scale factor of 100 on angles. Dead band ANADBV on magnitudes and ANADBM on angles.

[c] Default scale factor is DECPLV and dead band is ANADBV.

[d] Default current scaling DECPLA on magnitudes and scale factor of 100 on angles. Dead band ANADBA on magnitudes and ANADBM on angles.

[e] Default scale factor is DECPLM and dead band is ANADBM.

[f] Default scale factor is DECPLA and dead band is ANADBA.

[g] Default scale factor is 1 and dead band ANADBM.

[h] Unless otherwise indicated, the default scale factor for these points is 1. The default dead band is ANADBM. Per-point scaling and dead-band settings specified in a custom DNP map override these defaults.

[i] Event data shall be generated for all Event Summary Analog Inputs if any of them change beyond their dead band after scaling.

[j] Default scale factor is 100.

Figure 10.15 shows the Analog Output reference map. See *Analog Outputs on page 16.23 in the SEL-400 Series Relays Instruction Manual* for additional information.

Table 10.15   SEL-487E Analog Output Reference Data Map

Object	Label	Description
40, 41	ACTGRP	Active settings group (1–6)
40, 41	RA001–RA256	Remote analogs

Binary Outputs

Use the Trip and Close, Latch On/Off and Pulse On operations with Object 12 control relay output block command messages to operate the points shown in *Table 10.16*. Pulse operations provide a pulse with a duration of one protection processing interval. Cancel an operation in progress by issuing a NUL Trip/Close Code with a NUL Operation Type.

Table 10.16   SEL-487E Object 12 Control Point Operations (Sheet 1 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RB01–RB32	Pulse on Remote Bits RB01–RB32	Pulse on Remote Bits RB01–RB32	Set Remote Bits RB01–RB32	Clear Remote Bits RB01–RB32	Pulse on Remote Bits RB01–RB32	Clear Remote Bits RB01–RB32
RB*xx*: RB*yy*	Pulse RB*yy*	Pulse RB*xx*	Pulse RB*yy*	Pulse RB*xx*	Pulse RB*yy*	Pulse RB*xx*
OCS	Open Circuit Breaker S (pulse OCS)	Open Circuit Breaker S (pulse OCS)	Set OCS	Clear OCS	Open Circuit Breaker S (pulse OCS)	Clear OCS
CCS	Close Circuit Breaker S (pulse CCS)	Close Circuit Breaker S (pulse CCS)	Set CCS	Clear CCS	Close Circuit Breaker S (pulse CCS)	Clear CCS
OCT	Open Circuit Breaker T (pulse OCT)	Open Circuit Breaker T (pulse OCT)	Set OCT	Clear OCT	Open Circuit Breaker T (pulse OCT)	Clear OCT
CCT	Close Circuit Breaker T (pulse CCT)	Close Circuit Breaker T (pulse CCT)	Set CCT	Clear CCT	Close Circuit Breaker T (pulse CCT)	Clear CCT
OCU	Open Circuit Breaker U (pulse OCU)	Open Circuit Breaker U (pulse OCU)	Set OCU	Clear OCU	Open Circuit Breaker U (pulse OCU)	Clear OCU

Table 10.16 SEL-487E Object 12 Control Point Operations (Sheet 2 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
CCU	Close Circuit Breaker U (pulse CCU)	Close Circuit Breaker U (pulse CCU)	Set CCU	Clear CCU	Close Circuit Breaker U (pulse CCU)	Clear CCU
OCW	Open Circuit Breaker W (pulse OCW)	Open Circuit Breaker W (pulse OCW)	Set OCW	Clear OCW	Open Circuit Breaker W (pulse OCW)	Clear OCW
CCW	Close Circuit Breaker W (pulse CCW)	Close Circuit Breaker W (pulse CCW)	Set CCW	Clear CCW	Close Circuit Breaker W (pulse CCW)	Clear CCW
OCX	Open Circuit Breaker X (pulse OCX)	Open Circuit Breaker X (pulse OCX)	Set OCX	Clear OCX	Open Circuit Breaker X (pulse OCX)	Clear OCX
CCX	Close Circuit Breaker X (pulse CCX)	Close Circuit Breaker X (pulse CCX)	Set CCX	Clear CCX	Close Circuit Breaker X (pulse CCX)	Clear CCX
OCS: CCS	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit	Pulse CCS, Circuit Breaker S close bit	Pulse OCS, Circuit Breaker S open bit
OCT: CCT	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit	Pulse CCT, Circuit Breaker T close bit	Pulse OCT, Circuit Breaker T open bit
OCU: CCU	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit	Pulse CCU, Circuit Breaker U close bit	Pulse OCU, Circuit Breaker U open bit
OCW: CCW	Pulse CCW, Circuit Breaker W close bit	Pulse OCW, Circuit Breaker W open bit	Pulse CCW, Circuit Breaker W close bit	Pulse OCW, Circuit Breaker W open bit	Pulse CCW, Circuit Breaker W close bit	Pulse OCW, Circuit Breaker W open bit
OCX: CCX	Pulse CCX, Circuit Breaker X close bit	Pulse OCX, Circuit Breaker X open bit	Pulse CCX, Circuit Breaker X close bit	Pulse OCX, Circuit Breaker X open bit	Pulse CCX, Circuit Breaker X close bit	Pulse OCX, Circuit Breaker X open bit
89OC01–89OC20	Pulse 89OC01–89OC20, disconnect open bit	Pulse 89OC01–89OC20, disconnect open bit	Set 89OC01–89OC20, disconnect open bit	Clear 89OC01–89OC20, disconnect open bit	Pulse 89OC01–89OC20, disconnect open bit	Clear 89OC01–89OC20, disconnect open bit
89CC01–89CC20	Pulse 89CC01–89CC20, disconnect close bit	Pulse 89CC01–89CC20, disconnect close bit	Set 89CC01–89CC20, disconnect close bit	Clear 89CC01–89CC20, disconnect close bit	Pulse 89CC01–89CC20, disconnect close bit	Clear 89CC01–89CC20, disconnect close bit
89OCx: 89CCx	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit	Pulse 89CCx, disconnect close bit	Pulse 89OCx, disconnect open bit
RST_DEM	Reset demand meter data	Reset demand meter data	Reset demand meter data	No action	Reset demand meter data	No action
RST_PDM	Reset peak demand meter data	Reset peak demand meter data	Reset peak demand meter data	No action	Reset peak demand meter data	No action
RST_ENE	Reset energy accumulators	Reset energy accumulators	Reset energy accumulators	No action	Reset energy accumulators	No action
RST_BKS	Reset Breaker Monitor S (pulse RSS_BKS)	Reset Breaker Monitor S (pulse RSS_BKS)	Reset Breaker Monitor S (pulse RSS_BKS)	No action	Reset Breaker Monitor S (pulse RSS_BKS)	No action

Table 10.16   SEL-487E Object 12 Control Point Operations (Sheet 3 of 3)

Label	Close/Any	Trip/Any	NUL/Latch On	NUL/Latch Off	NUL/Pulse On	NUL/Pulse Off
RST_BKT	Reset Breaker Monitor T (pulse RSS_BKT)	Reset Breaker Monitor T (pulse RSS_BKT)	Reset Breaker Monitor T (pulse RSS_BKT)	No action	Reset Breaker Monitor T (pulse RSS_BKT)	No action
RST_BKU	Reset Breaker Monitor U (pulse RSS_BKU)	Reset Breaker Monitor U (pulse RSS_BKU)	Reset Breaker Monitor U (pulse RSS_BKU)	No action	Reset Breaker Monitor U (pulse RSS_BKU)	No action
RST_BKW	Reset Breaker Monitor W (pulse RSS_BKW)	Reset Breaker Monitor W (pulse RSS_BKW)	Reset Breaker Monitor W (pulse RSS_BKW)	No action	Reset Breaker Monitor W (pulse RSS_BKW)	No action
RST_BKX	Reset Breaker Monitor X (pulse RSS_BKX)	Reset Breaker Monitor X (pulse RSS_BKX)	Reset Breaker Monitor X (pulse RSS_BKX)	No action	Reset Breaker Monitor X (pulse RSS_BKX)	No action
RST_BAT	Reset battery monitoring (pulse RSS_BAT)	Reset battery monitoring (pulse RSS_BAT)	Reset battery monitoring (pulse RSS_BAT)	No action	Reset battery monitoring (pulse RSS_-BAT)	No action
RST_HAL	Reset alarm pulsing (pulse RSS_HAL)	Reset alarm pulsing (pulse RSS_HAL)	Reset alarm pulsing (pulse RSS_HAL)	No action	Reset alarm pulsing (pulse RSS_HAL)	No action
RSTTRGT	Reset front-panel targets (pulse RSTTRGT)	Reset front-panel targets (pulse RSTTRGT)	Reset front-panel targets	No action	Reset front-panel targets	No action
RSTDNPE	Reset DNP event summary	Reset DNP event summary	Reset DNP event summary	No action	Reset DNP event summary	No action
NXTEVE	Load oldest event summary (FIFO)	Load oldest event summary (FIFO)	Load oldest event summary (FIFO)	Load newest event summary (LIFO)	Load oldest event summary (FIFO)	Load newest event summary (LIFO)

Relay Fault Summary Data

When a relay event occurs (TRIP asserts, ER asserts, or TRI asserts), the data shall be made available to DNP.

In either mode, DNP3 events for all event summary analog inputs (see *Table 10.14*) will be generated if any of them change beyond their dead band value after scaling (usually whenever a new relay event occurs and is loaded into the event summary analog inputs). Events are detected approximately twice a second by the scanning process.

See *Table 10.17* for the components of the FTYPE analog input point. The bit asserted in the upper byte indicates the event cause (Trigger, Trip, ER element, etc.). The lower byte of FTYPE is always 0. If no bits are asserted in the upper byte, there is no valid fault summary loaded.

Table 10.17   Object 30, 32, FTYPE Upper Byte-Event Cause

Bit Position								Value	Event Cause
7	6	5	4	3	2	1	0		
								0	No fault summary loaded
							X	1	Trigger command
					X			4	Trip element
				X				8	Event report element
			X					16	Breaker failure trip (87)
		X						32	Differential trip (60)

Default Data Map

Table 10.18–Table 10.22 shows the SEL-487E default data maps by DNP3 object or point type. The default data maps are automatically generated subsets of the reference map. All data maps are initialized to these default values. If the default maps do not fit your particular application, you can use the custom DNP mapping commands **SET D** *n* and **SHOW D** *n*, where *n* is the map number, to edit or create the map you require.

Table 10.18   SEL-487E DNP3 Default Binary Input Data Map (Sheet 1 of 3)

Object	Default Index	Label	Description
01, 02	0	RLYDIS	Relay disabled
01, 02	1	TRIPLED	Trip LED
01, 02	2	STFAIL	Relay diagnostic failure
01, 02	3	STWARN	Relay diagnostic warning
01, 02	4	STSET	Settings have changed or relay restarted
01, 02	5	UNRDEV	New relay event available
01, 02	6	52CLS	Breaker closed, Terminal S
01, 02	7	52ALS	Breaker alarm, Terminal S
01, 02	8	52CLT	Breaker closed, Terminal T
01, 02	9	52ALT	Breaker alarm, Terminal T
01, 02	10	52CLU	Breaker closed, Terminal U
01, 02	11	52ALU	Breaker alarm, Terminal U
01, 02	12	52CLW	Breaker closed, Terminal W
01, 02	13	52ALW	Breaker alarm, Terminal W
01, 02	14	52CLX	Breaker closed, Terminal X
01, 02	15	52ALX	Breaker alarm, Terminal X
01, 02	16	89CL01	Disconnect 1 closed
01, 02	17	89AL01	Disconnect 1 alarm
01, 02	18	89CL02	Disconnect 2 closed
01, 02	19	89AL02	Disconnect 2 alarm
01, 02	20	89CL03	Disconnect 3 closed
01, 02	21	89AL03	Disconnect 3 alarm
01, 02	22	89CL04	Disconnect 4 closed
01, 02	23	89AL04	Disconnect 4 alarm

Table 10.18 SEL-487E DNP3 Default Binary Input Data Map (Sheet 2 of 3)

Object	Default Index	Label	Description
01, 02	24	89CL05	Disconnect 5 closed
01, 02	25	89AL05	Disconnect 5 alarm
01, 02	26	89CL06	Disconnect 6 closed
01, 02	27	89AL06	Disconnect 6 alarm
01, 02	28	89CL07	Disconnect 7 closed
01, 02	29	89AL07	Disconnect 7 alarm
01, 02	30	89CL08	Disconnect 8 closed
01, 02	31	89AL08	Disconnect 8 alarm
01, 02	32	89CL09	Disconnect 9 closed
01, 02	33	89AL09	Disconnect 9 alarm
01, 02	34	89CL10	Disconnect 10 closed
01, 02	35	89AL10	Disconnect 10 alarm
01, 02	36	TLED_1	Target LED 1 on relay front panel
01, 02	37	TLED_2	Target LED 2 on relay front panel
01, 02	38	TLED_3	Target LED 3 on relay front panel
01, 02	39	TLED_4	Target LED 4 on relay front panel
01, 02	40	TLED_5	Target LED 5 on relay front panel
01, 02	41	TLED_6	Target LED 6 on relay front panel
01, 02	42	TLED_7	Target LED 7 on relay front panel
01, 02	43	TLED_8	Target LED 8 on relay front panel
01, 02	44	TLED_9	Target LED 9 on relay front panel
01, 02	45	TLED_10	Target LED 10 on relay front panel
01, 02	46	TLED_11	Target LED 11 on relay front panel
01, 02	47	TLED_12	Target LED 12 on relay front panel
01, 02	48	TLED_13	Target LED 13 on relay front panel
01, 02	49	TLED_14	Target LED 14 on relay front panel
01, 02	50	TLED_15	Target LED 15 on relay front panel
01, 02	51	TLED_16	Target LED 16 on relay front panel
01, 02	52	TLED_17	Target LED 17 on relay front panel
01, 02	53	TLED_18	Target LED 18 on relay front panel
01, 02	54	TLED_19	Target LED 19 on relay front panel
01, 02	55	TLED_20	Target LED 20 on relay front panel
01, 02	56	TLED_21	Target LED 21 on relay front panel
01, 02	57	TLED_22	Target LED 22 on relay front panel
01, 02	58	TLED_23	Target LED 23 on relay front panel
01, 02	59	TLED_24	Target LED 24 on relay front panel
01, 02	60	VALARMV	Voltage alarm Terminal V
01, 02	61	LOPV	Loss-of-potential Terminal V
01, 02	62	VALARMZ	Voltage alarm Terminal Z
01, 02	63	LOPZ	Loss-of-potential Terminal Z
01, 02	64	IN101	Main Board Input 1 asserted

Table 10.18   SEL-487E DNP3 Default Binary Input Data Map (Sheet 3 of 3)

Object	Default Index	Label	Description
01, 02	65	IN102	Main Board Input 2 asserted
01, 02	66	IN103	Main Board Input 3 asserted
01, 02	67	IN104	Main Board Input 4 asserted
01, 02	68	IN105	Main Board Input 5 asserted
01, 02	69	IN106	Main Board Input 6 asserted
01, 02	70	IN107	Main Board Input 7 asserted
01, 02	71	OUT101	Main Board Output 1 asserted
01, 02	72	OUT102	Main Board Output 2 asserted
01, 02	73	OUT103	Main Board Output 3 asserted
01, 02	74	OUT104	Main Board Output 4 asserted
01, 02	75	OUT105	Main Board Output 5 asserted
01, 02	76	OUT106	Main Board Output 6 asserted
01, 02	77	OUT107	Main Board Output 7 asserted
01, 02	78	OUT108	Main Board Output 8 asserted

Table 10.19   SEL-487E DNP3 Default Binary Output Data Map (Sheet 1 of 2)

Object	Default Index	Label	Description
10, 12	0–31	RB01–RB32	Remote Bits 1–32
10, 12	32	OCS	Breaker Open command, Terminal S
10, 12	33	CCS	Breaker Close command, Terminal S
10, 12	34	OCT	Breaker Open command, Terminal T
10, 12	35	CCT	Breaker Close command, Terminal T
10, 12	36	OCU	Breaker Open command, Terminal U
10, 12	37	CCU	Breaker Close command, Terminal U
10, 12	38	OCW	Breaker Open command, Terminal W
10, 12	39	CCW	Breaker Close command, Terminal W
10, 12	40	OCX	Breaker Open command, Terminal X
10, 12	41	CCX	Breaker Close command, Terminal X
10, 12	42	89OC01	Open Disconnect Control 1
10, 12	43	89CC01	Close Disconnect Control 1
10, 12	44	89OC02	Open Disconnect Control 2
10, 12	45	89CC02	Close Disconnect Control 2
10, 12	46	89OC03	Open Disconnect Control 3
10, 12	47	89CC03	Close Disconnect Control 3
10, 12	48	89OC04	Open Disconnect Control 4
10, 12	49	89CC04	Close Disconnect Control 4
10, 12	50	89OC05	Open Disconnect Control 5
10, 12	51	89CC05	Close Disconnect Control 5
10, 12	52	89OC06	Open Disconnect Control 6
10, 12	53	89CC06	Close Disconnect Control 6
10, 12	54	89OC07	Open Disconnect Control 7

Table 10.19 SEL-487E DNP3 Default Binary Output Data Map (Sheet 2 of 2)

Object	Default Index	Label	Description
10, 12	55	89CC07	Close Disconnect Control 7
10, 12	56	89OC08	Open Disconnect Control 8
10, 12	57	89CC08	Close Disconnect Control 8
10, 12	58	89OC09	Open Disconnect Control 9
10, 12	59	89CC09	Close Disconnect Control 9
10, 12	60	89OC10	Open Disconnect Control 10
10, 12	61	89CC10	Close Disconnect Control 10
10, 12	62	RSTTRGT	Reset front-panel targets
10, 12	63	RSTDNPE	Reset DNP fault summary data

Table 10.20 SEL-487E DNP3 Default Binary Counter Data Map

Object	Default Index	Label	Description
20, 22	0	BKRSOP	Number of Breaker S operations
20, 22	1	BKRTOP	Number of Breaker T operations
20, 22	2	BKRUOP	Number of Breaker U operations
20, 22	3	BKRWOP	Number of Breaker W operations
20, 22	4	BKRXOP	Number of Breaker X operations

Table 10.21 SEL-487E DNP3 Default Analog Input Map (Sheet 1 of 3)

Object	Default Index	Label	Description
30, 32	0	IASFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal S
30, 32	1	IASFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal S
30, 32	2	IBSFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal S
30, 32	3	IBSFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal S
30, 32	4	ICSFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal S
30, 32	5	ICSFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal S
30, 32	6	IATFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal T
30, 32	7	IATFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal T
30, 32	8	IBTFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal T
30, 32	9	IBTFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal T
30, 32	10	ICTFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal T
30, 32	11	ICTFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal T
30, 32	12	IAUFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal U
30, 32	13	IAUFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal U
30, 32	14	IBUFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal U
30, 32	15	IBUFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal U
30, 32	16	ICUFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal U
30, 32	17	ICUFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal U
30, 32	18	IAWFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal W
30, 32	19	IAWFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal W
30, 32	20	IBWFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal W

Table 10.21 SEL-487E DNP3 Default Analog Input Map (Sheet 2 of 3)

Object	Default Index	Label	Description
30, 32	21	IBWFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal W
30, 32	22	ICWFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal W
30, 32	23	ICWFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal W
30, 32	24	IAXFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal X
30, 32	25	IAXFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal X
30, 32	26	IBXFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal X
30, 32	27	IBXFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal X
30, 32	28	ICXFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal X
30, 32	29	ICXFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal X
30, 32	30	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
30, 32	31	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
30, 32	32	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
30, 32	33	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
30, 32	34	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
30, 32	35	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
30, 32	36	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
30, 32	37	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
30, 32	38	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
30, 32	39	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
30, 32	40	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
30, 32	41	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
30, 32	42	PASFC	1-cycle average phase fundamental active power, A-Phase, Terminal S
30, 32	43	PBSFC	1-cycle average phase fundamental active power, B-Phase, Terminal S
30, 32	44	PCSFC	1-cycle average phase fundamental active power, C-Phase, Terminal S
30, 32	45	PATFC	1-cycle average phase fundamental active power, A-Phase, Terminal T
30, 32	46	PBTFC	1-cycle average phase fundamental active power, B-Phase, Terminal T
30, 32	47	PCTFC	1-cycle average phase fundamental active power, C-Phase, Terminal T
30, 32	48	PAUFC	1-cycle average phase fundamental active power, A-Phase, Terminal U
30, 32	49	PBUFC	1-cycle average phase fundamental active power, B-Phase, Terminal U
30, 32	50	PCUFC	1-cycle average phase fundamental active power, C-Phase, Terminal U
30, 32	51	PAWFC	1-cycle average phase fundamental active power, A-Phase, Terminal W
30, 32	52	PBWFC	1-cycle average phase fundamental active power, B-Phase, Terminal W
30, 32	53	PCWFC	1-cycle average phase fundamental active power, C-Phase, Terminal W
30, 32	54	PAXFC	1-cycle average phase fundamental active power, A-Phase, Terminal X
30, 32	55	PBXFC	1-cycle average phase fundamental active power, B-Phase, Terminal X
30, 32	56	PCXFC	1-cycle average phase fundamental active power, C-Phase, Terminal X
30, 32	57	QASFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal S
30, 32	58	QBSFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal S
30, 32	59	QCSFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal S
30, 32	60	QATFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal T
30, 32	61	QBTFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal T

Table 10.21   SEL-487E DNP3 Default Analog Input Map (Sheet 3 of 3)

Object	Default Index	Label	Description
30, 32	62	QCTFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal T
30, 32	63	QAUFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal U
30, 32	64	QBUFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal U
30, 32	65	QCUFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal U
30, 32	66	QAWFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal W
30, 32	67	QBWFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal W
30, 32	68	QCWFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal W
30, 32	69	QAXFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal X
30, 32	70	QBXFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal X
30, 32	71	QCXFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal X
30, 32	72	ACTGRP	Active settings group
30, 32	73	RLYTEMP	Relay temperature (°C temperature of the box)
30, 32	74	FREQ	Tracking frequency
30, 32	75	VDC	Station battery DC voltage
30, 32	76	FTYPE	Fault type
30, 32	77	FTAR1	Fault targets (upper byte is 1st target row, lower byte is 2nd target row)
30, 32	78	FTAR2	Fault targets (upper byte is 3rd target row, lower byte is 0)
30, 32	79	FFREQ	Fault frequency
30, 32	80	FGRP	Fault active settings group (1–6)
30, 32	81	FTIMEUH	Fault time (UTC) in DNP format, high 16 bits
30, 32	82	FTIMEUM	Fault time (UTC) in DNP format, middle 16 bits
30, 32	83	FTIMEUL	Fault time (UTC) in DNP format, low 16 bits
30, 32	84	FUNR	Number of unread faults

Table 10.22   SEL-487E DNP3 Default Analog Output Data Map

Object	Default Index	Label	Description
40, 41	0	ACTGRP	Active settings group

IEC 61850 Communication

General IEC 61850 operation is described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of IEC 61850 that are specific to the SEL-487E.

Logical Nodes

Table 10.23 and *Table 10.24* show the logical nodes (LNs) supported in the SEL-487E and the Relay Word bits or Measured Values mapped to those LNs. Additionally, the relay supports the CON and ANN Logical Device logical nodes as described in *Section 17: IEC 61850 Communication in the SEL-400 Series Relays Instruction Manual*.

Table 10.23 shows the LNs associated with protection elements, defined as Logical Device PRO.

Table 10.23 Logical Device: PRO (Protection) (Sheet 1 of 15)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = CO			
DC1CSWI6	Pos.Oper.ctlVal	89CC01:89OC01[a]	ASCII Close/Open Disconnect 1 command
DC2CSWI7	Pos.Oper.ctlVal	89CC02:89OC02[a]	ASCII Close/Open Disconnect 2 command
DC3CSWI8	Pos.Oper.ctlVal	89CC03:89OC03[a]	ASCII Close/Open Disconnect 3 command
DC4CSWI9	Pos.Oper.ctlVal	89CC04:89OC04[a]	ASCII Close/Open Disconnect 4 command
DC5CSWI10	Pos.Oper.ctlVal	89CC05:89OC05[a]	ASCII Close/Open Disconnect 5 command
DC6CSWI11	Pos.Oper.ctlVal	89CC06:89OC06[a]	ASCII Close/Open Disconnect 6 command
DC7CSWI12	Pos.Oper.ctlVal	89CC07:89OC07[a]	ASCII Close/Open Disconnect 7 command
DC8CSWI13	Pos.Oper.ctlVal	89CC08:89OC08[a]	ASCII Close/Open Disconnect 8 command
DC9CSWI14	Pos.Oper.ctlVal	89CC09:89OC09[a]	ASCII Close/Open Disconnect 9 command
DC10CSWI15	Pos.Oper.ctlVal	89CC10:89OC10[a]	ASCII Close/Open Disconnect 10 command
DC11CSWI16	Pos.Oper.ctlVal	89CC11:89OC11[a]	ASCII Close/Open Disconnect 11 command
DC12CSWI17	Pos.Oper.ctlVal	89CC12:89OC12[a]	ASCII Close/Open Disconnect 12 command
DC13CSWI18	Pos.Oper.ctlVal	89CC13:89OC13[a]	ASCII Close/Open Disconnect 13 command
DC14CSWI19	Pos.Oper.ctlVal	89CC14:89OC14[a]	ASCII Close/Open Disconnect 14 command
DC15CSWI20	Pos.Oper.ctlVal	89CC15:89OC15[a]	ASCII Close/Open Disconnect 15 command
DC16CSWI21	Pos.Oper.ctlVal	89CC16:89OC16[a]	ASCII Close/Open Disconnect 16 command
DC17CSWI22	Pos.Oper.ctlVal	89CC17:89OC17[a]	ASCII Close/Open Disconnect 17 command
DC18CSWI23	Pos.Oper.ctlVal	89CC18:89OC18[a]	ASCII Close/Open Disconnect 18 command
DC19CSWI24	Pos.Oper.ctlVal	89CC19:89OC19[a]	ASCII Close/Open Disconnect 19 command
DC20CSWI25	Pos.Oper.ctlVal	89CC20:89OC20[a]	ASCII Close/Open Disconnect 20 command
SBKRCSWI1	Pos.Oper.ctlVal	CCS:OCS[a]	Circuit breaker close/open command, Terminal S
TBKRCSWI2	Pos.Oper.ctlVal	CCT:OCT[a]	Circuit breaker close/open command, Terminal T
UBKRCSWI3	Pos.Oper.ctlVal	CCU:OCU[a]	Circuit breaker close/open command, Terminal U
WBKRCSWI4	Pos.Oper.ctlVal	CCW:OCW[a]	Circuit breaker close/open command, Terminal W
XBKRCSWI5	Pos.Oper.ctlVal	CCX:OCX[a]	Circuit breaker close/open command, Terminal X
Functional Constraint = ST			
LLN0	Mod.stVal	I60MOD[b]	IEC 61850 mode/behavior status
LLN0	Health.stVal	EN?3:1[c]	Relay enabled
BFRSRBRF1	Str.general	BFIS	Circuit Breaker S breaker failure initiate SELOGIC control equation
BFRSRBRF1	OpEx.general	FBFS	Circuit Breaker S failure
BFRSRBRF1	OpIn.general	RTS	Circuit Breaker S retrip
BFRTRBRF2	Str.general	BFIT	Circuit Breaker T breaker failure initiate SELOGIC control equation
BFRTRBRF2	OpEx.general	FBFT	Circuit Breaker T failure
BFRTRBRF2	OpIn.general	RTT	Circuit Breaker T retrip
BFRURBRF3	Str.general	BFIU	Circuit Breaker U breaker failure initiate SELOGIC control equation
BFRURBRF3	OpEx.general	FBFU	Circuit Breaker U failure

Table 10.23 Logical Device: PRO (Protection) (Sheet 2 of 15)

Logical Node	Attribute	Data Source	Comment
BFRURBRF3	OpIn.general	RTU	Circuit Breaker U retrip
BFRWRBRF4	Str.general	BFIW	Circuit Breaker W breaker failure initiate SELOGIC control equation
BFRWRBRF4	OpEx.general	FBFW	Circuit Breaker W failure
BFRWRBRF4	OpIn.general	RTW	Circuit Breaker W retrip
BFRXRBRF5	Str.general	BFIX	Circuit Breaker X breaker failure initiate SELOGIC control equation
BFRXRBRF5	OpEx.general	FBFX	Circuit Breaker X failure
BFRXRBRF5	OpIn.general	RTX	Circuit Breaker X retrip
BSSASCBR1	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S
BSSASCBR1	ColOpn.stVal	OCS	Breaker Open command, Terminal S
BSSASCBR1	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSASCBR1	OpTmAlm.stVal	BSESOAL	Slow electrical operate alarm, Breaker S
BSSBSCBR2	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S
BSSBSCBR2	ColOpn.stVal	OCS	Breaker Open command, Terminal S
BSSBSCBR2	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSBSCBR2	OpTmAlm.stVal	BSESOAL	Slow electrical operate alarm, Breaker S
BSSCSCBR3	AbrAlm.stVal	BSBCWAL	Breaker contact wear alarm, Breaker S
BSSCSCBR3	ColOpn.stVal	OCS	Breaker Open command, Terminal S
BSSCSCBR3	MechTmAlm.stVal	BSMSOAL	Mechanical slow operation alarm, Breaker S
BSSCSCBR3	OpTmAlm.stVal	BSESOAL	Slow electrical operate alarm, Breaker S
BSTASCBR4	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTASCBR4	ColOpn.stVal	OCT	Breaker Open command, Terminal T
BSTASCBR4	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTASCBR4	OpTmAlm.stVal	BTESOAL	Slow electrical operate alarm, Breaker T
BSTBSCBR5	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTBSCBR5	ColOpn.stVal	OCT	Breaker Open command, Terminal T
BSTBSCBR5	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTBSCBR5	OpTmAlm.stVal	BTESOAL	Slow electrical operate alarm, Breaker T
BSTCSCBR6	AbrAlm.stVal	BTBCWAL	Breaker contact wear alarm, Breaker T
BSTCSCBR6	ColOpn.stVal	OCT	Breaker Open command, Terminal T
BSTCSCBR6	MechTmAlm.stVal	BTMSOAL	Mechanical slow operation alarm, Breaker T
BSTCSCBR6	OpTmAlm.stVal	BTESOAL	Slow electrical operate alarm, Breaker T
BSUASCBR7	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U
BSUASCBR7	ColOpn.stVal	OCU	Breaker Open command, Terminal U
BSUASCBR7	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUASCBR7	OpTmAlm.stVal	BUESOAL	Slow electrical operate alarm, Breaker U
BSUBSCBR8	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U
BSUBSCBR8	ColOpn.stVal	OCU	Breaker Open command, Terminal U
BSUBSCBR8	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUBSCBR8	OpTmAlm.stVal	BUESOAL	Slow electrical operate alarm, Breaker U
BSUCSCBR9	AbrAlm.stVal	BUBCWAL	Breaker contact wear alarm, Breaker U

Table 10.23   Logical Device: PRO (Protection) (Sheet 3 of 15)

Logical Node	Attribute	Data Source	Comment
BSUCSCBR9	ColOpn.stVal	OCU	Breaker Open command, Terminal U
BSUCSCBR9	MechTmAlm.stVal	BUMSOAL	Mechanical slow operation alarm, Breaker U
BSUCSCBR9	OpTmAlm.stVal	BUESOAL	Slow electrical operate alarm, Breaker U
BSWASCBR10	AbrAlm.stVal	BWBCWAL	Breaker contact wear alarm, Breaker W
BSWASCBR10	ColOpn.stVal	OCW	Breaker Open command, Terminal W
BSWASCBR10	MechTmAlm.stVal	BWMSOAL	Mechanical slow operation alarm, Breaker W
BSWASCBR10	OpTmAlm.stVal	BWESOAL	Slow electrical operate alarm, Breaker W
BSWBSCBR11	AbrAlm.stVal	BWBCWAL	Breaker contact wear alarm, Breaker W
BSWBSCBR11	ColOpn.stVal	OCW	Breaker Open command, Terminal W
BSWBSCBR11	MechTmAlm.stVal	BWMSOAL	Mechanical slow operation alarm, Breaker W
BSWBSCBR11	OpTmAlm.stVal	BWESOAL	Slow electrical operate alarm, Breaker W
BSWCSCBR12	AbrAlm.stVal	BWBCWAL	Breaker contact wear alarm, Breaker W
BSWCSCBR12	ColOpn.stVal	OCW	Breaker Open command, Terminal W
BSWCSCBR12	MechTmAlm.stVal	BWMSOAL	Mechanical slow operation alarm, Breaker W
BSWCSCBR12	OpTmAlm.stVal	BWESOAL	Slow electrical operate alarm, Breaker W
BSXASCBR13	AbrAlm.stVal	BXBCWAL	Breaker contact wear alarm, Breaker X
BSXASCBR13	ColOpn.stVal	OCX	Breaker Open command, Terminal X
BSXASCBR13	MechTmAlm.stVal	BXMSOAL	Mechanical slow operation alarm, Breaker X
BSXASCBR13	OpTmAlm.stVal	BXESOAL	Slow electrical operate alarm, Breaker X
BSXBSCBR14	AbrAlm.stVal	BXBCWAL	Breaker contact wear alarm, Breaker X
BSXBSCBR14	ColOpn.stVal	OCX	Breaker Open command, Terminal X
BSXBSCBR14	MechTmAlm.stVal	BXMSOAL	Mechanical slow operation alarm, Breaker X
BSXBSCBR14	OpTmAlm.stVal	BXESOAL	Slow electrical operate alarm, Breaker X
BSXCSCBR15	AbrAlm.stVal	BXBCWAL	Breaker contact wear alarm, Breaker X
BSXCSCBR15	ColOpn.stVal	OCX	Breaker Open command, Terminal X
BSXCSCBR15	MechTmAlm.stVal	BXMSOAL	Mechanical slow operation alarm, Breaker X
BSXCSCBR15	OpTmAlm.stVal	BXESOAL	Slow electrical operate alarm, Breaker X
D1PVPH1	Op.general	24D1T	Volts/Hertz Level 1 timed out
D1PVPH1	Str.general	24D1	Volts/Hertz Element Level 1 asserted
D2PVPH2	Op.general	24D2T	Volts/Hertz Level 2 timed out
D2PVPH2	Str.general	24D1	Volts/Hertz Element Level 1 asserted
D87QPDIF1	Str.general	87PQ	Minimum pickup and slope conditions satisfied for the negative-sequence differential element
D87QPDIF1	Op.general	87Q	Negative-sequence differential element operated
D87RAPDIF1	Op.general	87RA	Restrained Differential Element Operated A-Phase
D87RAPDIF1	Str.general	P87A	Differential Element Zone A picked up
D87RBPDIF2	Op.general	87RB	Restrained Differential Element Operated B-Phase
D87RBPDIF2	Str.general	P87B	Differential Element Zone B picked up
D87RCPDIF3	Op.general	87RC	Restrained Differential Element Operated C-Phase
D87RCPDIF3	Str.general	P87C	Differential Element Zone C picked up
D87RPDIF1	Op.general	87R	Restrained differential element operated

Table 10.23   Logical Device: PRO (Protection) (Sheet 4 of 15)

Logical Node	Attribute	Data Source	Comment
D87TPDIF1	Op.general	87T	Transformer differential element operated (87R OR 87Q or 87U)
D87UPDIF1	Op.general	87U	Unrestrained element operation
D87UPDIF1	Op.phsA	87UA	Unrestrained Element Asserted Zone A
D87UPDIF1	Op.phsB	87UB	Unrestrained Element Asserted Zone B
D87UPDIF1	Op.phsC	87UC	Unrestrained Element Asserted Zone C
DC1CSWI6	OpCls.general	89CL01	Disconnect 1 closed
DC1CSWI6	OpOpn.general	89OPN01	Disconnect 1 open
DC1CSWI6	Pos.stVal	89CL01|89OPN01?0:1:2:3[d]	Disconnect/Isolator 01 status
DC2CSWI7	OpCls.general	89CL02	Disconnect 2 closed
DC2CSWI7	OpOpn.general	89OPN02	Disconnect 2 open
DC2CSWI7	Pos.stVal	89CL02|89OPN02?0:1:2:3[d]	Disconnect/Isolator 02 status
DC3CSWI8	OpCls.general	89CL03	Disconnect 3 closed
DC3CSWI8	OpOpn.general	89OPN03	Disconnect 3 open
DC3CSWI8	Pos.stVal	89CL03|89OPN03?0:1:2:3[d]	Disconnect/Isolator 03 status
DC4CSWI9	OpCls.general	89CL04	Disconnect 4 closed
DC4CSWI9	OpOpn.general	89OPN04	Disconnect 4 open
DC4CSWI9	Pos.stVal	89CL04|89OPN04?0:1:2:3[d]	Disconnect/Isolator 04 status
DC5CSWI10	OpCls.general	89CL05	Disconnect 5 closed
DC5CSWI10	OpOpn.general	89OPN05	Disconnect 5 open
DC5CSWI10	Pos.stVal	89CL05|89OPN05?0:1:2:3[d]	Disconnect/Isolator 05 status
DC6CSWI11	OpCls.general	89CL06	Disconnect 6 closed
DC6CSWI11	OpOpn.general	89OPN06	Disconnect 6 open
DC6CSWI11	Pos.stVal	89CL06|89OPN06?0:1:2:3[d]	Disconnect/Isolator 06 status
DC7CSWI12	OpCls.general	89CL07	Disconnect 7 closed
DC7CSWI12	OpOpn.general	89OPN07	Disconnect 7 open
DC7CSWI12	Pos.stVal	89CL07|89OPN07?0:1:2:3[d]	Disconnect/Isolator 07 status
DC8CSWI13	OpCls.general	89CL08	Disconnect 8 closed
DC8CSWI13	OpOpn.general	89OPN08	Disconnect 8 open
DC8CSWI13	Pos.stVal	89CL08|89OPN08?0:1:2:3[d]	Disconnect/Isolator 08 status
DC9CSWI14	OpCls.general	89CL09	Disconnect 9 closed
DC9CSWI14	OpOpn.general	89OPN09	Disconnect 9 open
DC9CSWI14	Pos.stVal	89CL09|89OPN09?0:1:2:3[d]	Disconnect/Isolator 09 status
DC10CSWI15	OpCls.general	89CL10	Disconnect 10 closed
DC10CSWI15	OpOpn.general	89OPN10	Disconnect 10 open
DC10CSWI15	Pos.stVal	89CL10|89OPN10?0:1:2:3[d]	Disconnect/Isolator 10 status
DC11CSWI16	OpCls.general	89CL11	Disconnect 11 closed
DC11CSWI16	OpOpn.general	89OPN11	Disconnect 11 open
DC11CSWI16	Pos.stVal	89CL11|89OPN11?0:1:2:3[d]	Disconnect/Isolator 11 status
DC12CSWI17	OpCls.general	89CL12	Disconnect 12 closed
DC12CSWI17	OpOpn.general	89OPN12	Disconnect 12 open
DC12CSWI17	Pos.stVal	89CL12|89OPN12?0:1:2:3[d]	Disconnect/Isolator 12 status

Table 10.23 Logical Device: PRO (Protection) (Sheet 5 of 15)

Logical Node	Attribute	Data Source	Comment
DC13CSWI18	OpCls.general	89CL13	Disconnect 13 closed
DC13CSWI18	OpOpn.general	89OPN13	Disconnect 13 open
DC13CSWI18	Pos.stVal	89CL13|89OPN13?0:1:2:3[d]	Disconnect/Isolator 13 status
DC14CSWI19	OpCls.general	89CL14	Disconnect 14 closed
DC14CSWI19	OpOpn.general	89OPN14	Disconnect 14 open
DC14CSWI19	Pos.stVal	89CL14|89OPN14?0:1:2:3[d]	Disconnect/Isolator 14 status
DC15CSWI20	OpCls.general	89CL15	Disconnect 15 closed
DC15CSWI20	OpOpn.general	89OPN15	Disconnect 15 open
DC15CSWI20	Pos.stVal	89CL15|89OPN15?0:1:2:3[d]	Disconnect/Isolator 15 status
DC16CSWI21	OpCls.general	89CL16	Disconnect 16 closed
DC16CSWI21	OpOpn.general	89OPN16	Disconnect 16 open
DC16CSWI21	Pos.stVal	89CL16|89OPN16?0:1:2:3[d]	Disconnect/Isolator 16 status
DC17CSWI22	OpCls.general	89CL17	Disconnect 17 closed
DC17CSWI22	OpOpn.general	89OPN17	Disconnect 17 open
DC17CSWI22	Pos.stVal	89CL17|89OPN17?0:1:2:3[d]	Disconnect/Isolator 17 status
DC18CSWI23	OpCls.general	89CL18	Disconnect 18 closed
DC18CSWI23	OpOpn.general	89OPN18	Disconnect 18 open
DC18CSWI23	Pos.stVal	89CL18|89OPN18?0:1:2:3[d]	Disconnect/Isolator 18 status
DC19CSWI24	OpCls.general	89CL19	Disconnect 19 closed
DC19CSWI24	OpOpn.general	89OPN19	Disconnect 19 open
DC19CSWI24	Pos.stVal	89CL19|89OPN19?0:1:2:3[d]	Disconnect/Isolator 19 status
DC20CSWI25	OpCls.general	89CL20	Disconnect 20 closed
DC20CSWI25	OpOpn.general	89OPN20	Disconnect 20 open
DC20CSWI25	Pos.stVal	89CL20|89OPN20?0:1:2:3[d]	Disconnect/Isolator 20 status
FLTRDRE1	FltNum.stVal	FLRNUM	Event number
FLTRDRE1	RcdMade.stVal	FLREP	Event report present
HBPHAR2	Str.general	CSV02	87AHB OR 87BHB OR 87CHB
HBPHAR2	Str.phsA	87AHB	Harmonic-blocking differential element picked up A
HBPHAR2	Str.phsB	87BHB	Harmonic-blocking differential element picked up B
HBPHAR2	Str.phsC	87CHB	Harmonic-blocking differential element picked up C
HRPHAR1	Str.general	CSV01	87AHR OR 87BHR OR 87CHR
HRPHAR1	Str.phsA	87AHR	Harmonic-restraint differential element picked up A
HRPHAR1	Str.phsB	87BHR	Harmonic-restraint differential element picked up B
HRPHAR1	Str.phsC	87CHR	Harmonic-restraint differential element picked up C
IT1PTOC46	Op.general	51T01	Inverse-Time Element 01 timed out
IT1PTOC46	Str.general	51S01	Inverse-Time Element 01 picked up
IT2PTOC47	Op.general	51T02	Inverse-Time Element 02 timed out
IT2PTOC47	Str.general	51S02	Inverse-Time Element 02 picked up
IT3PTOC48	Op.general	51T03	Inverse-Time Element 03 timed out
IT3PTOC48	Str.general	51S03	Inverse-Time Element 03 picked up
IT4PTOC49	Op.general	51T04	Inverse-Time Element 04 timed out

Table 10.23   Logical Device: PRO (Protection) (Sheet 6 of 15)

Logical Node	Attribute	Data Source	Comment
IT4PTOC49	Str.general	51S04	Inverse-Time Element 04 picked up
IT5PTOC50	Op.general	51T05	Inverse-Time Element 05 timed out
IT5PTOC50	Str.general	51S05	Inverse-Time Element 05 picked up
IT6PTOC51	Op.general	51T06	Inverse-Time Element 06 timed out
IT6PTOC51	Str.general	51S06	Inverse-Time Element 06 picked up
IT7PTOC52	Op.general	51T07	Inverse-Time Element 07 timed out
IT7PTOC52	Str.general	51S07	Inverse-Time Element 07 picked up
IT8PTOC53	Op.general	51T08	Inverse-Time Element 08 timed out
IT8PTOC53	Str.general	51S08	Inverse-Time Element 08 picked up
IT9PTOC54	Op.general	51T09	Inverse-Time Element 09 timed out
IT9PTOC54	Str.general	51S09	Inverse-Time Element 09 picked up
IT10PTOC55	Op.general	51T10	Inverse-Time Element 10 timed out
IT10PTOC55	Str.general	51S10	Inverse-Time Element 10 picked up
LOPVPTUV1	Str.general	LOPV	Loss-of-potential Terminal V
LOPVPTUV1	Op.general	LOPV	Loss-of-potential Terminal V
LOPZPTUV2	Str.general	LOPZ	Loss-of-potential Terminal Z
LOPZPTUV2	Op.general	LOPZ	Loss-of-potential Terminal Z
O1P1PTOV1	Op.general	591P1T	Overvoltage Element 1, Level 1 timed out
O1P1PTOV1	Str.general	591P1	Overvoltage Element 1, Level 1 asserted
O1P2PTOV1	Str.general	591P2	Overvoltage Element 1, Level 2 asserted
O2P1PTOV2	Op.general	592P1T	Overvoltage Element 2, Level 1 timed out
O2P1PTOV2	Str.general	592P1	Overvoltage Element 2, Level 1 asserted
O2P2PTOV2	Str.general	592P2	Overvoltage Element 2, Level 2 asserted
O3P1PTOV3	Op.general	593P1T	Overvoltage Element 3, Level 1 timed out
O3P1PTOV3	Str.general	593P1	Overvoltage Element 3, Level 1 asserted
O3P2PTOV3	Str.general	593P2	Overvoltage Element 3, Level 2 asserted
O4P1PTOV4	Op.general	594P1T	Overvoltage Element 4, Level 1 timed out
O4P1PTOV4	Str.general	594P1	Overvoltage Element 4, Level 1 asserted
O4P2PTOV4	Str.general	594P2	Overvoltage Element 4, Level 2 asserted
O5P1PTOV5	Op.general	595P1T	Overvoltage Element 5, Level 1 timed out
O5P1PTOV5	Str.general	595P1	Overvoltage Element 5, Level 1 asserted
O5P2PTOV5	Str.general	595P2	Overvoltage Element 5, Level 2 asserted
PROLPHD1	PhyHealth.stVal	EN?3:1[c]	Relay enabled
REF501PIOC1	Str.general	REF501	Neutral Instantaneous Overcurrent Element 1 picked up
REF501PIOC1	Op.general	REF50T1	Neutral Instantaneous Overcurrent Element 1 timed out
REF502PIOC2	Str.general	REF502	Neutral Instantaneous Overcurrent Element 2 picked up
REF502PIOC2	Op.general	REF50T2	Neutral Instantaneous Overcurrent Element 2 timed out
REF503PIOC3	Str.general	REF503	Neutral Instantaneous Overcurrent Element 3 picked up
REF503PIOC3	Op.general	REF50T3	Neutral Instantaneous Overcurrent Element 3 timed out
REF511PTOC1	Str.general	REF511P	Inverse-Time Neutral Overcurrent Element 1 picked up
REF511PTOC1	Op.general	REF51T1	Inverse-Time Neutral Overcurrent Element 1 timed out

Table 10.23 Logical Device: PRO (Protection) (Sheet 7 of 15)

Logical Node	Attribute	Data Source	Comment
REF512PTOC2	Str.general	REF512P	Inverse-Time Neutral Overcurrent Element 2 picked up
REF512PTOC2	Op.general	REF51T2	Inverse-Time Neutral Overcurrent Element 2 timed out
REF513PTOC3	Str.general	REF513P	Inverse-Time Neutral Overcurrent Element 3 picked up
REF513PTOC3	Op.general	REF51T3	Inverse-Time Neutral Overcurrent Element 3 timed out
REFF1PDIF1	Op.general	REFF1	Earth-fault inside Restricted Zone 1
REFF2PDIF2	Op.general	REFF2	Earth-fault inside Restricted Zone 2
REFF3PDIF3	Op.general	REFF3	Earth-fault inside Restricted Zone 3
REFR1PDIF1	Op.general	REFR1	Earth-fault outside Restricted Zone 1
REFR2PDIF2	Op.general	REFR2	Earth-fault outside Restricted Zone 2
REFR3PDIF3	Op.general	REFR3	Earth-fault outside Restricted Zone 3
S52AXCBR1	Pos.stVal	52CLS?1:2[e]	Breaker Closed Terminal S
SBKRCSWI1	OpCls.general	CCS	Breaker Close Command Terminal S
SBKRCSWI1	OpOpn.general	OCS	Breaker Open Command Terminal S
SBKRCSWI1	Pos.stVal	52CLS?1:2[e]	Breaker Closed Terminal S
SG1PIOC7	Op.general	50SG1	Residual Definite-Time Element 1 Terminal S asserted
SG1PTOC7	Op.general	67SG1T	Residual Directional/Torque Controlled Element 1 Terminal S timed out
SG1PTOC7	Str.general	67SG1	Residual Directional/Torque Controlled Element 1 Terminal S picked up
SG2PIOC8	Op.general	50SG2	Residual Definite-Time Element 2 Terminal S asserted
SG2PTOC8	Op.general	67SG2T	Residual Directional/Torque Controlled Element 2 Terminal S timed out
SG2PTOC8	Str.general	67SG2	Residual Directional/Torque Controlled Element 2 Terminal S picked up
SG3PIOC9	Op.general	50SG3	Residual Definite-Time Element 3 Terminal S asserted
SG3PTOC9	Op.general	67SG3T	Residual Directional/Torque Controlled Element 3 Terminal S timed out
SG3PTOC9	Str.general	67SG3	Residual Directional/Torque Controlled Element 3 Terminal S picked up
SP1PIOC1	Op.general	50SP1	Phase Definite-Time Element 1 Terminal S asserted
SP1PTOC1	Op.general	67SP1T	Phase Directional/Torque Controlled Element 1 Terminal S timed out
SP1PTOC1	Str.general	67SP1	Phase Directional/Torque Controlled Element 1 Terminal S picked up
SP2PIOC2	Op.general	50SP2	Phase Definite-Time Element 2 Terminal S asserted
SP2PTOC2	Op.general	67SP2T	Phase Directional/Torque Controlled Element 2 Terminal S timed out
SP2PTOC2	Str.general	67SP2	Phase Directional/Torque Controlled Element 2 Terminal S picked up
SP3PIOC3	Op.general	50SP3	Phase Definite-Time Element 3 Terminal S asserted
SP3PTOC3	Op.general	67SP3T	Phase Directional/Torque Controlled Element 3 Terminal S timed out
SP3PTOC3	Str.general	67SP3	Phase Directional/Torque Controlled Element 3 Terminal S picked up
SQ1PIOC4	Op.general	50SQ1	Negative-Sequence Definite-Time Element 1 Terminal S asserted

Table 10.23   Logical Device: PRO (Protection) (Sheet 8 of 15)

Logical Node	Attribute	Data Source	Comment
SQ1PTOC4	Op.general	67SQ1T	Negative-Sequence Directional/Torque Controlled Element 1 Terminal S timed out
SQ1PTOC4	Str.general	67SQ1	Negative-Sequence Directional/Torque Controlled Element 1 Terminal S picked up
SQ2PIOC5	Op.general	50SQ2	Negative-Sequence Definite-Time Element 2 Terminal S asserted
SQ2PTOC5	Op.general	67SQ2T	Negative-Sequence Directional/Torque Controlled Element 2 Terminal S timed out
SQ2PTOC5	Str.general	67SQ2	Negative-Sequence Directional/Torque Controlled Element 2 Terminal S picked up
SQ3PIOC6	Op.general	50SQ3	Negative-Sequence Definite-Time Element 3 Terminal S asserted
SQ3PTOC6	Op.general	67SQ3T	Negative-Sequence Directional/Torque Controlled Element 3 Terminal S timed out
SQ3PTOC6	Str.general	67SQ3	Negative-Sequence Directional/Torque Controlled Element 3 Terminal S picked up
T52AXCBR2	Pos.stVal	52CLT?1:2[e]	Breaker Closed Terminal T
TBKRCSWI2	OpCls.general	CCT	Breaker Close Command Terminal T
TBKRCSWI2	OpOpn.general	OCT	Breaker Open Command Terminal T
TBKRCSWI2	Pos.stVal	52CLT?1:2[e]	Breaker Closed Terminal T
TG1PIOC16	Op.general	50TG1	Residual Definite-Time Element 1 Terminal T asserted
TG1PTOC16	Op.general	67TG1T	Residual Directional/Torque Controlled Element 1 Terminal T timed out
TG1PTOC16	Str.general	67TG1	Residual Directional/Torque Controlled Element 1 Terminal T picked up
TG2PIOC17	Op.general	50TG2	Residual Definite-Time Element 2 Terminal T asserted
TG2PTOC17	Op.general	67TG2T	Residual Directional/Torque Controlled Element 2 Terminal T timed out
TG2PTOC17	Str.general	67TG2	Residual Directional/Torque Controlled Element 2 Terminal T picked up
TG3PIOC18	Op.general	50TG3	Residual Definite-Time Element 3 Terminal T asserted
TG3PTOC18	Op.general	67TG3T	Residual Directional/Torque Controlled Element 3 Terminal T timed out
TG3PTOC18	Str.general	67TG3	Residual Directional/Torque Controlled Element 3 Terminal T picked up
TH1PTTR1	Op.general	THRLT1	Thermal element, Level 1 trip
TH1PTTR1	AlmThm.stVal	THRLA1	Thermal element, Level 1 alarm
TH2PTTR2	Op.general	THRLT2	Thermal element, Level 2 trip
TH2PTTR2	AlmThm.stVal	THRLA2	Thermal element, Level 2 alarm
TH3PTTR3	Op.general	THRLT3	Thermal element, Level 3 trip
TH3PTTR3	AlmThm.stVal	THRLA3	Thermal element, Level 3 alarm
TP1PIOC10	Op.general	50TP1	Phase Definite-Time Element 1 Terminal T asserted
TP1PTOC10	Op.general	67TP1T	Phase Directional/Torque Controlled Element 1 Terminal T timed out
TP1PTOC10	Str.general	67TP1	Phase Directional/Torque Controlled Element 1 Terminal T picked up
TP2PIOC11	Op.general	50TP2	Phase Definite-Time Element 2 Terminal T asserted

Table 10.23 Logical Device: PRO (Protection) (Sheet 9 of 15)

Logical Node	Attribute	Data Source	Comment
TP2PTOC11	Op.general	67TP2T	Phase Directional/Torque Controlled Element 2 Terminal T timed out
TP2PTOC11	Str.general	67TP2	Phase Directional/Torque Controlled Element 2 Terminal T picked up
TP3PIOC12	Op.general	50TP3	Phase Definite-Time Element 3 Terminal T asserted
TP3PTOC12	Op.general	67TP3T	Phase Directional/Torque Controlled Element 3 Terminal T timed out
TP3PTOC12	Str.general	67TP3	Phase Directional/Torque Controlled Element 3 Terminal T picked up
TQ1PIOC13	Op.general	50TQ1	Negative-Sequence Definite-Time Element 1 Terminal T asserted
TQ1PTOC13	Op.general	67TQ1T	Negative-sequence Directional/Torque Controlled Element 1 Terminal T timed out
TQ1PTOC13	Str.general	67TQ1	Negative-sequence Directional/Torque Controlled Element 1 Terminal T picked up
TQ2PIOC14	Op.general	50TQ2	Negative-Sequence Definite-Time Element 2 Terminal T asserted
TQ2PTOC14	Op.general	67TQ2T	Negative-sequence Directional/Torque Controlled Element 2 Terminal T timed out
TQ2PTOC14	Str.general	67TQ2	Negative-sequence Directional/Torque Controlled Element 2 Terminal T picked up
TQ3PIOC15	Op.general	50TQ3	Negative-Sequence Definite-Time Element 3 Terminal T asserted
TQ3PTOC15	Op.general	67TQ3T	Negative-sequence Directional/Torque Controlled Element 3 Terminal T timed out
TQ3PTOC15	Str.general	67TQ3	Negative-sequence Directional/Torque Controlled Element 3 Terminal T picked up
TRIPPTRC1	Tr.general	TRIP	Transformer or terminal trip signal asserted
TRIPSPTRC2	Tr.general	TRIPS	Terminal S trip output asserted
TRIPTPTRC3	Tr.general	TRIPT	Terminal T trip output asserted
TRIPUPTRC4	Tr.general	TRIPU	Terminal U trip output asserted
TRIPWPTRC5	Tr.general	TRIPW	Terminal W trip output asserted
TRIPXPTRC6	Tr.general	TRIPX	Terminal X trip output asserted
TRPXFM-RPTRC7	Tr.general	TRPXFMR	Transformer trip output asserted
U1P1PTUV1	Op.general	271P1T	Under voltage Element 1, Level 1 timed out
U1P1PTUV1	Str.general	271P1	Undervoltage Element 1, Level 1 asserted
U1P2PTUV1	Op.general	271P2	Under voltage Element 1, Level 2 asserted
U1P2PTUV1	Str.general	271P2	Under voltage Element 1, Level 2 asserted
U1PVPH3	Op.general	24U1T	User-Defined Volts/Hertz Curve 1 timed out
U1PVPH3	Str.general	24D1	Volts/Hertz Element Level 1 asserted
U2P1PTUV2	Op.general	272P1T	Under voltage Element 2, Level 1 timed out
U2P1PTUV2	Str.general	272P1	Under voltage Element 2, Level 1 asserted
U2P2PTUV2	Op.general	272P2	Under voltage Element 2, Level 2 asserted
U2P2PTUV2	Str.general	272P2	Under voltage Element 2, Level 2 asserted
U2PVPH4	Op.general	24U2T	User-Defined Volts/Hertz Curve 2 timed out
U2PVPH4	Str.general	24D1	Volts/Hertz Element Level 1 asserted
U3P1PTUV3	Op.general	273P1T	Under voltage Element 3, Level 1 timed out

Table 10.23   Logical Device: PRO (Protection) (Sheet 10 of 15)

Logical Node	Attribute	Data Source	Comment
U3P1PTUV3	Str.general	273P1	Under voltage Element 3, Level 1 asserted
U3P2PTUV3	Op.general	273P2	Under voltage Element 3, Level 2 asserted
U3P2PTUV3	Str.general	273P2	Under voltage Element 3, Level 2 asserted
U4P1PTUV4	Op.general	274P1T	Under voltage Element 4, Level 1 timed out
U4P1PTUV4	Str.general	274P1	Under voltage Element 4, Level 1 asserted
U4P2PTUV4	Op.general	274P2	Under voltage Element 4, Level 2 asserted
U4P2PTUV4	Str.general	274P2	Under voltage Element 4, Level 2 asserted
U52AXCBR3	Pos.stVal	52CLU?1:2[e]	Breaker Closed Terminal U
U5P1PTUV5	Op.general	275P1T	Under voltage Element 5, Level 1 timed out
U5P1PTUV5	Str.general	275P1	Under voltage Element 5, Level 1 asserted
U5P2PTUV5	Op.general	275P2	Under voltage Element 5, Level 2 asserted
U5P2PTUV5	Str.general	275P2	Under voltage Element 5, Level 2 asserted
UBKRCSWI3	OpCls.general	CCU	Breaker Close Command Terminal U
UBKRCSWI3	OpOpn.general	OCU	Breaker Open Command Terminal U
UBKRCSWI3	Pos.stVal	52CLU?1:2[e]	Breaker Closed Terminal U
UG1PIOC25	Op.general	50UG1	Residual Definite-Time Element 1 Terminal U asserted
UG1PTOC25	Op.general	67UG1T	Residual Directional/Torque Controlled Element 1 Terminal U timed out
UG1PTOC25	Str.general	67UG1	Residual Directional/Torque Controlled Element 1 Terminal U picked up
UG2PIOC26	Op.general	50UG2	Residual Definite-Time Element 2 Terminal U asserted
UG2PTOC26	Op.general	67UG2T	Residual Directional/Torque Controlled Element 2 Terminal U timed out
UG2PTOC26	Str.general	67UG2	Residual Directional/Torque Controlled Element 2 Terminal U picked up
UG3PIOC27	Op.general	50UG3	Residual Definite-Time Element 3 Terminal U asserted
UG3PTOC27	Op.general	67UG3T	Residual Directional/Torque Controlled Element 3 Terminal U timed out
UG3PTOC27	Str.general	67UG3	Residual Directional/Torque Controlled Element 3 Terminal U picked up
UP1PIOC19	Op.general	50UP1	Phase Definite-Time Element 1 Terminal U asserted
UP1PTOC19	Op.general	67UP1T	Phase Directional/Torque Controlled Element 1 Terminal U timed out
UP1PTOC19	Str.general	67UP1	Phase Directional/Torque Controlled Element 1 Terminal U picked up
UP2PIOC20	Op.general	50UP2	Phase Definite-Time Element 2 Terminal U Asserted
UP2PTOC20	Op.general	67UP2T	Phase Directional/Torque Controlled Element 2 Terminal U timed out
UP2PTOC20	Str.general	67UP2	Phase Directional/Torque Controlled Element 2 Terminal U picked up
UP3PIOC21	Op.general	50UP3	Phase Definite-Time Element 3 Terminal U Asserted
UP3PTOC21	Op.general	67UP3T	Phase Directional/Torque Controlled Element 3 Terminal U timed out
UP3PTOC21	Str.general	67UP3	Phase Directional/Torque Controlled Element 3 Terminal U picked up

Table 10.23   Logical Device: PRO (Protection) (Sheet 11 of 15)

Logical Node	Attribute	Data Source	Comment
UQ1PIOC22	Op.general	50UQ1	Negative-sequence Definite-Time Element 1 Terminal U asserted
UQ1PTOC22	Op.general	67UQ1T	Negative-sequence Directional/Torque Controlled Element 1 Terminal U timed out
UQ1PTOC22	Str.general	67UQ1	Negative-sequence Directional/Torque Controlled Element 1 Terminal U picked up
UQ2PIOC23	Op.general	50UQ2	Negative-sequence Definite-Time Element 2 Terminal U Asserted
UQ2PTOC23	Op.general	67UQ2T	Negative-sequence Directional/Torque Controlled Element 2 Terminal U timed out
UQ2PTOC23	Str.general	67UQ2	Negative-sequence Directional/Torque Controlled Element 2 Terminal U picked up
UQ3PIOC24	Op.general	50UQ3	Negative-sequence Definite-Time Element 3 Terminal U asserted
UQ3PTOC24	Op.general	67UQ3T	Negative-sequence Directional/Torque Controlled Element 3 Terminal U timed out
UQ3PTOC24	Str.general	67UQ3	Negative-sequence Directional/Torque Controlled Element 3 Terminal U picked up
W52AXCBR4	Pos.stVal	52CLW?1:2[e]	Breaker Closed Terminal W
WBKRCSWI4	OpCls.general	CCW	Breaker Close Command Terminal W
WBKRCSWI4	OpOpn.general	OCW	Breaker Open Command Terminal W
WBKRCSWI4	Pos.stVal	52CLW?1:2[e]	Breaker Closed Terminal W
WG1PIOC34	Op.general	50WG1	Residual Definite-Time Element 1 Terminal W asserted
WG1PTOC34	Op.general	67WG1T	Residual Directional/Torque Controlled Element 1 Terminal W timed out
WG1PTOC34	Str.general	67WG1	Residual Directional/Torque Controlled Element 1 Terminal W picked up
WG2PIOC35	Op.general	50WG2	Residual Definite-Time Element 2 Terminal W asserted
WG2PTOC35	Op.general	67WG2T	Residual Directional/Torque Controlled Element 2 Terminal W timed out
WG2PTOC35	Str.general	67WG2	Residual Directional/Torque Controlled Element 2 Terminal W picked up
WG3PIOC36	Op.general	50WG3	Residual Definite-Time Element 3 Terminal W asserted
WG3PTOC36	Op.general	67WG3T	Residual Directional/Torque Controlled Element 3 Terminal W timed out
WG3PTOC36	Str.general	67WG3	Residual Directional/Torque Controlled Element 3 Terminal W picked up
WP1PIOC28	Op.general	50WP1	Phase Definite-Time Element 1 Terminal W asserted
WP1PTOC28	Op.general	67WP1T	Phase Directional/Torque Controlled Element 1 Terminal W timed out
WP1PTOC28	Str.general	67WP1	Phase Directional/Torque Controlled Element 1 Terminal W picked up
WP2PIOC29	Op.general	50WP2	Phase Definite-Time Element 2 Terminal W asserted
WP2PTOC29	Op.general	67WP2T	Phase Directional/Torque Controlled Element 2 Terminal W timed out
WP2PTOC29	Str.general	67WP2	Phase Directional/Torque Controlled Element 2 Terminal W picked up
WP3PIOC30	Op.general	50WP3	Phase Definite-Time Element 3 Terminal W asserted

Table 10.23   Logical Device: PRO (Protection) (Sheet 12 of 15)

Logical Node	Attribute	Data Source	Comment
WP3PTOC30	Op.general	67WP3T	Phase Directional/Torque Controlled Element 3 Terminal W timed out
WP3PTOC30	Str.general	67WP3	Phase Directional/Torque Controlled Element 3 Terminal W picked up
WQ1PIOC31	Op.general	50WQ1	Negative-sequence Definite-Time Element 1 Terminal W asserted
WQ1PTOC31	Op.general	67WQ1T	Negative-sequence Directional/Torque Controlled Element 1 Terminal W timed out
WQ1PTOC31	Str.general	67WQ1	Negative-sequence Directional/Torque Controlled Element 1 Terminal W picked up
WQ2PIOC32	Op.general	50WQ2	Negative-sequence Definite-Time Element 2 Terminal W asserted
WQ2PTOC32	Op.general	67WQ2T	Negative-sequence Directional/Torque Controlled Element 2 Terminal W timed out
WQ2PTOC32	Str.general	67WQ2	Negative-sequence Directional/Torque Controlled Element 2 Terminal W picked up
WQ3PIOC33	Op.general	50WQ3	Negative-sequence Definite-Time Element 3 Terminal W asserted
WQ3PTOC33	Op.general	67WQ3T	Negative-sequence Directional/Torque Controlled Element 3 Terminal W timed out
WQ3PTOC33	Str.general	67WQ3	Negative-sequence Directional/Torque Controlled Element 3 Terminal W picked up
X52AXCBR5	Pos.stVal	52CLX?1:2[e]	Breaker Closed Terminal X
X89CLXSWI1	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI1	Pos.stVal	89CL01?1:2[e]	Disconnect 1 closed
X89CLXSWI2	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI2	Pos.stVal	89CL02?1:2[e]	Disconnect 2 closed
X89CLXSWI3	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI3	Pos.stVal	89CL03?1:2[e]	Disconnect 3 closed
X89CLXSWI4	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI4	Pos.stVal	89CL04?1:2[e]	Disconnect 4 closed
X89CLXSWI5	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI5	Pos.stVal	89CL05?1:2[e]	Disconnect 5 closed
X89CLXSWI6	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI6	Pos.stVal	89CL06?1:2[e]	Disconnect 6 closed
X89CLXSWI7	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI7	Pos.stVal	89CL07?1:2[e]	Disconnect 7 closed
X89CLXSWI8	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI8	Pos.stVal	89CL08?1:2[e]	Disconnect 8 closed
X89CLXSWI9	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI9	Pos.stVal	89CL09?1:2[e]	Disconnect 9 closed
X89CLXSWI10	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI10	Pos.stVal	89CL10?1:2[e]	Disconnect 10 closed
X89CLXSWI11	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI11	Pos.stVal	89CL11?1:2[e]	Disconnect 11 closed

Table 10.23   Logical Device: PRO (Protection) (Sheet 13 of 15)

Logical Node	Attribute	Data Source	Comment
X89CLXSWI12	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI12	Pos.stVal	89CL12?1:2[e]	Disconnect 12 closed
X89CLXSWI13	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI13	Pos.stVal	89CL13?1:2[e]	Disconnect 13 closed
X89CLXSWI14	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI14	Pos.stVal	89CL14?1:2[e]	Disconnect 14 closed
X89CLXSWI15	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI15	Pos.stVal	89CL15?1:2[e]	Disconnect 15 closed
X89CLXSWI16	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI16	Pos.stVal	89CL16?1:2[e]	Disconnect 16 closed
X89CLXSWI17	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI17	Pos.stVal	89CL17?1:2[e]	Disconnect 17 closed
X89CLXSWI18	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI18	Pos.stVal	89CL18?1:2[e]	Disconnect 18 closed
X89CLXSWI19	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI19	Pos.stVal	89CL19?1:2[e]	Disconnect 19 closed
X89CLXSWI20	Loc.stVal	LOCAL	Local front-panel control
X89CLXSWI20	Pos.stVal	89CL20?1:2[e]	Disconnect 20 closed
XBKRCSWI5	OpCls.general	CCX	Breaker Close Command Terminal X
XBKRCSWI5	OpOpn.general	OCX	Breaker Open Command Terminal X
XBKRCSWI5	Pos.stVal	52CLX?1:2[e]	Breaker Closed Terminal X
XG1PIOC43	Op.general	50XG1	Residual Definite-Time Element 1 Terminal X asserted
XG1PTOC43	Op.general	67XG1T	Residual Directional/Torque Controlled Element 1 Terminal X timed out
XG1PTOC43	Str.general	67XG1	Residual Directional/Torque Controlled Element 1 Terminal X picked up
XG2PIOC44	Op.general	50XG2	Residual Definite-Time Element 2 Terminal X asserted
XG2PTOC44	Op.general	67XG2T	Residual Directional/Torque Controlled Element 2 Terminal X timed out
XG2PTOC44	Str.general	67XG2	Residual Directional/Torque Controlled Element 2 Terminal X picked up
XG3PIOC45	Op.general	50XG3	Residual Definite-Time Element 3 Terminal X asserted
XG3PTOC45	Op.general	67XG3T	Residual Directional/Torque Controlled Element 3 Terminal X timed out
XG3PTOC45	Str.general	67XG3	Residual Directional/Torque Controlled Element 3 Terminal X picked up
XP1PIOC37	Op.general	50XP1	Phase Definite-Time Element 1 Terminal X asserted
XP1PTOC37	Op.general	67XP1T	Phase Directional/Torque Controlled Element 1 Terminal X timed out
XP1PTOC37	Str.general	67XP1	Phase Directional/Torque Controlled Element 1 Terminal X picked up
XP2PIOC38	Op.general	50XP2	Phase Definite-Time Element 2 Terminal X asserted

Table 10.23   Logical Device: PRO (Protection) (Sheet 14 of 15)

Logical Node	Attribute	Data Source	Comment
XP2PTOC38	Op.general	67XP2T	Phase Directional/Torque Controlled Element 2 Terminal X timed out
XP2PTOC38	Str.general	67XP2	Phase Directional/Torque Controlled Element 2 Terminal X picked up
XP3PIOC39	Op.general	50XP3	Phase Definite-Time Element 3 Terminal X asserted
XP3PTOC39	Op.general	67XP3T	Phase Directional/Torque Controlled Element 3 Terminal X timed out
XP3PTOC39	Str.general	67XP3	Phase Directional/Torque Controlled Element 3 Terminal X picked up
XQ1PIOC40	Op.general	50XQ1	Negative-sequence Definite-Time Element 1 Terminal X asserted
XQ1PTOC40	Op.general	67XQ1T	Negative-sequence Directional/Torque Controlled Element 1 Terminal X timed out
XQ1PTOC40	Str.general	67XQ1	Negative-sequence Directional/Torque Controlled Element 1 Terminal X picked up
XQ2PIOC41	Op.general	50XQ2	Negative-sequence Definite-Time Element 2 Terminal X asserted
XQ2PTOC41	Op.general	67XQ2T	Negative-sequence Directional/Torque Controlled Element 2 Terminal X timed out
XQ2PTOC41	Str.general	67XQ2	Negative-sequence Directional/Torque Controlled Element 2 Terminal X picked up
XQ3PIOC42	Op.general	50XQ3	Negative-sequence Definite-Time Element 3 Terminal X asserted
XQ3PTOC42	Op.general	67XQ3T	Negative-sequence Directional/Torque Controlled Element 3 Terminal X timed out
XQ3PTOC42	Str.general	67XQ3	Negative-sequence Directional/Torque Controlled Element 3 Terminal X picked up
Functional Constraint = MX			
BSSASCBR1	AccAbr.instMag.f	BSBCWPA	Breaker S contact wear for Pole A
BSSBSCBR2	AccAbr.instMag.f	BSBCWPB	Breaker S contact wear for Pole B
BSSCSCBR3	AccAbr.instMag.f	BSBCWPC	Breaker S contact wear for Pole C
BSTASCBR4	AccAbr.instMag.f	BTBCWPA	Breaker T contact wear for Pole A
BSTBSCBR5	AccAbr.instMag.f	BTBCWPB	Breaker T contact wear for Pole B
BSTCSCBR6	AccAbr.instMag.f	BTBCWPC	Breaker T contact wear for Pole C
BSUASCBR7	AccAbr.instMag.f	BUBCWPA	Breaker U contact wear for Pole A
BSUBSCBR8	AccAbr.instMag.f	BUBCWPB	Breaker U contact wear for Pole B
BSUCSCBR9	AccAbr.instMag.f	BUBCWPC	Breaker U contact wear for Pole C
BSWASCBR10	AccAbr.instMag.f	BWBCWPA	Breaker W contact wear for Pole A
BSWBSCBR11	AccAbr.instMag.f	BWBCWPB	Breaker W contact wear for Pole B
BSWCSCBR12	AccAbr.instMag.f	BWBCWPC	Breaker W contact wear for Pole C
BSXASCBR13	AccAbr.instMag.f	BXBCWPA	Breaker X contact wear for Pole A
BSXBSCBR14	AccAbr.instMag.f	BXBCWPB	Breaker X contact wear for Pole B
BSXCSCBR15	AccAbr.instMag.f	BXBCWPC	Breaker X contact wear for Pole C
Functional Constraint = DC			
HBPHAR2	NamPlt.swRev	VERFID	Relay FID string
HRPHAR1	NamPlt.swRev	VERFID	Relay FID string
LLN0	NamPlt.swRev	VERFID	Relay FID string

Table 10.23   Logical Device: PRO (Protection) (Sheet 15 of 15)

Logical Node	Attribute	Data Source	Comment
PROLPHD1	PhyNam.model	PARNUM	Relay part number
PROLPHD1	PhyNam.serNum	SERNUM	Relay serial number

[a] Writing a value of 1 pulses the first bit. Writing a value of 0 pulses the second bit.

[b] I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.

[c] If enabled, value = 1. If disabled, value = 3.

[d] If closed, value = 2. If open, value = 1. If intermediate, value = 0. A value of 3 is invalid.

[e] If closed, value = 2. If open, value = 1.

Table 10.24 shows the LNs associated with measuring elements, defined as Logical Device MET.

Table 10.24   Logical Device: MET (Metering) (Sheet 1 of 17)

Logical Node	Attribute	Data Source	Comment
Functional Constraint = ST			
LLN0	Mod.stVal	I60MOD[a]	IEC 61850 mode/behavior status
LLN0	Health.stVal	EN?3:1[b]	Relay enabled
DCZBAT1	BatWrn.stVal	DC1W	DC monitor warning alarm
DCZBAT1	BatFail.stVal	DC1F	DC monitor fail alarm
DCZBAT1	BatGndFlt.stVal	DC1G	DC monitor ground fault alarm
DCZBAT1	BatDvAlm.stVal	DC1R	DC monitor alarm for ac ripple
METLPHD1	PhyHealth.stVal	EN?3:1[b]	Relay enabled
Functional Constraint = MX			
DCZBAT1	Vol.instMag.f	VDC	Station battery dc voltage
METSMMXU1	TotW.instMag.f	3PSFC	1-cycle average three-phase fundamental active power, Terminal S
METSMMXU1	TotVAr.instMag.f	3QSFC	1-cycle average three-phase fundamental reactive power, Terminal S
METSMMXU1	TotVA.instMag.f	3SSFC	1-cycle average three-phase fundamental apparent power, Terminal S
METSMMXU1	TotPF.instMag.f	3DPFS	Three-phase displacement power factor, Terminal S
METSMMXU1	Hz.instMag.f	FREQ	Tracking frequency
METSMMXU1	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METSMMXU1	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METSMMXU1	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METSMMXU1	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METSMMXU1	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z
METSMMXU1	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METSMMXU1	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METSMMXU1	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral Voltage angle, A-Phase, Terminal V
METSMMXU1	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V

Table 10.24   Logical Device: MET (Metering) (Sheet 2 of 17)

Logical Node	Attribute	Data Source	Comment
METSMMXU1	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METSMMXU1	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METSMMXU1	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METSMMXU1	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METSMMXU1	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METSMMXU1	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METSMMXU1	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METSMMXU1	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METSMMXU1	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METSMMXU1	A1.phsA.instCVal.mag.f	IASFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal S
METSMMXU1	A1.phsA.instCVal.ang.f	IASFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal S
METSMMXU1	A1.phsB.instCVal.mag.f	IBSFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal S
METSMMXU1	A1.phsB.instCVal.ang.f	IBSFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal S
METSMMXU1	A1.phsC.instCVal.mag.f	ICSFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal S
METSMMXU1	A1.phsC.instCVal.ang.f	ICSFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal S
METSMMXU1	W.phsA.instCVal.mag.f	PASFC	1-cycle average phase fundamental active power, A-Phase, Terminal S
METSMMXU1	W.phsB.instCVal.mag.f	PBSFC	1-cycle average phase fundamental active power, B-Phase, Terminal S
METSMMXU1	W.phsC.instCVal.mag.f	PCSFC	1-cycle average phase fundamental active power, C-Phase, Terminal S
METSMMXU1	VAr.phsA.instCVal.mag.f	QASFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal S
METSMMXU1	VAr.phsB.instCVal.mag.f	QBSFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal S
METSMMXU1	VAr.phsC.instCVal.mag.f	QCSFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal S
METSMMXU1	VA.phsA.instCVal.mag.f	SASFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal S
METSMMXU1	VA.phsB.instCVal.mag.f	SBSFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal S
METSMMXU1	VA.phsC.instCVal.mag.f	SCSFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal S
METSMMXU1	PF.phsA.instCVal.mag.f	DPFAS	Phase displacement power factor, A-Phase, Terminal S
METSMMXU1	PF.phsB.instCVal.mag.f	DPFBS	Phase displacement power factor, B-Phase, Terminal S
METSMMXU1	PF.phsC.instCVal.mag.f	DPFCS	Phase displacement power factor, C-Phase, Terminal S
METTMMXU2	TotW.instMag.f	3PTFC	1-cycle average three-phase fundamental active power, Terminal T
METTMMXU2	TotVAr.instMag.f	3QTFC	1-cycle average three-phase fundamental reactive power, Terminal T

Table 10.24 Logical Device: MET (Metering) (Sheet 3 of 17)

Logical Node	Attribute	Data Source	Comment
METTMMXU2	TotVA.instMag.f	3STFC	1-cycle average three-phase fundamental apparent power, Terminal T
METTMMXU2	TotPF.instMag.f	3DPFT	Three-phase displacement power factor, Terminal T
METTMMXU2	Hz.instMag.f	FREQ	Tracking frequency
METTMMXU2	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METTMMXU2	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METTMMXU2	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METTMMXU2	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METTMMXU2	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z
METTMMXU2	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METTMMXU2	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METTMMXU2	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METTMMXU2	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METTMMXU2	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METTMMXU2	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METTMMXU2	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METTMMXU2	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METTMMXU2	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METTMMXU2	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METTMMXU2	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METTMMXU2	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METTMMXU2	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METTMMXU2	A1.phsA.instCVal.mag.f	IATFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal T
METTMMXU2	A1.phsA.instCVal.ang.f	IATFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal T
METTMMXU2	A1.phsB.instCVal.mag.f	IBTFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal T
METTMMXU2	A1.phsB.instCVal.ang.f	IBTFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal T
METTMMXU2	A1.phsC.instCVal.mag.f	ICTFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal T
METTMMXU2	A1.phsC.instCVal.ang.f	ICTFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal T

Table 10.24 Logical Device: MET (Metering) (Sheet 4 of 17)

Logical Node	Attribute	Data Source	Comment
METTMMXU2	W.phsA.instCVal.mag.f	PATFC	1-cycle average phase fundamental active power, A-Phase, Terminal T
METTMMXU2	W.phsB.instCVal.mag.f	PBTFC	1-cycle average phase fundamental active power, B-Phase, Terminal T
METTMMXU2	W.phsC.instCVal.mag.f	PCTFC	1-cycle average phase fundamental active power, C-Phase, Terminal T
METTMMXU2	VAr.phsA.instCVal.mag.f	QATFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal T
METTMMXU2	VAr.phsB.instCVal.mag.f	QBTFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal T
METTMMXU2	VAr.phsC.instCVal.mag.f	QCTFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal T
METTMMXU2	VA.phsA.instCVal.mag.f	SATFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal T
METTMMXU2	VA.phsB.instCVal.mag.f	SBTFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal T
METTMMXU2	VA.phsC.instCVal.mag.f	SCTFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal T
METTMMXU2	PF.phsA.instCVal.mag.f	DPFAT	Phase displacement power factor, A-Phase, Terminal T
METTMMXU2	PF.phsB.instCVal.mag.f	DPFBT	Phase displacement power factor, B-Phase, Terminal T
METTMMXU2	PF.phsC.instCVal.mag.f	DPFCT	Phase displacement power factor, C-Phase, Terminal T
METUMMXU3	TotW.instMag.f	3PUFC	1-cycle average three-phase fundamental active power, Terminal U
METUMMXU3	TotVAr.instMag.f	3QUFC	1-cycle average three-phase fundamental reactive power, Terminal U
METUMMXU3	TotVA.instMag.f	3SUFC	1-cycle average three-phase fundamental apparent power, Terminal U
METUMMXU3	TotPF.instMag.f	3DPFU	Three-phase displacement power factor, Terminal U
METUMMXU3	Hz.instMag.f	FREQ	Tracking frequency
METUMMXU3	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METUMMXU3	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METUMMXU3	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METUMMXU3	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METUMMXU3	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z
METUMMXU3	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METUMMXU3	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METUMMXU3	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METUMMXU3	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METUMMXU3	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METUMMXU3	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V

Table 10.24   Logical Device: MET (Metering) (Sheet 5 of 17)

Logical Node	Attribute	Data Source	Comment
METUMMXU3	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METUMMXU3	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METUMMXU3	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METUMMXU3	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METUMMXU3	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METUMMXU3	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METUMMXU3	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METUMMXU3	A1.phsA.instCVal.mag.f	IAUFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal U
METUMMXU3	A1.phsA.instCVal.ang.f	IAUFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal U
METUMMXU3	A1.phsB.instCVal.mag.f	IBUFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal U
METUMMXU3	A1.phsB.instCVal.ang.f	IBUFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal U
METUMMXU3	A1.phsC.instCVal.mag.f	ICUFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal U
METUMMXU3	A1.phsC.instCVal.ang.f	ICUFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal U
METUMMXU3	W.phsA.instCVal.mag.f	PAUFC	1-cycle average phase fundamental active power, A-Phase, Terminal U
METUMMXU3	W.phsB.instCVal.mag.f	PBUFC	1-cycle average phase fundamental active power, B-Phase, Terminal U
METUMMXU3	W.phsC.instCVal.mag.f	PCUFC	1-cycle average phase fundamental active power, C-Phase, Terminal U
METUMMXU3	VAr.phsA.instCVal.mag.f	QAUFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal U
METUMMXU3	VAr.phsB.instCVal.mag.f	QBUFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal U
METUMMXU3	VAr.phsC.instCVal.mag.f	QCUFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal U
METUMMXU3	VA.phsA.instCVal.mag.f	SAUFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal U
METUMMXU3	VA.phsB.instCVal.mag.f	SBUFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal U
METUMMXU3	VA.phsC.instCVal.mag.f	SCUFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal U
METUMMXU3	PF.phsA.instCVal.mag.f	DPFAU	Phase displacement power factor, A-Phase, Terminal U
METUMMXU3	PF.phsB.instCVal.mag.f	DPFBU	Phase displacement power factor, B-Phase, Terminal U
METUMMXU3	PF.phsC.instCVal.mag.f	DPFCU	Phase displacement power factor, C-Phase, Terminal U
METWMMXU4	TotW.instMag.f	3PWFC	1-cycle average three-phase fundamental active power, Terminal W
METWMMXU4	TotVAr.instMag.f	3QWFC	1-cycle average three-phase fundamental reactive power, Terminal W
METWMMXU4	TotVA.instMag.f	3SWFC	1-cycle average three-phase fundamental apparent power, Terminal W
METWMMXU4	TotPF.instMag.f	3DPFW	Three-Phase displacement power factor, Terminal W

Table 10.24   Logical Device: MET (Metering) (Sheet 6 of 17)

Logical Node	Attribute	Data Source	Comment
METWMMXU4	Hz.instMag.f	FREQ	Tracking frequency
METWMMXU4	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METWMMXU4	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METWMMXU4	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METWMMXU4	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METWMMXU4	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z
METWMMXU4	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METWMMXU4	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METWMMXU4	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METWMMXU4	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METWMMXU4	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METWMMXU4	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METWMMXU4	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METWMMXU4	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METWMMXU4	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METWMMXU4	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METWMMXU4	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METWMMXU4	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METWMMXU4	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METWMMXU4	A1.phsA.instCVal.mag.f	IAWFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal W
METWMMXU4	A1.phsA.instCVal.ang.f	IAWFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal W
METWMMXU4	A1.phsB.instCVal.mag.f	IBWFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal W
METWMMXU4	A1.phsB.instCVal.ang.f	IBWFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal W
METWMMXU4	A1.phsC.instCVal.mag.f	ICWFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal W
METWMMXU4	A1.phsC.instCVal.ang.f	ICWFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal W
METWMMXU4	W.phsA.instCVal.mag.f	PAWFC	1-cycle average phase fundamental active power, A-Phase, Terminal W

Table 10.24   Logical Device: MET (Metering) (Sheet 7 of 17)

Logical Node	Attribute	Data Source	Comment
METWMMXU4	W.phsB.instCVal.mag.f	PBWFC	1-cycle average phase fundamental active power, B-Phase, Terminal W
METWMMXU4	W.phsC.instCVal.mag.f	PCWFC	1-cycle average phase fundamental active power, C-Phase, Terminal W
METWMMXU4	VAr.phsA.instCVal.mag.f	QAWFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal W
METWMMXU4	VAr.phsB.instCVal.mag.f	QBWFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal W
METWMMXU4	VAr.phsC.instCVal.mag.f	QCWFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal W
METWMMXU4	VA.phsA.instCVal.mag.f	SAWFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal W
METWMMXU4	VA.phsB.instCVal.mag.f	SBWFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal W
METWMMXU4	VA.phsC.instCVal.mag.f	SCWFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal W
METWMMXU4	PF.phsA.instCVal.mag.f	DPFAW	Phase displacement power factor, A-Phase, Terminal W
METWMMXU4	PF.phsB.instCVal.mag.f	DPFBW	Phase displacement power factor, B-Phase, Terminal W
METWMMXU4	PF.phsC.instCVal.mag.f	DPFCW	Phase displacement power factor, C-Phase, Terminal W
METXMMXU5	TotW.instMag.f	3PXFC	1-cycle average three-phase fundamental active power, Terminal X
METXMMXU5	TotVAr.instMag.f	3QXFC	1-cycle average three-phase fundamental reactive power, Terminal X
METXMMXU5	TotVA.instMag.f	3SXFC	1-cycle average three-phase fundamental apparent power, Terminal X
METXMMXU5	TotPF.instMag.f	3DPFX	Three-phase displacement power factor, Terminal X
METXMMXU5	Hz.instMag.f	FREQ	Tracking frequency
METXMMXU5	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METXMMXU5	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METXMMXU5	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METXMMXU5	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METXMMXU5	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z
METXMMXU5	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METXMMXU5	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METXMMXU5	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METXMMXU5	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METXMMXU5	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METXMMXU5	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METXMMXU5	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V

Table 10.24 Logical Device: MET (Metering) (Sheet 8 of 17)

Logical Node	Attribute	Data Source	Comment
METXMMXU5	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METXMMXU5	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METXMMXU5	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METXMMXU5	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METXMMXU5	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METXMMXU5	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METXMMXU5	A1.phsA.instCVal.mag.f	IAXFMC	1-cycle average filtered phase-current magnitude, A-Phase, Terminal X
METXMMXU5	A1.phsA.instCVal.ang.f	IAXFAC	1-cycle average filtered phase-current angle, A-Phase, Terminal X
METXMMXU5	A1.phsB.instCVal.mag.f	IBXFMC	1-cycle average filtered phase-current magnitude, B-Phase, Terminal X
METXMMXU5	A1.phsB.instCVal.ang.f	IBXFAC	1-cycle average filtered phase-current angle, B-Phase, Terminal X
METXMMXU5	A1.phsC.instCVal.mag.f	ICXFMC	1-cycle average filtered phase-current magnitude, C-Phase, Terminal X
METXMMXU5	A1.phsC.instCVal.ang.f	ICXFAC	1-cycle average filtered phase-current angle, C-Phase, Terminal X
METXMMXU5	W.phsA.instCVal.mag.f	PAXFC	1-cycle average phase fundamental active power, A-Phase, Terminal X
METXMMXU5	W.phsB.instCVal.mag.f	PBXFC	1-cycle average phase fundamental active power, B-Phase, Terminal X
METXMMXU5	W.phsC.instCVal.mag.f	PCXFC	1-cycle average phase fundamental active power, C-Phase, Terminal X
METXMMXU5	VAr.phsA.instCVal.mag.f	QAXFC	1-cycle average phase fundamental reactive power, A-Phase, Terminal X
METXMMXU5	VAr.phsB.instCVal.mag.f	QBXFC	1-cycle average phase fundamental reactive power, B-Phase, Terminal X
METXMMXU5	VAr.phsC.instCVal.mag.f	QCXFC	1-cycle average phase fundamental reactive power, C-Phase, Terminal X
METXMMXU5	VA.phsA.instCVal.mag.f	SAXFC	1-cycle average phase fundamental apparent power, A-Phase, Terminal X
METXMMXU5	VA.phsB.instCVal.mag.f	SBXFC	1-cycle average phase fundamental apparent power, B-Phase, Terminal X
METXMMXU5	VA.phsC.instCVal.mag.f	SCXFC	1-cycle average phase fundamental apparent power, C-Phase, Terminal X
METXMMXU5	PF.phsA.instCVal.mag.f	DPFAX	Phase displacement power factor, A-Phase, Terminal X
METXMMXU5	PF.phsB.instCVal.mag.f	DPFBX	Phase displacement power factor, B-Phase, Terminal X
METXMMXU5	PF.phsC.instCVal.mag.f	DPFCX	Phase displacement power factor, C-Phase, Terminal X
METSTMMXU6	TotW.instMag.f	3PSTFC	1-cycle average three-phase fundamental active power, combined Terminals ST
METSTMMXU6	TotVAr.instMag.f	3QSTFC	1-cycle average three-phase fundamental reactive power, combined Terminals ST
METSTMMXU6	TotVA.instMag.f	3SSTFC	1-cycle average three-phase fundamental apparent power, combined Terminals ST

Table 10.24   Logical Device: MET (Metering) (Sheet 9 of 17)

Logical Node	Attribute	Data Source	Comment
METSTMMXU6	TotPF.instMag.f	3DPFST	Three-Phase displacement power factor, combined Terminals ST
METSTMMXU6	Hz.instMag.f	FREQ	Tracking frequency
METSTMMXU6	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METSTMMXU6	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METSTMMXU6	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METSTMMXU6	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METSTMMXU6	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z
METSTMMXU6	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METSTMMXU6	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METSTMMXU6	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METSTMMXU6	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METSTMMXU6	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METSTMMXU6	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METSTMMXU6	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METSTMMXU6	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METSTMMXU6	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METSTMMXU6	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METSTMMXU6	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METSTMMXU6	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METSTMMXU6	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METSTMMXU6	A1.phsA.instCVal.mag.f	IASTFMC	1-cycle average filtered phase-current magnitude, A-Phase, combined Terminals ST
METSTMMXU6	A1.phsA.instCVal.ang.f	IASTFAC	1-cycle average filtered phase-current angle, A-Phase, combined Terminals ST
METSTMMXU6	A1.phsB.instCVal.mag.f	IBSTFMC	1-cycle average filtered phase-current magnitude, B-Phase, combined Terminals ST
METSTMMXU6	A1.phsB.instCVal.ang.f	IBSTFAC	1-cycle average filtered phase-current angle, B-Phase, combined Terminals ST
METSTMMXU6	A1.phsC.instCVal.mag.f	ICSTFMC	1-cycle average filtered phase-current magnitude, C-Phase, combined Terminals ST

Table 10.24   Logical Device: MET (Metering) (Sheet 10 of 17)

Logical Node	Attribute	Data Source	Comment
METSTMMXU6	A1.phsC.instCVal.ang.f	ICSTFAC	1-cycle average filtered phase-current angle, C-Phase, combined Terminals ST
METSTMMXU6	W.phsA.instCVal.mag.f	PASTFC	1-cycle average phase fundamental active power, A-Phase, combined Terminals ST
METSTMMXU6	W.phsB.instCVal.mag.f	PBSTFC	1-cycle average phase fundamental active power, B-Phase, combined Terminals ST
METSTMMXU6	W.phsC.instCVal.mag.f	PCSTFC	1-cycle average phase fundamental active power, C-Phase, combined Terminals ST
METSTMMXU6	VAr.phsA.instCVal.mag.f	QASTFC	1-cycle average phase fundamental reactive power, A-Phase, combined Terminals ST
METSTMMXU6	VAr.phsB.instCVal.mag.f	QBSTFC	1-cycle average phase fundamental reactive power, B-Phase, combined Terminals ST
METSTMMXU6	VAr.phsC.instCVal.mag.f	QCSTFC	1-cycle average phase fundamental reactive power, C-Phase, combined Terminals ST
METSTMMXU6	VA.phsA.instCVal.mag.f	SASTFC	1-cycle average phase fundamental apparent power, A-Phase, combined Terminals ST
METSTMMXU6	VA.phsB.instCVal.mag.f	SBSTFC	1-cycle average phase fundamental apparent power, B-Phase, combined Terminals ST
METSTMMXU6	VA.phsC.instCVal.mag.f	SCSTFC	1-cycle average phase fundamental apparent power, C-Phase, combined Terminals ST
METSTMMXU6	PF.phsA.instCVal.mag.f	DPFAST	Phase displacement power factor, A-Phase, combined Terminals ST
METSTMMXU6	PF.phsB.instCVal.mag.f	DPFBST	Phase displacement power factor, B-Phase, combined Terminals ST
METSTMMXU6	PF.phsC.instCVal.mag.f	DPFCST	Phase displacement power factor, C-Phase, combined Terminals ST
METTUMMXU7	TotW.instMag.f	3PTUFC	1-cycle average three-phase fundamental active power, combined Terminals TU
METTUMMXU7	TotVAr.instMag.f	3QTUFC	1-cycle average three-phase fundamental reactive power, combined Terminals U
METTUMMXU7	TotVA.instMag.f	3STUFC	1-cycle average three-phase fundamental apparent power, combined Terminals TU
METTUMMXU7	TotPF.instMag.f	3DPFTU	Three-Phase displacement power factor, combined Terminals TU
METTUMMXU7	Hz.instMag.f	FREQ	Tracking frequency
METTUMMXU7	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METTUMMXU7	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METTUMMXU7	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METTUMMXU7	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METTUMMXU7	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z
METTUMMXU7	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METTUMMXU7	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METTUMMXU7	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METTUMMXU7	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V

Table 10.24 Logical Device: MET (Metering) (Sheet 11 of 17)

Logical Node	Attribute	Data Source	Comment
METTUMMXU7	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METTUMMXU7	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METTUMMXU7	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METTUMMXU7	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METTUMMXU7	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METTUMMXU7	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METTUMMXU7	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METTUMMXU7	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METTUMMXU7	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METTUMMXU7	A1.phsA.instCVal.mag.f	IATUFMC	1-cycle average filtered phase-current magnitude, A-Phase, combined Terminals TU
METTUMMXU7	A1.phsA.instCVal.ang.f	IATUFAC	1-cycle average filtered phase-current angle, A-Phase, combined Terminals TU
METTUMMXU7	A1.phsB.instCVal.mag.f	IBTUFMC	1-cycle average filtered phase-current magnitude, B-Phase, combined Terminals TU
METTUMMXU7	A1.phsB.instCVal.ang.f	IBTUFAC	1-cycle average filtered phase-current angle, B-Phase, combined Terminals TU
METTUMMXU7	A1.phsC.instCVal.mag.f	ICTUFMC	1-cycle average filtered phase-current magnitude, C-Phase, combined Terminals TU
METTUMMXU7	A1.phsC.instCVal.ang.f	ICTUFAC	1-cycle average filtered phase-current angle, C-Phase, combined Terminals TU
METTUMMXU7	W.phsA.instCVal.mag.f	PATUFC	1-cycle average phase fundamental active power, A-Phase, combined Terminals TU
METTUMMXU7	W.phsB.instCVal.mag.f	PBTUFC	1-cycle average phase fundamental active power, B-Phase, combined Terminals TU
METTUMMXU7	W.phsC.instCVal.mag.f	PCTUFC	1-cycle average phase fundamental active power, C-Phase, combined Terminals TU
METTUMMXU7	VAr.phsA.instCVal.mag.f	QATUFC	1-cycle average phase fundamental reactive power, A-Phase, combined Terminals TU
METTUMMXU7	VAr.phsB.instCVal.mag.f	QBTUFC	1-cycle average phase fundamental reactive power, B-Phase, combined Terminals TU
METTUMMXU7	VAr.phsC.instCVal.mag.f	QCTUFC	1-cycle average phase fundamental reactive power, C-Phase, combined Terminals TU
METTUMMXU7	VA.phsA.instCVal.mag.f	SATUFC	1-cycle average phase fundamental apparent power, A-Phase, combined Terminals TU
METTUMMXU7	VA.phsB.instCVal.mag.f	SBTUFC	1-cycle average phase fundamental apparent power, B-Phase, combined Terminals TU
METTUMMXU7	VA.phsC.instCVal.mag.f	SCTUFC	1-cycle average phase fundamental apparent power, C-Phase, combined Terminals TU
METTUMMXU7	PF.phsA.instCVal.mag.f	DPFATU	Phase displacement power factor, A-Phase, combined Terminals TU

Table 10.24   Logical Device: MET (Metering) (Sheet 12 of 17)

Logical Node	Attribute	Data Source	Comment
METTUMMXU7	PF.phsB.instCVal.mag.f	DPFBTU	Phase displacement power factor, B-Phase, combined Terminals TU
METTUMMXU7	PF.phsC.instCVal.mag.f	DPFCTU	Phase displacement power factor, C-Phase, combined Terminals TU
METUWMMXU8	TotW.instMag.f	3PUWFC	1-cycle average three-phase fundamental active power, combined Terminals UW
METUWMMXU8	TotVAr.instMag.f	3QUWFC	1-cycle average three-phase fundamental reactive power, combined Terminals UW
METUWMMXU8	TotVA.instMag.f	3SUWFC	1-cycle average three-phase fundamental apparent power, combined Terminals UW
METUWMMXU8	TotPF.instMag.f	3DPFUW	Three-phase displacement power factor, combined Terminals UW
METUWMMXU8	Hz.instMag.f	FREQ	Tracking frequency
METUWMMXU8	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METUWMMXU8	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METUWMMXU8	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METUWMMXU8	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METUWMMXU8	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z
METUWMMXU8	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METUWMMXU8	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METUWMMXU8	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METUWMMXU8	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METUWMMXU8	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METUWMMXU8	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METUWMMXU8	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METUWMMXU8	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METUWMMXU8	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METUWMMXU8	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METUWMMXU8	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METUWMMXU8	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METUWMMXU8	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METUWMMXU8	A1.phsA.instCVal.mag.f	IAUWFMC	1-cycle average filtered phase-current magnitude, A-Phase, combined Terminals UW

Table 10.24   Logical Device: MET (Metering) (Sheet 13 of 17)

Logical Node	Attribute	Data Source	Comment
METUWMMXU8	A1.phsA.instCVal.ang.f	IAUWFAC	1-cycle average filtered phase-current angle, A-Phase, combined Terminals UW
METUWMMXU8	A1.phsB.instCVal.mag.f	IBUWFMC	1-cycle average filtered phase-current magnitude, B-Phase, combined Terminals UW
METUWMMXU8	A1.phsB.instCVal.ang.f	IBUWFAC	1-cycle average filtered phase-current angle, B-Phase, combined Terminals UW
METUWMMXU8	A1.phsC.instCVal.mag.f	ICUWFMC	1-cycle average filtered phase-current magnitude, C-Phase, combined Terminals UW
METUWMMXU8	A1.phsC.instCVal.ang.f	ICUWFAC	1-cycle average filtered phase-current angle, C-Phase, combined Terminals UW
METUWMMXU8	W.phsA.instCVal.mag.f	PAUWFC	1-cycle average phase fundamental active power, A-Phase, combined Terminals UW
METUWMMXU8	W.phsB.instCVal.mag.f	PBUWFC	1-cycle average phase fundamental active power, B-Phase, combined Terminals UW
METUWMMXU8	W.phsC.instCVal.mag.f	PCUWFC	1-cycle average phase fundamental active power, C-Phase, combined Terminals UW
METUWMMXU8	VAr.phsA.instCVal.mag.f	QAUWFC	1-cycle average phase fundamental reactive power, A-Phase, combined Terminals UW
METUWMMXU8	VAr.phsB.instCVal.mag.f	QBUWFC	1-cycle average phase fundamental reactive power, B-Phase, combined Terminals UW
METUWMMXU8	VAr.phsC.instCVal.mag.f	QCUWFC	1-cycle average phase fundamental reactive power, C-Phase, combined Terminals UW
METUWMMXU8	VA.phsA.instCVal.mag.f	SAUWFC	1-cycle average phase fundamental apparent power, A-Phase, combined Terminals UW
METUWMMXU8	VA.phsB.instCVal.mag.f	SBUWFC	1-cycle average phase fundamental apparent power, B-Phase, combined Terminals UW
METUWMMXU8	VA.phsC.instCVal.mag.f	SCUWFC	1-cycle average phase fundamental apparent power, C-Phase, combined Terminals UW
METUWMMXU8	PF.phsA.instCVal.mag.f	DPFAUW	Phase displacement power factor, A-Phase, combined Terminals UW
METUWMMXU8	PF.phsB.instCVal.mag.f	DPFBUW	Phase displacement power factor, B-Phase, combined Terminals UW
METUWMMXU8	PF.phsC.instCVal.mag.f	DPFCUW	Phase displacement power factor, C-Phase, combined Terminals UW
METWXMMXU9	TotW.instMag.f	3PWXFC	1-cycle average three-phase fundamental active power, combined Terminals WX
METWXMMXU9	TotVAr.instMag.f	3QWXFC	1-cycle average three-phase fundamental reactive power, combined Terminals WX
METWXMMXU9	TotVA.instMag.f	3SWXFC	1-cycle average three-phase fundamental apparent power, combined Terminals WX
METWXMMXU9	TotPF.instMag.f	3DPFWX	Three-phase displacement power factor, combined Terminals WX
METWXMMXU9	Hz.instMag.f	FREQ	Tracking frequency
METWXMMXU9	PPV1.phsAB.instMag.f	VABVFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal V
METWXMMXU9	PPV1.phsBC.instMag.f	VBCVFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal V
METWXMMXU9	PPV1.phsCA.instMag.f	VCAVFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal V
METWXMMXU9	PPV2.phsAB.instMag.f	VABZFMC	1-cycle average filtered phase-to-phase voltage magnitude, AB-Phase, Terminal Z
METWXMMXU9	PPV2.phsBC.instMag.f	VBCZFMC	1-cycle average filtered phase-to-phase voltage magnitude, BC-Phase, Terminal Z

Table 10.24 Logical Device: MET (Metering) (Sheet 14 of 17)

Logical Node	Attribute	Data Source	Comment
METWXMMXU9	PPV2.phsCA.instMag.f	VCAZFMC	1-cycle average filtered phase-to-phase voltage magnitude, CA-Phase, Terminal Z
METWXMMXU9	PhV1.phsA.instCVal.mag.f	VAVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal V
METWXMMXU9	PhV1.phsA.instCVal.ang.f	VAVFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal V
METWXMMXU9	PhV1.phsB.instCVal.mag.f	VBVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal V
METWXMMXU9	PhV1.phsB.instCVal.ang.f	VBVFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal V
METWXMMXU9	PhV1.phsC.instCVal.mag.f	VCVFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal V
METWXMMXU9	PhV1.phsC.instCVal.ang.f	VCVFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal V
METWXMMXU9	PhV2.phsA.instCVal.mag.f	VAZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, A-Phase, Terminal Z
METWXMMXU9	PhV2.phsA.instCVal.ang.f	VAZFAC	1-cycle average filtered phase-to-neutral voltage angle, A-Phase, Terminal Z
METWXMMXU9	PhV2.phsB.instCVal.mag.f	VBZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, B-Phase, Terminal Z
METWXMMXU9	PhV2.phsB.instCVal.ang.f	VBZFAC	1-cycle average filtered phase-to-neutral voltage angle, B-Phase, Terminal Z
METWXMMXU9	PhV2.phsC.instCVal.mag.f	VCZFMC	1-cycle average filtered phase-to-neutral voltage magnitude, C-Phase, Terminal Z
METWXMMXU9	PhV2.phsC.instCVal.ang.f	VCZFAC	1-cycle average filtered phase-to-neutral voltage angle, C-Phase, Terminal Z
METWXMMXU9	A1.phsA.instCVal.mag.f	IAWXFMC	1-cycle average filtered phase-current magnitude, A-Phase, combined Terminals WX
METWXMMXU9	A1.phsA.instCVal.ang.f	IAWXFAC	1-cycle average filtered phase-current angle, A-Phase, combined Terminals WX
METWXMMXU9	A1.phsB.instCVal.mag.f	IBWXFMC	1-cycle average filtered phase-current magnitude, B-Phase, combined Terminals WX
METWXMMXU9	A1.phsB.instCVal.ang.f	IBWXFAC	1-cycle average filtered phase-current angle, B-Phase, combined Terminals WX
METWXMMXU9	A1.phsC.instCVal.mag.f	ICWXFMC	1-cycle average filtered phase-current magnitude, C-Phase, combined Terminals WX
METWXMMXU9	A1.phsC.instCVal.ang.f	ICWXFAC	1-cycle average filtered phase-current angle, C-Phase, combined Terminals WX
METWXMMXU9	W.phsA.instCVal.mag.f	PAWXFC	1-cycle average phase fundamental active power, A-Phase, combined Terminals WX
METWXMMXU9	W.phsB.instCVal.mag.f	PBWXFC	1-cycle average phase fundamental active power, B-Phase, combined Terminals WX
METWXMMXU9	W.phsC.instCVal.mag.f	PCWXFC	1-cycle average phase fundamental active power, C-Phase, combined Terminals WX
METWXMMXU9	VAr.phsA.instCVal.mag.f	QAWXFC	1-cycle average phase fundamental reactive power, A-Phase, combined Terminals WX
METWXMMXU9	VAr.phsB.instCVal.mag.f	QBWXFC	1-cycle average phase fundamental reactive power, B-Phase, combined Terminals WX
METWXMMXU9	VAr.phsC.instCVal.mag.f	QCWXFC	1-cycle average phase fundamental reactive power, C-Phase, combined Terminals WX

Table 10.24   Logical Device: MET (Metering) (Sheet 15 of 17)

Logical Node	Attribute	Data Source	Comment
METWXMMXU9	VA.phsA.instCVal.mag.f	SAWXFC	1-cycle average phase fundamental apparent power, A-Phase, combined Terminals WX
METWXMMXU9	VA.phsB.instCVal.mag.f	SBWXFC	1-cycle average phase fundamental apparent power, B-Phase, combined Terminals WX
METWXMMXU9	VA.phsC.instCVal.mag.f	SCWXFC	1-cycle average phase fundamental apparent power, C-Phase, combined Terminals WX
METWXMMXU9	PF.phsA.instCVal.mag.f	DPFAWX	Phase displacement power factor, A-Phase, combined Terminals WX
METWXMMXU9	PF.phsB.instCVal.mag.f	DPFBWX	Phase displacement power factor, B-Phase, combined Terminals WX
METWXMMXU9	PF.phsC.instCVal.mag.f	DPFCWX	Phase displacement power factor, C-Phase, combined Terminals WX
SEQSMSQI1	SeqA.c1.instCVal.mag.f	I1SMC	1-cycle average positive-sequence current magnitude Terminal S
SEQSMSQI1	SeqA.c1.instCVal.ang.f	I1SAC	1-cycle average positive-sequence current angle, Terminal S
SEQSMSQI1	SeqA.c2.instCVal.mag.f	3I2SMC	1-cycle average negative-sequence current magnitude, Terminal S
SEQSMSQI1	SeqA.c2.instCVal.ang.f	3I2SAC	1-cycle average negative-sequence current angle, Terminal S
SEQSMSQI1	SeqA.c3.instCVal.mag.f	3I0SMC	1-cycle average zero-sequence current magnitude, Terminal S
SEQSMSQI1	SeqA.c3.instCVal.ang.f	3I0SAC	1-cycle average zero-sequence current angle, Terminal S
SEQTMSQI2	SeqA.c1.instCVal.mag.f	I1TMC	1-cycle average positive-sequence current magnitude Terminal T
SEQTMSQI2	SeqA.c1.instCVal.ang.f	I1TAC	1-cycle average positive-sequence current angle, Terminal T
SEQTMSQI2	SeqA.c2.instCVal.mag.f	3I2TMC	1-cycle average negative-sequence current magnitude, Terminal T
SEQTMSQI2	SeqA.c2.instCVal.ang.f	3I2TAC	1-cycle average negative-sequence current angle, Terminal T
SEQTMSQI2	SeqA.c3.instCVal.mag.f	3I0TMC	1-cycle average zero-sequence current magnitude, Terminal T
SEQTMSQI2	SeqA.c3.instCVal.ang.f	3I0TAC	1-cycle average zero-sequence current angle, Terminal T
SEQUMSQI3	SeqA.c1.instCVal.mag.f	I1UMC	1-cycle average positive-sequence current magnitude Terminal U
SEQUMSQI3	SeqA.c1.instCVal.ang.f	I1UAC	1-cycle average positive-sequence current angle, Terminal U
SEQUMSQI3	SeqA.c2.instCVal.mag.f	3I2UMC	1-cycle average negative-sequence current magnitude, Terminal U
SEQUMSQI3	SeqA.c2.instCVal.ang.f	3I2UAC	1-cycle average negative-sequence current angle, Terminal U
SEQUMSQI3	SeqA.c3.instCVal.mag.f	3I0UMC	1-cycle average zero-sequence current magnitude, Terminal U
SEQUMSQI3	SeqA.c3.instCVal.ang.f	3I0UAC	1-cycle average zero-sequence current angle, Terminal U
SEQWMSQI4	SeqA.c1.instCVal.mag.f	I1WMC	1-cycle average positive-sequence current magnitude Terminal W
SEQWMSQI4	SeqA.c1.instCVal.ang.f	I1WAC	1-cycle average positive-sequence current angle, Terminal W
SEQWMSQI4	SeqA.c2.instCVal.mag.f	3I2WMC	1-cycle average negative-sequence current magnitude, Terminal W
SEQWMSQI4	SeqA.c2.instCVal.ang.f	3I2WAC	1-cycle average negative-sequence current angle, Terminal W
SEQWMSQI4	SeqA.c3.instCVal.mag.f	3I0WMC	1-cycle average zero-sequence current magnitude, Terminal W
SEQWMSQI4	SeqA.c3.instCVal.ang.f	3I0WAC	1-cycle average zero-sequence current angle, Terminal W
SEQXMSQI5	SeqA.c1.instCVal.mag.f	I1XMC	1-cycle average positive-sequence current magnitude Terminal X
SEQXMSQI5	SeqA.c1.instCVal.ang.f	I1XAC	1-cycle average positive-sequence current angle, Terminal X
SEQXMSQI5	SeqA.c2.instCVal.mag.f	3I2XMC	1-cycle average negative-sequence current magnitude, Terminal X
SEQXMSQI5	SeqA.c2.instCVal.ang.f	3I2XAC	1-cycle average negative-sequence current angle, Terminal X
SEQXMSQI5	SeqA.c3.instCVal.mag.f	3I0XMC	1-cycle average zero-sequence current magnitude, Terminal X
SEQXMSQI5	SeqA.c3.instCVal.ang.f	3I0XAC	1-cycle average zero-sequence current angle, Terminal X
SEQSTMSQI6	SeqA.c1.instCVal.mag.f	I1STMC	1-cycle average positive-sequence current magnitude combined Terminals ST
SEQSTMSQI6	SeqA.c1.instCVal.ang.f	I1STAC	1-cycle average positive-sequence current angle, combined Terminals ST

Table 10.24   Logical Device: MET (Metering) (Sheet 16 of 17)

Logical Node	Attribute	Data Source	Comment
SEQSTMSQI6	SeqA.c2.instCVal.mag.f	3I2STMC	1-cycle average negative-sequence current magnitude, combined Terminals ST
SEQSTMSQI6	SeqA.c2.instCVal.ang.f	3I2STAC	1-cycle average negative-sequence current angle, combined Terminals ST
SEQSTMSQI6	SeqA.c3.instCVal.mag.f	3I0STMC	1-cycle average zero-sequence current magnitude, combined Terminals ST
SEQSTMSQI6	SeqA.c3.instCVal.ang.f	3I0STAC	1-cycle average zero-sequence current angle, combined Terminals ST
SEQTUMSQI7	SeqA.c1.instCVal.mag.f	I1TUMC	1-cycle average positive-sequence current magnitude combined Terminals TU
SEQTUMSQI7	SeqA.c1.instCVal.ang.f	I1TUAC	1-cycle average positive-sequence current angle, combined Terminals TU
SEQTUMSQI7	SeqA.c2.instCVal.mag.f	3I2TUMC	1-cycle average negative-sequence current magnitude, combined Terminals TU
SEQTUMSQI7	SeqA.c2.instCVal.ang.f	3I2TUAC	1-cycle average negative-sequence current angle, combined Terminals TU
SEQTUMSQI7	SeqA.c3.instCVal.mag.f	3I0TUMC	1-cycle average zero-sequence current magnitude, combined Terminals TU
SEQTUMSQI7	SeqA.c3.instCVal.ang.f	3I0TUAC	1-cycle average zero-sequence current angle, combined Terminals TU
SEQUWMSQI8	SeqA.c1.instCVal.mag.f	I1UWMC	1-cycle average positive-sequence current magnitude combined Terminals UW
SEQUWMSQI8	SeqA.c1.instCVal.ang.f	I1UWAC	1-cycle average positive-sequence current angle, combined Terminals UW
SEQUWMSQI8	SeqA.c2.instCVal.mag.f	3I2UWMC	1-cycle average negative-sequence current magnitude, combined Terminals UW
SEQUWMSQI8	SeqA.c2.instCVal.ang.f	3I2UWAC	1-cycle average negative-sequence current angle, combined Terminals UW
SEQUWMSQI8	SeqA.c3.instCVal.mag.f	3I0UWMC	1-cycle average zero-sequence current magnitude, combined Terminals UW
SEQUWMSQI8	SeqA.c3.instCVal.ang.f	3I0UWAC	1-cycle average zero-sequence current angle, combined Terminals UW
SEQWXMSQI9	SeqA.c1.instCVal.mag.f	I1WXMC	1-cycle average positive-sequence current magnitude combined Terminals WX
SEQWXMSQI9	SeqA.c1.instCVal.ang.f	I1WXAC	1-cycle average positive-sequence current angle, combined Terminals WX
SEQWXMSQI9	SeqA.c2.instCVal.mag.f	3I2WXMC	1-cycle average negative-sequence current magnitude, combined Terminals WX
SEQWXMSQI9	SeqA.c2.instCVal.ang.f	3I2WXAC	1-cycle average negative-sequence current angle, combined Terminals WX
SEQWXMSQI9	SeqA.c3.instCVal.mag.f	3I0WXMC	1-cycle average zero-sequence current magnitude, combined Terminals WX
SEQWXMSQI9	SeqA.c3.instCVal.ang.f	3I0WXAC	1-cycle average zero-sequence current angle, combined Terminals WX
SEQVMSQI1	SeqV1.c1.instCVal.mag.f	V1VMC	1-cycle average positive-sequence voltage magnitude, Terminal V
SEQVMSQI1	SeqV1.c1.instCVal.ang.f	V1VAC	1-cycle average positive-sequence voltage angle, Terminal V
SEQVMSQI1	SeqV1.c2.instCVal.mag.f	3V2VMC	1-cycle average negative-sequence voltage magnitude, Terminal V
SEQVMSQI1	SeqV1.c2.instCVal.ang.f	3V2VAC	1-cycle average negative-sequence voltage angle, Terminal V
SEQVMSQI1	SeqV1.c3.instCVal.mag.f	3V0VMC	1-cycle average zero-sequence voltage magnitude, Terminal V
SEQVMSQI1	SeqV1.c3.instCVal.ang.f	3V0VAC	1-cycle average zero-sequence voltage angle, Terminal V

Table 10.24   Logical Device: MET (Metering) (Sheet 17 of 17)

Logical Node	Attribute	Data Source	Comment
SEQVMSQI1	SeqV2.c1.instCVal.mag.f	V1ZMC	1-cycle average positive-sequence voltage magnitude, Terminal Z
SEQVMSQI1	SeqV2.c1.instCVal.ang.f	V1ZAC	1-cycle average positive-sequence voltage angle, Terminal Z
SEQVMSQI1	SeqV2.c2.instCVal.mag.f	3V2ZMC	1-cycle average negative-sequence voltage magnitude, Terminal Z
SEQVMSQI1	SeqV2.c2.instCVal.ang.f	3V2ZAC	1-cycle average negative-sequence voltage angle, Terminal Z
SEQVMSQI1	SeqV2.c3.instCVal.mag.f	3V0ZMC	1-cycle average zero-sequence voltage magnitude, Terminal Z
SEQVMSQI1	SeqV2.c3.instCVal.ang.f	3V0ZAC	1-cycle average zero-sequence voltage angle, Terminal Z
METYMMXN1	Amp01.instMag.f	IY1FMC	1-cycle average filtered current magnitude, Channel 1, Terminal Y
METYMMXN1	Amp02.instMag.f	IY2FMC	1-cycle average filtered current magnitude, Channel 2, Terminal Y
METYMMXN1	Amp03.instMag.f	IY3FMC	1-cycle average filtered current magnitude, Channel 3, Terminal Y
Functional Constraint = DC			
LLN0	NamPlt.swRev	VERFID	Relay FID string
METLPHD1	PhyNam.serNum	SERNUM	Relay serial number
METLPHD1	PhyNam.model	PARNUM	Relay part number

[a] I60MOD is an internal data source derived from the I850MOD analog quantity and is not available to the user.

[b] If enabled, value = 1. If disabled, value = 3.

Synchrophasors

General synchrophasor operation is described in *Section 18: Synchrophasors in the SEL-400 Series Relays Instruction Manual*. This section describes characteristics of synchrophasors that are unique to the SEL-487E.

The SEL-487E has 18 current channels and 6 voltage channels. Current Terminals S, T, U, W, X, and voltage Terminals V, Z are three-phase channels. The SEL-487E considers Channels Y1, Y2, and Y3 as a single Terminal Y.

From these 24 channels, the SEL-487E can measure as many as 32 synchrophasors (24 phase synchrophasors and 8 positive-sequence synchrophasors). Synchrophasors are always in primary, so set the CT and PT ratios in the group settings appropriately. Note that CTRY1 applies to all the channels in Terminal Y.

Table 10.25 shows the default voltage synchrophasor name, enable conditions and the PT ratio used to scale to the primary values.

Table 10.25   Voltage Synchrophasor Names

Phasor Name	Phasor Enable Conditions	PT Ratio
V1VPM	PHDVq = V1 or ALL AND Terminal V included	PTRV
VAVPM	PHDVq = PH or ALL AND Terminal V included	PTRV
VBVPM	PHDVq = PH or ALL AND Terminal V included	PTRV
VCVPM	PHDVq = PH or ALL AND Terminal V included	PTRV
V1ZPM	PHDVq = V1 or ALL AND Terminal Z included	PTRZ
VAZPM	PHDVq = PH or ALL AND Terminal Z included	PTRZ
VBZPM	PHDVq = PH or ALL AND Terminal Z included	PTRZ
VCZPM	PHDVq = PH or ALL AND Terminal Z included	PTRZ

Table 10.26 shows the default current synchrophasor names, enable conditions, and the CT ratio used to scale to the primary values.

Table 10.26   Current Synchrophasor Names

Phasor Name	Phasor Enable Conditions	CT Ratio
I1SPM	PHDIq = I1 or ALL AND Terminal S included	CTRS
IASPM	PHDIq = PH or ALL AND Terminal S included	CTRS
IBSPM	PHDIq = PH or ALL AND Terminal S included	CTRS
ICSPM	PHDIq = PH or ALL AND Terminal S included	CTRS
I1TPM	PHDIq = I1 or ALL AND Terminal T included	CTRT
IATPM	PHDIq = PH or ALL AND Terminal T included	CTRT
IBTPM	PHDIq = PH or ALL AND Terminal T included	CTRT
ICTPM	PHDIq = PH or ALL AND Terminal T included	CTRT
I1UPM	PHDIq = I1 or ALL AND Terminal U included	CTRU
IAUPM	PHDIq = PH or ALL AND Terminal U included	CTRU
IBUPM	PHDIq = PH or ALL AND Terminal U included	CTRU
ICUPM	PHDIq = PH or ALL AND Terminal U included	CTRU
I1WPM	PHDIq = I1 or ALL AND Terminal W included	CTRW
IAWPM	PHDIq = PH or ALL AND Terminal W included	CTRW
IBWPM	PHDIq = PH or ALL AND Terminal W included	CTRW
ICWPM	PHDIq = PH or ALL AND Terminal W included	CTRW
I1XPM	PHDIq = I1 or ALL AND Terminal X included	CTRX
IAXPM	PHDIq = PH or ALL AND Terminal X included	CTRX
IBXPM	PHDIq = PH or ALL AND Terminal X included	CTRX
ICXPM	PHDIq = PH or ALL AND Terminal X included	CTRX
I1YPM	PHDIq = I1 or ALL AND Terminal Y included	CTRY1
IAYPM	PHDIq = PH or ALL AND Terminal Y included	CTRY1
IBYPM	PHDIq = PH or ALL AND Terminal Y included	CTRY1
ICYPM	PHDIq = PH or ALL AND Terminal Y included	CTRY1

Table 10.27 describes the order of synchrophasors inside the data packet when operating in legacy mode (LEGACY = Y).

Table 10.27   Synchrophasor Order in Data Stream (Voltages and Currents) (Sheet 1 of 2)

Synchrophasors[a] (Analog Quantity Names)				Included When Global Settings Are as Follows:
Polar[b]		Rectangular[c]		
Magnitude	Angle	Real	Imaginary	
V1mPMM[d]	V1mPMA	V1mPMR	V1mPMI	PHDATAV := V1 or ALL
VAmPMM	VAmPMA	VAmPMR	VAmPMI	PHDATAV := PH or ALL
VBmPMM	VBmPMA	VBmPMR	VBmPMI	
VCmPMM	VCmPMA	VCmPMR	VCmPMI	

Table 10.27 Synchrophasor Order in Data Stream (Voltages and Currents) (Sheet 2 of 2)

| Synchrophasors[a] (Analog Quantity Names) | | | | Included When Global Settings Are as Follows: |
| Polar[b] | | Rectangular[c] | | |
Magnitude	Angle	Real	Imaginary	
I1nPMM[e]	I1nPMA	I1nPMR	I1nPMI	PHDATAI := I1 or ALL
IAnPMM	IAnPMA	IAnPMR	IAnPMI	PHDATAI := PH or ALL
IBnPMM	IBnPMA	IBnPMR	IBnPMI	
ICnPMM	ICnPMA	ICnPMR	ICnPMI	

[a] Synchrophasors are included in the order shown (i.e., voltages, if selected, will always precede currents).

[b] Polar coordinate values are sent when PHFMT := P.

[c] Rectangular (real and imaginary) values are sent when PHFMT := R.

[d] Where:
   m = V if PHVOLT includes V.
   m = Z if PHVOLT includes Z.

[e] Where:
   n = S if PHCURR includes S.
   n = T if PHCURR includes T.
   n = U if PHCURR includes U.
   n = W if PHCURR includes W.
   n = X if PHCURR includes X.
   n = Y if PHCURR includes Y.

In addition to the Y/N PMLEGCY options available in other SEL-400 series relays, the SEL-487E supports an N1 option. The N1 option is the same as the N option, except that the configuration of the analog and digital portions of the messages use the following settings.

NUMANq

Selects the number of user-definable analog values to be included in the synchrophasor data stream q.

➤ NUMANq := 0 sends no user-definable analog values.

➤ NUMANq := 1–16 sends the user-definable analog values.

NUMDWq

Selects the number of user-definable digital status words to be included in the synchrophasor data stream q.

➤ NUMDWq := 0 sends no user-definable binary status words.

➤ NUMDWq := 1, 2, 3, or 4 sends the user-definable binary status words.

Relay Word Bits

This section contains tables of the Relay Word bits available within the SEL-487E relay. *Table 11.1* lists the Relay Word bits in alphabetic order; *Table 11.2* lists every Relay Word bit row and the bits contained within each row.

Alphabetical List

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 1 of 69)

Name	Bit Description	Row
132QE	Negative-sequence phase directional element enabled, Terminal ST	492
132QGE	Negative-sequence ground directional element enabled, Terminal ST	492
132VE	Zero-sequence voltage directional element enabled, Terminal ST	492
150GF	Zero-sequence current above forward threshold, Terminal ST	492
150GR	Zero-sequence current above reverse threshold, Terminal ST	492
150QF	Negative-sequence current above forward threshold, Terminal ST	492
150QR	Negative-sequence current above reverse threshold, Terminal ST	492
1F32G	Forward ground directional element asserted, Terminal ST	493
1F32P	Forward phase directional element asserted, Terminal ST	500
1F32Q	Forward negative-sequence phase directional element asserted, Terminal ST	500
1F32QG	Forward negative-sequence ground directional element asserted, Terminal ST	492
1F32V	Forward zero-sequence ground directional element asserted, Terminal ST	493
1R32G	Reverse ground directional element asserted, Terminal ST	493
1R32P	Reverse phase directional element asserted, Terminal ST	500
1R32Q	Reverse negative-sequence phase directional element asserted, Terminal ST	500
1R32QG	Reverse negative-sequence phase directional element asserted, Terminal ST	493
1R32V	Reverse zero-sequence ground directional element asserted, Terminal ST	493
232QE	Negative-sequence phase directional element enabled, Terminal TU	494
232QGE	Negative-sequence ground directional element enabled, Terminal TU	494
232VE	Zero-sequence voltage directional element enabled, Terminal TU	494
24D1	Volts-Per-Hertz Element Level 1 asserted	98
24D1T	Volts-Per-Hertz Level 1 timed out	98
24D2R	Volts-Per-Hertz Element Level 2 reset	98
24D2T	Volts-Per-Hertz Level 2 timed out	98
24TC	Volts-per-hertz predefined element, torque control	98
24U1R	User-Defined Volts-Per-Hertz Curve 1 reset	99
24U1T	User-Defined Volts-Per-Hertz Curve 1 timed out	99
24U1TC	User-Defined Volts-Per-Hertz Curve 1, torque control	99

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 2 of 69)

Name	Bit Description	Row
24U2R	User-Defined Volts-Per-Hertz Curve 2 reset	99
24U2T	User-Defined Volts-Per-Hertz Curve 2 timed out	99
24U2TC	User-Defined Volts-Per-Hertz Curve 1, torque control	99
250GF	Zero-sequence current above forward threshold, Terminal TU	494
250GR	Zero-sequence current above reverse threshold, Terminal TU	494
250QF	Negative-sequence current above forward threshold, Terminal TU	494
250QR	Negative-sequence current above reverse threshold, Terminal TU	494
25A1BKS	Breaker S voltages within Sync Angle 1	540
25A1BKT	Breaker T voltages within Sync Angle 1	540
25A1BKU	Breaker U voltages within Sync Angle 1	540
25A1BKW	Breaker W voltages within Sync Angle 1	540
25A1BKX	Breaker X voltages within Sync Angle 1	540
25A1S	Breaker S voltage within Sync Angle 1 window uncompensated	445
25A1T	Breaker T voltage within Sync Angle 1 window uncompensated	445
25A1U	Breaker U voltage within Sync Angle 1 window uncompensated	445
25A1W	Breaker W voltage within Sync Angle 1 window uncompensated	445
25A1X	Breaker X voltage within Sync Angle 1 window uncompensated	445
25A2BKS	Breaker S voltages within Sync Angle 2	540
25A2BKT	Breaker T voltages within Sync Angle 2	540
25A2BKU	Breaker U voltages within Sync Angle 2	540
25A2BKW	Breaker W voltages within Sync Angle 2	540
25A2BKX	Breaker X voltages within Sync Angle 2	540
25A2S	Breaker S voltage within Sync Angle 2 window uncompensated	445
25A2T	Breaker T voltage within Sync Angle 2 window uncompensated	446
25A2U	Breaker U voltage within Sync Angle 2 window uncompensated	446
25A2W	Breaker W voltage within Sync Angle 2 window uncompensated	446
25A2X	Breaker X voltage within Sync Angle 2 window uncompensated	446
25C1S	Breaker S voltages within Sync Angle 1 window compensated	449
25C1T	Breaker T voltages within Sync Angle 1 window compensated	449
25C1U	Breaker U voltages within Sync Angle 1 window compensated	449
25C1W	Breaker W voltages within Sync Angle 1 window compensated	449
25C1X	Breaker X voltages within Sync Angle 1 window compensated	449
25C2S	Breaker S voltages within Sync Angle 2 window compensated	449
25C2T	Breaker T voltages within Sync Angle 2 window compensated	450
25C2U	Breaker U voltages within Sync Angle 2 window compensated	450
25C2W	Breaker W voltages within Sync Angle 2 window compensated	450
25C2X	Breaker X voltages within Sync Angle 2 window compensated	450
25ENBKS	Breaker S synchronism check enabled	452
25ENBKT	Breaker T synchronism check enabled	452
25ENBKU	Breaker U synchronism check enabled	452
25ENBKW	Breaker W synchronism check enabled	453

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 3 of 69)

Name	Bit Description	Row
25ENBKX	Breaker X synchronism check enabled	453
25WA1S	Breaker S voltages within Sync Angle 1 window uncompensated and unsupervised	542
25WA1T	Breaker T voltages within Sync Angle 1 window uncompensated and unsupervised	542
25WA1U	Breaker U voltages within Sync Angle 1 window uncompensated and unsupervised	542
25WA1W	Breaker W voltages within Sync Angle 1 window uncompensated and unsupervised	542
25WA1X	Breaker X voltages within Sync Angle 1 window uncompensated and unsupervised	542
25WA2S	Breaker S voltages within Sync Angle 2 window uncompensated and unsupervised	543
25WA2T	Breaker T voltages within Sync Angle 2 window uncompensated and unsupervised	543
25WA2U	Breaker U voltages within Sync Angle 2 window uncompensated and unsupervised	543
25WA2W	Breaker W voltages within Sync Angle 2 window uncompensated and unsupervised	543
25WA2X	Breaker X voltages within Sync Angle 2 window uncompensated and unsupervised	543
25WC1S	Breaker S voltages within Sync Angle 1 window compensated and unsupervised	448
25WC1T	Breaker T voltages within Sync Angle 1 window compensated and unsupervised	448
25WC1U	Breaker U voltages within Sync Angle 1 window compensated and unsupervised	448
25WC1W	Breaker W voltages within Sync Angle 1 window compensated and unsupervised	448
25WC1X	Breaker X voltages within Sync Angle 1 window compensated and unsupervised	448
25WC2S	Breaker S voltages within Sync Angle 2 window compensated and unsupervised	448
25WC2T	Breaker T voltages within Sync Angle 2 window compensated and unsupervised	448
25WC2U	Breaker U voltages within Sync Angle 2 window compensated and unsupervised	448
25WC2W	Breaker W voltages within Sync Angle 2 window compensated and unsupervised	449
25WC2X	Breaker X voltages within Sync Angle 2 window compensated and unsupervised	449
271P1	Undervoltage Element 1, Level 1 asserted	78
271P1T	Undervoltage Element 1, Level 1 timed out	78
271P2	Undervoltage Element 1, Level 2 asserted	78
272P1	Undervoltage Element 2, Level 1 asserted	78
272P1T	Undervoltage Element 2, Level 1 timed out	78
272P2	Undervoltage Element 2, Level 2 asserted	78
273P1	Undervoltage Element 3, Level 1 asserted	79
273P1T	Undervoltage Element 3, Level 1 timed out	79
273P2	Undervoltage Element 3, Level 2 asserted	79
274P1	Undervoltage Element 4, Level 1 asserted	79
274P1T	Undervoltage Element 4, Level 1 timed out	79
274P2	Undervoltage Element 4, Level 2 asserted	79
275P1	Undervoltage Element 5, Level 1 asserted	80
275P1T	Undervoltage Element 5, Level 1 timed out	80
275P2	Undervoltage Element 5, Level 2 asserted	80
27B81	Frequency elements blocked because of undervoltage	97
27TC1	Undervoltage Element 1, torque-control	78
27TC2	Undervoltage Element 2, torque-control	78
27TC3	Undervoltage Element 3, torque-control	79
27TC4	Undervoltage Element 4, torque-control	79

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 4 of 69)

Name	Bit Description	Row
27TC5	Undervoltage Element 5, torque-control	80
2F32G	Forward ground directional element asserted, Terminal TU	495
2F32P	Forward phase directional element asserted, Terminal TU	501
2F32Q	Forward negative-sequence phase directional element asserted, Terminal TU	501
2F32QG	Forward negative-sequence ground directional element asserted, Terminal TU	494
2F32V	Forward zero-sequence ground directional element asserted, Terminal TU	495
2R32G	Reverse ground directional element asserted, Terminal TU	495
2R32P	Reverse phase directional element asserted, Terminal TU	501
2R32Q	Reverse negative-sequence phase directional element asserted, Terminal TU	501
2R32QG	Reverse negative-sequence phase directional element asserted, Terminal TU	495
2R32V	Reverse zero-sequence ground directional element asserted, Terminal TU	495
32OP01	Overpower Element 01 picked up	84
32OP02	Overpower Element 02 picked up	84
32OP03	Overpower Element 03 picked up	85
32OP04	Overpower Element 04 picked up	85
32OP05	Overpower Element 05 picked up	86
32OP06	Overpower Element 06 picked up	86
32OP07	Overpower Element 07 picked up	87
32OP08	Overpower Element 08 picked up	87
32OP09	Overpower Element 09 picked up	88
32OP10	Overpower Element 10 picked up	88
32OPT01	Overpower Element 01 timed out	84
32OPT02	Overpower Element 02 timed out	84
32OPT03	Overpower Element 03 timed out	85
32OPT04	Overpower Element 04 timed out	85
32OPT05	Overpower Element 05 timed out	86
32OPT06	Overpower Element 06 timed out	86
32OPT07	Overpower Element 07 timed out	87
32OPT08	Overpower Element 08 timed out	87
32OPT09	Overpower Element 09 timed out	88
32OPT10	Overpower Element 10 timed out	88
32UP01	Underpower Element 01 picked up	89
32UP02	Underpower Element 02 picked up	89
32UP03	Underpower Element 03 picked up	90
32UP04	Underpower Element 04 picked up	90
32UP05	Underpower Element 05 picked up	91
32UP06	Underpower Element 06 picked up	91
32UP07	Underpower Element 07 picked up	92
32UP08	Underpower Element 08 picked up	92
32UP09	Underpower Element 09 picked up	93
32UP10	Underpower Element 10 picked up	93

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 5 of 69)

Name	Bit Description	Row
32UPT01	Underpower Element 01 timed out	89
32UPT02	Underpower Element 02 timed out	89
32UPT03	Underpower Element 03 timed out	90
32UPT04	Underpower Element 04 timed out	90
32UPT05	Underpower Element 05 timed out	91
32UPT06	Underpower Element 06 timed out	91
32UPT07	Underpower Element 07 timed out	92
32UPT08	Underpower Element 08 timed out	92
32UPT09	Underpower Element 09 timed out	93
32UPT10	Underpower Element 10 timed out	93
332QE	Negative-sequence phase directional element enabled, Terminal UW	496
332QGE	Negative-sequence ground directional element enabled, Terminal UW	496
332VE	Zero-sequence voltage directional element enabled, Terminal UW	496
350GF	Zero-sequence current above forward threshold, Terminal UW	496
350GR	Zero-sequence current above reverse threshold, Terminal UW	496
350QF	Negative-sequence current above forward threshold, Terminal UW	496
350QR	Negative-sequence current above reverse threshold, Terminal UW	496
3F32G	Forward ground directional element asserted, Terminal UW	497
3F32P	Forward phase directional element asserted, Terminal UW	502
3F32Q	Forward negative-sequence phase directional element asserted, Terminal UW	502
3F32QG	Forward negative-sequence ground directional element asserted, Terminal UW	496
3F32V	Forward zero-sequence ground directional element asserted, Terminal UW	497
3R32G	Reverse ground directional element asserted, Terminal UW	497
3R32P	Reverse phase directional element asserted, Terminal UW	502
3R32Q	Reverse negative-sequence phase directional element asserted, Terminal UW	502
3R32QG	Reverse negative-sequence phase directional element asserted, Terminal UW	497
3R32V	Reverse zero-sequence ground directional element asserted, Terminal UW	497
432QE	Negative-sequence phase directional element enabled, Terminal WX	498
432QGE	Negative-sequence ground directional element enabled, Terminal WX	498
432VE	Zero-sequence voltage directional element enabled, Terminal WX	498
450GF	Zero-sequence current above forward threshold, Terminal WX	498
450GR	Zero-sequence current above reverse threshold, Terminal WX	498
450QF	Negative-sequence current above forward threshold, Terminal WX	498
450QR	Negative-sequence current above reverse threshold, Terminal WX	498
46SP	Current unbalance detected Terminal S	76
46ST	Current unbalance Terminal S timed out	76
46TP	Current unbalance detected Terminal T	76
46TT	Current unbalance Terminal T timed out	76
46UP	Current unbalance detected Terminal U	76
46UT	Current unbalance Terminal U timed out	76
46WP	Current unbalance detected Terminal W	76

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 6 of 69)

Name	Bit Description	Row
46WT	Current unbalance Terminal W timed out	76
46XP	Current unbalance detected Terminal X	77
46XT	Current unbalance Terminal X timed out	77
4F32G	Forward ground directional element asserted, Terminal WX	499
4F32P	Forward phase directional element asserted, Terminal WX	503
4F32Q	Forward negative-sequence phase directional element asserted, Terminal WX	503
4F32QG	Forward negative-sequence ground directional element asserted, Terminal WX	498
4F32V	Forward zero-sequence ground directional element asserted, Terminal WX	499
4R32G	Reverse ground directional element asserted, Terminal WX	499
4R32P	Reverse phase directional element asserted, Terminal WX	503
4R32Q	Reverse negative-sequence phase directional element asserted, Terminal WX	503
4R32QG	Reverse negative-sequence phase directional element asserted, Terminal WX	499
4R32V	Reverse zero-sequence ground directional element asserted, Terminal WX	499
501G1	Residual Definite-Time Element 1, Terminal ST asserted	508
501G2	Residual Definite-Time Element 2, Terminal ST asserted	508
501G3	Residual Definite-Time Element 3, Terminal ST asserted	509
501P1	Phase Definite-Time Element 1, Terminal ST asserted	504
501P2	Phase Definite-Time Element 2, Terminal ST asserted	504
501P3	Phase Definite-Time Element 3, Terminal ST asserted	505
501Q1	Negative-Sequence Definite-Time Element 1, Terminal ST asserted	506
501Q2	Negative-Sequence Definite-Time Element 2, Terminal ST asserted	506
501Q3	Negative-Sequence Definite-Time Element 3, Terminal ST asserted	507
502G1	Residual Definite-Time Element 1, Terminal TU asserted	514
502G2	Residual Definite-Time Element 2, Terminal TU asserted	514
502G3	Residual Definite-Time Element 3, Terminal TU asserted	515
502P1	Phase Definite-Time Element 1, Terminal TU asserted	510
502P2	Phase Definite-Time Element 2, Terminal TU asserted	510
502P3	Phase Definite-Time Element 3, Terminal TU asserted	511
502Q1	Negative-Sequence Definite-Time Element 1, Terminal TU asserted	512
502Q2	Negative-Sequence Definite-Time Element 2, Terminal TU asserted	512
502Q3	Negative-Sequence Definite-Time Element 3, Terminal TU asserted	513
503G1	Residual Definite-Time Element 1, Terminal UW asserted	520
503G2	Residual Definite-Time Element 2, Terminal UW asserted	520
503G3	Residual Definite-Time Element 3, Terminal UW asserted	521
503P1	Phase Definite-Time Element 1, Terminal UW asserted	516
503P2	Phase Definite-Time Element 2, Terminal UW asserted	516
503P3	Phase Definite-Time Element 3, Terminal UW asserted	517
503Q1	Negative-Sequence Definite-Time Element 1, Terminal UW asserted	518
503Q2	Negative-Sequence Definite-Time Element 2, Terminal UW asserted	518
503Q3	Negative-Sequence Definite-Time Element 3, Terminal UW asserted	519
504G1	Residual Definite-Time Element 1, Terminal WX asserted	526

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 7 of 69)

Name	Bit Description	Row
504G2	Residual Definite-Time Element 2, Terminal WX asserted	526
504G3	Residual Definite-Time Element 3, Terminal WX asserted	527
504P1	Phase Definite-Time Element 1, Terminal WX asserted	522
504P2	Phase Definite-Time Element 2, Terminal WX asserted	522
504P3	Phase Definite-Time Element 3, Terminal WX asserted	523
504Q1	Negative-Sequence Definite-Time Element 1, Terminal WX asserted	524
504Q2	Negative-Sequence Definite-Time Element 2, Terminal WX asserted	524
504Q3	Negative-Sequence Definite-Time Element 3, Terminal WX asserted	525
50FS	Phase or neutral current above pickup, Terminal S	110
50FT	Phase or neutral current above pickup, Terminal T	112
50FU	Phase or neutral current above pickup, Terminal U	114
50FW	Phase or neutral current above pickup, Terminal W	116
50FX	Phase or neutral current above pickup, Terminal X	118
50SG1	Residual Definite-Time Element 1, Terminal S asserted	39
50SG2	Residual Definite-Time Element 2, Terminal S asserted	39
50SG3	Residual Definite-Time Element 3, Terminal S asserted	40
50SP1	Phase Definite-Time Element 1, Terminal S asserted	35
50SP2	Phase Definite-Time Element 2, Terminal S asserted	35
50SP3	Phase Definite-Time Element 3, Terminal S asserted	36
50SQ1	Negative-Sequence Definite-Time Element 1, Terminal S asserted	37
50SQ2	Negative-Sequence Definite-Time Element 2, Terminal S asserted	37
50SQ3	Negative-Sequence Definite-Time Element 3, Terminal S asserted	38
50TG1	Residual Definite-Time Element 1, Terminal T asserted	45
50TG2	Residual Definite-Time Element 2, Terminal T asserted	45
50TG3	Residual Definite-Time Element 3, Terminal T asserted	46
50TP1	Phase Definite-Time Element 1, Terminal T asserted	41
50TP2	Phase Definite-Time Element 2, Terminal T asserted	41
50TP3	Phase Definite-Time Element 3, Terminal T asserted	42
50TQ1	Negative-Sequence Definite-Time Element 1, Terminal T asserted	43
50TQ2	Negative-Sequence Definite-Time Element 2, Terminal T asserted	43
50TQ3	Negative-Sequence Definite-Time Element 3, Terminal T asserted	44
50UG1	Residual Definite-Time Element 1, Terminal U asserted	51
50UG2	Residual Definite-Time Element 2, Terminal U asserted	51
50UG3	Residual Definite-Time Element 3, Terminal U asserted	52
50UP1	Phase Definite-Time Element 1, Terminal U asserted	47
50UP2	Phase Definite-Time Element 2, Terminal U asserted	47
50UP3	Phase Definite-Time Element 3, Terminal U asserted	48
50UQ1	Negative-Sequence Definite-Time Element 1, Terminal U asserted	49
50UQ2	Negative-Sequence Definite-Time Element 2, Terminal U asserted	49
50UQ3	Negative-Sequence Definite-Time Element 3, Terminal U asserted	50
50WG1	Residual Definite-Time Element 1, Terminal W asserted	57

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 8 of 69)

Name	Bit Description	Row
50WG2	Residual Definite-Time Element 2, Terminal W asserted	57
50WG3	Residual Definite-Time Element 3, Terminal W asserted	58
50WP1	Phase Definite-Time Element 1, Terminal W asserted	53
50WP2	Phase Definite-Time Element 2, Terminal W asserted	53
50WP3	Phase Definite-Time Element 3, Terminal W asserted	54
50WQ1	Negative-Sequence Definite-Time Element 1, Terminal W asserted	55
50WQ2	Negative-Sequence Definite-Time Element 2, Terminal W asserted	55
50WQ3	Negative-Sequence Definite-Time Element 3, Terminal W asserted	56
50XG1	Residual Definite-Time Element 1, Terminal X asserted	63
50XG2	Residual Definite-Time Element 2, Terminal X asserted	63
50XG3	Residual Definite-Time Element 3, Terminal X asserted	64
50XP1	Phase Definite-Time Element 1, Terminal X asserted	59
50XP2	Phase Definite-Time Element 2, Terminal X asserted	59
50XP3	Phase Definite-Time Element 3, Terminal X asserted	60
50XQ1	Negative-Sequence Definite-Time Element 1, Terminal X asserted	61
50XQ2	Negative-Sequence Definite-Time Element 2, Terminal X asserted	61
50XQ3	Negative-Sequence Definite-Time Element 3, Terminal X asserted	62
51MM01	Inverse-Time Element 01 pickup setting outside of specified limits	65
51MM02	Inverse-Time Element 02 pickup setting outside of specified limits	66
51MM03	Inverse-Time Element 03 pickup setting outside of specified limits	67
51MM04	Inverse-Time Element 04 pickup setting outside of specified limits	68
51MM05	Inverse-Time Element 05 pickup setting outside of specified limits	69
51MM06	Inverse-Time Element 06 pickup setting outside of specified limits	70
51MM07	Inverse-Time Element 07 pickup setting outside of specified limits	71
51MM08	Inverse-Time Element 08 pickup setting outside of specified limits	72
51MM09	Inverse-Time Element 09 pickup setting outside of specified limits	73
51MM10	Inverse-Time Element 10 pickup setting outside of specified limits	74
51R01	Inverse-Time Element 01 reset	65
51R02	Inverse-Time Element 02 reset	66
51R03	Inverse-Time Element 03 reset	67
51R04	Inverse-Time Element 04 reset	68
51R05	Inverse-Time Element 05 reset	69
51R06	Inverse-Time Element 06 reset	70
51R07	Inverse-Time Element 07 reset	71
51R08	Inverse-Time Element 08 reset	72
51R09	Inverse-Time Element 09 reset	73
51R10	Inverse-Time Element 10 reset	74
51S01	Inverse-Time Element 01 picked up	65
51S02	Inverse-Time Element 02 picked up	66
51S03	Inverse-Time Element 03 picked up	67
51S04	Inverse-Time Element 04 picked up	68

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 9 of 69)

Name	Bit Description	Row
51S05	Inverse-Time Element 05 picked up	69
51S06	Inverse-Time Element 06 picked up	70
51S07	Inverse-Time Element 07 picked up	71
51S08	Inverse-Time Element 08 picked up	72
51S09	Inverse-Time Element 09 picked up	73
51S10	Inverse-Time Element 10 picked up	74
51T01	Inverse-Time Element 01 timed out	65
51T02	Inverse-Time Element 02 timed out	66
51T03	Inverse-Time Element 03 timed out	67
51T04	Inverse-Time Element 04 timed out	68
51T05	Inverse-Time Element 05 timed out	69
51T06	Inverse-Time Element 06 timed out	70
51T07	Inverse-Time Element 07 timed out	71
51T08	Inverse-Time Element 08 timed out	72
51T09	Inverse-Time Element 09 timed out	73
51T10	Inverse-Time Element 10 timed out	74
51TC01	Inverse-Time Element 01 enabled	65
51TC02	Inverse-Time Element 02 enabled	66
51TC03	Inverse-Time Element 03 enabled	67
51TC04	Inverse-Time Element 04 enabled	68
51TC05	Inverse-Time Element 05 enabled	69
51TC06	Inverse-Time Element 06 enabled	70
51TC07	Inverse-Time Element 07 enabled	71
51TC08	Inverse-Time Element 08 enabled	72
51TC09	Inverse-Time Element 09 enabled	73
51TC10	Inverse-Time Element 10 enabled	74
51TM01	Inverse-Time Element 01 time-dial setting outside of specified limits	65
51TM02	Inverse-Time Element 02 time-dial setting outside of specified limits	66
51TM03	Inverse-Time Element 03 time-dial setting outside of specified limits	67
51TM04	Inverse-Time Element 04 time-dial setting outside of specified limits	68
51TM05	Inverse-Time Element 05 time-dial setting outside of specified limits	69
51TM06	Inverse-Time Element 06 time-dial setting outside of specified limits	70
51TM07	Inverse-Time Element 07 time-dial setting outside of specified limits	71
51TM08	Inverse-Time Element 08 time-dial setting outside of specified limits	72
51TM09	Inverse-Time Element 09 time-dial setting outside of specified limits	73
51TM10	Inverse-Time Element 10 time-dial setting outside of specified limits	74
52ALS	Breaker alarm, Terminal S	120
52ALT	Breaker alarm, Terminal T	120
52ALU	Breaker alarm, Terminal U	120
52ALW	Breaker alarm, Terminal W	120
52ALX	Breaker alarm, Terminal X	121

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 10 of 69)

Name	Bit Description	Row
52CLS	Breaker closed, Terminal S	120
52CLT	Breaker closed, Terminal T	120
52CLU	Breaker closed, Terminal U	120
52CLW	Breaker closed, Terminal W	120
52CLX	Breaker closed, Terminal X	121
52SRACK	Breaker S rack position	489
52TRACK	Breaker T rack position	489
52URACK	Breaker U rack position	489
52WRACK	Breaker W rack position	489
52XRACK	Breaker X rack position	489
52STEST	Breaker S test position	489
52TTEST	Breaker T test position	489
52UTEST	Breaker U test position	489
52WTEST	Breaker W test position	490
52XTEST	Breaker X test position	490
591P1	Overvoltage Element 1, Level 1 asserted	81
591P1T	Overvoltage Element 1, Level 1 timed out	81
591P2	Overvoltage Element 1, Level 2 asserted	81
592P1	Overvoltage Element 2, Level 1 asserted	81
592P1T	Overvoltage Element 2, Level 1 timed out	81
592P2	Overvoltage Element 2, Level 2 asserted	81
593P1	Overvoltage Element 3, Level 1 asserted	82
593P1T	Overvoltage Element 3, Level 1 timed out	82
593P2	Overvoltage Element 3, Level 2 asserted	82
594P1	Overvoltage Element 4, Level 1 asserted	82
594P1T	Overvoltage Element 4, Level 1 timed out	82
594P2	Overvoltage Element 4, Level 2 asserted	82
595P1	Overvoltage Element 5, Level 1 asserted	83
595P1T	Overvoltage Element 5, Level 1 timed out	83
595P2	Overvoltage Element 5, Level 2 asserted	83
59TC1	Overvoltage Element 1, torque-control	81
59TC2	Overvoltage Element 2, torque-control	81
59TC3	Overvoltage Element 3, torque-control	82
59TC4	Overvoltage Element 4, torque-control	82
59TC5	Overvoltage Element 5, torque-control	83
59VPS	Breaker S polarizing voltage within healthy voltage window	536
59VPT	Breaker T polarizing voltage within healthy voltage window	536
59VPU	Breaker U polarizing voltage within healthy voltage window	536
59VPW	Breaker W polarizing voltage within healthy voltage window	536
59VPX	Breaker X polarizing voltage within healthy voltage window	536
59VP	Polarizing voltage within healthy voltage window	450

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 11 of 69)

Name	Bit Description	Row
59VSS	Breaker S synchronizing voltage within healthy voltage window	453
59VST	Breaker T synchronizing voltage within healthy voltage window	453
59VSU	Breaker U synchronizing voltage within healthy voltage window	453
59VSW	Breaker W synchronizing voltage within healthy voltage window	453
59VSX	Breaker X synchronizing voltage within healthy voltage window	453
671G1	Residual Directional/Torque-Controlled Element 1, Terminal ST picked up	508
671G1T	Residual Directional/Torque-Controlled Element 1, Terminal ST timed out.	508
671G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal ST	508
671G2	Residual Directional/Torque-Controlled Element 2, Terminal ST picked up	508
671G2T	Residual Directional/Torque-Controlled Element 2, Terminal ST timed out.	508
671G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal ST	508
671G3	Residual Directional/Torque-Controlled Element 3, Terminal ST picked up	509
671G3T	Residual Directional/Torque-Controlled Element 3, Terminal ST timed out.	509
671G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal ST	509
671P1	Phase Directional/Torque-Controlled Element 1, Terminal ST picked up	504
671P1T	Phase Directional/Torque-Controlled Element 1, Terminal ST timed out.	504
671P1TC	Phase Directional/Torque-Control Enable definite-time Element 1, Terminal ST	504
671P2	Phase Directional/Torque-Controlled Element 2, Terminal ST picked up	504
671P2T	Phase Directional/Torque-Controlled Element 2, Terminal ST timed out.	504
671P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal ST	504
671P3	Phase Directional/Torque-Controlled Element 3, Terminal ST picked up	505
671P3T	Phase Directional/Torque-Controlled Element 3, Terminal ST timed out.	505
671P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal ST	505
671Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal ST picked up	506
671Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal ST timed out.	506
671Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal ST	506
671Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal ST picked up	506
671Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal ST timed out.	506
671Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal ST	506
671Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal ST picked up	507
671Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal ST timed out.	507
671Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal ST	507
672G1	Residual Directional/Torque-Controlled Element 1, Terminal TU picked up	514
672G1T	Residual Directional/Torque-Controlled Element 1, Terminal TU timed out.	514
672G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	514
672G2	Residual Directional/Torque-Controlled Element 2, Terminal TU picked up	514
672G2T	Residual Directional/Torque-Controlled Element 2, Terminal TU timed out.	514
672G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	514
672G3	Residual Directional/Torque-Controlled Element 3, Terminal TU picked up	515
672G3T	Residual Directional/Torque-Controlled Element 3, Terminal TU timed out.	515
672G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	515

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 12 of 69)

Name	Bit Description	Row
672P1	Phase Directional/Torque-Controlled Element 1, Terminal TU picked up	510
672P1T	Phase Directional/Torque-Controlled Element 1, Terminal TU timed out.	510
672P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	510
672P2	Phase Directional/Torque-Controlled Element 2, Terminal TU picked up	510
672P2T	Phase Directional/Torque-Controlled Element 2, Terminal TU timed out.	510
672P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	510
672P3	Phase Directional/Torque-Controlled Element 3, Terminal TU picked up	511
672P3T	Phase Directional/Torque-Controlled Element 3, Terminal TU timed out.	511
672P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	511
672Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal TU picked up	512
672Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal TU timed out.	512
672Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	512
672Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal TU picked up	512
672Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal TU timed out.	512
672Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	512
672Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal TU picked up	513
672Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal TU timed out.	513
672Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	513
673G1	Residual Directional/Torque-Controlled Element 1, Terminal UW picked up	520
673G1T	Residual Directional/Torque-Controlled Element 1, Terminal UW timed out.	520
673G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	520
673G2	Residual Directional/Torque-Controlled Element 2, Terminal UW picked up	520
673G2T	Residual Directional/Torque-Controlled Element 2, Terminal UW timed out.	520
673G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	520
673G3	Residual Directional/Torque-Controlled Element 3, Terminal UW picked up	521
673G3T	Residual Directional/Torque-Controlled Element 3, Terminal UW timed out.	521
673G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	521
673P1	Phase Directional/Torque-Controlled Element 1, Terminal UW picked up	516
673P1T	Phase Directional/Torque-Controlled Element 1, Terminal UW timed out.	516
673P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	516
673P2	Phase Directional/Torque-Controlled Element 2, Terminal UW picked up	516
673P2T	Phase Directional/Torque-Controlled Element 2, Terminal UW timed out.	516
673P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	516
673P3	Phase Directional/Torque-Controlled Element 3, Terminal UW picked up	517
673P3T	Phase Directional/Torque-Controlled Element 3, Terminal UW timed out.	517
673P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	517
673Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal UW picked up	518
673Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal UW timed out.	518
673Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	518
673Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal UW picked up	518
673Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal UW timed out.	518

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 13 of 69)

Name	Bit Description	Row
673Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	518
673Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal UW picked up	519
673Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal UW timed out.	519
673Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	519
674G1	Residual Directional/Torque-Controlled Element 1, Terminal WX picked up	526
674G1T	Residual Directional/Torque-Controlled Element 1, Terminal WX timed out.	526
674G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	526
674G2	Residual Directional/Torque-Controlled Element 2, Terminal WX picked up	526
674G2T	Residual Directional/Torque-Controlled Element 2, Terminal WX timed out.	526
674G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	526
674G3	Residual Directional/Torque-Controlled Element 3, Terminal WX picked up	527
674G3T	Residual Directional/Torque-Controlled Element 3, Terminal WX timed out.	527
674G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	527
674P1	Phase Directional/Torque-Controlled Element 1, Terminal WX picked up	522
674P1T	Phase Directional/Torque-Controlled Element 1, Terminal WX timed out.	522
674P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	522
674P2	Phase Directional/Torque-Controlled Element 2, Terminal WX picked up	522
674P2T	Phase Directional/Torque-Controlled Element 2, Terminal WX timed out.	522
674P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	522
674P3	Phase Directional/Torque-Controlled Element 3, Terminal WX picked up	523
674P3T	Phase Directional/Torque-Controlled Element 3, Terminal WX timed out.	523
674P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	523
674Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal WX picked up	524
674Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal WX timed out.	524
674Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	524
674Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal WX picked up	524
674Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal WX timed out.	524
674Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	524
674Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal WX picked up	525
674Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal WX timed out.	525
674Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	525
67SG1	Residual Directional/Torque-Controlled Element 1, Terminal S picked up	39
67SG1T	Residual Directional/Torque-Controlled Element 1, Terminal S timed out	39
67SG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal S	39
67SG2	Residual Directional/Torque-Controlled Element 2, Terminal S picked up	39
67SG2T	Residual Directional/Torque-Controlled Element 2, Terminal S timed out	39
67SG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal S	39
67SG3	Residual Directional/Torque-Controlled Element 3, Terminal S picked up	40
67SG3T	Residual Directional/Torque-Controlled Element 3, Terminal S timed out	40
67SG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal S	40
67SP1	Phase Directional/Torque-Controlled Element 1, Terminal S picked up	35

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 14 of 69)

Name	Bit Description	Row
67SP1T	Phase Directional/Torque-Controlled Element 1, Terminal S timed out	35
67SP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal S	35
67SP2	Phase Directional/Torque-Controlled Element 2, Terminal S picked up	35
67SP2T	Phase Directional/Torque-Controlled Element 2, Terminal S timed out	35
67SP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal S	35
67SP3	Phase Directional/Torque-Controlled Element 3, Terminal S picked up	36
67SP3T	Phase Directional/Torque-Controlled Element 3, Terminal S timed out	36
67SP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal S	36
67SQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal S picked up	37
67SQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal S timed out	37
67SQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal S	37
67SQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal S picked up	37
67SQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal S timed out	37
67SQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal S	37
67SQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal S picked up	38
67SQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal S timed out	38
67SQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal S	38
67TG1	Residual Directional/Torque-Controlled Element 1, Terminal T picked up	45
67TG1T	Residual Directional/Torque-Controlled Element 1, Terminal T timed out	45
67TG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal T	45
67TG2	Residual Directional/Torque-Controlled Element 2, Terminal T picked up	45
67TG2T	Residual Directional/Torque-Controlled Element 2, Terminal T timed out	45
67TG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal T	45
67TG3	Residual Directional/Torque-Controlled Element 3, Terminal T picked up	46
67TG3T	Residual Directional/Torque-Controlled Element 3, Terminal T timed out	46
67TG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal T	46
67TP1	Phase Directional/Torque-Controlled Element 1, Terminal T picked up	41
67TP1T	Phase Directional/Torque-Controlled Element 1, Terminal T timed out	41
67TP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal T	41
67TP2	Phase Directional/Torque-Controlled Element 2, Terminal T picked up	41
67TP2T	Phase Directional/Torque-Controlled Element 2, Terminal T timed out	41
67TP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal T	41
67TP3	Phase Directional/Torque-Controlled Element 3, Terminal T picked up	42
67TP3T	Phase Directional/Torque-Controlled Element 3, Terminal T timed out	42
67TP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal T	42
67TQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal T picked up	43
67TQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal T timed out	43
67TQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal T	43
67TQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal T picked up	43
67TQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal T timed out	43
67TQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal T	43

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 15 of 69)

Name	Bit Description	Row
67TQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal T picked up	44
67TQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal T timed out	44
67TQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal T	44
67UG1	Residual Directional/Torque-Controlled Element 1, Terminal U picked up	51
67UG1T	Residual Directional/Torque-Controlled Element 1, Terminal U timed out	51
67UG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal U	51
67UG2	Residual Directional/Torque-Controlled Element 2, Terminal U picked up	51
67UG2T	Residual Directional/Torque-Controlled Element 2, Terminal U timed out	51
67UG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal U	51
67UG3	Residual Directional/Torque-Controlled Element 3, Terminal U picked up	52
67UG3T	Residual Directional/Torque-Controlled Element 3, Terminal U timed out	52
67UG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal U	52
67UP1	Phase Directional/Torque-Controlled Element 1, Terminal U picked up	47
67UP1T	Phase Directional/Torque-Controlled Element 1, Terminal U timed out	47
67UP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal U	47
67UP2	Phase Directional/Torque-Controlled Element 2, Terminal U picked up	47
67UP2T	Phase Directional/Torque-Controlled Element 2, Terminal U timed out	47
67UP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal U	47
67UP3	Phase Directional/Torque-Controlled Element 3, Terminal U picked up	48
67UP3T	Phase Directional/Torque-Controlled Element 3, Terminal U timed out	48
67UP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal U	48
67UQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal U picked up	49
67UQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal U timed out	49
67UQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal U	49
67UQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal U picked up	49
67UQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal U timed out	49
67UQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal U	49
67UQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal U picked up	50
67UQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal U timed out	50
67UQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal U	50
67WG1	Residual Directional/Torque-Controlled Element 1, Terminal W picked up	57
67WG1T	Residual Directional/Torque-Controlled Element 1, Terminal W timed out	57
67WG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal W	57
67WG2	Residual Directional/Torque-Controlled Element 2, Terminal W picked up	57
67WG2T	Residual Directional/Torque-Controlled Element 2, Terminal W timed out	57
67WG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal W	57
67WG3	Residual Directional/Torque-Controlled Element 3, Terminal W picked up	58
67WG3T	Residual Directional/Torque-Controlled Element 3, Terminal W timed out	58
67WG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal W	58
67WP1	Phase Directional/Torque-Controlled Element 1, Terminal W picked up	53
67WP1T	Phase Directional/Torque-Controlled Element 1, Terminal W timed out	53

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 16 of 69)

Name	Bit Description	Row
67WP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal W	53
67WP2	Phase Directional/Torque-Controlled Element 2, Terminal W picked up	53
67WP2T	Phase Directional/Torque-Controlled Element 2, Terminal W timed out	53
67WP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal W	53
67WP3	Phase Directional/Torque-Controlled Element 3, Terminal W picked up	54
67WP3T	Phase Directional/Torque-Controlled Element 3, Terminal W timed out	54
67WP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal W	54
67WQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal W picked up	55
67WQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal W timed out	55
67WQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal W	55
67WQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal W picked up	55
67WQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal W timed out	55
67WQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal W	55
67WQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal W picked up	56
67WQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal W timed out	56
67WQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal W	56
67XG1	Residual Directional/Torque-Controlled Element 1, Terminal X picked up	63
67XG1T	Residual Directional/Torque-Controlled Element 1, Terminal X timed out	63
67XG1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal X	63
67XG2	Residual Directional/Torque-Controlled Element 2, Terminal X picked up	63
67XG2T	Residual Directional/Torque-Controlled Element 2, Terminal X timed out	63
67XG2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal X	63
67XG3	Residual Directional/Torque-Controlled Element 3, Terminal X picked up	64
67XG3T	Residual Directional/Torque-Controlled Element 3, Terminal X timed out	64
67XG3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal X	64
67XP1	Phase Directional/Torque-Controlled Element 1, Terminal X picked up	59
67XP1T	Phase Directional/Torque-Controlled Element 1, Terminal X timed out	59
67XP1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal X	59
67XP2	Phase Directional/Torque-Controlled Element 2, Terminal X picked up	59
67XP2T	Phase Directional/Torque-Controlled Element 2, Terminal X timed out	59
67XP2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal X	59
67XP3	Phase Directional/Torque-Controlled Element 3, Terminal X picked up	60
67XP3T	Phase Directional/Torque-Controlled Element 3, Terminal X timed out	60
67XP3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal X	60
67XQ1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal X picked up	61
67XQ1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal X timed out	61
67XQ1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal X	61
67XQ2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal X picked up	61
67XQ2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal X timed out	61
67XQ2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal X	61
67XQ3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal X picked up	62

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 17 of 69)

Name	Bit Description	Row
67XQ3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal X timed out	62
67XQ3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal X	62
81D1	Definite-time frequency element picked up, Level 1	94
81D1OVR	Definite-time overfrequency Level 1	94
81D1T	Definite-time over/underfrequency element delay for Level 1	94
81D1UDR	Definite-time underfrequency Level 1	94
81D2	Definite-time frequency element picked up, Level 2	94
81D2OVR	Definite-time overfrequency Level 2	94
81D2T	Definite-time over/underfrequency element delay for Level 2	94
81D2UDR	Definite-time underfrequency Level 2	94
81D3	Definite-time frequency element picked up, Level 3	95
81D3OVR	Definite-time overfrequency Level 3	95
81D3T	Definite-time over/underfrequency element delay for Level 3	95
81D3UDR	Definite-time underfrequency Level 3	95
81D4	Definite-time frequency element picked up, Level 4	95
81D4OVR	Definite-time overfrequency Level 4	95
81D4T	Definite-time over/underfrequency element delay for Level 4	95
81D4UDR	Definite-time underfrequency Level 4	95
81D5	Definite-time frequency element picked up, Level 5	96
81D5OVR	Definite-time overfrequency Level 5	96
81D5T	Definite-time over/underfrequency element delay for Level 5	96
81D5UDR	Definite-time underfrequency Level 5	96
81D6	Definite-time frequency element picked up, Level 6	96
81D6OVR	Definite-time overfrequency Level 6	96
81D6T	Definite-time over/underfrequency element delay for Level 6	96
81D6UDR	Definite-time underfrequency Level 6	96
87ABK2	Second- and fourth-harmonic blocking asserted, A-Phase	11
87ABK5	Fifth-harmonic blocking asserted, A-Phase	11
87AHB	Harmonic-blocked phase differential element asserted (no security timer), A-Phase	8
87AHR	Harmonic-restrained phase differential element asserted (no security timer), A-Phase	8
87BBK2	Second- and fourth-harmonic blocking asserted, B-Phase	11
87BBK5	Fifth-harmonic blocking asserted, B-Phase	11
87BHB	Harmonic-blocked phase differential element asserted (no security timer), B-Phase	8
87BHR	Harmonic-restrained phase differential element asserted (no security timer), B-Phase	8
87BPH	High-set bipolar differential overcurrent condition asserted	460
87BPHA	High-set bipolar differential overcurrent condition asserted, A-Phase	460
87BPHB	High-set bipolar differential overcurrent condition asserted, B-Phase	460
87BPHC	High-set bipolar differential overcurrent condition asserted, C-Phase	460
87BPL	Low-set bipolar differential overcurrent condition asserted	460
87BPLA	Low-set bipolar differential overcurrent condition asserted, A-Phase	460
87BPLB	Low-set bipolar differential overcurrent condition asserted, B-Phase	460

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 18 of 69)

Name	Bit Description	Row
87BPLC	Low-set bipolar differential overcurrent condition asserted, C-Phase	460
87CBK2	Second- and fourth-harmonic blocking asserted, C-Phase	11
87CBK5	Fifth-harmonic blocking asserted, C-Phase	11
87CHB	Harmonic-blocked phase differential element asserted (no security timer), C-Phase	8
87CHR	Harmonic-restrained phase differential element asserted (no security timer), C-Phase	8
87HBPA	Minimum pickup and slope conditions satisfied for harmonic-blocked phase differential, A-Phase	461
87HBPB	Minimum pickup and slope conditions satisfied for harmonic-blocked phase differential, B-Phase	461
87HBPC	Minimum pickup and slope conditions satisfied for harmonic-blocked phase differential, C-Phase	461
87HRPA	Minimum pickup and slope conditions satisfied for harmonic-restrained phase differential, A-Phase	461
87HRPB	Minimum pickup and slope conditions satisfied for harmonic-restrained phase differential, B-Phase	461
87HRPC	Minimum pickup and slope conditions satisfied for harmonic-restrained phase differential, C-Phase	461
87PQ	Minimum pickup and slope conditions satisfied for negative-sequence differential element	13
87Q	Negative-sequence differential element operated	13
87QB	Block negative-sequence differential element	11
87R	Phase percentage-restrained differential element operated	10
87RA	Percentage-restrained differential element operated, A-Phase	10
87RB	Percentage-restrained differential element operated, B-Phase	10
87RC	Percentage-restrained differential element operated, C-Phase	10
87T	Transformer differential element operated (87R OR 87Q OR 87U)	461
87T_B1A	Bipolar low-set signature detected in operate current, A-Phase	7
87T_B1B	Bipolar low-set signature detected in operate current, B-Phase	7
87T_B1C	Bipolar low-set signature detected in operate current, C-Phase	7
87T_B2A	Bipolar high-set signature detected in operate current, A-Phase	12
87T_B2B	Bipolar high-set signature detected in operate current, B-Phase	12
87T_B2C	Bipolar high-set signature detected in operate current, C-Phase	12
87T_BP1	Bipolar low-set signature detected	6
87T_BP2	Bipolar high-set signature detected	6
87T_M	Sufficient differential current to enable three-legged transformer waveshape logic	10
87T_MA	Sufficient differential current to enable non-three-legged transformer waveshape logic, A-Phase	4
87T_MB	Sufficient differential current to enable non-three-legged transformer waveshape logic, B-Phase	4
87T_MC	Sufficient differential current to enable non-three-legged transformer waveshape logic, C-Phase	4
87T_S	Dwell periods identified in differential current, non-three-legged transformer	5
87T_SA	Dwell periods identified in differential current, non-three-legged transformer, A-Phase	5
87T_SB	Dwell periods identified in differential current, non-three-legged transformer, B-Phase	5
87T_SC	Dwell periods identified in differential current, non-three-legged transformer, C-Phase	5
87T_SF	Magnetizing inrush current detected by waveshape logic (three-legged transformer)	9
87T_SFA	Magnetizing inrush current detected by waveshape logic, A-Phase (non-three-legged transformer)	9
87T_SFB	Magnetizing inrush current detected by waveshape logic, B-Phase (non-three-legged transformer)	9
87T_SFC	Magnetizing inrush current detected by waveshape logic, C-Phase (non-three-legged transformer)	9
87U	Unrestrained differential element operated	9
87UA	Unrestrained differential overcurrent element operated, A-Phase	9

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 19 of 69)

Name	Bit Description	Row
87UB	Unrestrained differential overcurrent element operated, B-Phase	9
87UC	Unrestrained differential overcurrent element operated, C-Phase	9
87UFA	Unrestrained differential element operated from filtered current, A-Phase	462
87UFB	Unrestrained differential element operated from filtered current, B-Phase	462
87UFC	Unrestrained differential element operated from filtered current, C-Phase	462
87UNBL	Waveshape-based inrush unblocking condition asserted	463
87UNBLA	Waveshape-based inrush unblocking condition asserted, A-Phase	463
87UNBLB	Waveshape-based inrush unblocking condition asserted, B-Phase	463
87UNBLC	Waveshape-based inrush unblocking condition asserted, C-Phase	463
87URA	Unrestrained differential element operated from raw current, A-Phase	462
87URB	Unrestrained differential element operated from raw current, B-Phase	462
87URC	Unrestrained differential element operated from raw current, C-Phase	462
87WB	Magnetizing inrush current detected by waveshape logic	463
87WBA	Magnetizing inrush current detected by waveshape logic, A-Phase	463
87WBB	Magnetizing inrush current detected by waveshape logic, B-Phase	463
87WBC	Magnetizing inrush current detected by waveshape logic, C-Phase	463
87WS	Waveshape-based differential element operated (87R OR 87U)	7
87XBK2	Second- and fourth-harmonic cross blocking asserted	11
87XBK5	Fifth-harmonic cross blocking asserted	8
89AL	Any disconnect alarm	122
89AL01	Disconnect 1 alarm	122
89AL02	Disconnect 2 alarm	123
89AL03	Disconnect 3 alarm	124
89AL04	Disconnect 4 alarm	125
89AL05	Disconnect 5 alarm	126
89AL06	Disconnect 6 alarm	127
89AL07	Disconnect 7 alarm	128
89AL08	Disconnect 8 alarm	129
89AL09	Disconnect 9 alarm	130
89AL10	Disconnect 10 alarm	131
89AL11	Disconnect 11 alarm	132
89AL12	Disconnect 12 alarm	133
89AL13	Disconnect 13 alarm	134
89AL14	Disconnect 14 alarm	135
89AL15	Disconnect 15 alarm	136
89AL16	Disconnect 16 alarm	137
89AL17	Disconnect 17 alarm	138
89AL18	Disconnect 18 alarm	139
89AL19	Disconnect 19 alarm	140
89AL20	Disconnect 20 alarm	141
89AM01	Disconnect 1 N/O auxiliary contact	122

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 20 of 69)

Name	Bit Description	Row
89AM02	Disconnect 2 N/O auxiliary contact	123
89AM03	Disconnect 3 N/O auxiliary contact	124
89AM04	Disconnect 4 N/O auxiliary contact	125
89AM05	Disconnect 5 N/O auxiliary contact	126
89AM06	Disconnect 6 N/O auxiliary contact	127
89AM07	Disconnect 7 N/O auxiliary contact	128
89AM08	Disconnect 8 N/O auxiliary contact	129
89AM09	Disconnect 9 N/O auxiliary contact	130
89AM10	Disconnect 10 N/O auxiliary contact	131
89AM11	Disconnect 11 N/O auxiliary contact	132
89AM12	Disconnect 12 N/O auxiliary contact	133
89AM13	Disconnect 13 N/O auxiliary contact	134
89AM14	Disconnect 14 N/O auxiliary contact	135
89AM15	Disconnect 15 N/O auxiliary contact	136
89AM16	Disconnect 16 N/O auxiliary contact	137
89AM17	Disconnect 17 N/O auxiliary contact	138
89AM18	Disconnect 18 N/O auxiliary contact	139
89AM19	Disconnect 19 N/O auxiliary contact	140
89AM20	Disconnect 20 N/O auxiliary contact	141
89BM01	Disconnect 1 N/C auxiliary contact	122
89BM02	Disconnect 2 N/C auxiliary contact	123
89BM03	Disconnect 3 N/A auxiliary contact	124
89BM04	Disconnect 4 N/C auxiliary contact	125
89BM05	Disconnect 5 N/A auxiliary contact	126
89BM06	Disconnect 6 N/A auxiliary contact	127
89BM07	Disconnect 7 N/A auxiliary contact	128
89BM08	Disconnect 8 N/A auxiliary contact	129
89BM09	Disconnect 9 N/A auxiliary contact	130
89BM10	Disconnect 10 N/A auxiliary contact	131
89BM11	Disconnect 11 N/C auxiliary contact	132
89BM12	Disconnect 12 N/C auxiliary contact	133
89BM13	Disconnect 13 N/A auxiliary contact	134
89BM14	Disconnect 14 N/C auxiliary contact	135
89BM15	Disconnect 15 N/A auxiliary contact	136
89BM16	Disconnect 16 N/A auxiliary contact	137
89BM17	Disconnect 17 N/A auxiliary contact	138
89BM18	Disconnect 18 N/A auxiliary contact	139
89BM19	Disconnect 19 N/A auxiliary contact	140
89BM20	Disconnect 20 N/A auxiliary contact	141
89CBL01	Disconnect 01 close block	168
89CBL02	Disconnect 02 close block	170

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 21 of 69)

Name	Bit Description	Row
89CBL03	Disconnect 03 close block	171
89CBL04	Disconnect 04 close block	173
89CBL05	Disconnect 05 close block	174
89CBL06	Disconnect 06 close block	176
89CBL07	Disconnect 07 close block	177
89CBL08	Disconnect 08 close block	179
89CBL09	Disconnect 09 close block	180
89CBL10	Disconnect 10 close block	182
89CBL11	Disconnect 11 close block	183
89CBL12	Disconnect 12 close block	185
89CBL13	Disconnect 13 close block	187
89CBL14	Disconnect 14 close block	188
89CBL15	Disconnect 15 close block	190
89CBL16	Disconnect 16 close block	191
89CBL17	Disconnect 17 close block	193
89CBL18	Disconnect 18 close block	194
89CBL19	Disconnect 19 close block	196
89CBL20	Disconnect 20 close block	197
89CC01	ASCII Close Disconnect 1 command	145
89CC02	ASCII Close Disconnect 2 command	146
89CC03	ASCII Close Disconnect 3 command	147
89CC04	ASCII Close Disconnect 4 command	148
89CC05	ASCII Close Disconnect 5 command	149
89CC06	ASCII Close Disconnect 6 command	150
89CC07	ASCII Close Disconnect 7 command	151
89CC08	ASCII Close Disconnect 8 command	152
89CC09	ASCII Close Disconnect 9 command	153
89CC10	ASCII Close Disconnect 10 command	154
89CC11	ASCII Close Disconnect 11 command	155
89CC12	ASCII Close Disconnect 12 command	156
89CC13	ASCII Close Disconnect 13 command	157
89CC14	ASCII Close Disconnect 14 command	158
89CC15	ASCII Close Disconnect 15 command	159
89CC16	ASCII Close Disconnect 16 command	160
89CC17	ASCII Close Disconnect 17 command	161
89CC18	ASCII Close Disconnect 18 command	162
89CC19	ASCII Close Disconnect 19 command	163
89CC20	ASCII Close Disconnect 20 command	164
89CCM01	Mimic Disconnect 1 close control	145
89CCM02	Mimic Disconnect 2 close control	146
89CCM03	Mimic Disconnect 3 close control	147

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 22 of 69)

Name	Bit Description	Row
89CCM04	Mimic Disconnect 4 close control	148
89CCM05	Mimic Disconnect 5 close control	149
89CCM06	Mimic Disconnect 6 close control	150
89CCM07	Mimic Disconnect 7 close control	151
89CCM08	Mimic Disconnect 8 close control	152
89CCM09	Mimic Disconnect 9 close control	153
89CCM10	Mimic Disconnect 10 close control	154
89CCM11	Mimic Disconnect 11 close control	155
89CCM12	Mimic Disconnect 12 close control	156
89CCM13	Mimic Disconnect 13 close control	157
89CCM14	Mimic Disconnect 14 close control	158
89CCM15	Mimic Disconnect 15 close control	159
89CCM16	Mimic Disconnect 16 close control	160
89CCM17	Mimic Disconnect 17 close control	161
89CCM18	Mimic Disconnect 18 close control	162
89CCM19	Mimic Disconnect 19 close control	163
89CCM20	Mimic Disconnect 20 close control	164
89CCN01	Close Disconnect 1	146
89CCN02	Close Disconnect 2	147
89CCN03	Close Disconnect 3	148
89CCN04	Close Disconnect 4	149
89CCN05	Close Disconnect 5	150
89CCN06	Close Disconnect 6	151
89CCN07	Close Disconnect 7	152
89CCN08	Close Disconnect 8	153
89CCN09	Close Disconnect 9	154
89CCN10	Close Disconnect 10	155
89CCN11	Close Disconnect 11	156
89CCN12	Close Disconnect 12	157
89CCN13	Close Disconnect 13	158
89CCN14	Close Disconnect 14	159
89CCN15	Close Disconnect 15	160
89CCN16	Close Disconnect 16	161
89CCN17	Close Disconnect 17	162
89CCN18	Close Disconnect 18	163
89CCN19	Close Disconnect 19	164
89CCN20	Close Disconnect 20	165
89CIM01	Disconnect 01 close immobility timer timed out	169
89CIM02	Disconnect 02 close immobility timer timed out	171
89CIM03	Disconnect 03 close immobility timer timed out	172
89CIM04	Disconnect 04 close immobility timer timed out	174

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 23 of 69)

Name	Bit Description	Row
89CIM05	Disconnect 05 close immobility timer timed out	175
89CIM06	Disconnect 06 close immobility timer timed out	177
89CIM07	Disconnect 07 close immobility timer timed out	178
89CIM08	Disconnect 08 close immobility timer timed out	180
89CIM09	Disconnect 09 close immobility timer timed out	181
89CIM10	Disconnect 10 close immobility timer timed out	183
89CIM11	Disconnect 11 close immobility timer timed out	184
89CIM12	Disconnect 12 close immobility timer timed out	186
89CIM13	Disconnect 13 close immobility timer timed out	188
89CIM14	Disconnect 14 close immobility timer timed out	189
89CIM15	Disconnect 15 close immobility timer timed out	191
89CIM16	Disconnect 16 close immobility timer timed out	192
89CIM17	Disconnect 17 close immobility timer timed out	194
89CIM18	Disconnect 18 close immobility timer timed out	195
89CIM19	Disconnect 19 close immobility timer timed out	197
89CIM20	Disconnect 20 close immobility timer timed out	198
89CIR01	Disconnect 01 close immobility timer reset	168
89CIR02	Disconnect 02 close immobility timer reset	170
89CIR03	Disconnect 03 close immobility timer reset	172
89CIR04	Disconnect 04 close immobility timer reset	173
89CIR05	Disconnect 05 close immobility timer reset	175
89CIR06	Disconnect 06 close immobility timer reset	176
89CIR07	Disconnect 07 close immobility timer reset	178
89CIR08	Disconnect 08 close immobility timer reset	179
89CIR09	Disconnect 09 close immobility timer reset	181
89CIR10	Disconnect 10 close immobility timer reset	182
89CIR11	Disconnect 11 close immobility timer reset	184
89CIR12	Disconnect 12 close immobility timer reset	186
89CIR13	Disconnect 13 lose immobility timer reset	187
89CIR14	Disconnect 14 close immobility timer reset	189
89CIR15	Disconnect 15 close immobility timer reset	190
89CIR16	Disconnect 16 close immobility timer reset	192
89CIR17	Disconnect 17 close immobility timer reset	193
89CIR18	Disconnect 18 close immobility timer reset	195
89CIR19	Disconnect 19 close immobility timer reset	196
89CIR20	Disconnect 20 close immobility timer reset	198
89CL01	Disconnect 1 closed	122
89CL02	Disconnect 2 closed	123
89CL03	Disconnect 3 closed	124
89CL04	Disconnect 4 closed	125
89CL05	Disconnect 5 closed	126

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 24 of 69)

Name	Bit Description	Row
89CL06	Disconnect 6 closed	127
89CL07	Disconnect 7 closed	128
89CL08	Disconnect 8 closed	129
89CL09	Disconnect 9 closed	130
89CL10	Disconnect 10 closed	131
89CL11	Disconnect 11 closed	132
89CL12	Disconnect 12 closed	133
89CL13	Disconnect 13 closed	134
89CL14	Disconnect 14 closed	135
89CL15	Disconnect 15 closed	136
89CL16	Disconnect 16 closed	137
89CL17	Disconnect 17 closed	138
89CL18	Disconnect 18 closed	139
89CL19	Disconnect 19 closed	140
89CL20	Disconnect 20 closed	141
89CLB01	Disconnect 1 bus-zone protection	142
89CLB02	Disconnect 2 bus-zone protection	142
89CLB03	Disconnect 3 bus-zone protection	142
89CLB04	Disconnect 4 bus-zone protection	142
89CLB05	Disconnect 5 bus-zone protection	142
89CLB06	Disconnect 6 bus-zone protection	142
89CLB07	Disconnect 7 bus-zone protection	142
89CLB08	Disconnect 8 bus-zone protection	142
89CLB09	Disconnect 9 bus-zone protection	143
89CLB10	Disconnect 10 bus-zone protection	143
89CLB11	Disconnect 11 bus-zone protection	143
89CLB12	Disconnect 12 bus-zone protection	143
89CLB13	Disconnect 13 bus-zone protection	143
89CLB14	Disconnect 14 bus-zone protection	143
89CLB15	Disconnect 15 bus-zone protection	143
89CLB16	Disconnect 16 bus-zone protection	143
89CLB17	Disconnect 17 bus-zone protection	144
89CLB18	Disconnect 18 bus-zone protection	144
89CLB19	Disconnect 19 bus-zone protection	144
89CLB20	Disconnect 20 bus-zone protection	144
89CLS01	Disconnect Close 1 output	145
89CLS02	Disconnect Close 2 output	146
89CLS03	Disconnect Close 3 output	147
89CLS04	Disconnect Close 4 output	148
89CLS05	Disconnect Close 5 output	149
89CLS06	Disconnect Close 6 output	150

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 25 of 69)

Name	Bit Description	Row
89CLS07	Disconnect Close 7 output	151
89CLS08	Disconnect Close 8 output	152
89CLS09	Disconnect Close 9 output	153
89CLS10	Disconnect Close 10 output	154
89CLS11	Disconnect Close 11 output	155
89CLS12	Disconnect Close 12 output	156
89CLS13	Disconnect Close 13 output	157
89CLS14	Disconnect Close 14 output	158
89CLS15	Disconnect Close 15 output	159
89CLS16	Disconnect Close 16 output	160
89CLS17	Disconnect Close 17 output	161
89CLS18	Disconnect Close 18 output	162
89CLS19	Disconnect Close 19 output	163
89CLS20	Disconnect Close 20 output	164
89CRS01	Disconnect 01 close reset	168
89CRS02	Disconnect 02 close reset	170
89CRS03	Disconnect 03 close reset	172
89CRS04	Disconnect 04 close reset	173
89CRS05	Disconnect 05 close reset	175
89CRS06	Disconnect 06 close reset	176
89CRS07	Disconnect 07 close reset	178
89CRS08	Disconnect 08 close reset	179
89CRS09	Disconnect 09 close reset	181
89CRS10	Disconnect 10 close reset	182
89CRS11	Disconnect 11 close reset	184
89CRS12	Disconnect 12 close reset	186
89CRS13	Disconnect 13 close reset	187
89CRS14	Disconnect 14 close reset	189
89CRS15	Disconnect 15 close reset	190
89CRS16	Disconnect 16 close reset	192
89CRS17	Disconnect 17 close reset	193
89CRS18	Disconnect 18 close reset	195
89CRS19	Disconnect 19 close reset	196
89CRS20	Disconnect 20 close reset	198
89CSI01	Disconnect 01 close seal-in timer timed out	168
89CSI02	Disconnect 02 close seal-in timer timed out	170
89CSI03	Disconnect 03 close seal-in timer timed out	171
89CSI04	Disconnect 04 close seal-in timer timed out	173
89CSI05	Disconnect 05 close seal-in timer timed out	174
89CSI06	Disconnect 06 close seal-in timer timed out	176
89CSI07	Disconnect 07 close seal-in timer timed out	177

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 26 of 69)

Name	Bit Description	Row
89CSI08	Disconnect 08 close seal-in timer timed out	179
89CSI09	Disconnect 09 close seal-in timer timed out	180
89CSI10	Disconnect 10 close seal-in timer timed out	182
89CSI11	Disconnect 11 close seal-in timer timed out	183
89CSI12	Disconnect 12 close seal-in timer timed out	185
89CSI13	Disconnect 13 close seal-in timer timed out	187
89CSI14	Disconnect 14 close seal-in timer timed out	188
89CSI15	Disconnect 15 close seal-in timer timed out	190
89CSI16	Disconnect 16 close seal-in timer timed out	191
89CSI17	Disconnect 17 close seal-in timer timed out	193
89CSI18	Disconnect 18 close seal-in timer timed out	194
89CSI19	Disconnect 19 close seal-in timer timed out	196
89CSI20	Disconnect 20 close seal-in timer timed out	197
89OBL01	Disconnect 01 open block	168
89OBL02	Disconnect 02 open block	170
89OBL03	Disconnect 03 open block	172
89OBL04	Disconnect 04 open block	173
89OBL05	Disconnect 05 open block	175
89OBL06	Disconnect 06 open block	176
89OBL07	Disconnect 07 open block	178
89OBL08	Disconnect 08 open block	179
89OBL09	Disconnect 09 open block	181
89OBL10	Disconnect 10 open block	182
89OBL11	Disconnect 11 open block	184
89OBL12	Disconnect 12 open block	186
89OBL13	Disconnect 13 open block	187
89OBL14	Disconnect 14 open block	189
89OBL15	Disconnect 15 open block	190
89OBL16	Disconnect 16 open block	192
89OBL17	Disconnect 17 open block	193
89OBL18	Disconnect 18 open block	195
89OBL19	Disconnect 19 open block	196
89OBL20	Disconnect 20 open block	198
89OC01	ASCII Open Disconnect 1 command	145
89OC02	ASCII Open Disconnect 2 command	146
89OC03	ASCII Open Disconnect 3 command	147
89OC04	ASCII Open Disconnect 4 command	148
89OC05	ASCII Open Disconnect 5 command	149
89OC06	ASCII Open Disconnect 6 command	150
89OC07	ASCII Open Disconnect 7 command	151
89OC08	ASCII Open Disconnect 8 command	152

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 27 of 69)

Name	Bit Description	Row
89OC09	ASCII Open Disconnect 9 command	153
89OC10	ASCII Open Disconnect 10 command	154
89OC11	ASCII Open Disconnect 11 command	155
89OC12	ASCII Open Disconnect 12 command	156
89OC13	ASCII Open Disconnect 13 command	157
89OC14	ASCII Open Disconnect 14 command	158
89OC15	ASCII Open Disconnect 15 command	159
89OC16	ASCII Open Disconnect 16 command	160
89OC17	ASCII Open Disconnect 17 command	161
89OC18	ASCII Open Disconnect 18 command	162
89OC19	ASCII Open Disconnect 19 command	163
89OC20	ASCII Open Disconnect 20 command	164
89OCM01	Mimic Disconnect 1 open control	145
89OCM02	Mimic Disconnect 2 open control	146
89OCM03	Mimic Disconnect 3 open control	147
89OCM04	Mimic Disconnect 4 open control	148
89OCM05	Mimic Disconnect 5 open control	149
89OCM06	Mimic Disconnect 6 open control	150
89OCM07	Mimic Disconnect 7 open control	151
89OCM08	Mimic Disconnect 8 open control	152
89OCM09	Mimic Disconnect 9 open control	153
89OCM10	Mimic Disconnect 10 open control	154
89OCM11	Mimic Disconnect 11 open control	155
89OCM12	Mimic Disconnect 12 open control	156
89OCM13	Mimic Disconnect 13 open control	157
89OCM14	Mimic Disconnect 14 open control	158
89OCM15	Mimic Disconnect 15 open control	159
89OCM16	Mimic Disconnect 16 open control	160
89OCM17	Mimic Disconnect 17 open control	161
89OCM18	Mimic Disconnect 18 open control	162
89OCM19	Mimic Disconnect 19 open control	163
89OCM20	Mimic Disconnect 20 open control	164
89OCN01	Open Disconnect 1	146
89OCN02	Open Disconnect 2	147
89OCN03	Open Disconnect 3	148
89OCN04	Open Disconnect 4	149
89OCN05	Open Disconnect 5	150
89OCN06	Open Disconnect 6	151
89OCN07	Open Disconnect 7	152
89OCN08	Open Disconnect 8	153
89OCN09	Open Disconnect 9	154

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 28 of 69)

Name	Bit Description	Row
89OCN10	Open Disconnect 10	155
89OCN11	Open Disconnect 11	156
89OCN12	Open Disconnect 12	157
89OCN13	Open Disconnect 13	158
89OCN14	Open Disconnect 14	159
89OCN15	Open Disconnect 15	160
89OCN16	Open Disconnect 16	161
89OCN17	Open Disconnect 17	162
89OCN18	Open Disconnect 18	163
89OCN19	Open Disconnect 19	164
89OCN20	Open Disconnect 20	165
89OIM01	Disconnect 01 open immobility timer timed out	169
89OIM02	Disconnect 02 open immobility timer timed out	171
89OIM03	Disconnect 03 open immobility timer timed out	172
89OIM04	Disconnect 04 open immobility timer timed out	174
89OIM05	Disconnect 05 open immobility timer timed out	175
89OIM06	Disconnect 06 open immobility timer timed out	177
89OIM07	Disconnect 07 open immobility timer timed out	178
89OIM08	Disconnect 08 open immobility timer timed out	180
89OIM09	Disconnect 09 open immobility timer timed out	181
89OIM10	Disconnect 10 open immobility timer timed out	183
89OIM11	Disconnect 11 open immobility timer timed out	184
89OIM12	Disconnect 12 open immobility timer timed out	186
89OIM13	Disconnect 13 open immobility timer timed out	188
89OIM14	Disconnect 14 open immobility timer timed out	189
89OIM15	Disconnect 15 open immobility timer timed out	191
89OIM16	Disconnect 16 open immobility timer timed out	192
89OIM17	Disconnect 17 open immobility timer timed out	194
89OIM18	Disconnect 18 open immobility timer timed out	195
89OIM19	Disconnect 19 open immobility timer timed out	197
89OIM20	Disconnect 20 open immobility timer timed out	198
89OIP	Any Disconnect operation in progress	123
89OIP01	Disconnect 1 operation in progress	122
89OIP02	Disconnect 2 operation in progress	123
89OIP03	Disconnect 3 operation in progress	124
89OIP04	Disconnect 4 operation in progress	125
89OIP05	Disconnect 5 operation in progress	126
89OIP06	Disconnect 6 operation in progress	127
89OIP07	Disconnect 7 operation in progress	128
89OIP08	Disconnect 8 operation in progress	129
89OIP09	Disconnect 9 operation in progress	130

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 29 of 69)

Name	Bit Description	Row
89OIP10	Disconnect 10 operation in progress	131
89OIP11	Disconnect 11 operation in progress	132
89OIP12	Disconnect 12 operation in progress	133
89OIP13	Disconnect 13 operation in progress	134
89OIP14	Disconnect 14 operation in progress	135
89OIP15	Disconnect 15 operation in progress	136
89OIP16	Disconnect 16 operation in progress	137
89OIP17	Disconnect 17 operation in progress	138
89OIP18	Disconnect 18 operation in progress	139
89OIP19	Disconnect 19 operation in progress	140
89OIP20	Disconnect 20 operation in progress	141
89OIR01	Disconnect 01 open immobility timer reset	168
89OIR02	Disconnect 02 open immobility timer reset	170
89OIR03	Disconnect 03 open immobility timer reset	171
89OIR04	Disconnect 04 open immobility timer reset	173
89OIR05	Disconnect 05 open immobility timer reset	174
89OIR06	Disconnect 06 open immobility timer reset	176
89OIR07	Disconnect 07 open immobility timer reset	177
89OIR08	Disconnect 08 open immobility timer reset	179
89OIR09	Disconnect 09 open immobility timer reset	180
89OIR10	Disconnect 10 open immobility timer reset	182
89OIR11	Disconnect 11 open immobility timer reset	183
89OIR12	Disconnect 12 open immobility timer reset	185
89OIR13	Disconnect 13 open immobility timer reset	187
89OIR14	Disconnect 14 open immobility timer reset	188
89OIR15	Disconnect 15 open immobility timer reset	190
89OIR16	Disconnect 16 open immobility timer reset	191
89OIR17	Disconnect 17 open immobility timer reset	193
89OIR18	Disconnect 18 open immobility timer reset	194
89OIR19	Disconnect 19 open immobility timer reset	196
89OIR20	Disconnect 20 open immobility timer reset	197
89OPE01	Disconnect Open 1 output	145
89OPE02	Disconnect Open 2 output	146
89OPE03	Disconnect Open 3 output	147
89OPE04	Disconnect Open 4 output	148
89OPE05	Disconnect Open 5 output	149
89OPE06	Disconnect Open 6 output	150
89OPE07	Disconnect Open 7 output	151
89OPE08	Disconnect Open 8 output	152
89OPE09	Disconnect Open 9 output	153
89OPE10	Disconnect Open 10 output	154

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 30 of 69)

Name	Bit Description	Row
89OPE11	Disconnect Open 11 output	155
89OPE12	Disconnect Open 12 output	156
89OPE13	Disconnect Open 13 output	157
89OPE14	Disconnect Open 14 output	158
89OPE15	Disconnect Open 15 output	159
89OPE16	Disconnect Open 16 output	160
89OPE17	Disconnect Open 17 output	161
89OPE18	Disconnect Open 18 output	162
89OPE19	Disconnect Open 19 output	163
89OPE20	Disconnect Open 20 output	164
89OPN01	Disconnect 1 open	122
89OPN02	Disconnect 2 open	123
89OPN03	Disconnect 3 open	124
89OPN04	Disconnect 4 open	125
89OPN05	Disconnect 5 open	126
89OPN06	Disconnect 6 open	127
89OPN07	Disconnect 7 open	128
89OPN08	Disconnect 8 open	129
89OPN09	Disconnect 9 open	130
89OPN10	Disconnect 10 open	131
89OPN11	Disconnect 11 open	132
89OPN12	Disconnect 12 open	133
89OPN13	Disconnect 13 open	134
89OPN14	Disconnect 14 open	135
89OPN15	Disconnect 15 open	136
89OPN16	Disconnect 16 open	137
89OPN17	Disconnect 17 open	138
89OPN18	Disconnect 18 open	139
89OPN19	Disconnect 19 open	140
89OPN20	Disconnect 20 open	141
89ORS01	Disconnect 01 open reset	168
89ORS02	Disconnect 02 open reset	170
89ORS03	Disconnect 03 open reset	172
89ORS04	Disconnect 04 open reset	173
89ORS05	Disconnect 05 open reset	175
89ORS06	Disconnect 06 open reset	176
89ORS07	Disconnect 07 open reset	178
89ORS08	Disconnect 08 open reset	179
89ORS09	Disconnect 09 open reset	181
89ORS10	Disconnect 10 open reset	182
89ORS11	Disconnect 11 open reset	184

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 31 of 69)

Name	Bit Description	Row
89ORS12	Disconnect 12 open reset	186
89ORS13	Disconnect 13 open reset	187
89ORS14	Disconnect 14 open reset	189
89ORS15	Disconnect 15 open reset	190
89ORS16	Disconnect 16 open reset	192
89ORS17	Disconnect 17 open reset	193
89ORS18	Disconnect 18 open reset	195
89ORS19	Disconnect 19 open reset	196
89ORS20	Disconnect 20 open reset	198
89OSI01	Disconnect 01 open seal-in timer timed out	168
89OSI02	Disconnect 02 open seal-in timer timed out	170
89OSI03	Disconnect 03 open seal-in timer timed out	171
89OSI04	Disconnect 04 open seal-in timer timed out	173
89OSI05	Disconnect 05 open seal-in timer timed out	174
89OSI06	Disconnect 06 open seal-in timer timed out	176
89OSI07	Disconnect 07 open seal-in timer timed out	177
89OSI08	Disconnect 08 open seal-in timer timed out	179
89OSI09	Disconnect 09 open seal-in timer timed out	180
89OSI10	Disconnect 10 open seal-in timer timed out	182
89OSI11	Disconnect 11 open seal-in timer timed out	183
89OSI12	Disconnect 12 open seal-in timer timed out	185
89OSI13	Disconnect 13 open seal-in timer timed out	187
89OSI14	Disconnect 14 open seal-in timer timed out	188
89OSI15	Disconnect 15 open seal-in timer timed out	190
89OSI16	Disconnect 16 open seal-in timer timed out	191
89OSI17	Disconnect 17 open seal-in timer timed out	193
89OSI18	Disconnect 18 open seal-in timer timed out	194
89OSI19	Disconnect 19 open seal-in timer timed out	196
89OSI20	Disconnect 20 open seal-in timer timed out	197
ABFITS	Alternate breaker failure, Terminal S	111
ABFITT	Alternate breaker failure, Terminal T	113
ABFITU	Alternate breaker failure, Terminal U	115
ABFITW	Alternate breaker failure, Terminal W	117
ABFITX	Alternate breaker failure, Terminal X	119
ACCESS	A user is logged in at Access Level B or above	346
ACCESSP	Pulsed alarm for logins to Access Level B or above	346
ACN01Q	Automation SELOGIC Counter 01 asserted	336
ACN01R	Automation SELOGIC Counter 01 reset	340
ACN02Q	Automation SELOGIC Counter 02 asserted	336
ACN02R	Automation SELOGIC Counter 02 reset	340
ACN03Q	Automation SELOGIC Counter 03 asserted	336

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 32 of 69)

Name	Bit Description	Row
ACN03R	Automation SELOGIC Counter 03 reset	340
ACN04Q	Automation SELOGIC Counter 04 asserted	336
ACN04R	Automation SELOGIC Counter 04 reset	340
ACN05Q	Automation SELOGIC Counter 05 asserted	336
ACN05R	Automation SELOGIC Counter 05 reset	340
ACN06Q	Automation SELOGIC Counter 06 asserted	336
ACN06R	Automation SELOGIC Counter 06 reset	340
ACN07Q	Automation SELOGIC Counter 07 asserted	336
ACN07R	Automation SELOGIC Counter 07 reset	340
ACN08Q	Automation SELOGIC Counter 08 asserted	336
ACN08R	Automation SELOGIC Counter 08 reset	340
ACN09Q	Automation SELOGIC Counter 09 asserted	337
ACN09R	Automation SELOGIC Counter 09 reset	341
ACN10Q	Automation SELOGIC Counter 10 asserted	337
ACN10R	Automation SELOGIC Counter 10 reset	341
ACN11Q	Automation SELOGIC Counter 11 asserted	337
ACN11R	Automation SELOGIC Counter 11 reset	341
ACN12Q	Automation SELOGIC Counter 12 asserted	337
ACN12R	Automation SELOGIC Counter 12 reset	341
ACN13Q	Automation SELOGIC Counter 13 asserted	337
ACN13R	Automation SELOGIC Counter 13 reset	341
ACN14Q	Automation SELOGIC Counter 14 asserted	337
ACN14R	Automation SELOGIC Counter 14 reset	341
ACN15Q	Automation SELOGIC Counter 15 asserted	337
ACN15R	Automation SELOGIC Counter 15 reset	341
ACN16Q	Automation SELOGIC Counter 16 asserted	337
ACN16R	Automation SELOGIC Counter 16 reset	341
ACN17Q	Automation SELOGIC Counter 17 asserted	338
ACN17R	Automation SELOGIC Counter 17 reset	342
ACN18Q	Automation SELOGIC Counter 18 asserted	338
ACN18R	Automation SELOGIC Counter 18 reset	342
ACN19Q	Automation SELOGIC Counter 19 asserted	338
ACN19R	Automation SELOGIC Counter 19 reset	342
ACN20Q	Automation SELOGIC Counter 20 asserted	338
ACN20R	Automation SELOGIC Counter 20 reset	342
ACN21Q	Automation SELOGIC Counter 21 asserted	338
ACN21R	Automation SELOGIC Counter 21 reset	342
ACN22Q	Automation SELOGIC Counter 22 asserted	338
ACN22R	Automation SELOGIC Counter 22 reset	342
ACN23Q	Automation SELOGIC Counter 23 asserted	338
ACN23R	Automation SELOGIC Counter 23 reset	342

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 33 of 69)

Name	Bit Description	Row
ACN24Q	Automation SELOGIC Counter 24 asserted	338
ACN24R	Automation SELOGIC Counter 24 reset	342
ACN25Q	Automation SELOGIC Counter 25 asserted	339
ACN25R	Automation SELOGIC Counter 25 reset	343
ACN26Q	Automation SELOGIC Counter 26 asserted	339
ACN26R	Automation SELOGIC Counter 26 reset	343
ACN27Q	Automation SELOGIC Counter 27 asserted	339
ACN27R	Automation SELOGIC Counter 27 reset	343
ACN28Q	Automation SELOGIC Counter 28 asserted	339
ACN28R	Automation SELOGIC Counter 28 reset	343
ACN29Q	Automation SELOGIC Counter 29 asserted	339
ACN29R	Automation SELOGIC Counter 29 reset	343
ACN30Q	Automation SELOGIC Counter 30 asserted	339
ACN30R	Automation SELOGIC Counter 30 reset	343
ACN31Q	Automation SELOGIC Counter 31 asserted	339
ACN31R	Automation SELOGIC Counter 31 reset	343
ACN32Q	Automation SELOGIC Counter 32 asserted	339
ACN32R	Automation SELOGIC Counter 32 reset	343
ACT01Q	Automation SELOGIC Conditioning Timer 01 asserted	548
ACT02Q	Automation SELOGIC Conditioning Timer 02 asserted	548
ACT03Q	Automation SELOGIC Conditioning Timer 03 asserted	548
ACT04Q	Automation SELOGIC Conditioning Timer 04 asserted	548
ACT05Q	Automation SELOGIC Conditioning Timer 05 asserted	548
ACT06Q	Automation SELOGIC Conditioning Timer 06 asserted	548
ACT07Q	Automation SELOGIC Conditioning Timer 07 asserted	548
ACT08Q	Automation SELOGIC Conditioning Timer 08 asserted	548
ACT09Q	Automation SELOGIC Conditioning Timer 09 asserted	549
ACT10Q	Automation SELOGIC Conditioning Timer 10 asserted	549
ACT11Q	Automation SELOGIC Conditioning Timer 11 asserted	549
ACT12Q	Automation SELOGIC Conditioning Timer 12 asserted	549
ACT13Q	Automation SELOGIC Conditioning Timer 13 asserted	549
ACT14Q	Automation SELOGIC Conditioning Timer 14 asserted	549
ACT15Q	Automation SELOGIC Conditioning Timer 15 asserted	549
ACT16Q	Automation SELOGIC Conditioning Timer 16 asserted	549
ACT17Q	Automation SELOGIC Conditioning Timer 17 asserted	550
ACT18Q	Automation SELOGIC Conditioning Timer 18 asserted	550
ACT19Q	Automation SELOGIC Conditioning Timer 19 asserted	550
ACT20Q	Automation SELOGIC Conditioning Timer 20 asserted	550
ACT21Q	Automation SELOGIC Conditioning Timer 21 asserted	550
ACT22Q	Automation SELOGIC Conditioning Timer 22 asserted	550
ACT23Q	Automation SELOGIC Conditioning Timer 23 asserted	550

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 34 of 69)

Name	Bit Description	Row
ACT24Q	Automation SELOGIC Conditioning Timer 24 asserted	550
ACT25Q	Automation SELOGIC Conditioning Timer 25 asserted	551
ACT26Q	Automation SELOGIC Conditioning Timer 26 asserted	551
ACT27Q	Automation SELOGIC Conditioning Timer 27 asserted	551
ACT28Q	Automation SELOGIC Conditioning Timer 28 asserted	551
ACT29Q	Automation SELOGIC Conditioning Timer 29 asserted	551
ACT30Q	Automation SELOGIC Conditioning Timer 30 asserted	551
ACT31Q	Automation SELOGIC Conditioning Timer 31 asserted	551
ACT32Q	Automation SELOGIC Conditioning Timer 32 asserted	551
AFRTEXA	Automation SELOGIC control equation first execution after Automation settings change	344
AFRTEXP	Automation SELOGIC control equation first execution after Protection settings change	344
ALT01	Automation SELOGIC Latch 01 asserted	324
ALT02	Automation SELOGIC Latch 02 asserted	324
ALT03	Automation SELOGIC Latch 03 asserted	324
ALT04	Automation SELOGIC Latch 04 asserted	324
ALT05	Automation SELOGIC Latch 05 asserted	324
ALT06	Automation SELOGIC Latch 06 asserted	324
ALT07	Automation SELOGIC Latch 07 asserted	324
ALT08	Automation SELOGIC Latch 08 asserted	324
ALT09	Automation SELOGIC Latch 09 asserted	325
ALT10	Automation SELOGIC Latch 10 asserted	325
ALT11	Automation SELOGIC Latch 11 asserted	325
ALT12	Automation SELOGIC Latch 12 asserted	325
ALT13	Automation SELOGIC Latch 13 asserted	325
ALT14	Automation SELOGIC Latch 14 asserted	325
ALT15	Automation SELOGIC Latch 15 asserted	325
ALT16	Automation SELOGIC Latch 16 asserted	325
ALT17	Automation SELOGIC Latch 17 asserted	326
ALT18	Automation SELOGIC Latch 18 asserted	326
ALT19	Automation SELOGIC Latch 19 asserted	326
ALT20	Automation SELOGIC Latch 20 asserted	326
ALT21	Automation SELOGIC Latch 21 asserted	326
ALT22	Automation SELOGIC Latch 22 asserted	326
ALT23	Automation SELOGIC Latch 23 asserted	326
ALT24	Automation SELOGIC Latch 24 asserted	326
ALT25	Automation SELOGIC Latch 25 asserted	327
ALT26	Automation SELOGIC Latch 26 asserted	327
ALT27	Automation SELOGIC Latch 27 asserted	327
ALT28	Automation SELOGIC Latch 28 asserted	327
ALT29	Automation SELOGIC Latch 29 asserted	327
ALT30	Automation SELOGIC Latch 30 asserted	327

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 35 of 69)

Name	Bit Description	Row
ALT31	Automation SELOGIC Latch 31 asserted	327
ALT32	Automation SELOGIC Latch 32 asserted	327
ALTPS1	Breaker S Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	537
ALTPT1	Breaker T Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	537
ALTPU1	Breaker U Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	537
ALTPW1	Breaker W Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	537
ALTPX1	Breaker X Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	537
ALTPS2	Breaker S Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	538
ALTPT2	Breaker T Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	538
ALTPU2	Breaker U Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	538
ALTPW2	Breaker W Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	538
ALTPX2	Breaker X Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	538
ALTSS	Breaker S alternate synchronizing voltage source selected (SELOGIC control equation)	450
ALTST	Breaker T alternate synchronizing voltage source selected (SELOGIC control equation)	450
ALTSU	Breaker U alternate synchronizing voltage source selected (SELOGIC control equation)	450
ALTSW	Breaker W alternate synchronizing voltage source selected (SELOGIC control equation)	451
ALTSX	Breaker X alternate synchronizing voltage source selected (SELOGIC control equation)	451
AMB_F	Ambient temperature fault condition	213
ANOKA	Analog transfer on MIRRORED BITS Channel A	376
ANOKB	Analog transfer on MIRRORED BITS Channel B	377
AST01Q	Automation SELOGIC Sequencing Timer 01 asserted	328
AST01R	Automation SELOGIC Sequencing Timer 01 reset	332
AST02Q	Automation SELOGIC Sequencing Timer 02 asserted	328
AST02R	Automation SELOGIC Sequencing Timer 02 reset	332
AST03Q	Automation SELOGIC Sequencing Timer 03 asserted	328
AST03R	Automation SELOGIC Sequencing Timer 03 reset	332
AST04Q	Automation SELOGIC Sequencing Timer 04 asserted	328
AST04R	Automation SELOGIC Sequencing Timer 04 reset	332
AST05Q	Automation SELOGIC Sequencing Timer 05 asserted	328
AST05R	Automation SELOGIC Sequencing Timer 05 reset	332
AST06Q	Automation SELOGIC Sequencing Timer 06 asserted	328
AST06R	Automation SELOGIC Sequencing Timer 06 reset	332
AST07Q	Automation SELOGIC Sequencing Timer 07 asserted	328
AST07R	Automation SELOGIC Sequencing Timer 07 reset	332
AST08Q	Automation SELOGIC Sequencing Timer 08 asserted	328
AST08R	Automation SELOGIC Sequencing Timer 08 reset	332
AST09Q	Automation SELOGIC Sequencing Timer 09 asserted	329
AST09R	Automation SELOGIC Sequencing Timer 09 reset	333
AST10Q	Automation SELOGIC Sequencing Timer 10 asserted	329
AST10R	Automation SELOGIC Sequencing Timer 10 reset	333
AST11Q	Automation SELOGIC Sequencing Timer 11 asserted	329

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 36 of 69)

Name	Bit Description	Row
AST11R	Automation SELOGIC Sequencing Timer 11 reset	333
AST12Q	Automation SELOGIC Sequencing Timer 12 asserted	329
AST12R	Automation SELOGIC Sequencing Timer 12 reset	333
AST13Q	Automation SELOGIC Sequencing Timer 13 asserted	329
AST13R	Automation SELOGIC Sequencing Timer 13 reset	333
AST14Q	Automation SELOGIC Sequencing Timer 14 asserted	329
AST14R	Automation SELOGIC Sequencing Timer 14 reset	333
AST15Q	Automation SELOGIC Sequencing Timer 15 asserted	329
AST15R	Automation SELOGIC Sequencing Timer 15 reset	333
AST16Q	Automation SELOGIC Sequencing Timer 16 asserted	329
AST16R	Automation SELOGIC Sequencing Timer 16 reset	333
AST17Q	Automation SELOGIC Sequencing Timer 17 asserted	330
AST17R	Automation SELOGIC Sequencing Timer 17 reset	334
AST18Q	Automation SELOGIC Sequencing Timer 18 asserted	330
AST18R	Automation SELOGIC Sequencing Timer 18 reset	334
AST19Q	Automation SELOGIC Sequencing Timer 19 asserted	330
AST19R	Automation SELOGIC Sequencing Timer 19 reset	334
AST20Q	Automation SELOGIC Sequencing Timer 20 asserted	330
AST20R	Automation SELOGIC Sequencing Timer 20 reset	334
AST21Q	Automation SELOGIC Sequencing Timer 21 asserted	330
AST21R	Automation SELOGIC Sequencing Timer 21 reset	334
AST22Q	Automation SELOGIC Sequencing Timer 22 asserted	330
AST22R	Automation SELOGIC Sequencing Timer 22 reset	334
AST23Q	Automation SELOGIC Sequencing Timer 23 asserted	330
AST23R	Automation SELOGIC Sequencing Timer 23 reset	334
AST24Q	Automation SELOGIC Sequencing Timer 24 asserted	330
AST24R	Automation SELOGIC Sequencing Timer 24 reset	334
AST25Q	Automation SELOGIC Sequencing Timer 25 asserted	331
AST25R	Automation SELOGIC Sequencing Timer 25 reset	335
AST26Q	Automation SELOGIC Sequencing Timer 26 asserted	331
AST26R	Automation SELOGIC Sequencing Timer 26 reset	335
AST27Q	Automation SELOGIC Sequencing Timer 27 asserted	331
AST27R	Automation SELOGIC Sequencing Timer 27 reset	335
AST28Q	Automation SELOGIC Sequencing Timer 28 asserted	331
AST28R	Automation SELOGIC Sequencing Timer 28 reset	335
AST29Q	Automation SELOGIC Sequencing Timer 29 asserted	331
AST29R	Automation SELOGIC Sequencing Timer 29 reset	335
AST30Q	Automation SELOGIC Sequencing Timer 30 asserted	331
AST30R	Automation SELOGIC Sequencing Timer 30 reset	335
AST31Q	Automation SELOGIC Sequencing Timer 31 asserted	331
AST31R	Automation SELOGIC Sequencing Timer 31 reset	335

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 37 of 69)

Name	Bit Description	Row
AST32Q	Automation SELOGIC Sequencing Timer 32 asserted	331
AST32R	Automation SELOGIC Sequencing Timer 32 reset	335
ASV001–ASV008	Automation SELOGIC Variable 001–Variable 008 asserted	292
ASV009–ASV016	Automation SELOGIC Variable 009–Variable 016 asserted	293
ASV017–ASV024	Automation SELOGIC Variable 017–Variable 024 asserted	294
ASV025–ASV032	Automation SELOGIC Variable 025–Variable 032 asserted	295
ASV033–ASV040	Automation SELOGIC Variable 033–Variable 040 asserted	296
ASV041–ASV048	Automation SELOGIC Variable 041–Variable 048 asserted	297
ASV049–ASV056	Automation SELOGIC Variable 049–Variable 056 asserted	298
ASV057–ASV064	Automation SELOGIC Variable 057–Variable 064 asserted	299
ASV065–ASV072	Automation SELOGIC Variable 065–Variable 072 asserted	300
ASV073–ASV080	Automation SELOGIC Variable 073–Variable 080 asserted	301
ASV081–ASV088	Automation SELOGIC Variable 081–Variable 088 asserted	302
ASV089–ASV096	Automation SELOGIC Variable 089–Variable 096 asserted	303
ASV097–ASV104	Automation SELOGIC Variable 097–Variable 104 asserted	304
ASV105–ASV112	Automation SELOGIC Variable 105–Variable 112 asserted	305
ASV113–ASV120	Automation SELOGIC Variable 113–Variable 120 asserted	306
ASV121–ASV128	Automation SELOGIC Variable 121–Variable 128 asserted	307
ASV129–ASV136	Automation SELOGIC Variable 129–Variable 136 asserted	308
ASV137–ASV144	Automation SELOGIC Variable 137–Variable 144 asserted	309
ASV145–ASV152	Automation SELOGIC Variable 145–Variable 152 asserted	310
ASV153–ASV160	Automation SELOGIC Variable 153–Variable 160 asserted	311
ASV161–ASV168	Automation SELOGIC Variable 161–Variable 168 asserted	312
ASV169–ASV176	Automation SELOGIC Variable 169–Variable 176 asserted	313
ASV177–ASV184	Automation SELOGIC Variable 177–Variable 184 asserted	314

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 38 of 69)

Name	Bit Description	Row
ASV185–ASV192	Automation SELOGIC Variable 185–Variable 192 asserted	315
ASV193–ASV200	Automation SELOGIC Variable 193–Variable 200 asserted	316
ASV201–ASV208	Automation SELOGIC Variable 201–Variable 208 asserted	317
ASV209–ASV216	Automation SELOGIC Variable 209–Variable 216 asserted	318
ASV217–ASV224	Automation SELOGIC Variable 217–Variable 224 asserted	319
ASV225–ASV232	Automation SELOGIC Variable 225–Variable 232 asserted	320
ASV233–ASV240	Automation SELOGIC Variable 233–Variable 240 asserted	321
ASV241–ASV248	Automation SELOGIC Variable 241–Variable 248 asserted	322
ASV249–ASV256	Automation SELOGIC Variable 249–Variable 256 asserted	323
ATBFIS	Alternate breaker failure initiated, Terminal S	110
ATBFIT	Alternate breaker failure initiated, Terminal T	112
ATBFIU	Alternate breaker failure initiated, Terminal U	114
ATBFIW	Alternate breaker failure initiated, Terminal W	116
ATBFIX	Alternate breaker failure initiated, Terminal X	118
ATBFTS	Alternate breaker failure timer timed out, Terminal S	110
ATBFTT	Alternate breaker failure timer timed out, Terminal T	112
ATBFTU	Alternate breaker failure timer timed out, Terminal U	114
ATBFTW	Alternate breaker failure timer timed out, Terminal W	116
ATBFTX	Alternate breaker failure timer timed out, Terminal X	118
AUNRLBL	Automation SELOGIC control equation unresolved label	344
BADPASS	Invalid password attempt alarm	345
BFIS	Breaker failure initiated, Terminal S	110
BFISPTS	Breaker failure seal-in timer timed out, Terminal S	111
BFISPTT	Breaker failure seal-in timer timed out, Terminal T	113
BFISPTU	Breaker failure seal-in timer timed out, Terminal U	115
BFISPTW	Breaker failure seal-in timer timed out, Terminal W	117
BFISPTX	Breaker failure seal-in timer timed out, Terminal X	119
BFIT	Breaker failure initiated, Terminal T	112
BFITS	Breaker failure timer timed out, Terminal S	110
BFITT	Breaker failure timer timed out, Terminal T	112
BFITU	Breaker failure timer timed out, Terminal U	114
BFITW	Breaker failure timer timed out, Terminal W	116
BFITX	Breaker failure timer timed out, Terminal X	118
BFIU	Breaker failure initiated, Terminal U	114
BFIW	Breaker failure initiated, Terminal W	116

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 39 of 69)

Name	Bit Description	Row
BFIX	Breaker failure initiated, Terminal X	118
BLKLPTS	Block low-priority source from updating relay time	350
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	464
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	464
BNC_RST	Disqualify BNC IRIG-B high-accuracy time source	464
BNC_SET	Qualify BNC IRIG-B high-accuracy time source	464
BNC_TIM	A valid IRIG-B time source is detected on BNC port	465
BNCSYNC	Synchronized to high-quality BNC IRIG source	465
BRKENAB	Breaker Control Enable Jumper is installed	346
BSBCWAL	Breaker contact wear alarm, Breaker S	200
BSBITAL	Inactivity time alarm, Breaker S	200
BSESOAL	Slow electrical operate alarm, Breaker S	200
BSKAIAL	Interrupted rms current alarm, Breaker S	200
BSMRTAL	Motor run time alarm, Breaker S	200
BSMSOAL	Mechanical slow operation alarm, Breaker S	200
BSYNBKS	Breaker S synchronism check blocked	452
BSYNBKT	Breaker T synchronism check blocked	452
BSYNBKU	Breaker U synchronism check blocked	452
BSYNBKW	Breaker W synchronism check blocked	452
BSYNBKX	Breaker X synchronism check blocked	452
BTBCWAL	Breaker contact wear alarm, Breaker T	201
BTBITAL	Inactivity time alarm, Breaker T	201
BTESOAL	Slow electrical operation alarm, Breaker T	201
BTKAIAL	Interrupted rms current alarm, Breaker T	201
BTMRTAL	Motor run time alarm, Breaker T	201
BTMSOAL	Mechanical slow operation alarm, Breaker T	201
BUBCWAL	Breaker contact wear alarm, Breaker U	202
BUBITAL	Inactivity time alarm, Breaker U	202
BUESOAL	Slow electrical operation alarm, Breaker U	202
BUKAIAL	Interrupted rms current alarm, Breaker U	202
BUMRTAL	Motor run time alarm, Breaker U	202
BUMSOAL	Mechanical slow operation alarm, Breaker U	202
BWBCWAL	Breaker contact wear alarm, Breaker W	203
BWBITAL	Inactivity time alarm, Breaker W	203
BWESOAL	Slow electrical operation alarm, Breaker W	203
BWKAIAL	Interrupted rms current alarm, Breaker W	203
BWMRTAL	Motor run time alarm, Breaker W	203
BWMSOAL	Mechanical slow operation alarm, Breaker W	203
BXBCWAL	Breaker contact wear alarm, Breaker X	204
BXBITAL	Inactivity time alarm, Breaker X	204
BXESOAL	Slow electrical operation alarm, Breaker X	204

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 40 of 69)

Name	Bit Description	Row
BXKAIAL	Interrupted rms current alarm, Breaker X	204
BXMRTAL	Motor run time alarm, Breaker X	204
BXMSOAL	Mechanical slow operation alarm, Breaker X	204
CBADA	Unavailability threshold exceeded for normal MIRRORED BITS communication, Channel A	376
CBADB	Unavailability threshold exceeded for normal MIRRORED BITS communication, Channel B	377
CCS	Breaker close command, Terminal S	224
CCT	Breaker close command, Terminal T	224
CCU	Breaker close command, Terminal U	224
CCW	Breaker close command, Terminal W	224
CCX	Breaker close command, Terminal X	225
CHSG	Settings group changed	244
CLS	Close breaker Terminal S equation	103
CLSS	Close breaker Terminal S output	104
CLST	Close breaker Terminal T output	104
CLSU	Close breaker Terminal U output	104
CLSW	Close breaker Terminal W output	104
CLSX	Close breaker Terminal X output	104
CLT	Close breaker Terminal T equation	103
CLU	Close breaker Terminal U equation	103
CLW	Close breaker Terminal W equation	103
CLX	Close breaker Terminal X equation	103
CON	External fault detected	5
CONA	External fault detected, A-Phase	5
CONB	External fault detected, B-Phase	5
CONC	External fault detected, C-Phase	5
CSALRM	Cooling stage determination alarm	210
CSCM	Cooling coefficient or measurement alarm	209
CSCM_1	Transformer 1, cooling coefficient or measurement alarm	209
CSCM_2	Transformer 2, cooling coefficient or measurement alarm	209
CSCM_3	Transformer 3, cooling coefficient or measurement alarm	209
CSE	Cooling stage efficiency alarm	209
CSE_1	Transformer 1, cooling stage efficiency alarm	209
CSE_2	Transformer 2, cooling stage efficiency alarm	209
CSE_3	Transformer 3, cooling stage efficiency alarm	209
CTUA	Current transformer in unsaturated state following an external fault, A-Phase	12
CTUB	Current transformer in unsaturated state following an external fault, B-Phase	12
CTUC	Current transformer in unsaturated state following an external fault, C-Phase	12
DC1F	DC Channel 1 failed	220
DC1G	DC Channel 1 ground fault detected	220
DC1R	DC Channel 1 excess ripples detected	220
DC1W	DC Channel 1 warning	220

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 41 of 69)

Name	Bit Description	Row
DIRBLK1	Block Phase And Ground Directional Element ST	528
DIRBLK2	Block Phase And Ground Directional Element TU	528
DIRBLK3	Block Phase And Ground Directional Element UW	528
DIRBLK4	Block Phase And Ground Directional Element WX	528
DIRBLKS	Block Phase And Ground Directional Element S	75
DIRBLKT	Block Phase And Ground Directional Element T	75
DIRBLKU	Block Phase And Ground Directional Element U	75
DIRBLKW	Block Phase And Ground Directional Element W	75
DIRBLKX	Block Phase And Ground Directional Element X	75
DMP01	Demand Metering Element 01 asserted	221
DMP02	Demand Metering Element 02 asserted	221
DMP03	Demand Metering Element 03 asserted	221
DMP04	Demand Metering Element 04 asserted	221
DMP05	Demand Metering Element 05 asserted	222
DMP06	Demand Metering Element 06 asserted	222
DMP07	Demand Metering Element 07 asserted	222
DMP08	Demand Metering Element 08 asserted	222
DMP09	Demand Metering Element 09 asserted	223
DMP10	Demand Metering Element 10 asserted	223
DOKA	MIRRORED BITS Channel A in normal mode	376
DOKB	MIRRORED BITS Channel B in normal mode	377
DST	Daylight-saving time	422
DSTP	IRIG-B daylight-saving time pending	422
E32OP01	Overpower Element 01 enabled	84
E32OP02	Overpower Element 02 enabled	84
E32OP03	Overpower Element 03 enabled	85
E32OP04	Overpower Element 04 enabled	85
E32OP05	Overpower Element 05 enabled	86
E32OP06	Overpower Element 06 enabled	86
E32OP07	Overpower Element 07 enabled	87
E32OP08	Overpower Element 08 enabled	87
E32OP09	Overpower Element 09 enabled	88
E32OP10	Overpower Element 10 enabled	88
E32UP01	Underpower Element 01 enabled	89
E32UP02	Underpower Element 02 enabled	89
E32UP03	Underpower Element 03 enabled	90
E32UP04	Underpower Element 04 enabled	90
E32UP05	Underpower Element 05 enabled	91
E32UP06	Underpower Element 06 enabled	91
E32UP07	Underpower Element 07 enabled	92
E32UP08	Underpower Element 08 enabled	92

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 42 of 69)

Name	Bit Description	Row
E32UP09	Underpower Element 09 enabled	93
E32UP10	Underpower Element 10 enabled	93
E87TS	Terminal S currents included in differential zone	4
E87TT	Terminal T currents included in differential zone	4
E87TU	Terminal U currents included in differential zone	4
E87TW	Terminal W currents included in differential zone	4
E87TX	Terminal X currents included in differential zone	4
EAFSRC	Alternate frequency source (SELOGIC control equation)	348
EBFITS	Externally initiated breaker failure timer timed out, Terminal S	110
EBFITT	Externally initiated breaker failure timer timed out, Terminal T	112
EBFITU	Externally initiated breaker failure timer timed out, Terminal U	114
EBFITW	Externally initiated breaker failure timer timed out, Terminal W	116
EBFITX	Externally initiated breaker failure timer timed out, Terminal X	118
EBSMON	Breaker monitoring Terminal S enabled	200
EBTMON	Breaker monitoring Terminal T enabled	201
EBUMON	Breaker monitoring Terminal U enabled	202
EBWMON	Breaker monitoring Terminal W enabled	203
EBXMON	Breaker monitoring Terminal X enabled	204
EDM01	Demand Metering Element 01 enabled	221
EDM02	Demand Metering Element 02 enabled	221
EDM03	Demand Metering Element 03 enabled	221
EDM04	Demand Metering Element 04 enabled	221
EDM05	Demand Metering Element 05 enabled	222
EDM06	Demand Metering Element 06 enabled	222
EDM07	Demand Metering Element 07 enabled	222
EDM08	Demand Metering Element 08 enabled	222
EDM09	Demand Metering Element 09 enabled	223
EDM10	Demand Metering Element 10 enabled	223
EFDTA	EFD extension timer output, A-Phase	75
EFDTB	EFD extension timer output, B-Phase	75
EFDTC	EFD extension timer output, C-Phase	75
EN	Enable LED on relay front panel	0
ENINBFS	Neutral/residual breaker failure function enabled, Terminal S	111
ENINBFT	Neutral/residual breaker failure function enabled, Terminal T	113
ENINBFU	Neutral/residual breaker failure function enabled, Terminal U	115
ENINBFW	Neutral/residual breaker failure function enabled, Terminal W	117
ENINBFX	Neutral/residual breaker failure function enabled, Terminal X	119
ER	Event report triggered	370
ETHRFLT	Through-fault element enabled	219
EVELOCK	Lock DNP events	427
EXBFS	External breaker failure input initiated, Terminal S	110

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 43 of 69)

Name	Bit Description	Row
EXBFT	External breaker failure input initiated, Terminal T	112
EXBFU	External breaker failure input initiated, Terminal U	114
EXBFW	External breaker failure input initiated, Terminal W	116
EXBFX	External breaker failure input initiated, Terminal X	118
FAA1	Aging insulation acceleration factor alarm, Level 1	207
FAA1_1	Transformer 1, aging insulation acceleration factor alarm, Level 1	207
FAA1_2	Transformer 1, aging insulation acceleration factor alarm, Level 2	207
FAA2	Aging insulation acceleration factor alarm, Level 2	207
FAA2_1	Transformer 2, aging insulation acceleration factor alarm, Level 1	207
FAA2_2	Transformer 2, aging insulation acceleration factor alarm, Level 2	207
FAA3_1	Transformer 3, aging insulation acceleration factor alarm, Level 1	207
FAA3_2	Transformer 3, aging insulation acceleration factor alarm, Level 2	207
FASTS	Breaker S synchronizing voltage slipping faster than polarizing voltage	444
FASTT	Breaker T synchronizing voltage slipping faster than polarizing voltage	444
FASTU	Breaker U synchronizing voltage slipping faster than polarizing voltage	444
FASTW	Breaker W synchronizing voltage slipping faster than polarizing voltage	444
FASTX	Breaker X synchronizing voltage slipping faster than polarizing voltage	444
FAULT	Fault detected	370
FBFS	Breaker failure asserted/initiated, Terminal S	111
FBFT	Breaker failure asserted/initiated, Terminal T	113
FBFU	Breaker failure asserted/initiated, Terminal U	115
FBFW	Breaker failure asserted/initiated, Terminal W	117
FBFX	Breaker failure asserted/initiated, Terminal X	119
FIDEN_S	FIDEN logic enabled, Terminal S	457
FIDEN_T	FIDEN logic enabled, Terminal T	457
FIDEN_U	FIDEN logic enabled, Terminal U	457
FIDEN_W	FIDEN logic enabled, Terminal W	457
FIDEN_X	FIDEN logic enabled, Terminal X	457
FOP1_01	Port 1 Fast Operate Transmit Bit 1	432
FOP1_02	Port 1 Fast Operate Transmit Bit 2	432
FOP1_03	Port 1 Fast Operate Transmit Bit 3	432
FOP1_04	Port 1 Fast Operate Transmit Bit 4	432
FOP1_05	Port 1 Fast Operate Transmit Bit 5	432
FOP1_06	Port 1 Fast Operate Transmit Bit 6	432
FOP1_07	Port 1 Fast Operate Transmit Bit 7	432
FOP1_08	Port 1 Fast Operate Transmit Bit 8	432
FOP1_09	Port 1 Fast Operate Transmit Bit 9	433
FOP1_10	Port 1 Fast Operate Transmit Bit 10	433
FOP1_11	Port 1 Fast Operate Transmit Bit 11	433
FOP1_12	Port 1 Fast Operate Transmit Bit 12	433
FOP1_13	Port 1 Fast Operate Transmit Bit 13	433

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 44 of 69)

Name	Bit Description	Row
FOP1_14	Port 1 Fast Operate Transmit Bit 14	433
FOP1_15	Port 1 Fast Operate Transmit Bit 15	433
FOP1_16	Port 1 Fast Operate Transmit Bit 16	433
FOP1_17	Port 1 Fast Operate Transmit Bit 17	434
FOP1_18	Port 1 Fast Operate Transmit Bit 18	434
FOP1_19	Port 1 Fast Operate Transmit Bit 19	434
FOP1_20	Port 1 Fast Operate Transmit Bit 20	434
FOP1_21	Port 1 Fast Operate Transmit Bit 21	434
FOP1_22	Port 1 Fast Operate Transmit Bit 22	434
FOP1_23	Port 1 Fast Operate Transmit Bit 23	434
FOP1_24	Port 1 Fast Operate Transmit Bit 24	434
FOP1_25	Port 1 Fast Operate Transmit Bit 25	435
FOP1_26	Port 1 Fast Operate Transmit Bit 26	435
FOP1_27	Port 1 Fast Operate Transmit Bit 27	435
FOP1_28	Port 1 Fast Operate Transmit Bit 28	435
FOP1_29	Port 1 Fast Operate Transmit Bit 29	435
FOP1_30	Port 1 Fast Operate Transmit Bit 30	435
FOP1_31	Port 1 Fast Operate Transmit Bit 31	435
FOP1_32	Port 1 Fast Operate Transmit Bit 32	435
FOP2_01	Port 2 Fast Operate Transmit Bit 1	436
FOP2_02	Port 2 Fast Operate Transmit Bit 2	436
FOP2_03	Port 2 Fast Operate Transmit Bit 3	436
FOP2_04	Port 2 Fast Operate Transmit Bit 4	436
FOP2_05	Port 2 Fast Operate Transmit Bit 5	436
FOP2_06	Port 2 Fast Operate Transmit Bit 6	436
FOP2_07	Port 2 Fast Operate Transmit Bit 7	436
FOP2_08	Port 2 Fast Operate Transmit Bit 8	436
FOP2_09	Port 2 Fast Operate Transmit Bit 9	437
FOP2_10	Port 2 Fast Operate Transmit Bit 10	437
FOP2_11	Port 2 Fast Operate Transmit Bit 11	437
FOP2_12	Port 2 Fast Operate Transmit Bit 12	437
FOP2_13	Port 2 Fast Operate Transmit Bit 13	437
FOP2_14	Port 2 Fast Operate Transmit Bit 14	437
FOP2_15	Port 2 Fast Operate Transmit Bit 15	437
FOP2_16	Port 2 Fast Operate Transmit Bit 16	437
FOP2_17	Port 2 Fast Operate Transmit Bit 17	438
FOP2_18	Port 2 Fast Operate Transmit Bit 18	438
FOP2_19	Port 2 Fast Operate Transmit Bit 19	438
FOP2_20	Port 2 Fast Operate Transmit Bit 20	438
FOP2_21	Port 2 Fast Operate Transmit Bit 21	438
FOP2_22	Port 2 Fast Operate Transmit Bit 22	438

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 45 of 69)

Name	Bit Description	Row
FOP2_23	Port 2 Fast Operate Transmit Bit 23	438
FOP2_24	Port 2 Fast Operate Transmit Bit 24	438
FOP2_25	Port 2 Fast Operate Transmit Bit 25	439
FOP2_26	Port 2 Fast Operate Transmit Bit 26	439
FOP2_27	Port 2 Fast Operate Transmit Bit 27	439
FOP2_28	Port 2 Fast Operate Transmit Bit 28	439
FOP2_29	Port 2 Fast Operate Transmit Bit 29	439
FOP2_30	Port 2 Fast Operate Transmit Bit 30	439
FOP2_31	Port 2 Fast Operate Transmit Bit 31	439
FOP2_32	Port 2 Fast Operate Transmit Bit 32	439
FOP3_01	Port 3 Fast Operate Transmit Bit 1	440
FOP3_02	Port 3 Fast Operate Transmit Bit 2	440
FOP3_03	Port 3 Fast Operate Transmit Bit 3	440
FOP3_04	Port 3 Fast Operate Transmit Bit 4	440
FOP3_05	Port 3 Fast Operate Transmit Bit 5	440
FOP3_06	Port 3 Fast Operate Transmit Bit 6	440
FOP3_07	Port 3 Fast Operate Transmit Bit 7	440
FOP3_08	Port 3 Fast Operate Transmit Bit 8	440
FOP3_09	Port 3 Fast Operate Transmit Bit 9	441
FOP3_10	Port 3 Fast Operate Transmit Bit 10	441
FOP3_11	Port 3 Fast Operate Transmit Bit 11	441
FOP3_12	Port 3 Fast Operate Transmit Bit 12	441
FOP3_13	Port 3 Fast Operate Transmit Bit 13	441
FOP3_14	Port 3 Fast Operate Transmit Bit 14	441
FOP3_15	Port 3 Fast Operate Transmit Bit 15	441
FOP3_16	Port 3 Fast Operate Transmit Bit 16	441
FOP3_17	Port 3 Fast Operate Transmit Bit 17	442
FOP3_18	Port 3 Fast Operate Transmit Bit 18	442
FOP3_19	Port 3 Fast Operate Transmit Bit 19	442
FOP3_20	Port 3 Fast Operate Transmit Bit 20	442
FOP3_21	Port 3 Fast Operate Transmit Bit 21	442
FOP3_22	Port 3 Fast Operate Transmit Bit 22	442
FOP3_23	Port 3 Fast Operate Transmit Bit 23	442
FOP3_24	Port 3 Fast Operate Transmit Bit 24	442
FOP3_25	Port 3 Fast Operate Transmit Bit 25	443
FOP3_26	Port 3 Fast Operate Transmit Bit 26	443
FOP3_27	Port 3 Fast Operate Transmit Bit 27	443
FOP3_28	Port 3 Fast Operate Transmit Bit 28	443
FOP3_29	Port 3 Fast Operate Transmit Bit 29	443
FOP3_30	Port 3 Fast Operate Transmit Bit 30	443
FOP3_31	Port 3 Fast Operate Transmit Bit 31	443

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 46 of 69)

Name	Bit Description	Row
FOP3_32	Port 3 Fast Operate Transmit Bit 32	443
FOPF_01	Port F (front-panel) Fast Operate Transmit Bit 1	428
FOPF_02	Port F (front-panel) Fast Operate Transmit Bit 2	428
FOPF_03	Port F (front-panel) Fast Operate Transmit Bit 3	428
FOPF_04	Port F (front-panel) Fast Operate Transmit Bit 4	428
FOPF_05	Port F (front-panel) Fast Operate Transmit Bit 5	428
FOPF_06	Port F (front-panel) Fast Operate Transmit Bit 6	428
FOPF_07	Port F (front-panel) Fast Operate Transmit Bit 7	428
FOPF_08	Port F (front-panel) Fast Operate Transmit Bit 8	428
FOPF_09	Port F (front-panel) Fast Operate Transmit Bit 9	429
FOPF_10	Port F (front-panel) Fast Operate Transmit Bit 10	429
FOPF_11	Port F (front-panel) Fast Operate Transmit Bit 11	429
FOPF_12	Port F (front-panel) Fast Operate Transmit Bit 12	429
FOPF_13	Port F (front-panel) Fast Operate Transmit Bit 13	429
FOPF_14	Port F (front-panel) Fast Operate Transmit Bit 14	429
FOPF_15	Port F (front-panel) Fast Operate Transmit Bit 15	429
FOPF_16	Port F (front-panel) Fast Operate Transmit Bit 16	429
FOPF_17	Port F (front-panel) Fast Operate Transmit Bit 17	430
FOPF_18	Port F (front-panel) Fast Operate Transmit Bit 18	430
FOPF_19	Port F (front-panel) Fast Operate Transmit Bit 19	430
FOPF_20	Port F (front-panel) Fast Operate Transmit Bit 20	430
FOPF_21	Port F (front-panel) Fast Operate Transmit Bit 21	430
FOPF_22	Port F (front-panel) Fast Operate Transmit Bit 22	430
FOPF_23	Port F (front-panel) Fast Operate Transmit Bit 23	430
FOPF_24	Port F (front-panel) Fast Operate Transmit Bit 24	430
FOPF_25	Port F (front-panel) Fast Operate Transmit Bit 25	431
FOPF_26	Port F (front-panel) Fast Operate Transmit Bit 26	431
FOPF_27	Port F (front-panel) Fast Operate Transmit Bit 27	431
FOPF_28	Port F (front-panel) Fast Operate Transmit Bit 28	431
FOPF_29	Port F (front-panel) Fast Operate Transmit Bit 29	431
FOPF_30	Port F (front-panel) Fast Operate Transmit Bit 30	431
FOPF_31	Port F (front-panel) Fast Operate Transmit Bit 31	431
FOPF_32	Port F (front-panel) Fast Operate Transmit Bit 32	431
FREQFZ	Assert if relay is not calculating frequency	348
FREQOK	Assert if relay is estimating frequency	348
FROKPM	Synchrophasor frequency measurement OK	413
FSA_S	A-Phase sector fault (AG or BCG fault)	457
FSA_T	A-Phase sector fault (AG or BCG fault)	457
FSA_U	A-Phase sector fault (AG or BCG fault)	457
FSA_W	A-Phase sector fault (AG or BCG fault)	458
FSA_X	A-Phase sector fault (AG or BCG fault)	458

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 47 of 69)

Name	Bit Description	Row
FSB_S	B-Phase sector fault (BG or CAG fault)	458
FSB_T	B-Phase sector fault (BG or CAG fault)	458
FSB_U	B-Phase sector fault (BG or CAG fault)	458
FSB_W	B-Phase sector fault (BG or CAG fault)	458
FSB_X	B-Phase sector fault (BG or CAG fault)	458
FSC_S	C-Phase sector fault (CG or ABG fault)	458
FSC_T	C-Phase sector fault (CG or ABG fault)	459
FSC_U	C-Phase sector fault (CG or ABG fault)	459
FSC_W	C-Phase sector fault (CG or ABG fault)	459
FSC_X	C-Phase sector fault (CG or ABG fault)	459
FSERP1	Fast SER enabled for Port 1	412
FSERP2	Fast SER enabled for Port 2	412
FSERP3	Fast SER enabled for Port 3	412
FSERP5	Fast SER enabled for network port	412
FSERPF	Fast SER enabled for front port	412
GFLTA	Instantaneous fault detector asserted, A-Phase	6
GFLTB	Instantaneous fault detector asserted, B-Phase	6
GFLTC	Instantaneous fault detector asserted, C-Phase	6
GROUNDS	Ground involved in the fault, Terminal S	455
GROUNDT	Ground involved in the fault, Terminal T	456
GROUNDU	Ground involved in the fault, Terminal U	456
GROUNDW	Ground involved in the fault, Terminal W	456
GROUNDX	Ground involved in the fault, Terminal X	456
GRPSW	Pulsed alarm for Group switches	345
HALARM	Hardware alarm	345
HALARMA	Pulse stream for unacknowledged diagnostic warnings	345
HALARML	Latched alarm for diagnostic failures	345
HALARMP	Pulsed alarm for diagnostic warnings	345
HS1	Hot-spot alarm Level 1	206
HS1_1	Transformer 1, hot-spot temperature alarm Level 1	206
HS1_2	Transformer 1, hot-spot temperature alarm Level 2	206
HS2	Hot-spot alarm Level 2	206
HS2_1	Transformer 2, hot-spot temperature alarm Level 1	206
HS2_2	Transformer 2, hot-spot temperature alarm Level 2	206
HS3_1	Transformer 3, hot-spot temperature alarm Level 1	206
HS3_2	Transformer 3, hot-spot temperature alarm Level 2	206
IASBF	A-Phase current above threshold, Terminal S	111
IATBF	A-Phase current above threshold, Terminal T	113
IAUBF	A-Phase current above threshold, Terminal U	115
IAWBF	A-Phase current above threshold, Terminal W	117
IAXBF	A-Phase current above threshold, Terminal X	119

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 48 of 69)

Name	Bit Description	Row
IBSBF	B-Phase current above threshold, Terminal S	111
IBTBF	B-Phase current above threshold, Terminal T	113
IBUBF	B-Phase current above threshold, Terminal U	115
IBWBF	B-Phase current above threshold, Terminal W	117
IBXBF	B-Phase current above threshold, Terminal X	119
ICSBF	C-Phase current above threshold, Terminal S	111
ICTBF	C-Phase current above threshold, Terminal T	113
ICUBF	C-Phase current above threshold, Terminal U	115
ICWBF	C-Phase current above threshold, Terminal W	117
ICXBF	C-Phase current above threshold, Terminal X	119
IFLTA	Internal fault detected, A-Phase	7
IFLTB	Internal fault detected, B-Phase	7
IFLTC	Internal fault detected, C-Phase	7
IN101–IN107	Input 101–107 asserted	248
IN201–IN208	Input 201–208 asserted	252
IN209–IN216	Input 209–216 asserted	253
IN217–IN224	Input 217–224 asserted	254
IN301–IN308	Input 301–308 asserted	256
IN309–IN316	Input 309–316 asserted	257
IN317–IN324	Input 317–324 asserted	258
IN401–IN408	Input 401–408 asserted	468
IN409–IN416	Input 409–416 asserted	469
IN417–IN424	Input 417–424 asserted	470
IN501–IN508	Input 501–508 asserted	472
IN509–IN516	Input 509–516 asserted	473
IN517–IN524	Input 517–524 asserted	474
INSBF	Neutral current above threshold, Terminal S	111
INTBF	Neutral/residual current exceeds pickup threshold, Terminal T	113
INUBF	Neutral/residual current exceeds pickup threshold, Terminal U	115
INWBF	Neutral/residual current exceeds pickup threshold, Terminal W	117
INXBF	Neutral/residual current exceeds pickup threshold, Terminal X	119
IO300OK	Communications status of Interface Board 300 when installed or commissioned	467
IO400OK	Communications status of Interface Board 400 when installed or commissioned	467
IO500OK	Communications status of Interface Board 500 when installed or commissioned	467
LB_DP01–LB_DP08	Local Bit 01–Local Bit 08 status display enabled	235
LB_DP09–LB_DP16	Local Bit 09–Local Bit 16 status display enabled	236
LB_DP17–LB_DP24	Local Bit 17–Local Bit 24 status display enabled	237
LB_DP25–LB_DP32	Local Bit 25–Local Bit 32 status display enabled	238

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 49 of 69)

Name	Bit Description	Row
LB_SP01–LB_SP08	Local Bit 01–Local Bit 08 supervision enabled	231
LB_SP09–LB_SP16	Local Bit 09–Local Bit 16 supervision enabled	232
LB_SP17–LB_SP24	Local Bit 17–Local Bit 24 supervision enabled	233
LB_SP25–LB_SP32	Local Bit 25–Local Bit 32 supervision enabled	234
LB01–LB08	Local Bit 01–Local Bit 08 asserted	227
LB09–LB16	Local Bit 09–Local Bit 16 asserted	228
LB17–LB24	Local Bit 17–Local Bit 24 asserted	229
LB25–LB32	Local Bit 25–Local Bit 32 asserted	230
LBOKA	MIRRORED BITS channel in loopback mode, Channel A	376
LBOKB	MIRRORED BITS channel in loopback mode, Channel B	377
LD_3PFS	Leading three-phase power factor, Terminal S	480
LD_3PFT	Leading three-phase power factor, Terminal T	481
LD_3PFU	Leading three-phase power factor, Terminal U	482
LD_3PFW	Leading three-phase power factor, Terminal W	483
LD_3PFX	Leading three-phase power factor, Terminal X	484
LD_APFS	Leading power factor, A-Phase, Terminal S	480
LD_APFT	Leading power factor, A-Phase, Terminal T	481
LD_APFU	Leading power factor, A-Phase, Terminal U	482
LD_APFW	Leading power factor, A-Phase, Terminal W	483
LD_APFX	Leading power factor, A-Phase, Terminal X	484
LD_BPFS	Leading power factor, B-Phase, Terminal S	480
LD_BPFT	Leading power factor, B-Phase, Terminal T	481
LD_BPFU	Leading power factor, B-Phase, Terminal U	482
LD_BPFW	Leading power factor, B-Phase, Terminal W	483
LD_BPFX	Leading power factor, B-Phase, Terminal X	484
LD_CPFS	Leading power factor, C-Phase, Terminal S	480
LD_CPFT	Leading power factor, C-Phase, Terminal T	481
LD_CPFU	Leading power factor, C-Phase, Terminal U	482
LD_CPFW	Leading power factor, C-Phase, Terminal W	483
LD_CPFX	Leading power factor, C-Phase, Terminal X	484
LD3PFST	Leading three-phase power factor, combined terminals ST	485
LD3PFTU	Leading three-phase power factor, combined terminals TU	486
LD3PFUW	Leading three-phase power factor, combined terminals UW	487
LD3PFWX	Leading three-phase power factor, combined terminals WX	488
LDAPFST	Leading power factor, A-Phase, combined terminals ST	485
LDAPFTU	Leading power factor, A-Phase, combined terminals TU	486
LDAPFUW	Leading power factor, A-Phase, combined terminals UW	487
LDAPFWX	Leading power factor, A-Phase, combined terminals WX	488

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 50 of 69)

Name	Bit Description	Row
LDBPFST	Leading power factor, B-Phase, combined terminals ST	485
LDBPFTU	Leading power factor, B-Phase, combined terminals TU	486
LDBPFUW	Leading power factor, B-Phase, combined terminals UW	487
LDBPFWX	Leading power factor, B-Phase, combined terminals WX	488
LDCPFST	Leading power factor, C-Phase, combined terminals ST	485
LDCPFTU	Leading power factor, C-Phase, combined terminals TU	486
LDCPFUW	Leading power factor, C-Phase, combined terminals UW	487
LDCPFWX	Leading power factor, C-Phase, combined terminals WX	488
LG_3PFS	Lagging three-phase power factor, Terminal S	480
LG_3PFT	Lagging three-phase power factor, Terminal T	481
LG_3PFU	Lagging three-phase power factor, Terminal U	482
LG_3PFW	Lagging three-phase power factor, Terminal W	483
LG_3PFX	Lagging three-phase power factor, Terminal X	484
LG_APFS	Lagging power factor, A-Phase, Terminal S	480
LG_APFT	Lagging power factor, A-Phase, Terminal T	481
LG_APFU	Lagging power factor, A-Phase, Terminal U	482
LG_APFW	Lagging power factor, A-Phase, Terminal W	483
LG_APFX	Lagging power factor, A-Phase, Terminal X	484
LG_BPFS	Lagging power factor, B-Phase, Terminal S	480
LG_BPFT	Lagging power factor, B-Phase, Terminal T	481
LG_BPFU	Lagging power factor, B-Phase, Terminal U	482
LG_BPFW	Lagging power factor, B-Phase, Terminal W	483
LG_BPFX	Lagging power factor, B-Phase, Terminal X	484
LG_CPFS	Lagging power factor, C-Phase, Terminal S	480
LG_CPFT	Lagging power factor, C-Phase, Terminal T	481
LG_CPFU	Lagging power factor, C-Phase, Terminal U	482
LG_CPFW	Lagging power factor, C-Phase, Terminal W	483
LG_CPFX	Lagging power factor, C-Phase, Terminal X	484
LG3PFST	Lagging three-phase power factor, combined terminals ST	485
LG3PFTU	Lagging three-phase power factor, combined terminals TU	486
LG3PFUW	Lagging three-phase power factor, combined terminals UW	487
LG3PFWX	Lagging three-phase power factor, combined terminals WX	488
LGAPFST	Lagging power factor, A-Phase, combined terminals ST	485
LGAPFTU	Lagging power factor, A-Phase, combined terminals TU	486
LGAPFUW	Lagging power factor, A-Phase, combined terminals UW	487
LGAPFWX	Lagging power factor, A-Phase, combined terminals WX	488
LGBPFST	Lagging power factor, B-Phase, combined terminals ST	485
LGBPFTU	Lagging power factor, B-Phase, combined terminals TU	486
LGBPFUW	Lagging power factor, B-Phase, combined terminals UW	487
LGBPFWX	Lagging power factor, B-Phase, combined terminals WX	488
LGCPFST	Lagging power factor, C-Phase, combined terminals ST	485

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 51 of 69)

Name	Bit Description	Row
LGCPFTU	Lagging power factor, C-Phase, combined terminals TU	486
LGCPFUW	Lagging power factor, C-Phase, combined terminals UW	487
LGCPFWX	Lagging power factor, C-Phase, combined terminals WX	488
LINK5A	Link status of the Port 5A connection	424
LINK5B	Link status of the Port 5B connection	424
LINK5C	Link status of the Port 5C connection	424
LINK5D	Link status of the Port 5D connection	424
LNKFAIL	Link status of the active port	424
LOCAL	Local front-panel control	124
LOPV	Loss-of-potential Terminal V	109
LOPZ	Loss-of-potential Terminal Z	109
LPHDSIM	IEC 61850 logical node for physical device simulation	378
LPSEC	Leap second is added	422
LPSECP	Leap second pending	422
MAMB_OK	Ambient temperature measurement RTD healthy	210
MATHERR	SELOGIC control equation Math error	344
MTO1_OK	Transformer 1, top-oil temperature measurement RTD healthy	210
MTO2_OK	Transformer 2, top-oil temperature measurement RTD healthy	210
MTO3_OK	Transformer 3, top-oil temperature measurement RTD healthy	210
NDREF1	Nondirectional REF Element 1 enabled	14
NDREF2	Nondirectional REF Element 2 enabled	16
NDREF3	Nondirectional REF Element 3 enabled	18
OCS	Breaker open command, Terminal S	224
OCT	Breaker open command, Terminal T	224
OCU	Breaker open command, Terminal U	224
OCW	Breaker open command, Terminal W	224
OCX	Breaker open command, Terminal X	225
OPHAS	A-Phase, Terminal S open	106
OPHAT	A-Phase, Terminal T open	106
OPHAU	A-Phase, Terminal U open	107
OPHAW	A-Phase, Terminal W open	107
OPHAX	A-Phase, Terminal X open	108
OPHBS	B-Phase, Terminal S open	106
OPHBT	B-Phase, Terminal T open	106
OPHBU	B-Phase, Terminal U open	107
OPHBW	B-Phase, Terminal W open	107
OPHBX	B-Phase, Terminal X open	108
OPHCS	C-Phase, Terminal S open	106
OPHCT	C-Phase, Terminal T open	106
OPHCU	C-Phase, Terminal U open	107
OPHCW	C-Phase, Terminal W open	107

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 52 of 69)

Name	Bit Description	Row
OPHCX	C-Phase, Terminal X open	108
OPHS	Terminal S open	106
OPHT	Terminal T open	106
OPHU	Terminal U open	107
OPHW	Terminal W open	107
OPHX	Terminal X open	108
OUT101–OUT108	Output 101–108 asserted	352
OUT201–OUT208	Output 201–208 asserted	356
OUT209–OUT216	Output 209–216 asserted	357
OUT301–OUT308	Output 301–308 asserted	358
OUT309–OUT316	Output 309–316 asserted	359
OUT401–OUT408	Output 401–408 asserted	476
OUT409–OUT416	Output 409–416 asserted	477
OUT501–OUT508	Output 501–508 asserted	478
OUT509–OUT516	Output 509–516 asserted	479
P5ABSW	Port 5A or 5B has just become active	465
P5ASEL	Port 5A Active/Inactive	425
P5BSEL	Port 5B Active/Inactive	425
P5CSEL	Port 5C Active/Inactive	425
P5DSEL	Port 5D Active/Inactive	425
P87A	Restrained differential element asserted (no security timer), A-Phase	10
P87B	Restrained differential element asserted (no security timer), B-Phase	10
P87C	Restrained differential element asserted (no security timer), C-Phase	10
PASSDIS	Password Disable Jumper is Installed	346
PB1	Pushbutton 01 asserted	360
PB1_LED	Pushbutton 01 LED illuminated	364
PB1_PUL	Pushbutton 01 pulsed for 1 processing interval	362
PB10	Pushbutton 10 asserted	361
PB10LED	Pushbutton 10 LED illuminated	365
PB10PUL	Pushbutton 10 pulsed for 1 processing interval	363
PB11	Pushbutton 11 asserted	361
PB11LED	Pushbutton 11 LED illuminated	365
PB11PUL	Pushbutton 11 pulsed for 1 processing interval	363
PB12	Pushbutton 12 asserted	361
PB12LED	Pushbutton 12 LED illuminated	365

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 53 of 69)

Name	Bit Description	Row
PB12PUL	Pushbutton 12 pulsed for 1 processing interval	363
PB2	Pushbutton 2 asserted	360
PB2_LED	Pushbutton 2 LED illuminated	364
PB2_PUL	Pushbutton 2 pulsed for 1 processing interval	362
PB3	Pushbutton 3 asserted	360
PB3_LED	Pushbutton 3 LED illuminated	364
PB3_PUL	Pushbutton 3 pulsed for 1 processing interval	362
PB4	Pushbutton 4 asserted	360
PB4_LED	Pushbutton 4 LED illuminated	364
PB4_PUL	Pushbutton 4 pulsed for 1 processing interval	362
PB5	Pushbutton 5 asserted	360
PB5_LED	Pushbutton 5 LED illuminated	364
PB5_PUL	Pushbutton 5 pulsed for 1 processing interval	362
PB6	Pushbutton 6 asserted	360
PB6_LED	Pushbutton 6 LED illuminated	364
PB6_PUL	Pushbutton 6 pulsed for 1 processing interval	362
PB7	Pushbutton 7 asserted	360
PB7_LED	Pushbutton 7 LED illuminated	364
PB7_PUL	Pushbutton 7 pulsed for 1 processing interval	362
PB8	Pushbutton 8 asserted	360
PB8_LED	Pushbutton 8 LED illuminated	364
PB8_PUL	Pushbutton 8 pulsed for 1 processing interval	362
PB9	Pushbutton 9 asserted	361
PB9_LED	Pushbutton 9 LED illuminated	365
PB9_PUL	Pushbutton 9 pulsed for 1 processing interval	363
PCN01Q	Protection SELOGIC Counter 01 asserted	284
PCN01R	Protection SELOGIC Counter 01 reset	288
PCN02Q	Protection SELOGIC Counter 02 asserted	284
PCN02R	Protection SELOGIC Counter 02 reset	288
PCN03Q	Protection SELOGIC Counter 03 asserted	284
PCN03R	Protection SELOGIC Counter 03 reset	288
PCN04Q	Protection SELOGIC Counter 04 asserted	284
PCN04R	Protection SELOGIC Counter 04 reset	288
PCN05Q	Protection SELOGIC Counter 05 asserted	284
PCN05R	Protection SELOGIC Counter 05 reset	288
PCN06Q	Protection SELOGIC Counter 06 asserted	284
PCN06R	Protection SELOGIC Counter 06 reset	288
PCN07Q	Protection SELOGIC Counter 07 asserted	284
PCN07R	Protection SELOGIC Counter 07 reset	288
PCN08Q	Protection SELOGIC Counter 08 asserted	284
PCN08R	Protection SELOGIC Counter 08 reset	288

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 54 of 69)

Name	Bit Description	Row
PCN09Q	Protection SELOGIC Counter 09 asserted	285
PCN09R	Protection SELOGIC Counter 09 reset	289
PCN10Q	Protection SELOGIC Counter 10 asserted	285
PCN10R	Protection SELOGIC Counter 10 reset	289
PCN11Q	Protection SELOGIC Counter 11 asserted	285
PCN11R	Protection SELOGIC Counter 11 reset	289
PCN12Q	Protection SELOGIC Counter 12 asserted	285
PCN12R	Protection SELOGIC Counter 12 reset	289
PCN13Q	Protection SELOGIC Counter 13 asserted	285
PCN13R	Protection SELOGIC Counter 13 reset	289
PCN14Q	Protection SELOGIC Counter 14 asserted	285
PCN14R	Protection SELOGIC Counter 14 reset	289
PCN15Q	Protection SELOGIC Counter 15 asserted	285
PCN15R	Protection SELOGIC Counter 15 reset	289
PCN16Q	Protection SELOGIC Counter 16 asserted	285
PCN16R	Protection SELOGIC Counter 16 reset	289
PCN17Q	Protection SELOGIC Counter 17 asserted	286
PCN17R	Protection SELOGIC Counter 17 reset	290
PCN18Q	Protection SELOGIC Counter 18 asserted	286
PCN18R	Protection SELOGIC Counter 18 reset	290
PCN19Q	Protection SELOGIC Counter 19 asserted	286
PCN19R	Protection SELOGIC Counter 19 reset	290
PCN20Q	Protection SELOGIC Counter 20 asserted	286
PCN20R	Protection SELOGIC Counter 20 reset	290
PCN21Q	Protection SELOGIC Counter 21 asserted	286
PCN21R	Protection SELOGIC Counter 21 reset	290
PCN22Q	Protection SELOGIC Counter 22 asserted	286
PCN22R	Protection SELOGIC Counter 22 reset	290
PCN23Q	Protection SELOGIC Counter 23 asserted	286
PCN23R	Protection SELOGIC Counter 23 reset	290
PCN24Q	Protection SELOGIC Counter 24 asserted	286
PCN24R	Protection SELOGIC Counter 24 reset	290
PCN25Q	Protection SELOGIC Counter 25 asserted	287
PCN25R	Protection SELOGIC Counter 25 reset	291
PCN26Q	Protection SELOGIC Counter 26 asserted	287
PCN26R	Protection SELOGIC Counter 26 reset	291
PCN27Q	Protection SELOGIC Counter 27 asserted	287
PCN27R	Protection SELOGIC Counter 27 reset	291
PCN28Q	Protection SELOGIC Counter 28 asserted	287
PCN28R	Protection SELOGIC Counter 28 reset	291
PCN29Q	Protection SELOGIC Counter 29 asserted	287

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 55 of 69)

Name	Bit Description	Row
PCN29R	Protection SELOGIC Counter 29 reset	291
PCN30Q	Protection SELOGIC Counter 30 asserted	287
PCN30R	Protection SELOGIC Counter 30 reset	291
PCN31Q	Protection SELOGIC Counter 31 asserted	287
PCN31R	Protection SELOGIC Counter 31 reset	291
PCN32Q	Protection SELOGIC Counter 32 asserted	287
PCN32R	Protection SELOGIC Counter 32 reset	291
PCT01Q	Protection SELOGIC Conditioning Timer 01 asserted	272
PCT02Q	Protection SELOGIC Conditioning Timer 02 asserted	272
PCT03Q	Protection SELOGIC Conditioning Timer 03 asserted	272
PCT04Q	Protection SELOGIC Conditioning Timer 04 asserted	272
PCT05Q	Protection SELOGIC Conditioning Timer 05 asserted	272
PCT06Q	Protection SELOGIC Conditioning Timer 06 asserted	272
PCT07Q	Protection SELOGIC Conditioning Timer 07 asserted	272
PCT08Q	Protection SELOGIC Conditioning Timer 08 asserted	272
PCT09Q	Protection SELOGIC Conditioning Timer 09 asserted	273
PCT10Q	Protection SELOGIC Conditioning Timer 10 asserted	273
PCT11Q	Protection SELOGIC Conditioning Timer 11 asserted	273
PCT12Q	Protection SELOGIC Conditioning Timer 12 asserted	273
PCT13Q	Protection SELOGIC Conditioning Timer 13 asserted	273
PCT14Q	Protection SELOGIC Conditioning Timer 14 asserted	273
PCT15Q	Protection SELOGIC Conditioning Timer 15 asserted	273
PCT16Q	Protection SELOGIC Conditioning Timer 16 asserted	273
PCT17Q	Protection SELOGIC Conditioning Timer 17 asserted	274
PCT18Q	Protection SELOGIC Conditioning Timer 18 asserted	274
PCT19Q	Protection SELOGIC Conditioning Timer 19 asserted	274
PCT20Q	Protection SELOGIC Conditioning Timer 20 asserted	274
PCT21Q	Protection SELOGIC Conditioning Timer 21 asserted	274
PCT22Q	Protection SELOGIC Conditioning Timer 22 asserted	274
PCT23Q	Protection SELOGIC Conditioning Timer 23 asserted	274
PCT24Q	Protection SELOGIC Conditioning Timer 24 asserted	274
PCT25Q	Protection SELOGIC Conditioning Timer 25 asserted	275
PCT26Q	Protection SELOGIC Conditioning Timer 26 asserted	275
PCT27Q	Protection SELOGIC Conditioning Timer 27 asserted	275
PCT28Q	Protection SELOGIC Conditioning Timer 28 asserted	275
PCT29Q	Protection SELOGIC Conditioning Timer 29 asserted	275
PCT30Q	Protection SELOGIC Conditioning Timer 30 asserted	275
PCT31Q	Protection SELOGIC Conditioning Timer 31 asserted	275
PCT32Q	Protection SELOGIC Conditioning Timer 32 asserted	275
PFRTEX	Protection SELOGIC control equation first execution	344
PHA_S	A-Phase involved in the fault, Terminal S	454

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 56 of 69)

Name	Bit Description	Row
PHA_T	A-Phase involved in the fault, Terminal T	454
PHA_U	A-Phase involved in the fault, Terminal U	454
PHA_W	A-Phase involved in the fault, Terminal W	454
PHA_X	A-Phase involved in the fault, Terminal X	454
PHB_S	B-Phase involved in the fault, Terminal S	454
PHB_T	B-Phase involved in the fault, Terminal T	454
PHB_U	B-Phase involved in the fault, Terminal U	454
PHB_W	B-Phase involved in the fault, Terminal W	455
PHB_X	B-Phase involved in the fault, Terminal X	455
PHC_S	C-Phase involved in the fault, Terminal S	455
PHC_T	C-Phase involved in the fault, Terminal T	455
PHC_U	C-Phase involved in the fault, Terminal U	455
PHC_W	C-Phase involved in the fault, Terminal W	455
PHC_X	C-Phase involved in the fault, Terminal X	455
PLT01–PLT08	Protection SELOGIC Latch 01–Latch 08 asserted	268
PLT09–PLT16	Protection SELOGIC Latch 09–Latch 16 asserted	269
PLT17–PLT24	Protection SELOGIC Latch 17–Latch 24 asserted	270
PLT25–PLT32	Protection SELOGIC Latch 25–Latch 32 asserted	271
PMDOK	Assert if data acquisition system is operating correctly	349
PMTEST	Synchrophasor test mode	413
PMTRIG	Synchrophasor SELOGIC control equation trigger	413
PST01Q	Protection SELOGIC Sequencing Timer 01 asserted	276
PST01R	Protection SELOGIC Sequencing Timer 01 reset	280
PST02Q	Protection SELOGIC Sequencing Timer 02 asserted	276
PST02R	Protection SELOGIC Sequencing Timer 02 reset	280
PST03Q	Protection SELOGIC Sequencing Timer 03 asserted	276
PST03R	Protection SELOGIC Sequencing Timer 03 reset	280
PST04Q	Protection SELOGIC Sequencing Timer 04 asserted	276
PST04R	Protection SELOGIC Sequencing Timer 04 reset	280
PST05Q	Protection SELOGIC Sequencing Timer 05 asserted	276
PST05R	Protection SELOGIC Sequencing Timer 05 reset	280
PST06Q	Protection SELOGIC Sequencing Timer 06 asserted	276
PST06R	Protection SELOGIC Sequencing Timer 06 reset	280
PST07Q	Protection SELOGIC Sequencing Timer 07 asserted	276
PST07R	Protection SELOGIC Sequencing Timer 07 reset	280
PST08Q	Protection SELOGIC Sequencing Timer 08 asserted	276
PST08R	Protection SELOGIC Sequencing Timer 08 reset	280
PST09Q	Protection SELOGIC Sequencing Timer 09 asserted	277
PST09R	Protection SELOGIC Sequencing Timer 09 reset	281
PST10Q	Protection SELOGIC Sequencing Timer 10 asserted	277
PST10R	Protection SELOGIC Sequencing Timer 10 reset	281

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 57 of 69)

Name	Bit Description	Row
PST11Q	Protection SELOGIC Sequencing Timer 11 asserted	277
PST11R	Protection SELOGIC Sequencing Timer 11 reset	281
PST12Q	Protection SELOGIC Sequencing Timer 12 asserted	277
PST12R	Protection SELOGIC Sequencing Timer 12 reset	281
PST13Q	Protection SELOGIC Sequencing Timer 13 asserted	277
PST13R	Protection SELOGIC Sequencing Timer 13 reset	281
PST14Q	Protection SELOGIC Sequencing Timer 14 asserted	277
PST14R	Protection SELOGIC Sequencing Timer 14 reset	281
PST15Q	Protection SELOGIC Sequencing Timer 15 asserted	277
PST15R	Protection SELOGIC Sequencing Timer 15 reset	281
PST16Q	Protection SELOGIC Sequencing Timer 16 asserted	277
PST16R	Protection SELOGIC Sequencing Timer 16 reset	281
PST17Q	Protection SELOGIC Sequencing Timer 17 asserted	278
PST17R	Protection SELOGIC Sequencing Timer 17 reset	282
PST18Q	Protection SELOGIC Sequencing Timer 18 asserted	278
PST18R	Protection SELOGIC Sequencing Timer 18 reset	282
PST19Q	Protection SELOGIC Sequencing Timer 19 asserted	278
PST19R	Protection SELOGIC Sequencing Timer 19 reset	282
PST20Q	Protection SELOGIC Sequencing Timer 20 asserted	278
PST20R	Protection SELOGIC Sequencing Timer 20 reset	282
PST21Q	Protection SELOGIC Sequencing Timer 21 asserted	278
PST21R	Protection SELOGIC Sequencing Timer 21 reset	282
PST22Q	Protection SELOGIC Sequencing Timer 22 asserted	278
PST22R	Protection SELOGIC Sequencing Timer 22 reset	282
PST23Q	Protection SELOGIC Sequencing Timer 23 asserted	278
PST23R	Protection SELOGIC Sequencing Timer 23 reset	282
PST24Q	Protection SELOGIC Sequencing Timer 24 asserted	278
PST24R	Protection SELOGIC Sequencing Timer 24 reset	282
PST25Q	Protection SELOGIC Sequencing Timer 25 asserted	279
PST25R	Protection SELOGIC Sequencing Timer 25 reset	283
PST26Q	Protection SELOGIC Sequencing Timer 26 asserted	279
PST26R	Protection SELOGIC Sequencing Timer 26 reset	283
PST27Q	Protection SELOGIC Sequencing Timer 27 asserted	279
PST27R	Protection SELOGIC Sequencing Timer 27 reset	283
PST28Q	Protection SELOGIC Sequencing Timer 28 asserted	279
PST28R	Protection SELOGIC Sequencing Timer 28 reset	283
PST29Q	Protection SELOGIC Sequencing Timer 29 asserted	279
PST29R	Protection SELOGIC Sequencing Timer 29 reset	283
PST30Q	Protection SELOGIC Sequencing Timer 30 asserted	279
PST30R	Protection SELOGIC Sequencing Timer 30 reset	283
PST31Q	Protection SELOGIC Sequencing Timer 31 asserted	279

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 58 of 69)

Name	Bit Description	Row
PST31R	Protection SELOGIC Sequencing Timer 31 reset	283
PST32Q	Protection SELOGIC Sequencing Timer 32 asserted	279
PST32R	Protection SELOGIC Sequencing Timer 32 reset	283
PSV01–PSV08	Protection SELOGIC Variable 01–Variable 08 asserted	260
PSV09–PSV16	Protection SELOGIC Variable 09–Variable 16 asserted	261
PSV17–PSV24	Protection SELOGIC Variable 17–Variable 24 asserted	262
PSV25–PSV32	Protection SELOGIC Variable 25–Variable 32 asserted	263
PSV33–PSV40	Protection SELOGIC Variable 33–Variable 40 asserted	264
PSV41–PSV48	Protection SELOGIC Variable 41–Variable 48 asserted	265
PSV49–PSV56	Protection SELOGIC Variable 49–Variable 56 asserted	266
PSV57–PSV64	Protection SELOGIC Variable 57–Variable 64 asserted	267
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	466
PTP_OK	PTP is available and has sufficient quality	465
PTP_RST	Disqualify PTP high-accuracy time source	465
PTP_SET	Qualify PTP high-accuracy time source	465
PTP_TIM	A valid PTP time source is detected	465
PTPSYNC	Synchronized to high-quality PTP source	466
PUNRLBL	Protection SELOGIC control equation unresolved label	344
RB01–RB08	Remote Bit 01–Remote Bit 08 asserted	243
RB09–RB16	Remote Bit 09–Remote Bit 16 asserted	242
RB17–RB24	Remote Bit 17–Remote Bit 24 asserted	241
RB25–RB32	Remote Bit 25–Remote Bit 32 asserted	240
RBADA	Outage too large for normal MIRRORED BITS communication, Channel A	376
RBADB	Outage too large for normal MIRRORED BITS communication, Channel B	377
REF501	Neutral (operating current) Instantaneous Overcurrent REF Element 1 picked up	14
REF502	Neutral (operating current) Instantaneous Overcurrent REF Element 2 picked up	16
REF503	Neutral (operating current) Instantaneous Overcurrent REF Element 3 picked up	18
REF50T1	Neutral Instantaneous Overcurrent REF Element 1 timed out	14
REF50T2	Neutral Instantaneous Overcurrent REF Element 2 timed out	16
REF50T3	Neutral Instantaneous Overcurrent REF Element 3 timed out	18
REF511P	REF Element 1 TOC element picked up	15
REF512P	REF Element 2 TOC element picked up	17
REF513P	REF Element 3 TOC element picked up	19
REF51R1	REF Element 1 TOC element reset	15
REF51R2	REF Element 2 TOC element reset	17
REF51R3	REF Element 3 TOC element reset	19
REF51T1	REF Element 1 TOC element timed out	14
REF51T2	REF Element 2 TOC element timed out	16
REF51T3	REF Element 3 TOC element timed out	18
REFF1	Earth Fault Inside REF Element 1 zone	14
REFF2	Earth Fault Inside REF Element 2 zone	16

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 59 of 69)

Name	Bit Description	Row
REFF3	Earth Fault Inside REF Element 3 zone	18
REFR1	Earth Fault Outside REF Element 1 zone	14
REFR2	Earth Fault Outside REF Element 2 zone	16
REFR3	Earth Fault Outside REF Element 3 zone	18
RF51TC1	Inverse-Time Neutral Overcurrent REF Element 1 enabled	14
RF51TC2	Inverse-Time Neutral Overcurrent REF Element 2 enabled	16
RF51TC3	Inverse-Time Neutral Overcurrent REF Element 3 enabled	18
RLL	Rate of loss-of-life alarm	208
RLL_1	Transformer 1, rate of loss-of-life alarm	208
RLL_2	Transformer 2, rate of loss-of-life alarm	208
RLL_3	Transformer 3, rate of loss-of-life alarm	208
RMB1A	Received MIRRORED BITS 1, Channel A	372
RMB1B	Received MIRRORED BITS 1, Channel B	374
RMB2A	Received MIRRORED BITS 2, Channel A	372
RMB2B	Received MIRRORED BITS 2, Channel B	374
RMB3A	Received MIRRORED BITS 3, Channel A	372
RMB3B	Received MIRRORED BITS 3, Channel B	374
RMB4A	Received MIRRORED BITS 4, Channel A	372
RMB4B	Received MIRRORED BITS 4, Channel B	374
RMB5A	Received MIRRORED BITS 5, Channel A	372
RMB5B	Received MIRRORED BITS 5, Channel B	374
RMB6A	Received MIRRORED BITS 6, Channel A	372
RMB6B	Received MIRRORED BITS 6, Channel B	374
RMB7A	Received MIRRORED BITS 7, Channel A	372
RMB7B	Received MIRRORED BITS 7, Channel B	374
RMB8A	Received MIRRORED BITS 8, Channel A	372
RMB8B	Received MIRRORED BITS 8, Channel B	374
ROKA	MIRRORED BITS Channel A normal status in non-loopback mode	376
ROKB	MIRRORED BITS Channel B normal status in non-loopback mode	377
RST_BAT	Reset battery monitoring	369
RST_BKS	Reset Breaker S monitoring	368
RST_BKT	Reset Breaker T monitoring	368
RST_BKU	Reset Breaker U monitoring	368
RST_BKW	Reset Breaker W monitoring	368
RST_BKX	Reset Breaker X monitoring	368
RST_DEM	Reset demand metering	368
RST_ENE	Reset energy metering	368
RST_HAL	Reset HALARMA	369
RST_PDM	Reset peak demand metering	368
RSTDNPE	Reset DNP fault summary data	369
RSTTRGT	Reset front-panel targets	369

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 60 of 69)

Name	Bit Description	Row
RTCAD01	RTC Channel A Remote Data Bit 01	416
RTCAD02	RTC Channel A Remote Data Bit 02	416
RTCAD03	RTC Channel A Remote Data Bit 03	416
RTCAD04	RTC Channel A Remote Data Bit 04	416
RTCAD05	RTC Channel A Remote Data Bit 05	416
RTCAD06	RTC Channel A Remote Data Bit 06	416
RTCAD07	RTC Channel A Remote Data Bit 07	416
RTCAD08	RTC Channel A Remote Data Bit 08	416
RTCAD09	RTC Channel A Remote Data Bit 09	417
RTCAD10	RTC Channel A Remote Data Bit 10	417
RTCAD11	RTC Channel A Remote Data Bit 11	417
RTCAD12	RTC Channel A Remote Data Bit 12	417
RTCAD13	RTC Channel A Remote Data Bit 13	417
RTCAD14	RTC Channel A Remote Data Bit 14	417
RTCAD15	RTC Channel A Remote Data Bit 15	417
RTCAD16	RTC Channel A Remote Data Bit 16	417
RTCBD01	RTC Channel B Remote Data Bit 01	418
RTCBD02	RTC Channel B Remote Data Bit 02	418
RTCBD03	RTC Channel B Remote Data Bit 03	418
RTCBD04	RTC Channel B Remote Data Bit 04	418
RTCBD05	RTC Channel B Remote Data Bit 05	418
RTCBD06	RTC Channel B Remote Data Bit 06	418
RTCBD07	RTC Channel B Remote Data Bit 07	418
RTCBD08	RTC Channel B Remote Data Bit 08	418
RTCBD09	RTC Channel B Remote Data Bit 09	419
RTCBD10	RTC Channel B Remote Data Bit 10	419
RTCBD11	RTC Channel B Remote Data Bit 11	419
RTCBD12	RTC Channel B Remote Data Bit 12	419
RTCBD13	RTC Channel B Remote Data Bit 13	419
RTCBD14	RTC Channel B Remote Data Bit 14	419
RTCBD15	RTC Channel B Remote Data Bit 15	419
RTCBD16	RTC Channel B Remote Data Bit 16	419
RTCCFGA	RTC Channel A configuration complete	414
RTCCFGB	RTC Channel B configuration complete	414
RTCDLYA	Max RTC delay exceeded for Channel A	414
RTCDLYB	Max RTC delay exceeded for Channel B	414
RTCENA	Valid remote synchrophasors received on Channel A	415
RTCENB	Valid remote synchrophasors received on Channel B	415
RTCROK	Valid aligned RTC data available on all enabled channels	414
RTCROKA	Valid aligned RTC data available on Channel A	415
RTCROKB	Valid aligned RTC data available on Channel B	415

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 61 of 69)

Name	Bit Description	Row
RTCSEQA	RTC Channel A data in sequence	414
RTCSEQB	RTC Channel B data in sequence	414
RTD01OC	RTD01 open-circuited	216
RTD01OK	RTD01 healthy	212
RTD01SC	RTD01 short-circuited	214
RTD02OC	RTD02 open-circuited	216
RTD02OK	RTD02 healthy	212
RTD02SC	RTD02 short-circuited	214
RTD03OC	RTD03 open-circuited	216
RTD03OK	RTD03 healthy	212
RTD03SC	RTD03 short-circuited	214
RTD04OC	RTD04 open-circuited	216
RTD04OK	RTD04 healthy	212
RTD04SC	RTD04 short-circuited	214
RTD05OC	RTD05 open-circuited	216
RTD05OK	RTD05 healthy	212
RTD05SC	RTD05 short-circuited	214
RTD06OC	RTD06 open-circuited	216
RTD06OK	RTD06 healthy	212
RTD06SC	RTD06 short-circuited	214
RTD07OC	RTD07 open-circuited	216
RTD07OK	RTD07 healthy	212
RTD07SC	RTD07 short-circuited	214
RTD08OC	RTD08 open-circuited	216
RTD08OK	RTD08 healthy	212
RTD08SC	RTD08 short-circuited	214
RTD09OC	RTD09 open-circuited	217
RTD09OK	RTD09 healthy	213
RTD09SC	RTD09 short-circuited	215
RTD10OC	RTD10 open-circuited	217
RTD10OK	RTD10 healthy	213
RTD10SC	RTD10 short-circuited	215
RTD11OC	RTD11 open-circuited	217
RTD11OK	RTD11 healthy	213
RTD11SC	RTD11 short-circuited	215
RTD12OC	RTD12 open-circuited	217
RTD12OK	RTD12 healthy	213
RTD12SC	RTD12 short-circuited	215
RTDCOMF	SEL-2600 Communication Failure	218
RTDFL	SEL-2600 RAM failure	218
RTS	Retrip Timer timed out/retrip command issued, Terminal S	110

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 62 of 69)

Name	Bit Description	Row
RTT	Retrip Timer timed out/retrip command issued, Terminal T	112
RTU	Retrip Timer timed out/retrip command issued, Terminal U	114
RTW	Retrip Timer timed out/retrip command issued, Terminal W	116
RTX	Retrip Timer timed out/retrip command issued, Terminal X	118
S32QE	Negative-sequence phase directional element enabled, Terminal S	20
S32QGE	Negative-sequence ground directional element enabled, Terminal S	20
S32VE	Zero-sequence voltage directional element enabled, Terminal S	20
S50GF	Zero-sequence current above forward threshold, Terminal S	20
S50GR	Zero-sequence current above reverse threshold, Terminal S	20
S50QF	Negative-sequence current above forward threshold, Terminal S	20
S50QR	Negative-sequence current above reverse threshold, Terminal S	20
SALARM	Software alarm	345
SC850BM	SELOGIC control for IEC 61850 Blocked Mode	532
SC850TM	SELOGIC control for IEC 61850 Test Mode	532
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	465
SER_OK	IRIG-B signal from serial Port 1 is available and has sufficient quality	464
SER_RST	Disqualify serial IRIG-B high-accuracy time source	464
SER_SET	Qualify serial IRIG-B high-accuracy time source	464
SER_TIM	A valid IRIG-B time source is detected on serial port	465
SERSYNC	Synchronized to high-quality serial IRIG source	466
SETCHG	Pulsed alarm for settings changes	345
SF32G	Forward ground directional element asserted, Terminal S	21
SF32P	Forward phase directional element asserted, Terminal S	30
SF32Q	Forward negative-sequence phase directional element asserted, Terminal S	30
SF32QG	Forward negative-sequence ground directional element asserted, Terminal S	20
SF32V	Forward zero-sequence ground directional element asserted, Terminal S	21
SFBKS	Breaker S slip frequency is within acceptable slip frequency window	447
SFBKT	Breaker T slip frequency is within acceptable slip frequency window	447
SFBKU	Breaker U slip frequency is within acceptable slip frequency window	447
SFBKW	Breaker W slip frequency is within acceptable slip frequency window	447
SFBKX	Breaker X slip frequency is within acceptable slip frequency window	447
SFZBKS	Breaker S slip frequency is less than 5 MHz	446
SFZBKT	Breaker T slip frequency is less than 5 MHz	446
SFZBKU	Breaker U slip frequency is less than 5 MHz	446
SFZBKW	Breaker W slip frequency is less than 5 MHz	446
SFZBKX	Breaker X slip frequency is less than 5 MHz	447
SG1	Setting Group 1 is active	244
SG2	Setting Group 2 is active	244
SG3	Setting Group 3 is active	244
SG4	Setting Group 4 is active	244
SG5	Setting Group 5 is active	244

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 63 of 69)

Name	Bit Description	Row
SG6	Setting Group 6 is active	244
SLOWS	Breaker S synchronizing voltage slipping slower than polarizing voltage	444
SLOWT	Breaker T synchronizing voltage slipping slower than polarizing voltage	444
SLOWU	Breaker U synchronizing voltage slipping slower than polarizing voltage	444
SLOWW	Breaker W synchronizing voltage slipping slower than polarizing voltage	445
SLOWX	Breaker X synchronizing voltage slipping slower than polarizing voltage	445
SPCER1	Synchrophasor configuration error on Port 1	347
SPCER2	Synchrophasor configuration error on Port 2	347
SPCER3	Synchrophasor configuration error on Port 3	347
SPCERF	Synchrophasor configuration error on Port F	347
SPEN	Signal profiling enabled	426
SR32G	Reverse ground directional element asserted, Terminal S	21
SR32P	Reverse phase directional element asserted, Terminal S	30
SR32Q	Reverse negative-sequence phase directional element asserted, Terminal S	30
SR32QG	Reverse negative-sequence phase directional element asserted, Terminal S	21
SR32V	Reverse zero-sequence ground directional element asserted, Terminal S	21
T1CS2	Transformer 1 Cooling Stage 2	211
T1CS3	Transformer 1 Cooling Stage 3	211
T1OIL_F	Transformer 1 oil temperature fault condition	213
T2CS2	Transformer 2 Cooling Stage 2	211
T2CS3	Transformer 2 Cooling Stage 3	211
T2OIL_F	Transformer 2 oil temperature fault condition	213
T32QE	Negative-sequence phase directional element enabled, Terminal T	22
T32QGE	Negative-sequence ground directional element enabled, Terminal T	22
T32VE	Zero-sequence voltage directional element enabled, Terminal T	22
T3CS2	Transformer 3 Cooling Stage 2	211
T3CS3	Transformer 3 Cooling Stage 3	211
T3OIL_F	Transformer 3 oil temperature fault condition	213
T50GF	Zero-sequence current above forward threshold, Terminal T	22
T50GR	Zero-sequence current above reverse threshold, Terminal T	22
T50QF	Negative-sequence current above forward threshold, Terminal T	22
T50QR	Negative-sequence current above reverse threshold, Terminal T	22
TBNC	Assert while time is based on a valid BNC IRIG source	350
TCREF1	REF Element 1 enabled	14
TCREF2	REF Element 2 enabled	16
TCREF3	REF Element 3 enabled	18
TESTDB	Database test bit	378
TESTDB2	Enhanced label based test bit	378
TESTFM	Fast Meter test bit	378
TESTPUL	Pulse test bit	378
TF32G	Forward ground directional element asserted, Terminal T	23

Table 11.1 Alphabetical List of Relay Word Bits (Sheet 64 of 69)

Name	Bit Description	Row
TF32P	Forward phase directional element asserted, Terminal T	31
TF32Q	Forward negative-sequence phase directional element asserted, Terminal T	31
TF32QG	Forward negative-sequence ground directional element asserted, Terminal T	22
TF32V	Forward zero-sequence ground directional element asserted, Terminal T	23
TFLTALA	Through-fault alarm, A-Phase	219
TFLTALB	Through-fault alarm, B-Phase	219
TFLTALC	Through-fault alarm, C-Phase	219
TGLOBAL	Relay calendar clock and ADC sampling synchronized to C37.118 high-accuracy IRIG-B time source	350
TH5AD	Fifth-harmonic delayed alarm asserted	12
TH5AP	Fifth-harmonic instantaneous alarm asserted	12
THRLA1	Thermal element, Level 1 alarm	530
THRLA2	Thermal element, Level 2 alarm	530
THRLA3	Thermal element, Level 3 alarm	530
THRLT1	Thermal element, Level 1 trip	530
THRLT2	Thermal element, Level 2 trip	530
THRLT3	Thermal element, Level 3 trip	530
TIRIG	Assert while time is based on IRIG for both mark and value	349
TLED_1	Target LED 1 on relay front panel	1
TLED_10	Target LED 10 on relay front panel	2
TLED_11	Target LED 11 on relay front panel	2
TLED_12	Target LED 12 on relay front panel	2
TLED_13	Target LED 13 on relay front panel	2
TLED_14	Target LED 14 on relay front panel	2
TLED_15	Target LED 15 on relay front panel	2
TLED_16	Target LED 16 on relay front panel	2
TLED_17	Target LED 17 on relay front panel	3
TLED_18	Target LED 18 on relay front panel	3
TLED_19	Target LED 19 on relay front panel	3
TLED_2	Target LED 2 on relay front panel	1
TLED_20	Target LED 20 on relay front panel	3
TLED_21	Target LED 21 on relay front panel	3
TLED_22	Target LED 22 on relay front panel	3
TLED_23	Target LED 23 on relay front panel	3
TLED_24	Target LED 24 on relay front panel	3
TLED_3	Target LED 3 on relay front panel	1
TLED_4	Target LED 4 on relay front panel	1
TLED_5	Target LED 5 on relay front panel	1
TLED_6	Target LED 6 on relay front panel	1
TLED_7	Target LED 7 on relay front panel	1
TLED_8	Target LED 8 on relay front panel	1
TLED_9	Target LED 9 on relay front panel	2

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 65 of 69)

Name	Bit Description	Row
TLL	Total loss-of-life alarm	208
TLL_1	Transformer 1, total loss-of-life alarm	208
TLL_2	Transformer 2, total loss-of-life alarm	208
TLL_3	Transformer 3, total loss-of-life alarm	208
TLOCAL	Relay calendar clock and ADC sampling synchronized to non-C37.118-compliant, high-accuracy IRIG-B time source	350
TMB1A	Transmitted MIRRORED BITS 1, Channel A	373
TMB1B	Transmitted MIRRORED BITS 1, Channel B	375
TMB2A	Transmitted MIRRORED BITS 2, Channel A	373
TMB2B	Transmitted MIRRORED BITS 2, Channel B	375
TMB3A	Transmitted MIRRORED BITS 3, Channel A	373
TMB3B	Transmitted MIRRORED BITS 3, Channel B	375
TMB4A	Transmitted MIRRORED BITS 4, Channel A	373
TMB4B	Transmitted MIRRORED BITS 4, Channel B	375
TMB5A	Transmitted MIRRORED BITS 5, Channel A	373
TMB5B	Transmitted MIRRORED BITS 5, Channel B	375
TMB6A	Transmitted MIRRORED BITS 6, Channel A	373
TMB6B	Transmitted MIRRORED BITS 6, Channel B	375
TMB7A	Transmitted MIRRORED BITS 7, Channel A	373
TMB7B	Transmitted MIRRORED BITS 7, Channel B	375
TMB8A	Transmitted MIRRORED BITS 8, Channel A	373
TMB8B	Transmitted MIRRORED BITS 8, Channel B	375
TO1	Top-oil temperature alarm Level 1	205
TO1_1	Transformer 1, top-oil temperature alarm Level 1	205
TO1_2	Transformer 1, top-oil temperature alarm Level 2	205
TO2	Top-oil temperature alarm Level 2	205
TO2_1	Transformer 2, top-oil temperature alarm Level 1	205
TO2_2	Transformer 2, top-oil temperature alarm Level 2	205
TO3_1	Transformer 3, top-oil temperature alarm Level 1	205
TO3_2	Transformer 3, top-oil temperature alarm Level 2	205
TPLLEXT	Update PLL using external signal	350
TPTP	Assert while time is based on a valid PTP source	350
TQUAL1	Time quality, binary, add 1 when asserted	422
TQUAL2	Time quality, binary, add 2 when asserted	422
TQUAL4	Time quality, binary, add 4 when asserted	422
TQUAL8	Time quality, binary, add 8 when asserted	422
TR32G	Reverse ground directional element asserted, Terminal T	23
TR32P	Reverse phase directional element asserted, Terminal T	31
TR32Q	Reverse negative-sequence phase directional element asserted, Terminal T	31
TR32QG	Reverse negative-sequence phase directional element asserted, Terminal T	23
TR32V	Reverse zero-sequence ground directional element asserted, Terminal T	23
TRDE	Transformer de-energize	211

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 66 of 69)

Name	Bit Description	Row
TREA1	Synchrophasor SELOGIC control equation trigger Reason 1	413
TREA2	Synchrophasor SELOGIC control equation trigger Reason 2	413
TREA3	Synchrophasor SELOGIC control equation trigger Reason 3	413
TREA4	Synchrophasor SELOGIC control equation trigger Reason 4	413
TRGTR	Target reset	370
TRIP	Transformer or terminal trip signal asserted	101
TRIPLED	Trip LED on front of relay front panel	0
TRIPS	Terminal S trip output asserted	101
TRIPT	Terminal T trip output asserted	101
TRIPU	Terminal U trip output asserted	101
TRIPW	Terminal W trip output asserted	101
TRIPX	Terminal X trip output asserted	101
TRPXFMR	Transformer trip output asserted	101
TRS	Terminal S trip equation asserted	100
TRT	Terminal T trip equation asserted	100
TRU	Terminal U trip equation asserted	100
TRW	Terminal W trip equation asserted	100
TRX	Terminal X trip equation asserted	100
TRXFMR	Transformer trip equation asserted	100
TSER	Assert while time is based on a valid serial IRIG source	350
TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired	350
TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired	350
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	349
TSSW	High-priority time source switching	350
TSYNC	Assert when ADC sampling is synchronized to an IRIG-B time source	349
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	349
TUPDH	Assert if update source is high-accuracy time source	349
TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted	421
TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted	421
TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted	421
TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted	421
TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted	421
TUTCS	IRIG-B offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	421
U32QE	Negative-sequence phase directional element enabled, Terminal U	24
U32QGE	Negative-sequence ground directional element enabled, Terminal U	24
U32VE	Zero-sequence voltage directional element enabled, Terminal U	24
U50GF	Zero-sequence current above forward threshold, Terminal U	24
U50GR	Zero-sequence current above reverse threshold, Terminal U	24
U50QF	Negative-sequence current above forward threshold, Terminal U	24
U50QR	Negative-sequence current above reverse threshold, Terminal U	24
UF32G	Forward ground directional element asserted, Terminal U	25

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 67 of 69)

Name	Bit Description	Row
UF32P	Forward phase directional element asserted, Terminal U	32
UF32Q	Forward negative-sequence phase directional element asserted, Terminal U	32
UF32QG	Forward negative-sequence ground directional element asserted, Terminal U	24
UF32V	Forward zero-sequence ground directional element asserted, Terminal U	25
ULCLS	Unlatch close Terminal S	105
ULCLT	Unlatch close Terminal T	105
ULCLU	Unlatch close Terminal U	105
ULCLW	Unlatch close Terminal W	105
ULCLX	Unlatch close Terminal X	105
ULTRS	Unlatch Terminal S trip	102
ULTRT	Unlatch Terminal T trip	102
ULTRU	Unlatch Terminal U trip	102
ULTRW	Unlatch Terminal W trip	102
ULTRX	Unlatch Terminal X trip	102
ULTXFMR	Unlatch transformer trip	102
UPD_BLK	Block updating internal clock period and master time	464
UPD_EN	Enable updating internal clock with selected external time source	350
UR32G	Reverse ground directional element asserted, Terminal U	25
UR32P	Reverse phase directional element asserted, Terminal U	32
UR32Q	Reverse negative-sequence phase directional element asserted, Terminal U	32
UR32QG	Reverse negative-sequence phase directional element asserted, Terminal U	25
UR32V	Reverse zero-sequence ground directional element asserted, Terminal U	25
VALARMV	Voltage alarm Terminal V	109
VALARMZ	Voltage alarm Terminal Z	109
VB001–VB008	Virtual Bit 001–Virtual Bit 008	411
VB009–VB016	Virtual Bit 009–Virtual Bit 016	410
VB017–VB024	Virtual Bit 017–Virtual Bit 024	409
VB025–VB032	Virtual Bit 025–Virtual Bit 032	408
VB033–VB040	Virtual Bit 033–Virtual Bit 040	407
VB041–VB048	Virtual Bit 041–Virtual Bit 048	406
VB049–VB056	Virtual Bit 049–Virtual Bit 056	405
VB057–VB064	Virtual Bit 057–Virtual Bit 064	404
VB065–VB072	Virtual Bit 065–Virtual Bit 072	403
VB073–VB080	Virtual Bit 073–Virtual Bit 080	402
VB081–VB088	Virtual Bit 081–Virtual Bit 088	401
VB089–VB096	Virtual Bit 089–Virtual Bit 096	400
VB097–VB104	Virtual Bit 097–Virtual Bit 104	399
VB105–VB112	Virtual Bit 105–Virtual Bit 112	398
VB113–VB120	Virtual Bit 113–Virtual Bit 120	397
VB121–VB128	Virtual Bit 121–Virtual Bit 128	396
VB129–VB136	Virtual Bit 129–Virtual Bit 136	395

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 68 of 69)

Name	Bit Description	Row
VB137–VB144	Virtual Bit 137–Virtual Bit 144	394
VB145–VB152	Virtual Bit 145–Virtual Bit 152	393
VB153–VB160	Virtual Bit 153–Virtual Bit 160	392
VB161–VB168	Virtual Bit 161–Virtual Bit 168	391
VB169–VB176	Virtual Bit 169–Virtual Bit 176	390
VB177–VB184	Virtual Bit 177–Virtual Bit 184	389
VB185–VB192	Virtual Bit 185–Virtual Bit 192	388
VB193–VB200	Virtual Bit 193–Virtual Bit 200	387
VB201–VB208	Virtual Bit 201–Virtual Bit 208	386
VB209–VB216	Virtual Bit 209–Virtual Bit 216	385
VB217–VB224	Virtual Bit 217–Virtual Bit 224	384
VB225–VB232	Virtual Bit 225–Virtual Bit 232	383
VB233–VB240	Virtual Bit 233–Virtual Bit 240	382
VB241–VB248	Virtual Bit 241–Virtual Bit 248	381
VB249–VB256	Virtual Bit 249–Virtual Bit 256	380
VPOLV	Polarizing voltage available, Terminal V	109
VPOLZ	Polarizing voltage available, Terminal Z	109
W32QE	Negative-sequence phase directional element enabled, Terminal W	26
W32QGE	Negative-sequence ground directional element enabled, Terminal W	26
W32VE	Zero-sequence voltage directional element enabled, Terminal W	26
W50GF	Zero-sequence current above forward threshold, Terminal W	26
W50GR	Zero-sequence current above reverse threshold, Terminal W	26
W50QF	Negative-sequence current above forward threshold, Terminal W	26
W50QR	Negative-sequence current above reverse threshold, Terminal W	26
WF32G	Forward ground directional element asserted, Terminal W	27
WF32P	Forward phase directional element asserted, Terminal W	33
WF32Q	Forward negative-sequence phase directional element asserted, Terminal W	33
WF32QG	Forward negative-sequence ground directional element asserted, Terminal W	26
WF32V	Forward zero-sequence ground directional element asserted, Terminal W	27
WFLTA	Windowed fault detector asserted, A-Phase	6
WFLTB	Windowed fault detector asserted, B-Phase	6
WFLTC	Windowed fault detector asserted, C-Phase	6
WR32G	Reverse ground directional element asserted, Terminal W	27
WR32P	Reverse phase directional element asserted, Terminal W	33
WR32Q	Reverse negative-sequence phase directional element asserted, Terminal W	33
WR32QG	Reverse negative-sequence phase directional element asserted, Terminal W	27
WR32V	Reverse zero-sequence ground directional element asserted, Terminal W	27
X32QE	Negative-sequence phase directional element enabled, Terminal X	28
X32QGE	Negative-sequence ground directional element enabled, Terminal X	28
X32VE	Zero-sequence voltage directional element enabled, Terminal X	28
X50GF	Zero-sequence current above forward threshold, Terminal X	28

Table 11.1   Alphabetical List of Relay Word Bits (Sheet 69 of 69)

Name	Bit Description	Row
X50GR	Zero-sequence current above reverse threshold, Terminal X	28
X50QF	Negative-sequence current above forward threshold, Terminal X	28
X50QR	Negative-sequence current above reverse threshold, Terminal X	28
XF32G	Forward ground directional element asserted, Terminal X	29
XF32P	Forward phase directional element asserted, Terminal X	34
XF32Q	Forward negative-sequence phase directional element asserted, Terminal X	34
XF32QG	Forward negative-sequence ground directional element asserted, Terminal X	28
XF32V	Forward zero-sequence ground directional element asserted, Terminal X	29
XR32G	Reverse ground directional element asserted, Terminal X	29
XR32P	Reverse phase directional element asserted, Terminal X	34
XR32Q	Reverse negative-sequence phase directional element asserted, Terminal X	34
XR32QG	Reverse negative-sequence phase directional element asserted, Terminal X	29
XR32V	Reverse zero-sequence ground directional element asserted, Terminal X	29
YEAR1	IRIG-B year information (add 1 years if bit asserted)	420
YEAR10	IRIG-B year information (add 10 years if bit asserted)	420
YEAR2	IRIG-B year information (add 2 years if bit asserted)	420
YEAR20	IRIG-B year information (add 20 years if bit asserted)	420
YEAR4	IRIG-B year information (add 4 years if bit asserted)	420
YEAR40	IRIG-B year information (add 40 years if bit asserted)	420
YEAR8	IRIG-B year information (add 8 years if bit asserted)	420
YEAR80	IRIG-B year information (add 80 years if bit asserted)	420

Row List

Table 11.2   Row List of Relay Word Bits (Sheet 1 of 23)

Name	Bit Description	Row
Enable and Tripping Bits		
EN	Enable LED on relay front panel	0
TRIPLED	Trip LED on front of relay front panel	0
TLED_xx	Target LED (01–24) on relay front panel	1–3
Phase Differential Elements 1		
E87Tm[a]	Terminal m currents included in differential zone	4
87T_Mp[b]	Sufficient differential current to enable non-three-legged transformer waveshape logic, p-Phase	4
CON	External fault detected	5
CONp[b]	External fault detected, p-Phase	5
87T_S	Dwell periods identified in differential current, three-legged transformer	5
87T_Sp[b]	Dwell periods identified in differential current, non-three-legged transformer, p-Phase	5
GFLTp[b]	Instantaneous fault detector asserted, p-Phase	6
WFLTp[b]	Windowed fault detector asserted, p-Phase	6

Table 11.2 Row List of Relay Word Bits (Sheet 2 of 23)

Name	Bit Description	Row
87T_BPx	Bipolar low-/high-set (1, 2) signature detected	6
IFLTp[b]	Internal fault detected, p-Phase	7
87T_B1p[b]	Bipolar low-set signature detected in operate current, p-Phase	7
87WS	Waveshape-based tripping element operated (87R OR 87U)	7
87pHB[b]	Harmonic-blocked phase differential element asserted (no security timer), p-Phase	8
87pHR[b]	Harmonic-restrained phase differential element asserted (no security timer), p-Phase	8
87XBK5	Fifth-harmonic cross blocking asserted	8
87T_SF	Magnetizing inrush current detected by waveshape logic (three-legged transformer)	9
87T_SFp[b]	Magnetizing inrush current detected by waveshape logic, p-Phase (non-three-legged transformer)	9
87U	Unrestrained differential element operated	9
87Up[b]	Unrestrained differential overcurrent element operated, p-Phase	9
P87p[b]	Restrained differential element asserted (no security timer), p-Phase	10
87R	Phase percentage-restrained differential element operated	10
87Rp[b]	Phase-restrained differential element operated, p-Phase	10
87T_M	Sufficient differential current to enable three-legged transformer waveshape logic	10
87pBK2[b]	Second- and fourth-harmonic blocking asserted, p-Phase	11
87pBK5[b]	Fifth-harmonic blocking asserted, p-Phase	11
87QB	Block negative-sequence differential element	11
87XBK2	Second- and fourth-harmonic cross blocking asserted	11
CTUp[b]	Current transformer in unsaturated state following an external fault, p-Phase	12
TH5AD	Fifth-harmonic delayed alarm asserted	12
TH5AP	Fifth-harmonic instantaneous alarm asserted	12
87T_B2p[b]	Bipolar high-set signature detected in operate current, p-Phase	12
DIRBLKm[a]	Block phase and ground directional Element m	75
EFDTp	EFD extension timer output, p-Phase	75
Negative-Sequence Differential Elements		
87Q	Negative-sequence differential element operated	13
87PQ	Minimum pickup and slope conditions satisfied for negative-sequence differential element	13
Restricted Earth Fault Elements		
NDREFx	Nondirectional REF Element (1–3) enabled	14, 16, 18
REF50x	Neutral (operating current) Instantaneous Overcurrent REF Element (1–3) picked up	14, 16, 18
REF50Tx	Neutral Instantaneous Overcurrent REF Element (1–3) timed out	14, 16, 18
REF51Tx	REF Element (1–3) TOC element timed out	14, 16, 18
RF51TCx	Inverse-Time Neutral Overcurrent REF Element (1–3) enabled	14, 16, 18
REFFx	Earth Fault Inside REF Element (1–3) zone	14, 16, 18
REFRx	Earth Fault Outside REF Element (1–3) zone	14, 16, 18
TCREFx	REF Element (1–3) enabled	14, 16, 18
REF51xP	REF Element (1–3) TOC element picked up	15, 17, 19
REF51Rx	REF Element (1–3) TOC element reset	15, 17, 19

Table 11.2 Row List of Relay Word Bits (Sheet 3 of 23)

Name	Bit Description	Row
Ground Directional Elements		
m32QE[a]	Negative-sequence phase directional element enabled, Terminal m	20, 22, 24, 26, 28
m32QGE[a]	Negative-sequence ground directional element enabled, Terminal m	20, 22, 24, 26, 28
m32VE[a]	Zero-sequence voltage directional element enabled, Terminal m	20, 22, 24, 26, 28
m50GF[a]	Zero-sequence current above forward threshold, Terminal m	20, 22, 24, 26, 28
m50GR[a]	Zero-sequence current above reverse threshold, Terminal m	20, 22, 24, 26, 28
m50QF[a]	Negative-sequence current above forward threshold, Terminal m	20, 22, 24, 26, 28
m50QR[a]	Negative-sequence current above reverse threshold, Terminal m	20, 22, 24, 26, 28
mF32QG[a]	Forward negative-sequence ground directional element asserted, Terminal m	20, 22, 24, 26, 28
mF32G[a]	Forward ground directional element asserted, Terminal m	21, 23, 25, 27, 29
mF32V[a]	Forward zero-sequence ground directional element asserted, Terminal m	21, 23, 25, 27, 29
mR32G[a]	Reverse ground directional element asserted, Terminal m	21, 23, 25, 27, 29
mR32QG[a]	Reverse negative-sequence phase directional element asserted, Terminal m	21, 23, 25, 27, 29
mR32V[a]	Reverse zero-sequence ground directional element asserted, Terminal m	21, 23, 25, 27, 29
Phase Directional Elements		
mF32P[a]	Forward phase directional element asserted, Terminal m	30, 31, 32, 33, 34
mF32Q[a]	Forward negative-sequence phase directional element asserted, Terminal m	30, 31, 32, 33, 34
mR32P[a]	Reverse phase directional element asserted, Terminal m	30, 31, 32, 33, 34
mR32Q[a]	Reverse negative-sequence phase directional element asserted, Terminal m	30, 31, 32, 33, 34
Definite and Directional Overcurrent Elements		
50mP1[a]	Phase Definite-Time Element 1, Terminal m asserted	35, 41, 47, 53, 59
50mP2[a]	Phase Definite-Time Element 2, Terminal m asserted	35, 41, 47, 53, 59
67mP1[a]	Phase Directional/Torque-Controlled Element 1, Terminal m picked up	35, 41, 47, 53, 59
67mP1T[a]	Phase Directional/Torque-Controlled Element 1, Terminal m timed out	35, 41, 47, 53, 59
67mP1TC[a]	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal m	35, 41, 47, 53, 59
67mP2[a]	Phase Directional/Torque-Controlled Element 2, Terminal m picked up	35, 41, 47, 53, 59
67mP2T[a]	Phase Directional/Torque-Controlled Element 2, Terminal m timed out	35, 41, 47, 53, 59
67mP2TC[a]	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal m	35, 41, 47, 53, 59
50mP3[a]	Phase Definite-Time Element 3, Terminal m asserted	36, 42, 48, 54, 60
67mP3[a]	Phase Directional/Torque-Controlled Element 3, Terminal m picked up	36, 42, 48, 54, 60
67mP3T[a]	Phase Directional/Torque-Controlled Element 3, Terminal m timed out	36, 42, 48, 54, 60
67mP3TC[a]	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal m	36, 42, 48, 54, 60
50mQ1[a]	Negative-Sequence Definite-Time Element 1, Terminal m asserted	37, 43, 49, 55, 61
50mQ2[a]	Negative-Sequence Definite-Time Element 2, Terminal m asserted	37, 43, 49, 55, 61
67mQ1[a]	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal m picked up	37, 43, 49, 55, 61
67mQ1T[a]	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal m timed out	37, 43, 49, 55, 61
67mQ1TC[a]	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal m	37, 43, 49, 55, 61
67mQ2[a]	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal m picked up	37, 43, 49, 55, 61
67mQ2T[a]	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal m timed out	37, 43, 49, 55, 61
67mQ2TC[a]	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal m	37, 43, 49, 55, 61
50mQ3[a]	Negative-Sequence Definite-Time Element 3, Terminal m asserted	38, 44, 50, 56, 62

Table 11.2   Row List of Relay Word Bits (Sheet 4 of 23)

Name	Bit Description	Row
67mQ3[a]	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal m picked up	38, 44, 50, 56, 62
67mQ3T[a]	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal m timed out	38, 44, 50, 56, 62
67mQ3TC[a]	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal m	38, 44, 50, 56, 62
50mG1[a]	Residual Definite-time Element 1, Terminal m asserted	39, 45, 51, 57, 63
50mG2[a]	Residual Definite-Time Element 2, Terminal m asserted	39, 45, 51, 57, 63
67mG1[a]	Residual Directional/Torque-Controlled Element 1, Terminal m picked up	39, 45, 51, 57, 63
67mG1T[a]	Residual Directional/Torque-Controlled Element 1, Terminal m timed out	39, 45, 51, 57, 63
67mG1TC[a]	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal m	39, 45, 51, 57, 63
67mG2[a]	Residual Directional/Torque-Controlled Element 2, Terminal m picked up	39, 45, 51, 57, 63
67mG2T[a]	Residual Directional/Torque-Controlled Element 2, Terminal m timed out	39, 45, 51, 57, 63
67mG2TC[a]	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal m	39, 45, 51, 57, 63
50mG3[a]	Residual Definite-Time Element 3, Terminal m asserted	40, 46, 52, 58, 64
67mG3[a]	Residual Directional/Torque-Controlled Element 3, Terminal m picked up	40, 46, 52, 58, 64
67mG3T[a]	Residual Directional/Torque-Controlled Element 3, Terminal m timed out	40, 46, 52, 58, 64
67mG3TC[a]	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal m	40, 46, 52, 58, 64
Inverse-Time Overcurrent Elements		
51MMxx	Inverse-Time Element (01–10) pickup setting outside of specified limits	65–74
51Rxx	Inverse-Time Element (01–10) reset	65–74
51Sxx	Inverse-Time Element (01–10) picked up	65–74
51Txx	Inverse-Time Element (01–10) timed out	65–74
51TCxx	Inverse-Time Element (01–10) enabled	65–74
51TMxx	Inverse-Time Element (01–10) time-dial setting outside of specified limits	65–74
Unbalance Logic		
46mP[a]	Current unbalance detected Terminal m	76, 77
46mT[a]	Current Unbalance Terminal m timed out	76, 77
Under- and Overvoltage Elements		
27xP1	Undervoltage Element (1–5), Level 1 asserted	78–80
27xP1T	Undervoltage Element (1–5), Level 1 timed out	78–80
27xP2	Undervoltage Element (1–5), Level 2 asserted	78–80
27TCx	Undervoltage Element (1–5), torque-control	78–80
59xP1	Overvoltage Element (1–5), Level 1 asserted	81–83
59xP1T	Overvoltage Element (1–5), Level 1 timed out	81–83
59xP2	Overvoltage Element (1–5), Level 2 asserted	81–83
59TCx	Overvoltage Element (1–5), torque-control	81–83
Under- and Overpower Elements		
E32OPxx	Overpower Element (01–10) enabled	84–88
32OPxx	Overpower Element (01–10) picked up	84–88
32OPTxx	Overpower Element (01–10) timed out	84–88
E32UPxx	Underpower Element (01–10) enabled	89–93
32UPxx	Underpower Element (01–10) picked up	89–93
32UPTxx	Underpower Element (01–10) timed out	89–93

Table 11.2   Row List of Relay Word Bits (Sheet 5 of 23)

Name	Bit Description	Row
Frequency Elements		
81D*x*	Definite-time frequency element picked up, Level (1–6)	94–96
81D*x*OVR	Definite-Time Overfrequency Level (1–6)	94–96
81D*x*T	Definite-time over and underfrequency element delay for Level (1–6)	94–96
81D*x*UDR	Definite-Time Underfrequency Level (1–6)	94–96
27B81	Frequency elements blocked because of undervoltage	97
Volts/Hertz Element		
24D1	Volts-per-hertz element Level 1 asserted	98
24D1T	Volts-per-hertz Level 1 timed out	98
24D2R	Volts-per-hertz element Level 2 reset	98
24D2T	Volts-per-hertz Level 2 timed out	98
24TC	Volts-per-hertz predefined element, torque control	98
24U*x*R	User-Defined Volts-Per-Hertz Curve (1–2) reset	99
24U*x*T	User-Defined Volts-Per-Hertz Curve (1–2) timed out	99
24U*x*TC	User-Defined Volts-Per-Hertz Curve (1–2), torque control	99
Breaker Trip and Close Logic Elements		
TR*m*[a]	Terminal *m* trip equation asserted	100
TRXFMR	Transformer trip equation asserted	100
TRIP	Transformer or terminal trip signal asserted	101
TRIP*m*[a]	Terminal *m* trip output asserted	101
TRPXFMR	Transformer trip output asserted	101
ULTR*m*[a]	Unlatch Terminal *m* trip	102
ULTXFMR	Unlatch transformer trip	102
CL*m*[a]	Close breaker Terminal *m* equation	103
CLS*m*[a]	Close breaker Terminal *m* output	104
ULCL*m*[a]	Unlatch close Terminal *m*	105
Open-Phase Detector		
OPH*pm*[a,b]	*p*-Phase, Terminal *m* open	106–108
OPH*m*[a]	Terminal *m* open	106–108
Loss-of-Potential and Polarizing Voltage		
LOP*k*[c]	Loss-of-potential Terminal *k*	109
VALARM*k*[c]	Voltage alarm Terminal *k*	109
VPOL*k*[c]	Polarizing voltage available, Terminal *k*	109
Breaker Failure Elements		
50F*m*[a]	Phase or neutral current above pickup, Terminal *m*	110, 112, 114, 116, 118
ATBFI*m*[a]	Alternate breaker failure initiated, Terminal *m*	110, 112, 114, 116, 118
ATBFT*m*[a]	Alternate breaker failure timer timed out, Terminal *m*	110, 112, 114, 116, 118
BFI*m*[a]	Breaker failure initiated, Terminal *m*	110, 112, 114, 116, 118

Table 11.2   Row List of Relay Word Bits (Sheet 6 of 23)

Name	Bit Description	Row
BFITm[a]	Breaker failure timer timed out, Terminal m	110, 112, 114, 116, 118
EBFITm[a]	Externally initiated breaker failure timer timed out, Terminal m	110, 112, 114, 116, 118
EXBFm[a]	External breaker failure input initiated, Terminal m	110, 112, 114, 116, 118
RTm[a]	Retrip timer timed out/retrip command issued, Terminal m	110, 112, 114, 116, 118
ABFITm[a]	Alternate breaker failure, Terminal m	111, 113, 115, 117, 119
BFISPTm[a]	Breaker failure seal-in timer timed out, Terminal m	111, 113, 115, 117, 119
ENINBFm[a]	Neutral/residual breaker failure function enabled, Terminal m	111, 113, 115, 117, 119
FBFm[a]	Breaker failure asserted/initiated, Terminal m	111, 113, 115, 117, 119
IpmBF[a,b]	p-Phase current above threshold, Terminal m	111, 113, 115, 117, 119
INmBF[a]	Neutral current above threshold, Terminal m	111, 113, 115, 117, 119
52 Status Elements		
52ALm[a]	Breaker alarm, Terminal m	120–121
52CLm[a]	Breaker closed, Terminal m	120–121
89 Disconnect Switch Status		
89AL	Any disconnect alarm	122
89ALxx	Disconnect (01–20) alarm	122–141
89AMxx	Disconnect (01–20) N/O auxiliary contact	122–141
89BMxx	Disconnect (01–20) N/C auxiliary contact	122–141
89CLxx	Disconnect (01–20) closed	122–141
89OIPxx	Disconnect (01–20) operation in progress	122–141
89OPNxx	Disconnect (01–20) open	122–141
89OIP	Any disconnect operation in progress	123
LOCAL	Local front-panel control	124
89CLBxx	Disconnect (01–20) bus-zone protection	142–144
89 Disconnect Switch Open and Close Control		
89CCxx	ASCII Close Disconnect (01–20) command	145–164
89CCMxx	Mimic Disconnect (01–20) close control	145–164
89CLSxx	Disconnect Close (01–20) output	145–164
89OCxx	ASCII Open Disconnect (01–20) command	145–164
89OCMxx	Mimic Disconnect (01–20) open control	145–164
89OPExx	Disconnect Open (01–20) output	145–164
89CCNxx	Close Disconnect (01–20)	146–165
89OCNxx	Open Disconnect (01–20)	146–165

Table 11.2   Row List of Relay Word Bits (Sheet 7 of 23)

Name	Bit Description	Row
89 Disconnect Switch Timers and Breaker Status		
89CBL*xx*	Disconnect (01–20) close block	168–197
89CSI*xx*	Disconnect (01–20) close seal-in timer timed out	168–197
89OIR*xx*	Disconnect (01–20) open immobility timer reset	168–197
89OSI*xx*	Disconnect (01–20) open seal-in timer timed out	168–197
89CIR*xx*	Disconnect (01–20) close immobility timer reset	168–198
89CRS*xx*	Disconnect (01–20) close reset	168–198
89OBL*xx*	Disconnect (01–20) open block	168–198
89ORS*xx*	Disconnect (01–20) open reset	168–198
89CIM*xx*	Disconnect (01–20) close immobility timer timed out	169–198
89OIM*xx*	Disconnect (01–20) open immobility timer timed out	169–198
Breaker Monitor		
B*m*BCWAL[a]	Breaker contact wear alarm, Breaker *m*	200–204
B*m*BITAL[a]	Inactivity time alarm, Breaker *m*	200–204
B*m*ESOAL[a]	Slow electrical operate alarm, Breaker *m*	200–204
B*m*KAIAL[a]	Interrupted rms current alarm, Breaker *m*	200–204
B*m*MRTAL[a]	Motor run time alarm, Breaker *m*	200–204
B*m*MSOAL[a]	Mechanical slow operation alarm, Breaker *m*	200–204
EB*m*MON[a]	Breaker monitoring Terminal *m* enabled	200–204
Thermal Element Bits		
TO*x*_1	Transformer (1–3), Top-Oil Temperature Alarm Level 1	205
TO*x*_2	Transformer (1–3), Top-Oil Temperature Alarm Level 2	205
TO1	Top-Oil Temperature Alarm Level 1	205
TO2	Top-Oil Temperature Alarm Level 2	205
HS*x*_1	Transformer (1–3), hot-spot temperature alarm Level 1	206
HS*x*_2	Transformer (1–3), hot-spot temperature alarm Level 2	206
HS1	Hot-Spot Alarm Level 1	206
HS2	Hot-Spot Alarm Level 2	206
FAA*x*_1	Transformer (1–3), aging insulation acceleration factor alarm, Level 1	207
FAA*x*_2	Transformer (1–3), aging insulation acceleration factor alarm, Level 2	207
FAA1	Aging insulation acceleration factor alarm, Level 1	207
FAA2	Aging insulation acceleration factor alarm, Level 2	207
RLL	Rate of loss-of-life alarm	208
RLL_*x*	Transformer (1–3), rate of loss-of-life alarm	208
TLL	Total loss-of-life alarm	208
TLL_*x*	Transformer (1–3), total-loss-of life alarm	208
CSCM	Cooling coefficient or measurement alarm	209
CSCM_*x*	Transformer (1–3), cooling coefficient or measurement alarm	209
CSE	Cooling stage efficiency alarm	209
CSE_*x*	Transformer (1–3), cooling stage efficiency alarm	209
CSALRM	Cooling stage determination alarm	210

Table 11.2   Row List of Relay Word Bits (Sheet 8 of 23)

Name	Bit Description	Row
MAMB_OK	Ambient temperature measurement RTD healthy	210
MTOx_OK	Transformer (1–3), top-oil temperature measurement RTD healthy	210
TxCS2	Transformer (1–3) cooling stage 2	211
TxCS3	Transformer (1–3) cooling stage 3	211
TRDE	Transformer de-energize	211
RTD Status Bits		
RTDxxOK	RTD (01–12) healthy	212–213
AMB_F	Ambient temperature fault condition	213
TxOIL_F	Transformer (1–3) oil temperature fault condition	213
RTDxxSC	RTD (01–12) short circuited	214–215
RTDxxOC	RTD (01–12) open circuited	216–217
RTDCOMF	SEL-2600 communication failure	218
RTDFL	SEL-2600 RAM failure	218
Through-Fault Monitor		
ETHRFLT	Through-fault element enabled	219
TFLTALp[b]	Through-fault alarm, p-Phase	219
Battery Monitor		
DC1F	DC Channel 1 failed	220
DC1G	DC Channel 1 ground fault detected	220
DC1R	DC Channel 1 excess ripples detected	220
DC1W	DC Channel 1 warning	220
Demand Metering		
DMPxx	Demand Metering Element (01–10) asserted	221–223
EDMxx	Demand Metering Element (01–10) enabled	221–223
52 Open and Close		
CCm[a]	Breaker close command, Terminal m	224–225
OCm[a]	Breaker open command, Terminal m	224–225
Local Control and Supervision Bits		
LBxx	Local Bit (01–32) asserted	227–230
LB_SPxx	Local Bit (01–32) supervision enabled	231–234
LB_DPxx	Local Bit (01–32) status display enabled	235–238
Remote Bits		
RBxx	Remote Bit (01–32) asserted	240–243
Settings Group Bits		
CHSG	Settings group changed	244
SGx	Settings Group (1–6) is active	244
Main Board Inputs		
IN1xx	Input 1xx (xx = 01–07) asserted	248
I/O Board Position B Inputs		
IN2xx	Input 2xx (xx = 01–24) asserted	252–254

Table 11.2   Row List of Relay Word Bits (Sheet 9 of 23)

Name	Bit Description	Row
I/O Board Position C Inputs		
IN3*xx*	Input 3*xx* (*xx* = 01–24) asserted	256–258
Protection SELOGIC Variables		
PSV*xx*	Protection SELOGIC Variable (01–64) asserted	260–267
Protection SELOGIC Latches		
PLT*xx*	Protection SELOGIC Latch (01–32) asserted	268–271
Protection SELOGIC Conditioning Timers		
PCT*xx*Q	Protection SELOGIC Conditioning Timer (01–32) asserted	272–275
Protection SELOGIC Sequencing Timers		
PST*xx*Q	Protection SELOGIC Sequencing Timer (01–32) asserted	276–279
PST*xx*R	Protection SELOGIC Sequencing Timer (01–32) reset	280–283
Protection SELOGIC Counters		
PCN*xx*Q	Protection SELOGIC Counter (01–32) asserted	284–287
PCN*xx*R	Protection SELOGIC Counter (01–32) reset	288–291
Automation SELOGIC Variables		
ASV*xxx*	Automation SELOGIC Variable (001–256) asserted	292–323
Automation SELOGIC Latches		
ALT*xx*	Automation SELOGIC Latch (01–32) asserted	324–327
Automation SELOGIC Sequencing Timers		
AST*xx*Q	Automation SELOGIC Sequencing Timer (01–32) asserted	328–331
AST*xx*R	Automation SELOGIC Sequencing Timer (01–32) reset	332–335
Automation SELOGIC Counters		
ACN*xx*Q	Automation SELOGIC Counter (01–32) asserted	336–339
ACN*xx*R	Automation SELOGIC Counter (01–32) reset	340–343
SELOGIC Error and Status Reporting		
AFRTEXA	Automation SELOGIC control equation first execution after automation settings change	344
AFRTEXP	Automation SELOGIC control equation first execution after protection settings change	344
AUNRLBL	Automation SELOGIC control equation unresolved label	344
MATHERR	SELOGIC control equation math error	344
PFRTEX	Protection SELOGIC control equation first execution	344
PUNRLBL	Protection SELOGIC control equation unresolved label	344
Alarms and Jumpers		
BADPASS	Invalid password attempt alarm	345
GRPSW	Pulsed alarm for group switches	345
HALARM	Hardware alarm	345
HALARMA	Pulse stream for unacknowledged diagnostic warnings	345
HALARML	Latched alarm for diagnostic failures	345
HALARMP	Pulsed alarm for diagnostic warnings	345
SALARM	Software alarm	345
SETCHG	Pulsed alarm for settings changes	345
ACCESS	A user is logged in at Access Level B or above	346

Table 11.2   Row List of Relay Word Bits (Sheet 10 of 23)

Name	Bit Description	Row
ACCESSP	Pulsed alarm for logins to Access Level B or above	346
BRKENAB	Breaker control enable jumper is installed	346
PASSDIS	Password disable jumper is installed	346
Synchrophasor Configuration Error		
SPCER1	Synchrophasor configuration error on Port 1	347
SPCER2	Synchrophasor configuration error on Port 2	347
SPCER3	Synchrophasor configuration error on Port 3	347
SPCERF	Synchrophasor configuration error on Port F	347
Frequency Calculation		
EAFSRC	Alternate frequency source (SELOGIC control equation)	348
FREQFZ	Assert if relay is not calculating frequency	348
FREQOK	Assert if relay is estimating frequency	348
Time and Date Management		
PMDOK	Assert if data acquisition system is operating correctly	349
TIRIG	Assert while time is based on IRIG for both mark and value	349
TSOK	Assert if current time source accuracy is sufficient for synchronized phasor measurements	349
TSYNC	Assert when ADC sampling is synchronized to an IRIG-B time source	349
TSYNCA	Assert while the time mark from time source or fixed internal source is not synchronized	349
TUPDH	Assert if update source is high-accuracy time source	349
BLKLPTS	Block low-priority source from updating relay time	350
UPD_EN	Enable updating internal clock with selected external time source	350
TLOCAL	Relay calendar clock and ADC sampling synchronized to non-C37.118-compliant, high-accuracy IRIG-B time source	350
TPLLEXT	Update PLL using external signal	350
TSSW	High-priority time source switching	350
TGLOBAL	Relay calendar clock and ADC sampling synchronized to C37.118 high-accuracy IRIG-B time source	350
TSNTPP	Asserts if time was synchronized with primary NTP server before SNTP time-out period expired	350
TSNTPB	Asserts if time was synchronized with backup NTP server before SNTP time-out period expired	350
TPTP	Assert while time is based on a valid PTP source	351
TBNC	Assert while time is based on a valid BNC IRIG source	351
TSER	Assert while time is based on a valid serial IRIG source	351
BNC_BNP	Bad jitter on BNC port and the IRIG-B signal is lost afterwards	464
BNC_OK	IRIG-B signal from BNC port is available and has sufficient quality	464
BNC_RST	Disqualify BNC IRIG-B high-accuracy time source	464
BNC_SET	Qualify BNC IRIG-B high-accuracy time source	464
SER_OK	IRIG-B signal from serial Port 1 is available and has sufficient quality	464
SER_RST	Disqualify serial IRIG-B high-accuracy time source	464
SER_SET	Qualify serial IRIG-B high-accuracy time source	464
UPD_BLK	Block updating internal clock period and master time	464

Table 11.2   Row List of Relay Word Bits (Sheet 11 of 23)

Name	Bit Description	Row
BNC_TIM	A valid IRIG-B time source is detected on BNC port	465
SER_BNP	Bad jitter on serial port and the IRIG-B signal is lost afterwards	465
SER_TIM	A valid IRIG-B time source is detected on serial port	465
PTP_TIM	A valid PTP time source is detected	465
PTP_SET	Qualify PTP high-accuracy time source	465
PTP_RST	Disqualify PTP high-accuracy time source	465
PTP_OK	PTP is available and has sufficient quality	465
P5ABSW	Port 5A or 5B has just become active	465
PTPSYNC	Synchronized to high-quality PTP source	466
PTP_BNP	Bad jitter on PTP signals and the PTP signal is lost afterwards	466
SERSYNC	Synchronized to high-quality serial IRIG source	466
BNCSYNC	Synchronized to high-quality BNC IRIG source	466
Main Board Outputs		
OUT1xx	Output 1xx (xx = 01–08) asserted	352
I/O Board Position B Outputs		
OUT2xx	Output 2xx (xx = 01–16) asserted	356–357
I/O Board Position C Outputs		
OUT3xx	Output 3xx (xx = 01–16) asserted	358–359
Pushbuttons		
PBxx	Pushbutton (1–12) asserted	360–361
PBxx_PUL	Pushbutton (1–12) pulsed for 1 processing interval	362–363
Pushbutton LED Bits		
PBxx_LED	Pushbutton (1–12) LED illuminated	364–365
Data Reset Bits		
RST_BKm[a]	Reset Breaker m monitoring	368
RST_DEM	Reset demand metering	368
RST_ENE	Reset energy metering	368
RST_PDM	Reset peak demand metering	368
RST_BAT	Reset battery monitoring	369
RST_HAL	Reset HALARMA	369
RSTDNPE	Reset DNP fault summary data	369
RSTTRGT	Reset front-panel targets	369
Target Logic Bits		
ER	Event report triggered	370
FAULT	Fault detected	370
TRGTR	Target reset	370
Mirrored Bits		
RMBxA	Received Mirrored Bits (1–8), Channel A	372
TMBxA	Transmitted Mirrored Bits (1–8), Channel A	373
RMBxB	Received Mirrored Bits (1–8), Channel B	374
TMBxB	Transmitted Mirrored Bits (1–8), Channel B	375

Table 11.2 Row List of Relay Word Bits (Sheet 12 of 23)

Name	Bit Description	Row
ANOKA	Analog transfer on MIRRORED BITS Channel A	376
CBADA	Unavailability threshold exceeded for normal MIRRORED BITS communication, Channel A	376
DOKA	MIRRORED BITS Channel A in normal mode	376
LBOKA	MIRRORED BITS channel in loopback mode, Channel A	376
RBADA	Outage too large for normal MIRRORED BITS communication, Channel A	376
ROKA	MIRRORED BITS Channel A normal status in non-loopback mode	376
ANOKB	Analog transfer on MIRRORED BITS Channel B	377
CBADB	Unavailability threshold exceeded for normal MIRRORED BITS communication, Channel B	377
DOKB	MIRRORED BITS Channel B in normal mode	377
LBOKB	MIRRORED BITS channel in loopback mode, Channel B	377
RBADB	Outage too large for normal MIRRORED BITS communication, Channel B	377
ROKB	MIRRORED BITS Channel B normal status in non-loopback mode	377
Test Bits		
LPHDSIM	IEC 61850 logical node for physical device simulation	378
TESTDB	Database test bit	378
TESTDB2	Enhanced label-based test bit	378
TESTFM	Fast Meter test bit	378
TESTPUL	Pulse test bit	378
Virtual Bits		
VB*xxx*	Virtual Bit (001–256)	380–411
Fast SER Enable Bits		
FSERP*x*	Fast SER enabled for Port (1, 2, 3, or 5)	412
FSERPF	Fast SER enabled for front port	412
Synchrophasor SELOGIC and Frequency OK Bits		
FROKPM	Synchrophasor frequency measurement OK	413
PMTEST	Synchrophasor test mode	413
PMTRIG	Synchrophasor SELOGIC control equation trigger	413
TREA*x*	Synchrophasor SELOGIC control equation trigger Reason (1–4)	413
RTC Synchrophasor Status Bits		
RTCCFGA	RTC Channel A configuration complete	414
RTCCFGB	RTC Channel B configuration complete	414
RTCDLYA	Max RTC delay exceeded for Channel A	414
RTCDLYB	Max RTC delay exceeded for Channel B	414
RTCROK	Valid aligned RTC data available on all enabled channels	414
RTCSEQA	RTC Channel A data in sequence	414
RTCSEQB	RTC Channel B data in sequence	414
RTCENA	Valid remote synchrophasors received on Channel A	415
RTCENB	Valid remote synchrophasors received on Channel B	415
RTCROKA	Valid aligned RTC data available on Channel A	415
RTCROKB	Valid aligned RTC data available on Channel B	415

Table 11.2   Row List of Relay Word Bits (Sheet 13 of 23)

Name	Bit Description	Row
RTC Remote Digital Status Bits		
RTCAD*xx*	RTC Channel A remote data Bit (01–16)	416–417
RTCBD*xx*	RTC Channel B remote data Bit (01–16)	418–419
IRIG-B Control Bits		
YEAR1	IRIG-B year information (add 1 year if bit asserted)	420
YEAR2	IRIG-B year information (add 2 years if bit asserted)	420
YEAR4	IRIG-B year information (add 4 years if bit asserted)	420
YEAR8	IRIG-B year information (add 8 years if bit asserted)	420
YEAR10	IRIG-B year information (add 10 years if bit asserted)	420
YEAR20	IRIG-B year information (add 20 years if bit asserted)	420
YEAR40	IRIG-B year information (add 40 years if bit asserted)	420
YEAR80	IRIG-B year information (add 80 years if bit asserted)	420
TUTCH	IRIG-B offset half-hour from UTC time, binary, add 0.5 if asserted	421
TUTC1	IRIG-B offset hours from UTC time, binary, add 1 if asserted	421
TUTC2	IRIG-B offset hours from UTC time, binary, add 2 if asserted	421
TUTC4	IRIG-B offset hours from UTC time, binary, add 4 if asserted	421
TUTC8	IRIG-B offset hours from UTC time, binary, add 8 if asserted	421
TUTCS	IRIG-B offset hours sign from UTC time, subtract the UTC offset if TUTCS is asserted, add otherwise	421
DST	Daylight-saving time	422
DSTP	IRIG-B daylight-saving time pending	422
LPSEC	Leap second is added	422
LPSECP	Leap second pending	422
TQUAL1	Time quality, binary, add 1 when asserted	422
TQUAL2	Time quality, binary, add 2 when asserted	422
TQUAL4	Time quality, binary, add 4 when asserted	422
TQUAL8	Time quality, binary, add 8 when asserted	422
Ethernet Switch		
LINK5A	Link status of the Port 5A connection	424
LINK5B	Link status of the Port 5B connection	424
LINK5C	Link status of the Port 5C connection	424
LINK5D	Link status of the Port 5D connection	424
LNKFAIL	Link status of the active port	424
P5ASEL	Port 5A active/inactive	425
P5BSEL	Port 5B active/inactive	425
P5CSEL	Port 5C active/inactive	425
P5DSEL	Port 5D active/inactive	425
Signal Profiling		
SPEN	Signal profiling enabled	426
DNP Event Lock		
EVELOCK	Lock DNP events	427

Table 11.2   Row List of Relay Word Bits (Sheet 14 of 23)

Name	Bit Description	Row
Fast Operate Transmit Bits		
FOPF_xx	Port F (front-panel) Fast Operate transmit Bit (01–32)	428–431
FOP1_xx	Port 1 Fast Operate transmit Bit (01–32)	432–435
FOP2_xx	Port 2 Fast Operate transmit Bit (01–32)	436–439
FOP3_xx	Port 3 Fast Operate transmit Bit (01–32)	440–443
Synchronism Check		
FASTm[a]	Breaker m synchronizing voltage slipping faster than polarizing voltage	444
SLOWm[a]	Breaker m synchronizing voltage slipping slower than polarizing voltage	444–445
25A1m[a]	Breaker m voltage within sync Angle 1 window uncompensated	445
25A2m[a]	Breaker m voltage within sync Angle 2 window uncompensated	445–446
SFZBKm[a]	Breaker m slip frequency is less than 5 MHz	446–447
SFBKm[a]	Breaker m slip frequency is within acceptable slip frequency window	447
25WC1m[a]	Breaker m voltages within sync Angle 1 window compensated and unsupervised	448
25WC2m[a]	Breaker m voltages within sync Angle 2 window compensated and unsupervised	448–449
25C1m[a]	Breaker m voltages within sync Angle 1 window compensated	449
25C2m[a]	Breaker m voltages within sync Angle 2 window compensated	449–450
59VP	Polarizing voltage within healthy voltage window	450
ALTSm[a]	Breaker m alternate synchronizing voltage source selected (SELOGIC control equation)	450–451
59VDFm[a]	Breaker m synchronizing voltage difference less than limit	451
BSYNBKm[a]	Breaker m synchronism check blocked	452
25ENBKm[a]	Breaker m synchronism check enabled	452–453
59VSm[a]	Breaker m synchronizing voltage within healthy voltage window	453
Faulted Phase and Terminal Identification Logic		
PHp_m[a, b]	p-Phase involved in the fault, Terminal m	454–455
GROUNDm[a]	Ground involved in the fault, Terminal m	455–456
Fault Identification Logic		
FIDEN_m[a]	FIDEN logic enabled, Terminal m	457
FSA_m[a]	A-Phase sector fault (AG or BCG fault), Terminal m	457–458
FSB_m[a]	B-Phase sector fault (BG or CAG fault), Terminal m	458
FSC_m[a]	C-Phase sector fault (CG or ABG fault), Terminal m	458–459
Phase Differential Elements 2		
87BPH	High-set bipolar differential overcurrent condition asserted	460
87BPHp	High-set bipolar differential overcurrent condition asserted, p-Phase	460
87BPL	Low-set bipolar differential overcurrent condition asserted	460
87BPLp	Low-set bipolar differential overcurrent condition asserted, p-Phase	460
87HBPp	Minimum pickup and slope conditions satisfied for harmonic-blocked phase differential, p-Phase	461
87HRPp	Minimum pickup and slope conditions satisfied for harmonic-restrained phase differential, p-Phase	461
87T	Transformer differential element operated (87R OR 87Q OR 87U)	461
87UFp	Unrestrained differential element operated from filtered current, p-Phase	462
87UNBL	Waveshape-based inrush unblocking condition asserted	463

Table 11.2   Row List of Relay Word Bits (Sheet 15 of 23)

Name	Bit Description	Row
87UNBL*p*	Waveshape-based inrush unblocking condition asserted, *p*-Phase	463
87UR*p*	Unrestrained differential element operated from raw current, *p*-Phase	462
87WB	Magnetizing inrush current detected by waveshape logic	463
87WB*p*	Magnetizing inrush current detected by waveshape logic, *p*-Phase	463
Remote Axion Status		
IO500OK	Communications status of Interface Board 500 when installed or commissioned	467
IO400OK	Communications status of Interface Board 400 when installed or commissioned	467
IO300OK	Communications status of Interface Board 300 when installed or commissioned	467
Instantaneous Metering		
LD_*p*PF*m*[a, b]	Leading power factor, *p*-phase, Terminal *m*	480–484
LD_3PF*m*[a]	Leading three-phase power factor, Terminal *m*	480–484
LG_*p*PF*m*[a, b]	Lagging power factor, *p*-phase, Terminal *m*	480–484
LG_3PF*m*[a]	Lagging three-phase power factor, Terminal *m*	480–484
LD*p*PF*qp*[a, d]	Leading power factor, *p*-phase, combined terminals *qp*	485–488
LD3PF*qp*[d]	Leading three-phase power factor, combined terminals *qp*	485–488
LG*p*PF*qp*[a, d]	Lagging power factor, *p*-phase, combined terminals *qp*	485–488
LG3PF*qp*[d]	Lagging three-phase power factor, combined terminals *qp*	485–488
Bay Control Disconnect Timers and Breaker Status		
52SRACK	Breaker S rack position	489
52TRACK	Breaker T rack position	489
52URACK	Breaker U rack position	489
52WRACK	Breaker W rack position	489
52XRACK	Breaker X rack position	489
52STEST	Breaker S test position	489
52TTEST	Breaker T test position	489
52UTEST	Breaker U test position	489
52WTEST	Breaker W test position	490
52XTEST	Breaker X test position	490
Combined Terminal Ground Directional Elements		
150QF	Negative-sequence current above forward threshold, Terminal ST	492
150QR	Negative-sequence current above reverse threshold, Terminal ST	492
132QE	Negative-sequence phase directional element enabled, Terminal ST	492
132QGE	Negative-sequence ground directional element enabled, Terminal ST	492
150GF	Zero-sequence current above forward threshold, Terminal ST	492
150GR	Zero-sequence current above reverse threshold, Terminal ST	492
132VE	Zero-sequence voltage directional element enabled, Terminal ST	492
1F32QG	Forward negative-sequence ground directional element asserted, Terminal ST	492
1R32QG	Reverse negative-sequence phase directional element asserted, Terminal ST	493
1F32V	Forward zero-sequence ground directional element asserted, Terminal ST	493
1R32V	Reverse zero-sequence ground directional element asserted, Terminal ST	493
1F32G	Forward ground directional element asserted, Terminal ST	493

Table 11.2 Row List of Relay Word Bits (Sheet 16 of 23)

Name	Bit Description	Row
1R32G	Reverse ground directional element asserted, Terminal ST	493
*	Reserved	493
*	Reserved	493
*	Reserved	493
250QF	Negative-sequence current above forward threshold, Terminal TU	494
250QR	Negative-sequence current above reverse threshold, Terminal TU	494
232QE	Negative-sequence phase directional element enabled, Terminal TU	494
232QGE	Negative-sequence ground directional element enabled, Terminal TU	494
250GF	Zero-sequence current above forward threshold, Terminal TU	494
250GR	Zero-sequence current above reverse threshold, Terminal TU	494
232VE	Zero-sequence voltage directional element enabled, Terminal TU	494
2F32QG	Forward negative-sequence ground directional element asserted, Terminal TU	494
2R32QG	Reverse negative-sequence phase directional element asserted, Terminal TU	495
2F32V	Forward zero-sequence ground directional element asserted, Terminal TU	495
2R32V	Reverse zero-sequence ground directional element asserted, Terminal TU	495
2F32G	Forward ground directional element asserted, Terminal TU	495
2R32G	Reverse ground directional element asserted, Terminal TU	495
*	Reserved	495
*	Reserved	495
*	Reserved	495
350QF	Negative-sequence current above forward threshold, Terminal UW	496
350QR	Negative-sequence current above reverse threshold, Terminal UW	496
332QE	Negative-sequence phase directional element enabled, Terminal UW	496
332QGE	Negative-sequence ground directional element enabled, Terminal UW	496
350GF	Zero-sequence current above forward threshold, Terminal UW	496
350GR	Zero-sequence current above reverse threshold, Terminal UW	496
332VE	Zero-sequence voltage directional element enabled, Terminal UW	496
3F32QG	Forward negative-sequence ground directional element asserted, Terminal UW	496
3R32QG	Reverse negative-sequence phase directional element asserted, Terminal UW	497
3F32V	Forward zero-sequence ground directional element asserted, Terminal UW	497
3R32V	Reverse zero-sequence ground directional element asserted, Terminal UW	497
3F32G	Forward ground directional element asserted, Terminal UW	497
3R32G	Reverse ground directional element asserted, Terminal UW	497
*	Reserved	497
*	Reserved	497
*	Reserved	497
450QF	Negative-sequence current above forward threshold, Terminal WX	498
450QR	Negative-sequence current above reverse threshold, Terminal WX	498
432QE	Negative-sequence phase directional element enabled, Terminal WX	498
432QGE	Negative-sequence ground directional element enabled, Terminal WX	498
450GF	Zero-sequence current above forward threshold, Terminal WX	498

Table 11.2   Row List of Relay Word Bits (Sheet 17 of 23)

Name	Bit Description	Row
450GR	Zero-sequence current above reverse threshold, Terminal WX	498
432VE	Zero-sequence voltage directional element enabled, Terminal WX	498
4F32QG	Forward negative-sequence ground directional element asserted, Terminal WX	498
4R32QG	Reverse negative-sequence phase directional element asserted, Terminal WX	499
4F32V	Forward zero-sequence ground directional element asserted, Terminal WX	499
4R32V	Reverse zero-sequence ground directional element asserted, Terminal WX	499
4F32G	Forward ground directional element asserted, Terminal WX	499
4R32G	Reverse ground directional element asserted, Terminal WX	499
*	Reserved	499
*	Reserved	499
*	Reserved	499
Combined Terminal Phase Directional Elements		
1F32P	Forward phase directional element asserted, Terminal ST	500
1R32P	Reverse phase directional element asserted, Terminal ST	500
1F32Q	Forward negative-sequence phase directional element asserted, Terminal ST	500
1R32Q	Reverse negative-sequence phase directional element asserted, Terminal ST	500
*	Reserved	500
*	Reserved	500
*	Reserved	500
*	Reserved	500
2F32P	Forward phase directional element asserted, Terminal TU	501
2R32P	Reverse phase directional element asserted, Terminal TU	501
2F32Q	Forward negative-sequence phase directional element asserted, Terminal TU	501
2R32Q	Reverse negative-sequence phase directional element asserted, Terminal TU	501
*	Reserved	501
*	Reserved	501
*	Reserved	501
*	Reserved	501
3F32P	Forward phase directional element asserted, Terminal UW	502
3R32P	Reverse phase directional element asserted, Terminal UW	502
3F32Q	Forward negative-sequence phase directional element asserted, Terminal UW	502
3R32Q	Reverse negative-sequence phase directional element asserted, Terminal UW	502
*	Reserved	502
*	Reserved	502
*	Reserved	502
*	Reserved	502
4F32P	Forward phase directional element asserted, Terminal WX	503
4R32P	Reverse phase directional element asserted, Terminal WX	503
4F32Q	Forward negative-sequence phase directional element asserted, Terminal WX	503
4R32Q	Reverse negative-sequence phase directional element asserted, Terminal WX	503
*	Reserved	503

Table 11.2   Row List of Relay Word Bits (Sheet 18 of 23)

Name	Bit Description	Row
*	Reserved	503
*	Reserved	503
*	Reserved	503
Combined Terminal Definite & Directional Overcurrent Elements		
501P1	Phase definite-time Element 1, Terminal ST asserted	504
671P1TC	Phase directional/torque-control enable definite-time Element 1, Terminal ST	504
671P1	Phase directional/torque-controlled Element 1, Terminal ST picked up	504
671P1T	Phase directional/torque-controlled Element 1, Terminal ST timed out	504
501P2	Phase definite-time Element 2, Terminal ST asserted	504
671P2TC	Phase directional/torque-control enable definite-time Element 2, Terminal ST	504
671P2	Phase directional/torque-controlled Element 2, Terminal ST picked up	504
671P2T	Phase directional/torque-controlled Element 2, Terminal ST timed out	504
501P3	Phase definite-time Element 3, Terminal ST asserted	505
671P3TC	Phase directional/torque-control enable definite-time Element 3, Terminal ST	505
671P3	Phase directional/torque-controlled Element 3, Terminal ST picked up	505
671P3T	Phase directional/torque-controlled Element 3, Terminal ST timed out	505
*	Reserved	505
*	Reserved	505
*	Reserved	505
*	Reserved	505
501Q1	Negative-sequence definite-time Element 1, Terminal ST asserted	506
671Q1TC	Negative-sequence directional/torque-control enable definite-time Element 1, Terminal ST	506
671Q1	Negative-sequence directional/torque-controlled Element 1, Terminal ST picked up	506
671Q1T	Negative-sequence directional/torque-controlled Element 1, Terminal ST timed out	506
501Q2	Negative-sequence definite-time Element 2, Terminal ST asserted	506
671Q2TC	Negative-sequence directional/torque-control enable definite-time Element 2, Terminal ST	506
671Q2	Negative-sequence directional/torque-controlled Element 2, Terminal ST picked up	506
671Q2T	Negative-sequence directional/torque-controlled Element 2, Terminal ST timed out	506
501Q3	Negative-sequence definite-time Element 3, Terminal ST asserted	507
671Q3TC	Negative-sequence directional/torque-control enable definite-time Element 3, Terminal ST	507
671Q3	Negative-sequence directional/torque-controlled Element 3, Terminal ST picked up	507
671Q3T	Negative-sequence directional/torque-controlled Element 3, Terminal ST timed out	507
*	Reserved	507
*	Reserved	507
*	Reserved	507
*	Reserved	507
501G1	Residual definite-time Element 1, Terminal ST asserted	508
671G1TC	Residual directional/torque-control enable definite-time Element 1, Terminal ST	508
671G1	Residual directional/torque-controlled Element 1, Terminal ST picked up	508
671G1T	Residual directional/torque-controlled Element 1, Terminal ST timed out	508
501G2	Residual definite-time Element 2, Terminal ST asserted	508

Table 11.2   Row List of Relay Word Bits (Sheet 19 of 23)

Name	Bit Description	Row
671G2TC	Residual directional/torque-control enable definite-time Element 2, Terminal ST	508
671G2	Residual directional/torque-controlled Element 2, Terminal ST picked up	508
671G2T	Residual directional/torque-controlled Element 2, Terminal ST timed out	508
501G3	Residual definite-time Element 3, Terminal ST asserted	509
671G3TC	Residual directional/torque-control enable definite-time Element 3, Terminal ST	509
671G3	Residual directional/torque-controlled Element 3, Terminal ST picked up	509
671G3T	Residual directional/torque-controlled Element 3, Terminal ST timed out	509
*	Reserved	509
*	Reserved	509
*	Reserved	509
*	Reserved	509
502P1	Phase definite-time Element 1, Terminal TU asserted	510
672P1TC	Phase directional/torque-control enable definite-time Element 1, Terminal TU	510
672P1	Phase directional/torque-controlled Element 1, Terminal TU picked up	510
672P1T	Phase directional/torque-controlled Element 1, Terminal TU timed out	510
502P2	Phase definite-time Element 2, Terminal TU asserted	510
672P2TC	Phase directional/torque-control enable definite-time Element 2, Terminal TU	510
672P2	Phase directional/torque-controlled Element 2, Terminal TU picked up	510
672P2T	Phase directional/torque-controlled Element 2, Terminal TU timed out	510
502P3	Phase definite-time Element 3, Terminal TU asserted	511
672P3TC	Phase directional/torque-control enable definite-time Element 3, Terminal TU	511
672P3	Phase directional/torque-controlled Element 3, Terminal TU picked up	511
672P3T	Phase directional/torque-controlled Element 3, Terminal TU timed out	511
*	Reserved	511
*	Reserved	511
*	Reserved	511
*	Reserved	511
502Q1	Negative-Sequence Definite-Time Element 1, Terminal TU asserted	512
672Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	512
672Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal TU picked up	512
672Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal TU timed out	512
502Q2	Negative-Sequence Definite-Time Element 2, Terminal TU asserted	512
672Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	512
672Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal TU picked up	512
672Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal TU timed out	512
502Q3	Negative-Sequence Definite-Time Element 3, Terminal TU asserted	513
672Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	513
672Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal TU picked up	513
672Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal TU timed out	513
*	Reserved	513
*	Reserved	513

Table 11.2 Row List of Relay Word Bits (Sheet 20 of 23)

Name	Bit Description	Row
*	Reserved	513
*	Reserved	513
502G1	Residual Definite-Time Element 1, Terminal TU asserted	514
672G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal TU	514
672G1	Residual Directional/Torque-Controlled Element 1, Terminal TU picked up	514
672G1T	Residual Directional/Torque-Controlled Element 1, Terminal TU timed out	514
502G2	Residual Definite-Time Element 2, Terminal TU asserted	514
672G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal TU	514
672G2	Residual Directional/Torque-Controlled Element 2, Terminal TU picked up	514
672G2T	Residual Directional/Torque-Controlled Element 2, Terminal TU timed out	514
502G3	Residual Definite-Time Element 3, Terminal TU asserted	515
672G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal TU	515
672G3	Residual Directional/Torque-Controlled Element 3, Terminal TU picked up	515
672G3T	Residual Directional/Torque-Controlled Element 3, Terminal TU timed out	515
*	Reserved	515
*	Reserved	515
*	Reserved	515
*	Reserved	515
503P1	Phase Definite-Time Element 1, Terminal UW asserted	516
673P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	516
673P1	Phase Directional/Torque-Controlled Element 1, Terminal UW picked up	516
673P1T	Phase Directional/Torque-Controlled Element 1, Terminal UW timed out	516
503P2	Phase Definite-Time Element 2, Terminal UW asserted	516
673P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	516
673P2	Phase Directional/Torque-Controlled Element 2, Terminal UW picked up	516
673P2T	Phase Directional/Torque-Controlled Element 2, Terminal UW timed out	516
503P3	Phase Definite-Time Element 3, Terminal UW asserted	517
673P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	517
673P3	Phase Directional/Torque-Controlled Element 3, Terminal UW picked up	517
673P3T	Phase Directional/Torque-Controlled Element 3, Terminal UW timed out	517
*	Reserved	517
*	Reserved	517
*	Reserved	517
*	Reserved	517
503Q1	Negative-Sequence Definite-Time Element 1, Terminal UW asserted	518
673Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	518
673Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal UW picked up	518
673Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal UW timed out	518
503Q2	Negative-Sequence Definite-Time Element 2, Terminal UW asserted	518
673Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	518

Table 11.2   Row List of Relay Word Bits (Sheet 21 of 23)

Name	Bit Description	Row
673Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal UW picked up	518
673Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal UW timed out	518
503Q3	Negative-Sequence Definite-Time Element 3, Terminal UW asserted	519
673Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	519
673Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal UW picked up	519
673Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal UW timed out	519
*	Reserved	519
*	Reserved	519
*	Reserved	519
*	Reserved	519
503G1	Residual Definite-Time Element 1, Terminal UW asserted	520
673G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal UW	520
673G1	Residual Directional/Torque-Controlled Element 1, Terminal UW picked up	520
673G1T	Residual Directional/Torque-Controlled Element 1, Terminal UW timed out	520
503G2	Residual Definite-Time Element 2, Terminal UW asserted	520
673G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal UW	520
673G2	Residual Directional/Torque-Controlled Element 2, Terminal UW picked up	520
673G2T	Residual Directional/Torque-Controlled Element 2, Terminal UW timed out	520
503G3	Residual Definite-Time Element 3, Terminal UW asserted	521
673G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal UW	521
673G3	Residual Directional/Torque-Controlled Element 3, Terminal UW picked up	521
673G3T	Residual Directional/Torque-Controlled Element 3, Terminal UW timed out	521
*	Reserved	521
*	Reserved	521
*	Reserved	521
*	Reserved	521
504P1	Phase Definite-Time Element 1, Terminal WX asserted	522
674P1TC	Phase Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	522
674P1	Phase Directional/Torque-Controlled Element 1, Terminal WX picked up	522
674P1T	Phase Directional/Torque-Controlled Element 1, Terminal WX timed out	522
504P2	Phase Definite-Time Element 2, Terminal WX asserted	522
674P2TC	Phase Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	522
674P2	Phase Directional/Torque-Controlled Element 2, Terminal WX picked up	522
674P2T	Phase Directional/Torque-Controlled Element 2, Terminal WX timed out	522
504P3	Phase Definite-Time Element 3, Terminal WX asserted	523
674P3TC	Phase Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	523
674P3	Phase Directional/Torque-Controlled Element 3, Terminal WX picked up	523
674P3T	Phase Directional/Torque-Controlled Element 3, Terminal WX timed out	523
*	Reserved	523
*	Reserved	523

Table 11.2   Row List of Relay Word Bits (Sheet 22 of 23)

Name	Bit Description	Row
*	Reserved	523
*	Reserved	523
504Q1	Negative-Sequence Definite-Time Element 1, Terminal WX asserted	524
674Q1TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	524
674Q1	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal WX picked up	524
674Q1T	Negative-Sequence Directional/Torque-Controlled Element 1, Terminal WX timed out	524
504Q2	Negative-Sequence Definite-Time Element 2, Terminal WX asserted	524
674Q2TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	524
674Q2	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal WX picked up	524
674Q2T	Negative-Sequence Directional/Torque-Controlled Element 2, Terminal WX timed out	524
504Q3	Negative-Sequence Definite-Time Element 3, Terminal WX asserted	525
674Q3TC	Negative-Sequence Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	525
674Q3	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal WX picked up	525
674Q3T	Negative-Sequence Directional/Torque-Controlled Element 3, Terminal WX timed out	525
*	Reserved	525
*	Reserved	525
*	Reserved	525
*	Reserved	525
504G1	Residual Definite-Time Element 1, Terminal WX asserted	526
674G1TC	Residual Directional/Torque-Control Enable Definite-Time Element 1, Terminal WX	526
674G1	Residual Directional/Torque-Controlled Element 1, Terminal WX picked up	526
674G1T	Residual Directional/Torque-Controlled Element 1, Terminal WX timed out	526
504G2	Residual Definite-Time Element 2, Terminal WX asserted	526
674G2TC	Residual Directional/Torque-Control Enable Definite-Time Element 2, Terminal WX	526
674G2	Residual Directional/Torque-Controlled Element 2, Terminal WX picked up	526
674G2T	Residual Directional/Torque-Controlled Element 2, Terminal WX timed out	526
504G3	Residual Definite-Time Element 3, Terminal WX asserted	527
674G3TC	Residual Directional/Torque-Control Enable Definite-Time Element 3, Terminal WX	527
674G3	Residual Directional/Torque-Controlled Element 3, Terminal WX picked up	527
674G3T	Residual Directional/Torque-Controlled Element 3, Terminal WX timed out	527
*	Reserved	527
*	Reserved	527
*	Reserved	527
*	Reserved	527
Combined Terminals Phase Differential Elements 2		
DIRBLK1	Block Phase and Ground Directional Element ST	528
DIRBLK2	Block Phase and Ground Directional Element TU	528
DIRBLK3	Block Phase and Ground Directional Element UW	528
DIRBLK4	Block Phase and Ground Directional Element WX	528

Table 11.2   Row List of Relay Word Bits (Sheet 23 of 23)

Name	Bit Description	Row
*	Reserved	528
*	Reserved	528
*	Reserved	528
*	Reserved	528
IEC Thermal Elements		
THRLA1	Thermal element, Level 1 alarm	530
THRLT1	Thermal element, Level 1 trip	530
THRLA2	Thermal element, Level 2 alarm	530
THRLT2	Thermal element, Level 2 trip	530
THRLA3	Thermal element, Level 3 alarm	530
THRLT3	Thermal element, Level 3 trip	530
*	Reserved	530
*	Reserved	530
IEC 62850 Mode Control Bits		
SC850TM	SELOGIC control for IEC 61850 Test Mode	532
SC850BM	SELOGIC control for IEC 61850 Blocked Mode	532
*	Reserved	532
*	Reserved	532
*	Reserved	532
*	Reserved	532
*	Reserved	532
*	Reserved	532
Synchronism Check		
59VPm^a	Breaker m Polarizing Voltage within healthy voltage window	536
ALTP$m1^a$	BKm Alternate Reference Source Selection Logic 1 (SELOGIC control equation)	537
ALTP$m2^a$	BKm Alternate Reference Source Selection Logic 2 (SELOGIC control equation)	538
25A1BKm^a	Breaker m voltages within Sync Angle 1	540
25A2BKm^a	Breaker m voltages within Sync Angle 2	541
25WA1m^a	Breaker m voltages within Sync Angle 1 window uncompensated and unsupervised	542
25WA2m^a	Breaker m voltages within Sync Angle 2 window uncompensated and unsupervised	543
Automation SELOGIC Conditioning Timers		
ACTxxQ^e	Automation SELOGIC Conditioning Timer (01–32) asserted	548–551

[a] m = S, T, U, W, X.

[b] p = A, B, C.

[c] k = V, Z.

[d] qp = ST, TU, UW, WX.

[e] xx = 01–32

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Analog Quantities

This section contains tables of the analog quantities available within the SEL-487E relay.

Use *Table 12.1* and *Table 12.2* as a reference for labels in this manual and as a resource for quantities you use in SELOGIC control equation relay settings. *Table 12.1* lists the analog quantities alphabetically, and *Table 12.2* groups the analog quantities by function.

Alphabetical List

Table 12.1   Analog Quantities Sorted Alphabetically (Sheet 1 of 9)

Label	Description	Units
24RPU	Volts/hertz ratio	%
25ANGm[a]	25 Synchronism-check angle difference for Breaker m	° (±180°)
25ANGCm[a]	25 Synchronism-check compensated angle difference for Breaker m	° (±180°)
25SLIPm[a]	25 Synchronism-check slip frequency for Breaker m	Hz
25VPmFA	25 Synchronism-check polarizing voltage angle for Breaker m	° (±180°)
25VPmFM	25 Synchronism-check polarizing voltage magnitude for Breaker m	V (secondary)
25VPFA	25 Synchronism-check polarizing voltage angle	° (±180°)
25VPFM	25 Synchronism-check polarizing voltage magnitude	V (secondary)
25VSmFA[a]	25 Synchronism-check synchronizing voltage angle for Breaker m	° (±180°)
25VSmFM[a]	25 Synchronism-check synchronizing voltage magnitude for Breaker m	V (secondary)
3DPFm[a]	Three-phase displacement power factor, Terminal m	
3DPFqp[b]	Three-phase displacement power factor, comb. Terminals qp	
3I0mA[a]	Instantaneous zero-sequence current angle, Terminal m	° (±180°)
3I0mAC[a]	1-cycle average zero-sequence current angle, Terminal m	° (±180°)
3I0mI[a]	Instantaneous zero-sequence current, imaginary component, Terminal m	A (secondary)
3I0mM	Instantaneous zero-sequence current magnitude, Terminal m	A (secondary)
3I0mMC	1-cycle average zero-sequence current magnitude, Terminal m	A (primary)
3I0mMS	1-second average zero-sequence current magnitude, Terminal m	A (secondary)
3I0mR	Instantaneous zero-sequence current, real component, Terminal m	A (secondary)
3I0qpA[b]	Instantaneous zero-sequence current angle, comb. Terminals qp	° (±180°)
3I0qpAC[b]	1-cycle average zero-sequence current angle, comb. Terminals qp	° (±180°)
3I0qpI[b]	Instantaneous zero-sequence current, imaginary component, comb. Terminals qp	A (secondary)
3I0qpM[b]	Instantaneous zero-sequence current magnitude, comb. Terminals qp	A (secondary)
3I0qpMC[b]	1-cycle average zero-sequence current magnitude, comb. Terminals qp	A (primary)
3I0qpMS[b]	1-second average zero-sequence current magnitude, comb. Terminals qp	A (secondary)

Table 12.1   Analog Quantities Sorted Alphabetically (Sheet 2 of 9)

Label	Description	Units
3I0qpR[b]	Instantaneous zero-sequence current, real component, comb. Terminals qp	A (secondary)
3I2mA[a]	Instantaneous negative-sequence current angle, Terminal m	° (±180°)
3I2mAC[a]	1-cycle average negative-sequence current angle, Terminal m	° (±180°)
3I2mI[a]	Instantaneous negative-sequence current, imaginary component, Terminal m	A (secondary)
3I2mM[a]	Instantaneous negative-sequence current magnitude, Terminal m	A (secondary)
3I2mMC[a]	1-cycle average negative-sequence current magnitude, Terminal m	A (primary)
3I2mMS[a]	1-second average negative-sequence current magnitude, Terminal m	A (secondary)
3I2mR[a]	Instantaneous negative-sequence current, real component, Terminal m	A (secondary)
3I2qpA[b]	Instantaneous negative-sequence current angle, comb. Terminals qp	° (±180°)
3I2qpAC[b]	1-cycle average negative-sequence current angle, comb. Terminals qp	° (±180°)
3I2qpI[b]	Instantaneous negative-sequence current, imaginary component, comb. Terminals qp	A (secondary)
3I2qpM[b]	Instantaneous negative-sequence current magnitude, comb. Terminals qp	A (secondary)
3I2qpMC[b]	1-cycle average negative-sequence current magnitude, comb. Terminals qp	A (primary)
3I2qpMS[b]	1-second average negative-sequence current magnitude, comb. Terminals qp	A (secondary)
3I2qpR[b]	Instantaneous negative-sequence current, real component, comb. Terminals qp	A (secondary)
3PmF[a]	Instantaneous three-phase fundamental active power, Terminal m	W (secondary)
3PmFC[a]	1-cycle average three-phase fundamental active power, Terminal m	MW (primary)
3PmMWhn[a]	Three-phase active energy imported, Terminal m	MWh (primary)
3PmMWhp[a]	Three-phase active energy exported, Terminal m	MWh (primary)
3PmMWhT[a]	Total three-phase active energy, Terminal m	MWh (primary)
3PqpF[b]	Instantaneous three-phase fundamental active power, comb. Terminals qp	W (secondary)
3PqpFC[b]	1-cycle average three-phase fundamental active power, comb. Terminals qp	MW (primary)
3PqpWHN[b]	Three-phase active energy imported, comb. Terminals qp	MWh (primary)
3PqpWHP[b]	Three-phase active energy exported, comb. Terminals qp	MWh (primary)
3PqpWHT[b]	Total three-phase active energy, comb. Terminals qp	MWh (primary)
3QmF[a]	Instantaneous three-phase fundamental reactive power, Terminal m	VAr (secondary)
3QmFC[a]	1-cycle average three-phase fundamental reactive power, Terminal m	MVAr (primary)
3QmMVHN[a]	Three-phase reactive energy imported, Terminal m	MVArh (primary)
3QmMVHP[a]	Three-phase reactive energy exported, Terminal m	MVArh (primary)
3QmMVHT[a]	Total three-phase reactive energy, Terminal m	MVArh (primary)
3QqpF[b]	Instantaneous three-phase fundamental reactive power, comb. Terminals qp	VAr (secondary)
3QqpFC[b]	1-cycle average three-phase fundamental reactive power, comb. Terminals qp	MVAr (primary)
3QqpVHN[b]	Three-phase reactive energy imported, comb. Terminals qp	MVArh (primary)
3QqpVHP[b]	Three-phase reactive energy exported, comb. Terminals qp	MVArh (primary)
3QqpVHT[b]	Total three-phase reactive energy, comb. Terminals qp	MVArh (primary)
3SmF[a]	Instantaneous three-phase fundamental apparent power, Terminal m	VA (secondary)
3SmFC[a]	1-cycle average three-phase fundamental apparent power, Terminal m	MVA (primary)
3SqpF[b]	Instantaneous three-phase fundamental apparent power, comb. Terminals qp	VA (secondary)
3SqpFC[b]	1-cycle average three-phase fundamental apparent power, comb. Terminals qp	MVA (primary)
3V0kA[c]	Instantaneous zero-sequence voltage angle, Terminal k	° (±180°)
3V0kAC[c]	1-cycle average zero-sequence voltage angle, Terminal k	° (±180°)

Table 12.1   Analog Quantities Sorted Alphabetically (Sheet 3 of 9)

Label	Description	Units
3V0kI[c]	Instantaneous zero-sequence voltage, imaginary component, Terminal k	V (secondary)
3V0kM[c]	Instantaneous zero-sequence voltage magnitude, Terminal k	V (secondary)
3V0kMC[c]	1-cycle average zero-sequence voltage magnitude, Terminal k	kV (primary)
3V0kR[c]	Instantaneous zero-sequence voltage, real component, Terminal k	V (secondary)
3V2kA[c]	Instantaneous negative-sequence voltage angle, Terminal k	° (±180°)
3V2kAC[c]	1-cycle average negative-sequence voltage angle, Terminal k	° (±180°)
3V2kI[c]	Instantaneous negative-sequence voltage, imaginary component, Terminal k	V (secondary)
3V2kM[c]	Instantaneous negative-sequence voltage magnitude, Terminal k	V (secondary)
3V2kMC[c]	1-cycle average negative-sequence voltage magnitude, Terminal k	kV (primary)
3V2kR[c]	Instantaneous negative-sequence voltage, real component, Terminal k	V (secondary)
46pm[a, d]	Current unbalance Phase p, Terminal m	%
51P01–51P10	51 Element 1–10 pickup value	A (secondary)
51TD01–51TD10	51 Element 1–10 time-dial setting	
87IOPpC[d]	1-cycle average differential element operating current	pu
87IRTpC[d]	1-cycle average differential element restraint current	pu
ACN01CV–ACN32CV	Automation SELOGIC counter current value	
ACN01PV–ACN32PV	Automation SELOGIC counter preset value	
ACT01DO-ACT32DO	Automation SELOGIC conditioning timer dropout time	s
ACT01PU-ACT32PU	Automation SELOGIC conditioning timer pickup time	s
ACTGRP	Active group setting	
AMV001–AMV256	Automation SELOGIC math variable	
AST01ET–AST32ET	Automation SELOGIC sequencing timer elapsed time	s
AST01PT–AST32PT	Automation SELOGIC sequencing timer preset time	s
BmBCWPp[a, d]	Breaker m breaker-contact wear for Pole p	%
BNCDSJI	BNC port 100PPS data stream jitter	μs
BNCOTJF	Fast converging BNC port ON TIME marker jitter, coarse accuracy	μs
BNCOTJS	Slow converging BNC port ON TIME marker jitter, fine accuracy	μs
BNCTBTW	Time between BNC 100PPS pulses	μs
CTRm[a]	Current transformer ratio for Terminal m	
CTRY1–CTRY3	Current transformer ratio for Terminal Y1–Y3	
CUR_SRC	Current high-accuracy time source	
DCMAX	Maximum DC 1 voltage	V
DCMIN	Minimum DC 1 voltage	V
DCNE	Average negative-to-ground DC 1 voltage	V
DCPO	Average positive-to-ground DC 1 voltage	V
DCRI	AC ripple of DC 1 voltage	V
DDOM	UTC date, day of the month (1–31)	day
DDOW	UTC date, day of the week (1–SU,.., 7–SA)	
DDOY	UTC date, day of the year (1–366)	day
DFDTP	Rate-of-change of frequency	Hz/s
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s

Table 12.1   Analog Quantities Sorted Alphabetically (Sheet 4 of 9)

Label	Description	Units
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s
DLDOM	Local date, day of the month (1–31)	day
DLDOW	Local date, day of the week (1–SU,.., 7–SA)	
DLDOY	Local date, day of the year (1–366)	day
DLMON	Local date, month (1–12)	month
DLYEAR	Local date, year (2000–2200)	year
DM01–DM10	Demand metering value	A (secondary)
DMM01–DMM10	Demand metering maximum value	A (secondary)
DMON	UTC date, month (1–12)	month
DPFpm[a, d]	Phase displacement power factor, Phase p, Terminal m	
DPFpqp[b, d]	Phase displacement power factor, Phase p, comb. Terminals qp	
DYEAR	UTC date, year (2000–2200)	year
FOSPM	Fraction of second of the synchrophasor data packet	s
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s
FREQ	Tracking frequency	Hz
FREQP	Frequency for over- and underfrequency elements	Hz
FREQPM	Frequency for synchrophasor data	Hz
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz
IpmFA[a, d]	Instantaneous filtered-phase current angle, Phase p, Terminal m	° (±180°)
IpmFAC[a, d]	1-cycle average filtered-phase current angle, Phase p, Terminal m	° (±180°)
IpmFI[a, d]	Instantaneous filtered-phase current, imaginary component, Phase p, Terminal m	A (secondary)
IpmFM[a, d]	Instantaneous filtered-phase current magnitude, Phase p, Terminal m	A (secondary)
IpmFMC[a, d]	1-cycle average filtered-phase current magnitude, Phase p, Terminal m	A (primary)
IpmFR[a, d]	Instantaneous filtered-phase current, real component, Phase p, Terminal m	A (secondary)
IpmRC[a, d]	1-cycle average rms phase current, Phase p, Terminal m	A (primary)
IpmRMS[a, d]	Instantaneous rms phase-current magnitude, Phase p, Terminal m	A (secondary)
IpmRS[a, d]	1-second average rms phase current, Phase p, Terminal m	A (secondary)
IpqpFA[b, d]	Instantaneous filtered-phase current angle, Phase p, comb. Terminals qp	° (±180°)
IpqpFAC[b, d]	1-cycle average filtered-phase current angle, Phase p, comb. Terminals qp	° (±180°)
IpqpFI[b, d]	Instantaneous filtered-phase current, imaginary component, Phase p, comb. Terminals qp	A (secondary)
IpqpFM[b, d]	Instantaneous filtered-phase current magnitude, Phase p, comb. Terminals qp	A (secondary)
IpqpFMC[b, d]	1-cycle average filtered-phase current magnitude, Phase p, comb. Terminals qp	A (primary)
IpqpFR[b, d]	Instantaneous filtered-phase current, real component, Phase p, comb. Terminals qp	A (secondary)
IpqpRC[b, d]	1-cycle average rms phase current, Phase p, comb. Terminals qp	A (primary)
IpqpRMS[b, d]	Instantaneous rms phase current, Phase p, comb. Terminals qp	A (secondary)
IpqpRS[b, d]	1-second average rms phase current, Phase p, comb. Terminals qp	A (secondary)
IprPMA[d, e]	Synchrophasor current angle, Phase p, Terminal r	° (±180°)
IprPMAD[d, e]	Synchrophasor current angle, Phase p, Terminal r, delayed for RTC alignment	° (±180°)
IprPMI[d, e]	Synchrophasor current imaginary component, Phase p, Terminal r	A (primary)
IprPMID[d, e]	Synchrophasor current imaginary component, Phase p, Terminal r, delayed for RTC alignment	A (primary)

Table 12.1   Analog Quantities Sorted Alphabetically (Sheet 5 of 9)

Label	Description	Units
IprPMM[d, e]	Synchrophasor current magnitude, Phase p, Terminal r	A (primary)
IprPMMD[d, e]	Synchrophasor current magnitude, Phase p, Terminal r, delayed for RTC alignment	A (primary)
IprPMR[d, e]	Synchrophasor current real component, Phase p, Terminal r	A (primary)
IprPMRD[d, e]	Synchrophasor current real component, Phase p, Terminal r, delayed for RTC alignment	A (primary)
IpM2[d]	Second-harmonic current content of operating current, Phase p	pu
IpM4[d]	Fourth-harmonic current content of operating current, Phase p	pu
IpM5[d]	Fifth-harmonic current content of operating current, Phase p	pu
I1mA[a]	Instantaneous positive-sequence current angle, Terminal m	° (±180°)
I1mAC	1-cycle average positive-sequence current angle, Terminal m	° (±180°)
I1mI[a]	Instantaneous positive-sequence current, imaginary component, Terminal m	A (secondary)
I1mM[a]	Instantaneous positive-sequence current magnitude, Terminal m	A (secondary)
I1mMC[a]	1-cycle average positive-sequence current magnitude, Terminal m	A (primary)
I1mR[a]	Instantaneous positive-sequence current, real component, Terminal m	A (secondary)
I1qpA[b]	Instantaneous positive-sequence current angle, comb. Terminals qp	° (±180°)
I1qpAC[b]	1-cycle average positive-sequence current angle, comb. Terminals qp	° (±180°)
I1qpI[b]	Instantaneous positive-sequence current, imaginary comp, comb. Terminals qp	A (secondary)
I1qpM[b]	Instantaneous positive-sequence current magnitude, comb. Terminals qp	A (secondary)
I1qpMC[b]	1-cycle average positive-sequence current magnitude, comb. Terminals qp	A (primary)
I1qpR[b]	Instantaneous positive-sequence current, real component, comb. Terminals qp	A (secondary)
I1rPMA[e]	Positive-sequence synchrophasor current angle, Terminal r	° (±180°)
I1rPMAD[e]	Positive-sequence synchrophasor current angle, Terminal r, delayed for RTC alignment	° (±180°)
I1rPMI[e]	Positive-sequence synchrophasor current imaginary component, Terminal r	A (primary)
I1rPMID[e]	Positive-sequence synchrophasor current imaginary component, Terminal r, delayed for RTC alignment	A (primary)
I1rPMM[e]	Positive-sequence synchrophasor current magnitude, Terminal r	A (primary)
I1rPMMD[e]	Positive-sequence synchrophasor current magnitude, Terminal r, delayed for RTC alignment	A (primary)
I1rPMR[e]	Positive-sequence synchrophasor current real component, Terminal r	A (primary)
I1rPMRD[e]	Positive-sequence synchrophasor current real component, Terminal r, delayed for RTC alignment	A (primary)
I850MOD	IEC 61850 mode/behavior status	N/A
IMAXmF[a]	Instantaneous filtered maximum phase-current magnitude, Terminal m	A (secondary)
IMAXmR[a]	Instantaneous rms maximum phase current, Terminal m	A (secondary)
IMAXqpF	Instantaneous filtered maximum phase-current magnitude, comb. Terminals qp	A (secondary)
IMAXqpR[b]	Instantaneous rms maximum phase current, comb. Terminals qp	A (secondary)
IMINmF[a]	Instantaneous filtered minimum phase-current magnitude, Terminal m	A (secondary)
IMINmR[a]	Instantaneous rms minimum phase current, Terminal m	A (secondary)
IMINqpF[b]	Instantaneous filtered minimum phase-current magnitude, comb. Terminals qp	A (secondary)
IMINqpR[b]	Instantaneous rms minimum phase current, comb. Terminals qp	A (secondary)
IMXmRS[a]	1-second average maximum rms phase current, Terminal m	A (secondary)
IMXqpRS[b]	1-second average maximum rms phase current, comb. Terminals qp	A (secondary)

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 6 of 9)

Label	Description	Units
IOPp[d]	Instantaneous operating current, Phase p	pu
IOP87Q	Negative-sequence operating current	pu
IRTp[d]	Instantaneous restraint current, Phase p	pu
IRT87Q	Negative-sequence restraint current	pu
IRTFKp[d]	Biased instantaneous-restraint current, Phase p	pu
IRTHRp[d]	Instantaneous harmonic-restraint current, Phase p	pu
IY1FA–IY3FA	Instantaneous filtered current angle, Channel 1–3, Terminal Y	° (±180°)
IY1FAC–IY3FAC	1-cycle average filtered current angle, Channel 1–3, Terminal Y	° (±180°)
IY1FI–IY3FI	Instantaneous filtered current, imaginary component, Channel 1–3, Terminal Y	A (secondary)
IY1FM–IY3FM	Instantaneous filtered-current magnitude, Channel 1–3, Terminal Y	A (secondary)
IY1FMC–IY3FMC	1-cycle average filtered-current magnitude, Channel 1–3, Terminal Y	A (primary)
IY1FR–IY3FR	Instantaneous filtered current, real component, Channel 1–3, Terminal Y	A (secondary)
MAMBT	Measured ambient temperature	°C
MB1A–MB7A	A Channel received MIRRORED BITS analog values	
MB1B–MB7B	B Channel received MIRRORED BITS analog values	
MTOIL1–MTOIL3	Measured top-oil temperature, Transformer 1–3	°C
NEW_SRC	Selected high-accuracy time source	
PpmF[a, d]	Instantaneous phase fundamental active power, Phase p, Terminal m	W (secondary)
PpmFC[a, d]	1-cycle average phase fundamental active power, Phase p, Terminal m	MW (primary)
PpqpF[b, d]	Instantaneous phase fundamental active power, Phase p, comb. Terminals qp	W (secondary)
PpqpFC[b, d]	1-cycle average phase fundamental active power, Phase p, comb. Terminals qp	MW (primary)
PCN01CV–PCN32CV	Protection SELOGIC counter current value	
PCN01PV–PCN32PV	Protection SELOGIC counter preset value	
PCT01DO–PCT32DO	Protection SELOGIC conditioning timer dropout time	cycles
PCT01PU–PCT32PU	Protection SELOGIC conditioning timer pickup time	cycles
PMV01–PMV64	Protection SELOGIC math variable	
PST01ET–PST32ET	Protection SELOGIC sequencing timer elapsed time	cycles
PST01PT–PST32PT	Protection SELOGIC sequencing timer preset time	cycles
PTPDSJI	PTP 100PPS data stream jitter in µs	µs
PTPMCC	PTP master clock class enumerated value	N/A
PTPOFST	Raw clock offset between PTP master and relay time	ns
PTPOTJF	Fast converging PTP ON TIME marker jitter in µs, coarse accuracy	µs
PTPOTJS	Slow converging PTP ON TIME marker jitter in µs, fine accuracy	µs
PTPPORT	Active PTP port number	N/A
PTPSTEN	PTP Port State enumerated value	
PTPTBTW	Time between PTP 100PPS pulses in µs	µs
PTRk	Potential transformer ratio for Terminal k	
QpmF[a, d]	Instantaneous phase fundamental reactive power, Phase p, Terminal m	VAr (secondary)
QpmFC[a, d]	1-cycle average phase fundamental reactive power, Phase p, Terminal m	MVAr (primary)
QpqpF[b, d]	Instantaneous phase fundamental reactive power, Phase p, comb. Terminals qp	VAr (secondary)
QpqpFC[b, d]	1-cycle average phase fundamental reactive power, Phase p, comb. Terminals qp	MVAr (primary)

Table 12.1   Analog Quantities Sorted Alphabetically (Sheet 7 of 9)

Label	Description	Units
RA001–RA256	Remote analogs	
RAO01–RAO64	Remote analog output	
REFTQ1–REFTQ3	Restricted earth fault Element 1–3 torque quantity	A (secondary)
RLYTEMP	Relay temperature (temperature of the box)	°C
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)	
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)	
RTCBA01–RTCBA08	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)	
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)	
RTCDFA	Rate-of-change of Channel A remote frequency (from remote synchrophasors)	Hz/s
RTCDFB	Rate-of-change of Channel B remote frequency (from remote synchrophasors)	Hz/s
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz
RTD01TV–RTD12TV	RTD01–RTD12 temperature value	°C
SpmF[a, d]	Instantaneous phase fundamental apparent power, Phase p, Terminal m	VA (secondary)
SpmFC[a, d]	1-cycle average phase fundamental apparent power, Phase p, Terminal m	MVA (primary)
SpqpF[b, d]	Instantaneous phase fundamental apparent power, Phase p, comb. Terminals qp	VA (secondary)
SpqpFC[b, d]	1-cycle average phase fundamental apparent power, Phase p, comb. Terminals qp	MVA (primary)
SERDSJI	Serial port 100PPS data stream jitter	µs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	µs
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	µs
SERTBTW	Time between serial 100PPS pulses	µs
SODPM	Second of day of the synchrophasor data packet	s
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s
SQUAL	IRIG-B synchronization accuracy	µs
T1FAA–T3FAA	Insulation aging acceleration factor, Transformer 1–3	
T1HS–T3HS	Calculated hot-spot temperature, Transformer 1–3	°C
T1LOAD–T3LOAD	Percentage of full load, Transformer 1–3	%
T1OILC–T3OILC	Calculated transformer top-oil temperature, Transformer 1–3	°C
T1RLOL–T3RLOL	Rate of loss-of-life, Transformer 1–3	%
T1TLL–T3TLL	Time to total loss-of-life alarm, Transformer 1–3	hr
T1TLOL–T3TLOL	Total loss-of-life, Transformer 1–3	%
TEC1–TEC3	Thermal element condition, Transformer 1–3	
THR	UTC time, hour (0–23)	hr
THRL1–THRL3	Thermal element measurement, Levels 1–3	Per unit (pu)
THTRIP1–THTRIP3	Thermal element remaining time before trip, Levels 1–3	Seconds [s]
THTCU1–THTCU3	Thermal element capacity used, Levels 1–3	Percent [%]
TLHR	Local time, hour (0–23)	hr
TLMIN	Local time, minute (0–59)	min

Table 12.1 Analog Quantities Sorted Alphabetically (Sheet 8 of 9)

Label	Description	Units
TLMSEC	Local time, milliseconds (0–999)	ms
TLNSEC	Local time, nanoseconds (0–999999)	ns
TLODMS	Local time of day in milliseconds (0–86400000)	ms
TLSEC	Local time, seconds (0–59)	s
TMIN	UTC time, minute (0–59)	min
TMSEC	UTC time, milliseconds (0–999)	ms
TNSEC	UTC time, nanoseconds (0–999999)	ns
TODMS	UTC time of day in milliseconds (0–86400000)	ms
TQUAL	Worst-case time source clock time error	s
TSEC	UTC time, seconds (0–59)	s
TUTC	Offset from local time to UTC time	hr
VpkFA[c, d]	Instantaneous filtered phase-to-neutral voltage angle, Phase p, Terminal k	° (±180°)
VpkFAC[c, d]	1-cycle average filtered phase-to-neutral voltage angle, Phase p, Terminal k	° (±180°)
VpkFI[c, d]	Instantaneous filtered phase-to-neutral voltage, imaginary component, Phase p, Terminal k	V (secondary)
VpkFM[c, d]	Instantaneous filtered phase-to-neutral voltage magnitude, Phase p, Terminal k	V (secondary)
VpkFMC[c, d]	1-cycle average filtered phase-to-neutral voltage magnitude, Phase p, Terminal k	kV (primary)
VpkFR[c, d]	Instantaneous filtered phase-to-neutral voltage, real component, Phase p, Terminal k	V (secondary)
VpkPMA[c, d]	Synchrophasor voltage angle, Phase p, Terminal k	° (±180°)
VpkPMAD[c, d]	Synchrophasor voltage angle, Phase p, Terminal k, delayed for RTC alignment	° (±180°)
VpkPMI[c, d]	Synchrophasor voltage imaginary component, Phase p, Terminal k	kV (primary)
VpkPMID[c, d]	Synchrophasor voltage imaginary component, Phase p, Terminal k, delayed for RTC alignment	kV (primary)
VpkPMM[c, d]	Synchrophasor voltage magnitude, Phase p, Terminal k	kV (primary)
VpkPMMD[c, d]	Synchrophasor voltage magnitude, Phase p, Terminal k, delayed for RTC alignment	kV (primary)
VpkPMR[c, d]	Synchrophasor voltage real component, Phase p, Terminal k	kV (primary)
VpkPMRD[c, d]	Synchrophasor voltage real component, Phase p, Terminal k, delayed for RTC alignment	kV (primary)
VpkRC[c, d]	1-cycle average rms phase-to-neutral voltage, Phase p, Terminal k	kV (primary)
VpkRMS[c, d]	Instantaneous rms phase-to-neutral voltage, Phase p, Terminal k	V (secondary)
VppkFA[c, f]	Instantaneous filtered phase-to-phase voltage angle, Phases pp, Terminal k	° (±180°)
VppkFAC[c, f]	1-cycle average filtered phase-to-phase voltage angle, Phases pp, Terminal k	° (±180°)
VppkFI[c, f]	Instantaneous filtered phase-to-phase voltage, imaginary component, Phases pp, Terminal k	V (secondary)
VppkFM[c, f]	Instantaneous filtered phase-to-phase voltage magnitude, Phases pp, Terminal k	V (secondary)
VppkFMC[c, f]	1-cycle average filtered phase-to-phase voltage magnitude, Phases pp, Terminal k	kV (primary)
VppkFR[c, f]	Instantaneous filtered phase-to-phase voltage, real component, Phases pp, Terminal k	V (secondary)
VppkRC[c, f]	1-cycle average rms phase-to-phase voltage, Phases pp, Terminal k	kV (primary)
VppkRMS[c, f]	Instantaneous rms phase-to-phase voltage Phases pp, Terminal k	V (secondary)
V1kA[c]	Instantaneous positive-sequence voltage angle, Terminal k	° (±180°)
V1kAC[c]	1-cycle average positive-sequence voltage angle, Terminal k	° (±180°)
V1kI[c]	Instantaneous positive-sequence voltage, imaginary component, Terminal k	V (secondary)

Table 12.1   Analog Quantities Sorted Alphabetically (Sheet 9 of 9)

Label	Description	Units
V1kM[c]	Instantaneous positive-sequence voltage magnitude, Terminal k	V (secondary)
V1kMC[c]	1-cycle average positive-sequence voltage magnitude, Terminal k	kV (primary)
V1kPMA[c]	Positive-sequence synchrophasor voltage angle, Terminal k	° (±180°)
V1kPMAD[c]	Positive-sequence synchrophasor voltage angle, Terminal k, delayed for RTC alignment	° (±180°)
V1kPMI[c]	Positive-sequence synchrophasor voltage imaginary component, Terminal k	kV (primary)
V1kPMID[c]	Positive-sequence synchrophasor voltage imaginary component, Terminal k, delayed for RTC alignment	kV (primary)
V1kPMM[c]	Positive-sequence synchrophasor voltage magnitude, Terminal k	kV (primary)
V1kPMMD[c]	Positive-sequence synchrophasor voltage magnitude, Terminal k, delayed for RTC alignment	kV (primary)
V1kPMR[c]	Positive-sequence synchrophasor voltage real component, Terminal k	kV (primary)
V1kPMRD[c]	Positive-sequence synchrophasor voltage real component, Terminal k, delayed for RTC alignment	kV (primary)
V1kR[c]	Instantaneous positive-sequence voltage, real component, Terminal k	V (secondary)
VDC	Station Battery 1 DC voltage	V
VNMAXkF[c]	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal k	V (secondary)
VNMAXkR[c]	Instantaneous rms maximum phase-to-neutral voltage, Terminal k	V (secondary)
VNMINkF[c]	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal k	V (secondary)
VNMINkR[c]	Instantaneous rms minimum phase-to-neutral voltage, Terminal k	V (secondary)
VPMAXkF[c]	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal k	V (secondary)
VPMAXkR[c]	Instantaneous rms maximum phase-to-phase voltage, Terminal k	V (secondary)
VPMINkF[c]	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal k	V (secondary)
VPMINkR[c]	Instantaneous rms minimum phase-to-phase voltage, Terminal k	V (secondary)
Z1Am[a]	Positive-sequence impedance angle, Terminal m	° (±180°)
Z1Mm[a]	Positive-sequence impedance magnitude, Terminal m	Ω (secondary)
Z1An[g]	Positive-sequence impedance angle, Terminal n	° (±180°)
Z1Mn[g]	Positive-sequence impedance magnitude, Terminal n	Ω (secondary)

[a] m = S, T, U, W, X.

[b] qp = ST, TU, UW, WX.

[c] k = V, Z.

[d] p = A, B, C.

[e] r = S, T, U, W, X, Y.

[f] pp = AB, BC, CA.

[g] n = 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

Function List

Table 12.2   Analog Quantities Sorted by Function (Sheet 1 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
Current and Potential Transformer Ratios			
CTRm[a]	Current transformer ratio, Terminal m		5
CTRY1–CTRY3	Current transformer ratio, Terminal Y1–Y3		3
PTRk[b]	Potential transformer ratio, Terminal k		2
Instantaneous Voltage			
VpkFM[b, c]	Instantaneous filtered phase-to-neutral voltage magnitude, phase p, Terminal k	V (secondary)	6
VpkFA[b, c]	Instantaneous filtered phase-to-neutral voltage angle, Phase p, Terminal k	° (±180°)	6
VpkFR[b, c]	Instantaneous filtered phase-to-neutral voltage, real component, Phase p, Terminal k	V (secondary)	6
VpkFI[b, c]	Instantaneous filtered phase-to-neutral voltage, imaginary component, Phase p, Terminal k	V (secondary)	6
VppkFM[b, d]	Instantaneous filtered phase-to-phase voltage magnitude, Phases pp, Terminal k	V (secondary)	6
VppkFA[b, d]	Instantaneous filtered phase-to-phase voltage angle, Phases pp, Terminal k	° (±180°)	6
VppkFR[b, d]	Instantaneous filtered phase-to-phase voltage, real component, Phases pp, Terminal k	V (secondary)	6
VppkFI[b, d]	Instantaneous filtered phase-to-phase voltage, imaginary component, Phases pp, Terminal k	V (secondary)	6
VNMAXkF[b]	Instantaneous filtered maximum phase-to-neutral voltage magnitude, Terminal k	V (secondary)	2
VNMINkF[b]	Instantaneous filtered minimum phase-to-neutral voltage magnitude, Terminal k	V (secondary)	2
VPMAXkF[b]	Instantaneous filtered maximum phase-to-phase voltage magnitude, Terminal k	V (secondary)	2
VPMINkF[b]	Instantaneous filtered minimum phase-to-phase voltage magnitude, Terminal k	V (secondary)	2
V1kM[b]	Instantaneous positive-sequence voltage magnitude, Terminal k	V (secondary)	2
V1kA[b]	Instantaneous positive-sequence voltage angle, Terminal k	° (±180°)	2
V1kR[b]	Instantaneous positive-sequence voltage, real component, Terminal k	V (secondary)	2
V1kI[b]	Instantaneous positive-sequence voltage, imaginary component, Terminal k	V (secondary)	2
3V2kM[b]	Instantaneous negative-sequence voltage magnitude, Terminal k	V (secondary)	2
3V2kA[b]	Instantaneous negative-sequence voltage angle, Terminal k	° (±180°)	2
3V2kR[b]	Instantaneous negative-sequence voltage, real component, Terminal k	V (secondary)	2
3V2kI[b]	Instantaneous negative-sequence voltage, imaginary component, Terminal k	V (secondary)	2
3V0kM[b]	Instantaneous zero-sequence voltage magnitude, Terminal k	V (secondary)	2
3V0kA[b]	Instantaneous zero-sequence voltage angle, Terminal k	° (±180°)	2
3V0kR[b]	Instantaneous zero-sequence voltage, real component, Terminal k	V (secondary)	2
3V0kI[b]	Instantaneous zero-sequence voltage, imaginary component, Terminal k	V (secondary)	2
Instantaneous Current			
IpmFM[a, c]	Instantaneous filtered-phase current magnitude, Phase p, Terminal m	A (secondary)	15
IpmFA[a, c]	Instantaneous filtered-phase current angle, Phase p, Terminal m	° (±180°)	15
IpmFR[a, c]	Instantaneous filtered-phase current, real component, Phase p, Terminal m	A (secondary)	15
IpmFI[a, c]	Instantaneous filtered-phase current, imaginary component, Phase p, Terminal m	A (secondary)	15
IY1FM–IY3FM	Instantaneous filtered-current magnitude, Channel 1–3, Terminal Y	A (secondary)	3
IY1FA–IY3FA	Instantaneous filtered current angle, Channel 1–3, Terminal Y	° (±180°)	3
IY1FR–IY3FR	Instantaneous filtered current, real component, Channel 1–3, Terminal Y	A (secondary)	3

Table 12.2   Analog Quantities Sorted by Function (Sheet 2 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
IY1FI–IY3FI	Instantaneous filtered current, imaginary component, Channel 1–3, Terminal Y	A (secondary)	3
IpqpFM[c, e]	Instantaneous filtered-phase current magnitude, Phase p, comb. Terminals qp	A (secondary)	12
IpqpFA[c, e]	Instantaneous filtered-phase current angle, Phase p, comb. Terminals qp	° (±180°)	12
IpqpFR[c, e]	Instantaneous filtered-phase current, real component, Phase p, comb. Terminals qp	A (secondary)	12
IpqpFI[c, e]	Instantaneous filtered-phase current, imaginary component, Phase p, comb. Terminals qp	A (secondary)	12
IMAXmF[a]	Instantaneous filtered maximum phase-current magnitude, Terminal m	A (secondary)	5
IMINmF[a]	Instantaneous filtered minimum phase-current magnitude, Terminal m	A (secondary)	5
IMAXqpF[e]	Instantaneous filtered maximum phase-current magnitude, comb. Terminals qp	A (secondary)	4
IMINqpF[e]	Instantaneous filtered minimum phase-current magnitude, comb. Terminals qp	A (secondary)	4
I1mM[a]	Instantaneous positive-sequence current magnitude, Terminal m	A (secondary)	5
I1mA[a]	Instantaneous positive-sequence current angle, Terminal m	° (±180°)	5
I1mR[a]	Instantaneous positive-sequence current, real component, Terminal m	A (secondary)	5
I1mI[a]	Instantaneous positive-sequence current, imaginary component, Terminal m	A (secondary)	5
3I2mM[a]	Instantaneous negative-sequence current magnitude, Terminal m	A (secondary)	5
3I2mA[a]	Instantaneous negative-sequence current angle, Terminal m	° (±180°)	5
3I2mR[a]	Instantaneous negative-sequence current, real component, Terminal m	A (secondary)	5
3I2mI[a]	Instantaneous negative-sequence current, imaginary component, Terminal m	A (secondary)	5
3I0mM[a]	Instantaneous zero-sequence current magnitude, Terminal m	A (secondary)	5
3I0mA[a]	Instantaneous zero-sequence current angle, Terminal m	° (±180°)	5
3I0mR[a]	Instantaneous zero-sequence current, real component, Terminal m	A (secondary)	5
3I0mI[a]	Instantaneous zero-sequence current, imaginary component, Terminal m	A (secondary)	5
I1qpM[e]	Instantaneous positive-sequence current magnitude, comb. Terminals qp	A (secondary)	4
I1qpA[e]	Instantaneous positive-sequence current angle, comb. Terminals qp	° (±180°)	4
I1qpR[e]	Instantaneous positive-sequence current, real component, comb. Terminals qp	A (secondary)	4
I1qpI[e]	Instantaneous positive-sequence current, imaginary comp, comb. Terminals qp	A (secondary)	4
3I2qpM[e]	Instantaneous negative-sequence current magnitude, comb. Terminals qp	A (secondary)	4
3I2qpA[e]	Instantaneous negative-sequence current angle, comb. Terminals qp	° (±180°)	4
3I2qpR[e]	Instantaneous negative-sequence current, real component, comb. Terminals qp	A (secondary)	4
3I2qpI[e]	Instantaneous negative-sequence current, imaginary component, comb. Terminals qp	A (secondary)	4
3I0qpM[e]	Instantaneous zero-sequence current magnitude, comb. Terminals qp	A (secondary)	4
3I0qpA[e]	Instantaneous zero-sequence current angle, comb. Terminals qp	° (±180°)	4
3I0qpR[e]	Instantaneous zero-sequence current, real component, comb. Terminals qp	A (secondary)	4
3I0qpI[e]	Instantaneous zero-sequence current, imaginary component, comb. Terminals qp	A (secondary)	4
Instantaneous RMS Voltage			
VpkRMS[b, c]	Instantaneous rms phase-to-neutral voltage, Phase p, Terminal k	V (secondary)	6
VppkRMS[b, d]	Instantaneous rms phase-to-phase voltage Phases pp, Terminal k	V (secondary)	6
VNMAXkR[b]	Instantaneous rms maximum phase-to-neutral voltage, Terminal k	V (secondary)	2
VNMINkR[b]	Instantaneous rms minimum phase-to-neutral voltage, Terminal k	V (secondary)	2
VPMAXkR[b]	Instantaneous rms maximum phase-to-phase voltage, Terminal k	V (secondary)	2
VPMINkR[b]	Instantaneous rms minimum phase-to-phase voltage, Terminal k	V (secondary)	2

Table 12.2   Analog Quantities Sorted by Function (Sheet 3 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
Instantaneous RMS Current			
IpmRMS[a, c]	Instantaneous rms phase-current magnitude, Phase p, Terminal m	A (secondary)	15
IpqpRMS[c, e]	Instantaneous rms phase current, Phase p, comb. Terminals qp	A (secondary)	12
IMAXmR[a]	Instantaneous rms maximum phase current, Terminal m	A (secondary)	5
IMINmR[a]	Instantaneous rms minimum phase current, Terminal m	A (secondary)	5
IMAXqpR[e]	Instantaneous rms maximum phase current, comb. Terminals qp	A (secondary)	4
IMINqpR[e]	Instantaneous rms minimum phase current, comb. Terminals qp	A (secondary)	4
Instantaneous Power			
PpmF[a, c]	Instantaneous phase fundamental active power, Phase p, Terminal m	W (secondary)	15
QpmF[a, c]	Instantaneous phase fundamental reactive power, Phase p, Terminal m	VAr (secondary)	15
SpmF[a, c]	Instantaneous phase fundamental apparent power, Phase p, Terminal m	VA (secondary)	15
3PmF[a]	Instantaneous three-phase fundamental active power, Terminal m	W (secondary)	5
3QmF[a]	Instantaneous three-phase fundamental reactive power, Terminal m	VAr (secondary)	5
3SmF[a]	Instantaneous three-phase fundamental apparent power, Terminal m	VA (secondary)	5
PpqpF[c, e]	Instantaneous phase fundamental active power, Phase p, comb. Terminals qp	W (secondary)	12
QpqpF[c, e]	Instantaneous phase fundamental reactive power, Phase p, comb. Terminals qp	VAr (secondary)	12
SpqpF[c, e]	Instantaneous phase fundamental apparent power, Phase p, comb. Terminals qp	VA (secondary)	12
3PqpF[e]	Instantaneous three-phase fundamental active power, comb. Terminals qp	W (secondary)	4
3QqpF[e]	Instantaneous three-phase fundamental reactive power, comb. Terminals qp	VAr (secondary)	4
3SqpF[e]	Instantaneous three-phase fundamental apparent power, comb. Terminals qp	VA (secondary)	4
Instantaneous Positive-Sequence Impedance			
Z1Mm[a]	Positive-sequence impedance magnitude, Terminal m	Ω (secondary)	5
Z1Am[a]	Positive-sequence impedance angle, Terminal m	° (±180°)	5
Z1Mn[f]	Positive-sequence impedance magnitude, Terminal n	Ω (secondary)	4
Z1An[f]	Positive-sequence impedance angle, Terminal n	° (±180°)	4
Synchrophasor Voltages			
VpkPMM[b, c]	Synchrophasor voltage magnitude, Phase p, Terminal k	kV (primary)	6
VpkPMA[b, c]	Synchrophasor voltage angle, Phase p, Terminal k	° (±180°)	6
VpkPMR[b, c]	Synchrophasor voltage real component, Phase p, Terminal k	kV (primary)	6
VpkPMI[b, c]	Synchrophasor voltage imaginary component, Phase p, Terminal k	kV (primary)	6
V1kPMM[b]	Positive-sequence synchrophasor voltage magnitude, Terminal k	kV (primary)	2
V1kPMA[b]	Positive-sequence synchrophasor voltage angle, Terminal k	° (±180°)	2
V1kPMR[b]	Positive-sequence synchrophasor voltage real component, Terminal k	kV (primary)	2
V1kPMI[b]	Positive-sequence synchrophasor voltage imaginary component, Terminal k	kV (primary)	2
Synchrophasor Currents			
IprPMM[c, g]	Synchrophasor current magnitude, Phase p, Terminal r	A (primary)	18
IprPMA[c, g]	Synchrophasor current angle, Phase p, Terminal r	° (±180°)	18
IprPMR[c, g]	Synchrophasor current real component, Phase p, Terminal r	A (primary)	18
IprPMI[c, g]	Synchrophasor current imaginary component, Phase p, Terminal r	A (primary)	18
I1rPMM[g]	Positive-sequence synchrophasor current magnitude, Terminal r	A (primary)	6

Table 12.2   Analog Quantities Sorted by Function (Sheet 4 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
I1rPMA[g]	Positive-sequence synchrophasor current angle, Terminal r	° (±180°)	6
I1rPMR[g]	Positive-sequence synchrophasor current real component, Terminal r	A (primary)	6
I1rPMI[g]	Positive-sequence synchrophasor current imaginary component, Terminal r	A (primary)	6
SODPM	Second of day of the synchrophasor data packet	s	1
FOSPM	Fraction of second of the synchrophasor data packet	s	1
Synchrophasor Frequency			
FREQPM	Frequency for synchrophasor data	Hz	1
DFDTPM	Rate-of-change of frequency for synchrophasor data	Hz/s	1
Synchrophasor RTC Analogs			
VpkPMMD[b, c]	Synchrophasor voltage magnitude, Phase p, Terminal k, delayed for RTC alignment	kV (primary)	6
VpkPMAD[b, c]	Synchrophasor voltage angle, Phase p, Terminal k, delayed for RTC alignment	° (±180°)	6
VpkPMRD[b, c]	Synchrophasor voltage real component, Phase p, Terminal k, delayed for RTC alignment	kV (primary)	6
VpkPMID[b, c]	Synchrophasor voltage imaginary component, Phase p, Terminal k, delayed for RTC alignment	kV (primary)	6
V1kPMMD[b]	Positive-sequence synchrophasor voltage magnitude, Terminal k, delayed for RTC alignment	kV (primary)	2
V1kPMAD[b]	Positive-sequence synchrophasor voltage angle, Terminal k, delayed for RTC alignment	° (±180°)	2
V1kPMRD[b]	Positive-sequence synchrophasor voltage real component, Terminal k, delayed for RTC alignment	kV (primary)	2
V1kPMID[b]	Positive-sequence synchrophasor voltage imaginary component, Terminal k, delayed for RTC alignment	kV (primary)	2
IprPMMD[c, g]	Synchrophasor current magnitude, Phase p, Terminal r, delayed for RTC alignment	A (primary)	18
IprPMAD[c, g]	Synchrophasor current angle, Phase p, Terminal r, delayed for RTC alignment	° (±180°)	18
IprPMRD[c, g]	Synchrophasor current real component, Phase p, Terminal r, delayed for RTC alignment	A (primary)	18
IprPMID[c, g]	Synchrophasor current imaginary component, Phase p, Terminal r, delayed for RTC alignment	A (primary)	18
I1rPMMD[g]	Positive-sequence synchrophasor current magnitude, Terminal r, delayed for RTC alignment	A (primary)	6
I1rPMAD[g]	Positive-sequence synchrophasor current angle, Terminal r, delayed for RTC alignment	° (±180°)	6
I1rPMRD[g]	Positive-sequence synchrophasor current real component, Terminal r, delayed for RTC alignment	A (primary)	6
I1rPMID[g]	Positive-sequence synchrophasor current imaginary component, Terminal r, delayed for RTC alignment	A (primary)	6
SODPMD	Second of day of the synchrophasor data packet, delayed for RTC alignment	s	1
FOSPMD	Fraction of second of the synchrophasor data packet, delayed for RTC alignment	s	1
FREQPMD	Frequency for synchrophasor data, delayed for RTC alignment	Hz	1
DFDTPMD	Rate-of-change of frequency for synchrophasor data, delayed for RTC alignment	Hz/s	1
RTCAP01–RTCAP32	Channel A remote synchrophasor phasors (units depends on remote synchrophasor contents)		32
RTCBP01–RTCBP32	Channel B remote synchrophasor phasors (units depends on remote synchrophasor contents)		32

Table 12.2   Analog Quantities Sorted by Function (Sheet 5 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
RTCAA01–RTCAA08	Channel A remote synchrophasor analogs (units depends on remote synchrophasor contents)		8
RTCBA01–RTCBA08	Channel B remote synchrophasor analogs (units depends on remote synchrophasor contents)		8
RTCFA	Channel A remote frequency (from remote synchrophasors)	Hz	1
RTCFB	Channel B remote frequency (from remote synchrophasors)	Hz	1
RTCDFA	Rate of change of Channel A remote frequency (from remote synchrophasors)	Hz/s	1
RTCDFB	Rate of change of Channel B remote frequency (from remote synchrophasors)	Hz/s	1
Averaged Voltage			
VpFMC[b, c]	1-cycle average filtered phase-to-neutral voltage magnitude, Phase p, Terminal k	kV (primary)	6
VpFAC[b, c]	1-cycle average filtered phase-to-neutral voltage angle, Phase p, Terminal k	° (±180°)	6
VppFMC[b, d]	1-cycle average filtered phase-to-phase voltage magnitude, Phases pp, Terminal k	kV (primary)	6
VppFAC[b, d]	1-cycle average filtered phase-to-phase voltage angle, Phases pp, Terminal k	° (±180°)	6
VpRC[b, c]	1-cycle average rms phase-to-neutral voltage, Phase p, Terminal k	kV (primary)	6
VppRC[b, d]	1-cycle average rms phase-to-phase voltage, Phases pp, Terminal k	kV (primary)	6
V1kMC[b]	1-cycle average positive-sequence voltage magnitude, Terminal k	kV (primary)	2
V1kAC[b]	1-cycle average positive-sequence voltage angle, Terminal k	° (±180°)	2
3V2kMC[b]	1-cycle average negative-sequence voltage magnitude, Terminal k	kV (primary)	2
3V2kAC[b]	1-cycle average negative-sequence voltage angle, Terminal k	° (±180°)	2
3V0kMC[b]	1-cycle average zero-sequence voltage magnitude, Terminal k	kV (primary)	2
3V0kAC[b]	1-cycle average zero-sequence voltage angle, Terminal k	° (±180°)	2
Averaged Current			
IpmFMC[a, c]	1-cycle average filtered-phase current magnitude, Phase p, Terminal m	A (primary)	15
IpmFAC[a, c]	1-cycle average filtered-phase current angle, Phase p, Terminal m	° (±180°)	15
IY1FMC–IY3FMC	1-cycle average filtered-current magnitude, Channel 1–3, Terminal Y	A (primary)	3
IY1FAC–IY3FAC	1-cycle average filtered current angle, Channel 1–3, Terminal Y	° (±180°)	3
IpmRC[a, c]	1-cycle average rms phase current, Phase p, Terminal m	A (primary)	15
IpqpFMC[c, e]	1-cycle average filtered-phase current magnitude, Phase p, comb. Terminals qp	A (primary)	12
IpqpFAC[c, e]	1-cycle average filtered-phase current angle, Phase p, comb. Terminals qp	° (±180°)	12
IpqpRC[c, e]	1-cycle average rms phase current, Phase p, comb. Terminals qp	A (primary)	12
I1mMC[a]	1-cycle average positive-sequence current magnitude, Terminal m	A (primary)	5
I1mAC[a]	1-cycle average positive-sequence current angle, Terminal m	° (±180°)	5
3I2mMC[a]	1-cycle average negative-sequence current magnitude, Terminal m	A Primary)	5
3I2mAC[a]	1-cycle average negative-sequence current angle, Terminal m	° (±180°)	5
3I0mMC[a]	1-cycle average zero-sequence current magnitude, Terminal m	A Primary)	5
3I0mAC[a]	1-cycle average zero-sequence current angle, Terminal m	° (±180°)	5
I1qpMC[e]	1-cycle average positive-sequence current magnitude, comb. Terminals qp	A (primary)	4
I1qpAC[e]	1-cycle average positive-sequence current angle, comb. Terminals qp	° (±180°)	4
3I2qpMC[e]	1-cycle average negative-sequence current magnitude, comb. Terminals qp	A (primary)	4
3I2qpAC[e]	1-cycle average negative-sequence current angle, comb. Terminals qp	° (±180°)	4

Table 12.2   Analog Quantities Sorted by Function (Sheet 6 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
3I0qpMC[e]	1-cycle average zero-sequence current magnitude, comb. Terminals qp	A (primary)	4
3I0qpAC[e]	1-cycle average zero-sequence current angle, comb. Terminals qp	° (±180°)	4
IpmRS[a, c]	1-second average rms phase current, Phase p, Terminal m	A (secondary)	15
IpqpRS[c, e]	1-second average rms phase current, Phase p, comb. Terminals qp	A (secondary)	12
IMXmRS[a]	1-second average maximum rms phase current, Terminal m	A (secondary)	5
IMXqpRS[e]	1-second average maximum rms phase current, comb. Terminals qp	A (secondary)	4
3I2mMS[a]	1-second average negative-sequence current magnitude, Terminal m	A (secondary)	5
3I2qpMS[e]	1-second average negative-sequence current magnitude, comb. Terminals qp	A (secondary)	4
3I0mMS[a]	1-second average zero-sequence current magnitude, Terminal m	A (secondary)	5
3I0qpMS[e]	1-second average zero-sequence current magnitude, comb. Terminals qp	A (secondary)	4
Averaged Power			
PpmFC[a, c]	1-cycle average phase fundamental active power, Phase p, Terminal m	MW (primary)	15
QpmFC[a, c]	1-cycle average phase fundamental reactive power, Phase p, Terminal m	MVAr (primary)	15
SpmFC[a, c]	1-cycle average phase fundamental apparent power, Phase p, Terminal m	MVA (primary)	15
3PmFC[a]	1-cycle average three-phase fundamental active power, Terminal m	MW (primary)	5
3QmFC[a]	1-cycle average three-phase fundamental reactive power, Terminal m	MVAr (primary)	5
3SmFC[a]	1-cycle average three-phase fundamental apparent power, Terminal m	MVA (primary)	5
PpqpFC[c, e]	1-cycle average phase fundamental active power, Phase p, comb. Terminals qp	MW (primary)	12
QpqpFC[c, e]	1-cycle average phase fundamental reactive power, Phase p, comb. Terminals qp	MVAr (primary)	12
SpqpFC[c, e]	1-cycle average phase fundamental apparent power, Phase p, comb. Terminals qp	MVA (primary)	12
3PqpFC[e]	1-cycle average three-phase fundamental active power, comb. Terminals qp	MW (primary)	4
3QqpFC[e]	1-cycle average three-phase fundamental reactive power, comb. Terminals qp	MVAr (primary)	4
3SqpFC[e]	1-cycle average three-phase fundamental apparent power, comb. Terminals qp	MVA (primary)	4
Averaged Power Factor			
DPFpm[a, c]	Phase displacement power factor, Phase p, Terminal m		15
3DPFm[a]	Three-phase displacement power factor, Terminal m		5
DPFpqp[c, e]	Phase displacement power factor, Phase p, comb. Terminals qp		12
3DPFqp[e]	Three-phase displacement power factor, comb. Terminals qp		4
Instantaneous Differential Quantities			
IOPp[c]	Instantaneous operating current, Phase p	pu	3
IRTp[c]	Instantaneous-restraint current, Phase p	pu	3
IRTFKp[c]	Biased instantaneous-restraint current, Phase p	pu	3
IRTHRp[c]	Instantaneous harmonic-restraint current, Phase p	pu	3
IpM2[c]	Second-harmonic current content of operating current, Phase p	pu	3
IpM4[c]	Fourth-harmonic current content of operating current, Phase p	pu	3
IpM5[c]	Fifth-harmonic current content of operating current, Phase p	pu	3
IOP87Q	Instantaneous negative-sequence operating current	pu	1
IRT87Q	Instantaneous negative-sequence restraint current	pu	1

Table 12.2 Analog Quantities Sorted by Function (Sheet 7 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
Averaged Differential Quantities			
87IOPpC[c]	1-cycle average differential element operating current	pu	3
87IRTpC[c]	1-cycle average differential element restraint current	pu	3
Demand Metering Analogs			
DM01–DM10	Demand metering value	A (secondary)	10
DMM01–DMM10	Demand metering maximum value	A (secondary)	10
Energy Metering Analogs			
3PmMWhp[a]	Three-phase active energy exported, Terminal m	MWh (primary)	5
3QmMVhp[a]	Three-phase reactive energy exported, Terminal m	MVArh (primary)	5
3PmMWhn[a]	Three-phase active energy imported, Terminal m	MWh (primary)	5
3QmMVhn[a]	Three-phase reactive energy imported, Terminal m	MVArh (primary)	5
3PmMWhT[a]	Total three-phase active energy, Terminal m	MWh (primary)	5
3QmMVhT[a]	Total three-phase reactive energy, Terminal m	MVArh (primary)	5
3PqpWhp[e]	Three-phase active energy exported, comb. Terminals qp	MWh (primary)	4
3QqpVhp[e]	Three-phase reactive energy exported, comb. Terminals qp	MVArh (primary)	4
3PqpWhn[e]	Three-phase active energy imported, comb. Terminals qp	MWh (primary)	4
3QqpVhn[e]	Three-phase reactive energy imported, comb. Terminals qp	MVArh (primary)	4
3PqpWhT[e]	Total three-phase active energy, comb. Terminals qp	MWh (primary)	4
3QqpVhT[e]	Total three-phase reactive energy, comb. Terminals qp	MVArh (primary)	4
Restricted Earth Fault Analogs			
REFTQ1–REFTQ3	Restricted earth fault Element 1–3 torque quantity	A (secondary)	3
Volts/Hertz Analog			
24RPU	Volts/hertz ratio	%	1
Current Unbalance Analogs			
46pm[a, c]	Current unbalance Phase p, Terminal m	%	15
Breaker Monitoring Analogs			
BmBCWPp[a, c]	Breaker m[a] breaker-contact wear for Pole p	%	15
Thermal Monitor Analogs			
T1LOAD–T3LOAD	Percentage of full load, Transformer 1–3	%	3
T1OILC–T3OILC	Calculated transformer top-oil temperature, Transformer 1–3	°C	3
MAMBT	Measured ambient temperature	°C	1
MTOIL1–MTOIL3	Measured top-oil temperature, Transformer 1–3	°C	3
T1HS–T3HS	Calculated hot-spot temperature, Transformer 1–3	°C	3
T1FAA–T3FAA	Insulation aging acceleration factor, Transformer 1–3		3
T1RLOL–T3RLOL	Rate of loss-of-life, Transformer 1–3	%	3
T1TLOL–T3TLOL	Total loss-of-life, Transformer 1–3	%	3

Table 12.2   Analog Quantities Sorted by Function (Sheet 8 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
T1TLL–T3TLL	Time to total loss-of-life alarm, Transformer 1–3	hr	3
RTD01TV–RTD12TV	RTD01–RTD12 temperature value	°C	12
TEC1–TEC3	Thermal element condition, Transformer 1–3		3
Protection Frequency			
FREQ	Tracking frequency	Hz	1
FREQP	Frequency for over- and underfrequency elements	Hz	1
DFDTP	Rate-of-change of frequency	Hz/s	1
Station DC Monitoring Analogs			
VDC	Station battery dc voltage	V	1
DCPO	Average positive-to-ground dc voltage	V	1
DCNE	Average negative-to-ground dc voltage	V	1
DCRI	AC ripple of dc voltage	V	1
DCMIN	Minimum dc voltage	V	1
DCMAX	Maximum dc voltage	V	1
Mirrored Bits Analogs			
MB1A–MB7A	A Channel received Mirrored Bits analog values		7
MB1B–MB7B	B Channel received Mirrored Bits analog values		7
SELogic Analogs			
PMV01–PMV64	Protection SELogic math variable		64
PCT01PU–PCT32PU	Protection SELogic conditioning timer pickup time		32
PCT01DO–PCT32DO	Protection SELogic conditioning timer dropout time		32
PST01ET–PST32ET	Protection SELogic sequencing timer elapsed time		32
PST01PT–PST32PT	Protection SELogic sequencing timer preset time		32
PCN01CV–PCN32CV	Protection SELogic counter current value		32
PCN01PV–PCN32PV	Protection SELogic counter preset value		32
AMV001–AMV256	Automation SELogic math variable		256
ACT01PU–ACT32PU	Automation SELogic conditioning timer pickup time		32
ACT01DO–ACT32DO	Automation SELogic conditioning timer dropout time		32
AST01ET–AST32ET	Automation SELogic sequencing timer elapsed time		32
AST01PT–AST32PT	Automation SELogic sequencing timer preset time		32

Table 12.2   Analog Quantities Sorted by Function (Sheet 9 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
ACN01CV–ACN32CV	Automation SELOGIC counter current value		32
ACN01PV–ACN32PV	Automation SELOGIC counter preset value		32
Group Switch			
ACTGRP	Active group setting		1
Time and Date Management (UTC and Local Time)			
TODMS	UTC time of day in milliseconds (0–86400000)	ms	1
THR	UTC time, hour (0–23)	hr	1
TMIN	UTC time, minute (0–59)	min	1
TSEC	UTC time, seconds (0–59)	s	1
TMSEC	UTC time, milliseconds (0–999)	ms	1
TNSEC	UTC time, nanoseconds (0–999999)	ns	1
DDOW	UTC date, day of the week (1–SU, ... , 7–SA)		1
DDOM	UTC date, day of the month (1–31)	day	1
DDOY	UTC date, day of the year (1–366)	day	1
DMON	UTC date, month (1–12)	month	1
DYEAR	UTC date, year (2000–2200)	year	1
TLODMS	Local time of day in milliseconds (0–86400000)	ms	1
TLHR	Local time, hour (0–23)	hr	1
TLMIN	Local time, minute (0–59)	min	1
TLSEC	Local time, seconds (0–59)	s	1
TLMSEC	Local time, milliseconds (0–999)	ms	1
TLNSEC	Local time, nanoseconds (0–999999)	ns	1
DLDOW	Local date, day of the week (1-SU, ... , 7-SA)		1
DLDOM	Local date, day of the month (1–31)	day	1
DLDOY	Local date, day of the year (1–366)	day	1
DLMON	Local date, month (1–12)	month	1
DLYEAR	Local date, year (2000–2200)	year	1
IRIG-B Control Bit Analogs			
TUTC	Offset from local time to UTC time	hr	1
TQUAL	Worst-case time source clock time error	s	1
NEW_SRC	Selected high-accuracy time source		1
CUR_SRC	Current high-accuracy time source		1
SQUAL	IRIG-B synchronization accuracy		1
BNCDSJI	BNC port 100PPS data stream jitter		1
BNCOTJS	Slow coverage BNC port ON TIME marker jitter, fine accuracy	µs	1
BNCOTJF	Fast coverage BNC port ON TIME marker jitter, coarse accuracy	µs	1
BNCTBTW	Time between BNC 100PPS pulses	µs	1
SERDSJI	Serial port 100PPS data stream jitter	µs	1
SEROTJS	Slow converging serial port ON TIME marker jitter, fine accuracy	µs	1

Table 12.2   Analog Quantities Sorted by Function (Sheet 10 of 10)

Analog Labels	Analog Quantity Description	Units	Number of Analogs
SEROTJF	Fast converging serial port ON TIME marker jitter, coarse accuracy	μs	1
SERTBTW	Time between serial 100PPS pulses	μs	1
Remote Analogs			
RA001–RA256	Remote analogs		256
RAO01–RAO64	Remote analog output		64
Relay Temperature			
RLYTEMP	Relay temperature (temperature of the box)	°C	1
IEC Thermal Elements			
THRL1–THRL3	Thermal element measurement, levels 1–3	Per unit (pu)	3
THTRIP1–THTRIP3	Thermal element remaining time before trip, levels 1–3	Seconds [s]	10
THTCU1–THTCU3	Thermal element capacity used, levels 1–3	Percent [%]	10
25 Synchronism Check Element Analogs			
25VP*m*FM	25 Synchronism-check polarizing voltage magnitude for Breaker *m*	V (secondary)	
25VP*m*FA	25 Synchronism-check polarizing voltage angle for Breaker *m*	° (±180°)	
25VPFM	25 Synchronism-check polarizing voltage magnitude	V (secondary)	1
25VPFA	25 Synchronism-check polarizing voltage angle	° (±180°)	1
25VS*m*FM[a]	25 Synchronism-check synchronizing voltage magnitude for Breaker *m*	V (secondary)	5
25VS*m*FA[a]	25 Synchronism-check synchronizing voltage angle for Breaker *m*	° (±180°)	5
25ANG*m*[a]	25 Synchronism-check angle difference for Breaker *m*	° (±180°)	5
25ANGC*m*[a]	25 Synchronism-check compensated angle difference for Breaker *m*	° (±180°)	5
25SLIP*m*[a]	25 Synchronism-check slip frequency for Breaker *m*	Hz	5
IEEE 1588 PTP Status			
PTPDSJI	PTP 100PPS data stream jitter in μs	μs	1
PTPMCC	PTP master clock class enumerated value	N/A	1
PTPOTJS	Slow converging PTP ON TIME marker jitter in μs, fine accuracy	μs	1
PTPOTJF	Fast converging PTP ON TIME marker jitter in μs, coarse accuracy	μs	1
PTPOFST	Raw clock offset between PTP master and relay time	ns	1
PTPPORT	Active PTP port number	N/A	1
PTPTBTW	Time between PTP 100PPS pulses in μs	μs	1
PTPSTEN	PTP Port State enumerated value		1
IEC 61850 Mode/Behavior Status			
I850MOD	IEC 61850 mode/behavior status	N/A	

[a] *m* = S, T, U, W, X.

[b] *k* = V, Z.

[c] *p* = A, B, C.

[d] *pp* = AB, BC, CA.

[e] *qp* = ST, TU, UW, WX.

[f] *n* = 1, 2, 3, 4 (combined terminals: 1 = ST, 2 = TU, 3 = UW, 4 = WX).

[g] *r* = S, T, U, W, X, Y.

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Firmware, ICD File, and Manual Versions

Firmware

Determining the Firmware Version

To determine the firmware version, view the status report by using the serial port **STATUS** command or the front-panel HMI. The status report displays the Firmware Identification (FID) number.

The firmware version will be either a standard release or a point release. A standard release adds new functionality to the firmware beyond the specifications of the existing version. A point release is reserved for modifying firmware functionality to conform to the specifications of the existing version.

A standard release is identified by a change in the R-number of the device FID number.

Existing firmware:

FID=SEL-487E-x-**R100**-V0-Z001001-Dxxxxxxxx

Standard release firmware:

FID=SEL-487E-x-**R101**-V0-Z001001-Dxxxxxxxx

A point release is identified by a change in the V-number of the device FID number.

Existing firmware:

FID=SEL-487E-x-R100-**V0**-Z001001-Dxxxxxxxx

Point release firmware:

FID=SEL-487E-x-R100-**V1**-Z001001-Dxxxxxxxx

The release date is after the D. For example, the following is firmware version number R100, release date December 10, 2003.

FID=SEL-487E-x-R100-V0-Z001001-**D20031210**

Similarly, the device SELBOOT firmware revision (BFID) will be reported as:

BFID=SLBT-4XX-Rxxx-Vx-Zxxxxxx-Dxxxxxxxx

⚠**CAUTION**
The SEL-487E-3 and SEL-487E-4 relays (firmware version R3xx) are incompatible with the previous SEL-487E-0 and SEL-487E-2 relays (firmware versions R1xx). Do not attempt to load R3xx firmware on the previous hardware or R1xx firmware on the new hardware.

Revision History

Table A.1 lists the firmware versions, revision descriptions, and corresponding instruction manual date codes.

Table A.1 Firmware Revision History (Sheet 1 of 8)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-3-R318-V1-Z111102-D20201009 SEL-487E-4-R318-V1-Z111102-D20201009	Includes all the functions of SEL-487E-3-R318-V0-Z111102-D20200229 and SEL-487E-4-R318-V0-Z111102-D20200229 with the following additions: ➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 "Blocked" or "Test/Blocked" operating mode. ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.	20201009
SEL-487E-3-R318-V0-Z111102-D20200229 SEL-487E-4-R318-V0-Z111102-D20200229 NOTE: This firmware release only supports .zds digitally signed firmware files. SELBOOT R300 or newer is required for this and all new firmware versions. See *Appendix B: Firmware Upgrade Instructions* for more information.	➤ Modified firmware to enable DNP and IEC 61850 breaker control only when the circuit breaker jumper is installed. ➤ Added the ability to remotely upgrade relay firmware over an Ethernet network. ➤ Improved relay response to three consecutive failed login attempts within a one-minute interval to pulse the BADPASS and SALARM Relay Word bits for all communications interfaces. ➤ Enhanced relay self-tests to detect current or voltage magnitudes that exceed the maximum analog-to-digital converter output and perform an automatic diagnostic restart. ➤ Enhanced FTP Network Security. ➤ Modified firmware to retain stored data after successful reads of SER.TXT, CSER.TXT, PRO.TXT, and CPRO.TXT over Ethernet connections. ➤ Modified firmware to support all printable ASCII characters in the password entry HMI screen. ➤ Added conditioning timers to Automation SELOGIC. ➤ Improved processing of control bits in Automation SELOGIC. ➤ Modified the synchronism-check function to allow alternate and independent polarizing sources. ➤ Modified firmware to apply DNP scaling of 100 to angles and slip frequency analog quantities related to the synchronism-check element. ➤ Modified firmware to increment the state number (stNum) in GOOSE messages for all changes in quality. ➤ Modified firmware to support the default profile for Precision Time Protocol when NETMODE = PRP. ➤ Added breaker wear analog quantities to DNP and IEC 61850 communications. ➤ Added support for new IEC 61850 control and settings common data classes. ➤ Enhanced wildcard parsing used in the YMODEM file-transfer operations. ➤ Improved synchrophasor current scaling when Phasor Numeric Representation is set to integer (PHNR = I) and large current transformer ratio (CTR) settings (CTR > 1200) are used.	20200229

Table A.1   Firmware Revision History (Sheet 2 of 8)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-3-R317-V3-Z110102-D20201009 SEL-487E-4-R317-V3-Z110102-D20201009	Includes all the functions of SEL-487E-3-R317-V2-Z110102-D20191210 and SEL-487E-4-R317-V2-Z110102-D20191210 with the following additions: ➤ Enhanced output contact behavior following a power cycle while the relay is in IEC 61850 "Blocked" or "Test/Blocked" operating mode. ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.	20201009
SEL-487E-3-R317-V2-Z110102-D20191210 SEL-487E-4-R317-V2-Z110102-D20191210	Includes all the functions of SEL-487E-3-R317-V1-Z110102-D20190211 and SEL-487E-4-R317-V1-Z110102-D20190211 with the following addition: ➤ Modified processing of pulsed Relay Word bits.	20191210
SEL-487E-3-R317-V1-Z110102-D20190211 SEL-487E-4-R317-V1-Z110102-D20190211	Includes all the functions of SEL-487E-3-R317-V0-Z110102-D20181105 and SEL-487E-4-R317-V0-Z110102-D20181105 with the following additions: ➤ Resolved an issue with Relay Word bit 87T, which previously would not assert when group setting E87Q = N. ➤ Resolved an issue with the rotating display, which previously would appear blank after accessing a one-line diagram within the HMI.	20190211
SEL-487E-3-R317-V0-Z110102-D20181105 SEL-487E-4-R317-V0-Z110102-D20181105	➤ Added IEC 61850 standard operating modes, including TEST, TEST-BLOCKED, ON, ON-BLOCKED, and OFF. ➤ Modified Ethernet communications to automatically correct a loss of synchronization between the communications subsystem and the other relay subsystems. ➤ Modified the relay to prevent rare cases of a CID file reverting to the previous version of the file during a firmware upgrade. ➤ Improved the processing consistency of remote and local control bits with a one-processing interval pulse width. ➤ Modified the firmware to verify that Precise Time Protocol (PTP) is enabled (EPTP = Y) as an initial validity check for all PTP messages being received by the relay. ➤ Added the 89CTL*nn* (where *nn* = 01–20) disconnect control setting to allow individual control of disconnects from the relay front-panel HMI. ➤ Added HMI support for display of rack-type breakers and corresponding settings 52*k*RACK and 52*k*TEST (where *k* = S, T, U, W, or X). ➤ Modified MMS file reads to allow mixed-case file names. ➤ Improved backward compatibility with certain MMS clients. ➤ Enhanced dc offset processing. ➤ Modified the firmware to prevent settings read/write issues when Port 5 is disabled and an IEC 61850 configuration file is loaded. ➤ Modified the firmware to address an issue in retransmitted TCP/IP frames with PRP trailer, which in previous firmware may have been discarded on reception. ➤ Improved error handling for Ethernet interface.	20181105
SEL-487E-3-R316-V2-Z109102-D20201009 SEL-487E-4-R316-V2-Z109102-D20201009	Includes all the functions of SEL-487E-3-R316-V1-Z109102-D20190211 and SEL-487E-4-R316-V1-Z109102-D20190211 with the following addition: ➤ Resolved an extremely rare issue that could cause the relay to perform a diagnostic restart when configured for Parallel Redundancy Protocol (NETMODE = PRP) and the relay received abnormal Ethernet traffic.	20201009
SEL-487E-3-R316-V1-Z109102-D20190211 SEL-487E-4-R316-V1-Z109102-D20190211	Includes all the functions of SEL-487E-3-R316-V0-Z109102-D20180329 and SEL-487E-4-R316-V0-Z109102-D20180329 with the following additions: ➤ Resolved an issue with Relay Word bit 87T, which previously would not assert when group setting E87Q = N.	20190211

Table A.1   Firmware Revision History (Sheet 3 of 8)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-3-R316-V0-Z109102-D20180329 SEL-487E-4-R316-V0-Z109102-D20180329	➤ Added bipolar low-set unblocking. ➤ Enhanced differential security timers for accelerated operating time. ➤ Added security logic for the bipolar elements. ➤ Added a raw unrestrained differential element. ➤ Added the 87T Relay Word bit. ➤ Added the setting E87Q to select the negative-sequence inrush security method. ➤ Added the setting E87U to select which types of unrestrained elements are active. ➤ Renamed the 87T_TYP setting to 87CORE. ➤ Integrated the setting E87T_WS into the waveshape logic. ➤ Modified the E87HR and E87HB settings to provide additional selections for waveshape detection. ➤ Modified access level requirements for the **TFE** and **THE** commands so that C, R, and P parameters are now available at access level B. ➤ Added the EINVPOL setting to allow changing the polarity of CT and PT inputs. ➤ Added IEC 60255-149 Thermal (49) Elements. ➤ Modified the **SUM** command to display breaker trip times in relay local time rather than UTC. ➤ Added combined overcurrent elements. ➤ Added the TFLTIPU ratio threshold setting to the transformer through-fault monitoring logic. ➤ Modified how settings with a large number of combinations are entered from the front-panel HMI. ➤ Modified the accuracy of the COMTRADE data to be more accurate when a small Potential Transformer Ratio (PTR) setting is used. ➤ Modified firmware to use only the first synchrophasor data configuration if the number of output data configurations exceeds the number of data configurations. ➤ Modified TCLSBKm default setting to be 8.00 (where m = S, T, U, W, or X). ➤ Added support for IEEE C37.111 2013 COMTRADE. ➤ Added the company name Global setting (CONAM). ➤ Modified Z2FTH and Z2RTH thresholds when CTPm is set to N. ➤ Modified firmware to avoid false GOOSE out of sequence errors while in PRP mode. ➤ The **ETH** command now shows both MAC addresses. ➤ Modified firmware to display the **History Region** correctly. ➤ Modified firmware to allow all settings changes when the relay is disabled. ➤ Modified firmware to only reset breaker monitor data for the breaker selected. In prior firmware, some data were being reset for all breakers. ➤ Modified firmware to indicate an enabled or disabled transition of the IEC 61850 Buffer Report Control Block (BRCB) by sending an overflow flag on the next report sent after the transition. ➤ Modified IEEE-1588 PTP power profile to be supported in Parallel Redundancy Protocol (PRP) mode.	20180329

Table A.1 Firmware Revision History (Sheet 4 of 8)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
	➤ Added a new analog quantity, PTPMCC, to indicate the clock class of the PTP master. ➤ DNP3 data are now reported with a LOCAL_FORCED flag when they have been overridden through use of the **TEST DB2** command. ➤ Updated IEC 61850 protocol implementation to IEC 61850 Edition 2. ➤ Modified the relay response to an MMS identify request so that it will respond with the firmware ID (FID) string. ➤ Improved MMS file services performance with successive file transfers. ➤ Enhanced wild card parsing used in MMS file transfer operations. ➤ Modified the **ID** command to display a string that uniquely identifies the IEC 61850 firmware present in the relay. ➤ Modified firmware to replace non-printable characters with question marks in settings that are sent to the front panel of the HMI. ➤ Modified firmware to allow SNTPPIP to be set to 0.0.0.0 when ESNTP = BROADCAST. ➤ Added Breaker Monitor settings to event reports. ➤ Modified the SELOGIC status report (STA S) to provide the SELOGIC flash memory availability for each settings class. Additionally, this firmware version increases the available storage capacity for SELOGIC equations. ➤ Modified the settings prompt for DMTC*gg* to only accept values that are divisible by 5. ➤ Added Monitor settings to the **EVE/CEV** command reports and event reporting files. ➤ Modified **Vector** command to show all Sequential Events Recorder (SER) entries.	
SEL-487E-3-R315-V0-Z108101-D20171008 SEL-487E-4-R315-V0-Z108101-D20171008	**Note:** This firmware did not production release. ➤ Released for IEC 61850 conformance testing only.	—
SEL-487E-3-R314-V4-Z108101-D20171021 SEL-487E-4-R314-V4-Z108101-D20171021	Includes all the functions of SEL-487E-3-R314-V3-Z108101-D20170809 and SEL-487E-4-R314-V3-Z108101-D20170809 with the following addition: ➤ Enhanced memory read diagnostics.	20171021
SEL-487E-3-R314-V3-Z108101-D20170809 SEL-487E-4-R314-V3-Z108101-D20170809	Includes all the functions of SEL-487E-3-R314-V2-Z108101-D20170606 and SEL-487E-4-R314-V2-Z108101-D20170606 with the following addition: ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.	20170809
SEL-487E-3-R314-V2-Z108101-D20170606 SEL-487E-4-R314-V2-Z108101-D20170606	Includes all the functions of SEL-487E-3-R314-V1-Z108101-D20170327 and SEL-487E-4-R314-V1-Z108101-D20170327 with the following addition: ➤ Modified firmware to allow the relay to synchronize to an external time source more responsively.	20170606
SEL-487E-3-R314-V1-Z108101-D20170327 SEL-487E-4-R314-V1-Z108101-D20170327	Includes all the functions of SEL-487E-3-R314-V0-Z108101-D20170105/SEL-487E-4-R314-V0-Z108101-D20170105 with the following additions: ➤ Modified firmware to prevent delays in periodic MMS reports. ➤ Modified firmware to allow the MMS inactivity time-out to be turned off. ➤ Modified firmware to allow for Simple Network Time Protocol (SNTP) time synchronization when the network operating mode is set to Parallel Redundancy Protocol (PRP).	20170327

Table A.1 Firmware Revision History (Sheet 5 of 8)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-3-R314-V0-Z108101-D20170105 SEL-487E-4-R314-V0-Z108101-D20170105	➤ Added an event report digital setting, ERDIG, which can be set to S (some) or A (all) to allow the option for all Relay Word bits to be added to COMTRADE event reports. ➤ Improved Simple Network Time Protocol (SNTP) accuracy to ±1 ms in an ideal network. ➤ Added time-domain link (TiDL) technology. ➤ Added digital input and digital output Relay Word bits to accommodate I/O from remote data acquisition modules. ➤ Added Relay Word bits to indicate a leading or lagging power factor. ➤ Enhanced frequency tracking to freeze for two cycles during toggling of open pole conditions. ➤ Added Relay Word bits 59VSn (where n = S, T, U, W, or X) to indicate that the synchronizing voltage for breaker n is within a healthy voltage window. ➤ Increased the event report nonvolatile storage capability to hold approximately three times more event reports.	20170105
SEL-487E-3-R313-V2-Z107101-D20171021 SEL-487E-4-R313-V2-Z107101-D20171021	Includes all the functions of SEL-487E-3-R313-V1-Z107101-D20170820 and SEL-487E-4-R313-V1-Z107101-D20170820 with the following addition: ➤ Enhanced memory read diagnostics.	20171021
SEL-487E-3-R313-V1-Z107101-D20170820 SEL-487E-4-R313-V1-Z107101-D20170820	Includes all the functions of SEL-487E-3-R313-V0-Z107101-D20160707 and SEL-487E-4-R313-V0-Z107101-D20160707 with the following addition: ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.	20170820
SEL-487E-3-R313-V0-Z107101-D20160707 SEL-487E-4-R313-V0-Z107101-D20160707	➤ Added support for IEEE 1588-2008, Precision Time Protocol (PTP) time synchronization. ➤ Added ordering option to select Ethernet Ports 5A/5B for PTP. ➤ Added EVEMODn (where n = 1–6 for DNP LAN/WAN, or empty for DNP serial) setting to force the relay to start in single- or multiple-event mode. ➤ Enhanced front-panel operations to show settings warnings, in addition to settings errors already displayed, during settings changes. ➤ Modified the firmware to allow all settings combinations of voltage terminals to be enabled when the synchronism check is enabled and the alternate synchronizing source setting is set to NA. ➤ Modified DNP Object 0, Variation 242 to report the firmware V-number. ➤ Improved MIRRORED BITS performance under a high level of GOOSE traffic. ➤ Improved relay start-up time. ➤ Modified Virtual Bits to reset upon a successful CID file download. ➤ Modified GOOSE subscription to update data after the messages transition from bad to good quality. ➤ Modified the Local Control menu on the front-panel HMI to include the Breaker Control submenu. This functionality was available in firmware versions R301–R310, but not in R311 or R312. ➤ Modified the handling of a leap year when the relay setting and clock disagree.	20160707
SEL-487E-3-R312-V1-Z106101-D20170820 SEL-487E-4-R312-V1-Z106101-D20170820	Includes all the functions of SEL-487E-3-R312-V0-Z106101-D20160115 and SEL-487E-4-R312-V0-Z106101-D20160115 with the following addition: ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.	20170820

Table A.1   Firmware Revision History (Sheet 6 of 8)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-3-R312-V0-Z106101-D20160115 SEL-487E-4-R312-V0-Z106101-D20160115	➤ Added additional synchronism-check schemes and a synchronous voltage difference setting, 25VDIF. ➤ Added a new breaker failure scheme selection setting, BF_SCHM, and a new breaker failure settings option, Y1. ➤ Modified the TEST DB2 functionality to override Relay Word bits that are in the Sequential Events Recorder (SER). ➤ Modified the **TEST DB2 OFF** command to disable the overridden remote analog output and digital values in IEC 61850 GOOSE messages.	20160115
SEL-487E-3-R311-V1-Z105101-D20170820 SEL-487E-4-R311-V1-Z105101-D20170820	Includes all the functions of SEL-487E-3-R311-V0-Z105101-D20150513 and SEL-487E-4-R311-V0-Z105101-D20150513 with the following addition: ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.	20170820
SEL-487E-3-R311-V0-Z105101-D20150513 SEL-487E-4-R311-V0-Z105101-D20150513	➤ Added the LPHD.Sim logical node so the relay will accept GOOSE messages with the test flag asserted. ➤ Added support for the stSeld attribute in IEC 61850 SBO controls. ➤ Added Isolated IP mode (NETMODE = ISOLATEIP) which permits IEC 61850 GOOSE messages on two ports, but restricts IP traffic to just one port. ➤ Added the option to change settings groups with IEC 61850. ➤ Added real and reactive energy analogs for imported, exported and total energy to the DNP3 analog input reference map. Added the real and reactive energy analogs for both imported and exported energy in kilowatts (kW) to the binary counter reference map. ➤ Changed the result of a SELOGIC equation math error from NAN (not a number) to the previously stored valid result. ➤ Modified the firmware to prevent IP traffic from becoming unresponsive when the Parallel Redundancy Protocol (PRP) is enabled. ➤ Modified the CEV event report header label FREQ to display the measured system frequency. ➤ Modified firmware to correctly process the last row of Relay Word bits in the four samples per cycle compressed event reports. ➤ Updated the profile and compressed profile commands (**PRO** and **CPRO**, respectively) to display the available analog signal profiling records regardless of the state of the signal profile enable (SPEN) setting. ➤ Modified the embedded HTTP server web access to always require a valid relay Access Level 1 (ACC) password. ➤ Reset the port time-out on transmitted Telnet messages. ➤ Modified the relay to support MMS file transfer service even if the relay contains an invalid CID file. ➤ Improved Port 5 functionality to disable automessages when the automessages setting is equal to no (AUTO=N). ➤ Changed the IEC 61850 Configured IED Description (CID) file to support non-Relay Word bit binary elements included in a GOOSE message. ➤ Enhanced the embedded HTTP server user interface to be consistent with other SEL relays. ➤ Enhanced the report time records to save the active UTC offset (UTCOFF) value with each report. Now, when the relay collects a report, it assigns the time stamp based on the UTC time and the UTCOFF value at the time the relay stores the report. ➤ Improved relay performance during certain incorrect memory reads. ➤ Clarified the message generated by the relay in response to an invalid CID file. ➤ Added local time and date analog quantities.	20150513

Table A.1   Firmware Revision History (Sheet 7 of 8)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-3-R310-V1-Z104101-D20170820 SEL-487E-4-R310-V1-Z104101-D20170820	Includes all the functions of SEL-487E-3-R310-V0-Z104101-D20140515 and SEL-487E-4-R310-V0-Z104101-D20140515 with the following addition: ➤ Resolved an issue where certain Ethernet traffic could cause diagnostic restarts.	20170820
SEL-487E-3-R310-V0-Z104101-D20140515 SEL-487E-4-R310-V0-Z104101-D20140515	➤ Modified bay screen breaker status setting (52mCLSM, m = S, T, U, W, X) and alarm setting (52m_ALM) to allow the user to assign any breaker (S, T, U, W, or X) in any order.	20140515
SEL-487E-3-R309-V0-Z104101-D20140513 SEL-487E-4-R309-V0-Z104101-D20140513	**Note:** This firmware did not production release.	—
SEL-487E-3-R308-V0-Z104101-D20140416 SEL-487E-4-R308-V0-Z104101-D20140416	➤ Added pulsed remote bits in Automation SELOGIC. ➤ Updated new bay screens to allow longer name lengths. ➤ Changed the Global setting Message Format (MFRMT) so that when it is set to Fast Message (FM), the freeform settings PMAQ, PMAA, PMDG, and PMDA are hidden. ➤ Changed Group and Global settings so that they are now available via the front-panel Human Machine Interface (HMI). ➤ Changed the scaling factor of the minimum value of the Restrained Element Operating Current Pickup setting (O87P) from 0.1 to 0.02. ➤ Increased the length of PMU triggered data (PMLER) settings range from 60 seconds to 120 seconds when messages per second (MRATE) is equal to 60. ➤ Changed the settings rules for Station ID label in the COMTRADE configuration file (.cfg) to prevent non-alphanumeric characters per the COMTRADE IEEE C37.111-1999 standard. ➤ Removed 87QB as an input to negative- and zero-sequence directional elements and replaced it with a SELOGIC equation for directional blocking, DIRBLKm. By default, DIRBLKm = 87QB (where m = S, T, U, W, or X). ➤ Added synchronism-check elements for as many as five breakers. ➤ Added the analog quantities for current and potential transformer ratios. ➤ Added the ability for the user to assign bay screen breakers to any terminal S, T, U, W, or X. ➤ Removed 87QB in the negative-sequence directional element logic because the m32QE element (where m = S, T, U, W, or X) was already supervised by 87QB. The logic was redundant. ➤ Added Low-Energy Analog (LEA) voltage inputs. ➤ Added waveshape-based current inrush detection with a bidirectional differential overcurrent scheme to differentiate between an inrush condition and an internal fault that occurs during an inrush condition. ➤ Added faulted phase indication on a per-terminal basis. ➤ Enhanced performance to ensure that the relay does not become unresponsive when MIRRORED BITS is used on the front port. In all previous firmware revisions, the relay could become unresponsive if the front EIA-232 port is set to MIRRORED BITS protocol. ➤ Modified the settings range for the overpower and underpower pickup settings 32OPPgg and 32UPPgg. The settings range cannot fall within ±I$_{NOM}m$ where m = S, T, U, W, or X. ➤ Removed the port uniqueness requirements for the PMOUDP[2] settings.	20140416

Table A.1   Firmware Revision History (Sheet 8 of 8)

Firmware Identification (FID) Number	Summary of Revisions	Manual Date Code
SEL-487E-3-R307-V0-Z103101-D20130524 SEL-487E-4-R307-V0-Z103101-D20130524	➤ Added FRQST and PMLEGCY settings to maintain backward settings compatibility. ➤ Added user-configurable analogs and digital quantities to synchrophasor data. ➤ Added aliasing capability for the phasors, analogs, and digitals in the synchrophasor data. ➤ Added support for **CEV C** command. ➤ Updated the PMSTN setting to accept all printing characters. ➤ Changed the 81UVSP default setting from 56 V to 85 V. ➤ Corrected breaker inactivity time measurement in the circuit breaker report. ➤ Improved firmware revision upgrade algorithm to avoid loss of relay settings during firmware revision upgrades. ➤ Improved the firmware revision upgrade algorithm to avoid loss of through-fault data during firmware revision upgrades. ➤ Improved memory usage by eliminating chattering binary GOOSE data. ➤ Corrected handling of unrecognized Ethertype frames that can cause Ethernet to stop responding. ➤ Made correction to points in the default DNP Binary Output map. ➤ Improved Read/Write resources to avoid communications interruptions.	20130524
SEL-487E-3-R306-V0-Z102101-D20121221 SEL-487E-4-R306-V0-Z102101-D20121221	➤ Added aliasing capability to the Synchrophasor names. ➤ Added inputs to the Thermal Models from Remote Analog GOOSE Messages. ➤ Allowed for user-selectable GOOSE Validity Check. ➤ Added Parallel Redundancy Protocol (PRP). ➤ Added Support for MMS Authentication. ➤ Added MMS File Transfer. ➤ Increased the number of GOOSE subscriptions to 128. ➤ Increased the number of buffered and unbuffered reports to seven for MMS reporting. ➤ Allowed for decimal place for PTR settings. ➤ Updated Close Logic to reset on rising edge of unlatch. ➤ Implemented multiple updates to the DNP3 control point operations.	20121221
SEL-487E-3-R305-V0-Z101100-D20120828 SEL-487E-4-R305-V0-Z101100-D20120828	**Note:** This firmware version was not production released. See R306, above, which also includes the enhancements in R305. ➤ Added Connectorized option.	20120828
SEL-487E-3-R304-V0-Z101100-D20120611 SEL-487E-4-R304-V0-Z101100-D20120611	➤ Fixed a problem with the restoration of SER data during a firmware upgrade.	20120611
SEL-487E-3-R303-V0-Z101100-D20120531 SEL-487E-4-R303-V0-Z101100-D20120531	➤ Increased number of disconnects to 20. ➤ Increased number of binary outputs to 100 in custom DNP map. ➤ Implemented mimic diagram "panning" function. ➤ Added HTTPPOR to Port 5 settings. ➤ Enhanced performance to ensure the relay does not become unresponsive when connected to another relay through the serial port with automessaging enabled on both ports (AUTO = Y).	20120531
SEL-487E-3-R302-V0-Z100100-D20120220 SEL-487E-4-R302-V0-Z100100-D20120220	➤ Updated for improved manufacturability.	20120220
SEL-487E-3-R301-V0-Z100100-D20111213 SEL-487E-4-R301-V0-Z100100-D20111213	➤ Initial version.	20120116

SELBOOT

SELBOOT is a firmware package inside the relay that handles hardware initialization and provides the functions needed to support firmware upgrades. *Table A.2* lists the SELBOOT releases used with the SEL-487E, their revision and a description of modifications. The most recent SELBOOT revision is listed first.

Table A.2   SELBOOT Revision History

SELBOOT Firmware Identification (BFID)	Summary of Revisions
SLBT-4XX-R300-V0-Z001002-D20200229	➤ Modified SELBOOT to support digitally signed firmware.
SLBT-4XX-R209-V0-Z001002-D20150130	➤ Modified the firmware to prevent an issue that could cause the relay to become unresponsive.
SLBT-4XX-R208-V0-Z001002-D20120220	➤ Added support for a new main board variant.
SLBT-4XX-R207-V0-Z001002-D20110922	➤ First revision used with SEL-487E-3, -4.

ICD File

To find the ICD revision number in your relay, view the configVersion by using the serial port **ID** command. The configVersion is the last item displayed in the information returned from the **ID** command.

configVersion = ICD-487E-R202-V0-Z306005-D20150421

The ICD revision number is after the R (e.g., 202) and the release date is after the D (e.g., 20150421). This revision number is not related to the relay firmware revision number. The configVersion revision displays the ICD file version used to create the CID file that is loaded in the relay.

The configVersion contains other useful information. The Z-number consists of six digits. The first three digits following the Z represent the minimum IED firmware required to be used with the ICD (e.g., 306). The second three digits represent the ICD ClassFileVersion (e.g., 005). The ClassFileVersion increments when there is a major addition or change to the IEC 61850 implementation of the relay.

Table A.3 list the ICD file versions, a description of modifications, and the instruction manual date code that corresponds to the versions. The most recent version is listed first.

Table A.3   ICD File Revision History

configVersion[a]	Summary of Revisions	Minimum Relay Firmware	ClassFile Version	Manual Date Code
ICD-487E-R402-V0-Z318006-D20200229	➤ Added REF50nPIOC, REF51nPTOC, D87QPDIF, D87TPDIF, REFFnPDIF, REFRnPDIF, LOPzPTUV, BSmpSCBR, BFRmRBRF, and THnPTTR protection logical nodes (where n = 1–3; m = S, T, U, W, X; p = A, B, C; z = V, Z). ➤ Added ALMGGIO, ETHGGIO, and SGGGIO annunciator logical nodes. ➤ Added DCZBAT metering logical node. ➤ Moved IEC 61850 mode/behavior control from logical node LPHD to LLN0. ➤ Improved consistency in deadband units for the ICD file to use voltage in kV and power in MW. ➤ Added system logical nodes LGOS, LTIM, LTMS, and LCCH.	R318	006	20200229
ICD-487E-R401-V0-Z317006-D20181105	➤ Added the ability to control mode and behavior through an MMS write to the LPHD local node Mod.ctlVal. ➤ Addressed nonfunctional settings link tab within ACSELERATOR Architect SEL-5032 Software by disabling "System setFilesSupported in the ICD file.	R317	006	20181105
ICD-487E-R400-V0-Z315006-D20171101	➤ IEC 61850 Edition 2 Conformance. ➤ Updated ClassFileVersion to 006. ➤ Increased the default MMS inactivity time-out value to 900 seconds. ➤ Updated data set and MMS report names. ➤ Added standard enum types FaultDirectionKind and PhaseFaultDirectionKind to PHAR logical node in the ICD file.	R315	006	20171008
ICD-487E-R301-V0-Z314005-D20170315	➤ Added the ability to turn off the MMS inactivity time-out.	R314-V1	005	20170327
ICD-487E-R300-V0-Z311005-D20150423	➤ Added support for 61850 group switch, Simulated GOOSE and stSeld.	R311	005	20150513
ICD-487E-R202-V0-Z306005-D20150421	➤ Enforced the 512 Boolean limit across all GOOSE messages and conformance updates.	R306	005	20150513
ICD-487E-R201-V0-Z000000-D20121228[b]	➤ Enable selectable GOOSE Filtering, Embedded relay settings files, 128 GOOSE subscriptions, 256 VBs, GOOSE Min TX time, 7 MMS reports/sessions, MMS Authentication.	R306	005	20121221
ICD-487E-R200-V0-Z000000-D20130311[b]	➤ SEL-487E-3, -4 Standard.	R304	004	20120611
ICD-487E-R200-V0-Z000000-D20120510[b]	➤ SEL-487E-3, -4 R303 or higher.	R303	004	20120531

[a] The configVersion can be determined for the IED by performing an ID ASCII command from a terminal connection.

[b] The minimum relay firmware and ClassFileVersion in this configVersion does not have a meaningful value.

Instruction Manual

The date code at the bottom of each page of this manual reflects the creation or revision date.

Table A.4 lists the instruction manual versions and revision descriptions. The most recent instruction manual version is listed first.

Table A.4   Instruction Manual Revision History (Sheet 1 of 3)

Revision Date	Summary of Revisions
20201204	**Preface** ➤ Updated *SEL-400 Series Relays Instruction Manual* and *Safety Marks*.
20201009	**Appendix A** ➤ Updated for firmware versions R316-V2, R317-V3, and R318-V1.
20200229	**Section 1** ➤ Updated *Specifications*. **Section 2** ➤ Updated *Jumpers* for new BREAKER jumper description. **Section 5** ➤ Updated *Equation 5.8*. ➤ Updated text and figures in *Circuit Breaker Failure Protection and Synchronism Check*. **Section 8** ➤ Updated *Table 8.55: Synchronism-Check (25) Elements*. **Section 10** ➤ Updated *Table 10.23: Logical Device: PRO (Protection)* and *Table 10.24: Logical Device: MET (Metering)*. **Appendix A** ➤ Updated for firmware version R318-V0. ➤ Updated for SELBOOT version R300. ➤ Updated for ICD file version R402.
20191210	**Appendix A** ➤ Updated for firmware version R317-V2.
20190211	**Appendix A** ➤ Updated for R317-V1. ➤ Updated for R316-V1.
20181210	**Appendix A** ➤ Updated for firmware version R317-V0.
20181115	**Appendix A** ➤ Updated for firmware version R317-V0.
20181105	**Section 5** ➤ Updated *"No-Slip" Synchronism Check*, *"Slip—No Compensation" Synchronism Check*. and *"Slip—With Compensation" Synchronism Check*. **Section 7** ➤ Updated *Through-Fault Monitor*. **Section 8** ➤ Updated *Table 8.68: Bay Settings*. **Section 9** ➤ Updated *Table 9.1: SEL-487E List of Commands*.

Table A.4   Instruction Manual Revision History (Sheet 2 of 3)

Revision Date	Summary of Revisions
	Section 11 ➤ Updated *Table 11.1: Alphabetical List of Relay Word Bits* and *Table 11.2: Row List of Relay Word Bits*. **Appendix A** ➤ Updated for firmware version R317-V0. ➤ Updated for ICD file version R401-V0.
20180329	**Section 1** ➤ Updated *Specifications*. **Section 3** ➤ Updated *Table 3.8: Unrestrained Phase-Differential Element Settings* and *Table 3.14: Settings for the Negative-Sequence Test*. ➤ Updated *Selected Elements Test*. **Section 5** ➤ Added *Inverting Polarity of Current and Voltage Inputs, Transformer Differential Protection Overview, Unrestrained Phase Differential Element (87U), Combined Differential Element (87T)*, and *IEC Thermal Elements*. ➤ Updated and incorporated *Adaptive Transformer Differential Element* and *Differential Element Operating Characteristic* into the new sections, *Differential Element Speed and Security Features* and *Phase Percentage-Restrained Differential Element (87R)*. ➤ Updated *Combined Overcurrent Values (51 Elements Only)* and changed to *Combined Overcurrent Values*. ➤ Updated *Overcurrent Elements, Selectable Time-Overcurrent Element (51), Directional Control for Ground-Overcurrent Elements*, and *Directional Control for Phase and Negative-Sequence Overcurrent Elements*. **Section 7** ➤ Updated *Through-Fault Monitor*. **Section 8** ➤ Updated *Table 8.3: General Global Settings, Table 8.4: Global Enables, Table 8.25: Monitor Setting Categories, Table 8.26: Enables, Table 8.29: Through-Fault Monitoring, Table 8.38: Group Setting Categories, Table 8.39: Relay Configuration, Table 8.43: Differential Element Configuration and Data*, and *Table 8.45: Overcurrent Elements for Terminals–Table 8.49: Directional Element Blocking*. ➤ Added *Table 8.36: IEC Thermal Model, Table 8.37: Thermal Ambient Compensation*. **Section 9** ➤ Updated *Table 9.10: TFE Command* and *Table 9.11: THE Command*. **Section 10** ➤ Updated *Table 10.23 Logical Device: PRO (Protection)* and *Table 10.24 Logical Device: MET (Metering)*. **Section 11** ➤ Updated *Table 11.1: Alphabetical List of Relay Word Bits* and *Table 11.2: Row List of Relay Word Bits*. **Section 12** ➤ Updated *Table 12.1: Analog Quantities Sorted Alphabetically* and *Table 12.2: Analog Quantities Sorted by Function*. **Appendix A** ➤ Updated for firmware versions R315 and R316. ➤ Updated for ICD firmware version R400.
20171021	**Appendix A** ➤ Updated for firmware versions R313-V2 and R314-V4.
20170820	**Appendix A** ➤ Updated for firmware versions R310-V1, R311-V1, R312-V1, and R313-V1.
20170809	**Appendix A** ➤ Updated for firmware version R314-V3.
20170606	**Appendix A** ➤ Updated for firmware version R314-V2.

Table A.4   Instruction Manual Revision History (Sheet 3 of 3)

Revision Date	Summary of Revisions
20170428	**Cover** ➤ Updated copyright information. **Section 1** ➤ Updated *Specifications*. **Section 2** ➤ Updated *Figure 2.27: SEL-2243 Power Coupler*. **Section 5** ➤ Updated *Figure 5.23: Programmable 51 REF Element*.
20170327	**Section 3** ➤ Updated *Selected Element Tests* for REFF1 and REFR1. **Section 5** ➤ Updated *Differential Element Operating Characteristic* and *Restricted Earth-Fault Element*. ➤ Updated *Figure 5.19: REF 1 Element Enable Logic*, *Figure 5.20: Algorithm That Performs the Directional Calculations*, and *Figure 5.21: REF Element Trip Output*. ➤ Updated *Table 5.11: Directional Element Summary and Example Settings (Terminal S)*. **Appendix A** ➤ Updated *Table A.1: Firmware Revision History* and *Table A.3: ICD File Revision History*.
20170105	**Section 1** ➤ Updated *Specifications*. **Section 2** ➤ Removed *Figure 2.17: IRIG-B Terminating Resistors* and the *IRIG-B Jumper* section. ➤ Added *TiDL Connections*. **Section 5** ➤ Updated *Figure 5.6: Logic for Harmonic Blocking and Cross-Blocking Functions*. ➤ Updated *Equation 5.7*. **Section 7** ➤ Updated *Table 7.15: Event Report Nonvolatile Storage Capability when ERDIG = S*. ➤ Added *Table 7.16: Event Report Nonvolatile Storage Capability when ERDIG = A*. ➤ Added *Instantaneous Power Metering*. **Section 9** ➤ Added **CFG CTNOM** and **CFG NFREQ** to *Table 9.1: SEL-487E List of Commands*. **Section 11** ➤ Updated *Table 11.1: Alphabetic List of Relay Word Bits*. ➤ Updated *Table 11.2: Row List of Relay Word Bits*. **Section 12** ➤ Updated *Table 12.2: Analog Quantities Sorted by Function*. **Command Summary** ➤ Added **COM PTP**, **CFG CTNOM** and **CFG NFREQ**.
20160707	➤ Initial version.

Converting Settings From SEL-487E-0, -2 to SEL-487E-3, -4

Because of hardware changes between the SEL-487E-0, -2 and the SEL-487E-3, -4 relays, the handling of a number of settings has changed. In particular, the replacement of the SEL-2702 Ethernet Processor with integrated Ethernet has significantly changed the handling of Ethernet-related settings. This appendix describes the key differences to aid users who need to convert their settings from an SEL-487E-0, -2 to an SEL-487E-3, -4.

Relay Word Bit Changes

Relay Word bits are used in SELOGIC control equations and many other settings. Some of these bits have different names or do not exist in the latest relay version. *Table B.1* lists these.

Table B.1   Relay Word Bit Differences

SEL-487E-0, -2 Relay Word Bit	Corresponding SEL-487E-3, -4 Relay Word Bit	Comments
CCALARM	--	No longer needed because of SEL-2702 removal.
CCOK	--	No longer needed because of SEL-2702 removal.
TESTDNP	TESTDB2	
CCIN001–CCIN128	VB001–VB128	
CCOUT01–CCOUT32	--	Any Relay Word bit may now be used for outgoing GOOSE.
CCSTA01–CCSTA32	--	No longer needed because of SEL-2702 removal. The previous bits provided communications card status information. New bits LINK5C, LINK5D, LNKFAIL, P5SEL, and P5DSEL have no direct correspondence to the previous bits, but provide status information about Ethernet connectivity.

Port Settings Changes

Serial Port Settings

Table B.2 highlights key differences in the serial port settings between the SEL-487E-0, -2 and the SEL-487E-3, -4.

Table B.2   Serial Port Settings Differences

SEL-487E-0, -2 Settings	SEL-487E-3, -4 Setting	Notes
--	DNPCL	This is a new setting. It needs to be set to Y to enable control operations on a DNP3 port. In the SEL-487E-0, -2, control was always enabled.

Ethernet Port (Port 5) Settings

In the SEL-487E-0, -2, Ethernet was supplied by the SEL-2702 Ethernet Processor. In the SEL-487E-3, -4, Ethernet is native to the relay, with the interfaces provided by the E4 daughter card. This has significant impact on the settings, as described in *Table B.3*.

Table B.3 Ethernet Port Settings Differences (Sheet 1 of 2)

SEL-487E-0, -2 Settings	SEL-487E-3, -4 Setting	Notes
IPADDR SUBNETM	IPADDR	This setting now operates using CIDR rules, which consolidates the old SUBNETM setting into the IPADDR setting.
FAILOVER	NETMODE	FAILOVER of N is equivalent to a NETMODE of FIXED. FAILOVER of Y is equivalent to a NETMODE of FAILOVER. NETMODE also has a SWITCHED open, which enables both ports.
NETPORT	NETPORT	The old setting had choices of A, B, and D, for ports A, B, and to disable. The SEL-487E-3, -4 setting has choices of C and D for ports C and D.
NETASPD	NETCSPD	
NETBSPD	NETDSPD	
HOST*n*	--	This setting no longer exists.
IPADR*n*	--	This setting no longer exists.
T1RECV	ETELNET	
T1CBAN	TCBAN	
T1INIT	--	This setting no longer exists.
T1PNUM	TPORT	
T2CBAN	--	The T2CBAN, T2RECV, and T2PNUM settings have been eliminated. They existed for access to the SEL-2702 local interface, which no longer exists.
T2RECV	--	
T2PNUM	--	
ENDNP	EDNP	While ENDNP was a Y, N selection, the EDNP setting in the SEL-487E-3, -4 provides a range, from 0 to 6, for the number of DNP3 sessions you can enable.
DNPPNUM	DNPPNUM	The range is slightly more restrictive in the SEL-487E-3, -4 implementation. The lowest assignable port is 1025.
DNPMAP	--	This setting has been eliminated. Maps are now always custom.
RPADR01–RPADR06	REPADR1–REPADR6	
RPADR07–RPADR10	--	This setting no longer exists; the SEL-487E-3, -4 supports six sessions instead of the prior 10.
DNIP01–DNIP06	DNPIP1–DNPIP6	
DNPIP07–DNPIP10	--	This setting no longer exists; now supports six sessions instead of the prior 10.
DNPTR01–DNPTR06	DNPTR1–DNPTR6	
DNPTR07–DNPTR10	--	This setting no longer exists; now supports six sessions instead of the prior 10.
DNPUP01–DNPUP06	DNPUDP1–DNPUDP6	The range is slightly more restrictive in the SEL-487E-3, -4 implementation. The lowest assignable port is 1025.
DNPUP07–DNPUP10	--	This setting no longer exists; now supports six sessions instead of the prior 10.
UNSL01–UNSL06	UNSOL1–UNSOL6	
UNSL07–UNSL10	--	This setting no longer exists; now supports six sessions instead of the prior 10.
PUNSL01–PUNSL06	PUNSOL1–PUNSOL6	
PUNSL07–PUNSL10	--	No longer exist; now support six sessions instead of the prior 10.

Table B.3   Ethernet Port Settings Differences (Sheet 2 of 2)

SEL-487E-0, -2 Settings	SEL-487E-3, -4 Setting	Notes
DNPMP01–DNPMP06	DNPMAP1–DNPMAP6	
DNPMP07–DNPMP10	--	No longer exist; now support six sessions instead of the prior 10.
DNPCL01–DNPCL06	DNPCL1–DNPCL6	
DNPCL07–DNPCL10	--	No longer exist; now support six sessions instead of the prior 10.
ECLASSA	CLASSA1–CLASSA6	Old setting allowed 0–3. SEL-487E-3, -4 setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
ECLASSB	CLASSB1–CLASSB6	Old setting allowed 0–3. SEL-487E-3, -4 setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
ECLASSC	CLASSC1–CLASSC6	Old setting allowed 0–3. SEL-487E-3, -4 setting has OFF, 1–3. Old setting 0 is equivalent to new setting OFF.
DECPL	DECPLA1–DECPLA6 DECPLV1–DECPLV6 DECPLM1–DECPLM6	
ANADB	ANADBA1–ANADBA6 ANADBV1–ANADBV6 ANADBM1–ANADBM6	
16BIT	AIVAR1–AIVAR6	The old setting allowed the choice between 16-bit and 32-bit variations. The SEL-487E-3, -4 settings allow the choice between any of the six valid analog input variations. The old setting of 16 is equivalent to 2, and 32 is equivalent to 1.
STIMEO	STIMEO1–STIMEO6	The SEL-487E-3, -4 settings accept integers only.
DNPPAIR	--	This setting no longer exists. Selection of paired controls is now a function of configuring the map.
DNPINA	DNPINA1–DNPINA6	
NUMEVE	NUMEVE1–NUMEVE6	
ETIMEO	ETIMEO1–ETIMEO6	
URETRY	URETRY1–URETRY6	
UTIMEO	UTIMEO1–UTIMEO6	
PMOIPA1–PMOIPA2	PMOIPA1–PMOIPA2	
PMOUDP1–PMOUDP2	PMOUDP1–PMOUDP2	The range is slightly more restrictive in the SEL-487E-3, -4 implementation. The lowest assignable port is 1025.

DNP3 Mapping Changes

DNP3 Settings Classes

In the SEL-487E-0, -2 versions of DNP3, there was one map (SET_D1.TXT) for serial DNP3 and five maps (CARD\SET_DNP*n*.TXT, where *n* = 1–5) for Ethernet DNP3. In the SEL-487E-3, -4, there are five maps (SET_D*n*.TXT, where *n* = 1–5) that can be used for serial or Ethernet DNP3.

Serial DNP3 Map Value Changes

The previous serial DNP3 map was based on numeric references for all data. The SEL-487E-3, -4 DNP3 mapping uses labels. The following tables show the relationships between the old numeric references and the labels.

Binary Inputs (MAPSEL = B)

For numeric references 0–799 and 800–1599, see *Table E.13: SEL-487E Object 1, 2 Relay Word Bit Mapping in the SEL-487E-0 Instruction Manual*. Note that the numeric reference ranges 0–799 and 800–1599 are equivalent, the only difference being whether SER quality time-tags are used. The labels from this table will work in the SEL-487E-3, -4, with the exception of those noted in the Relay Word bit mapping (*Table B.4*). Indexes that correspond to reserved points (*) can be treated as a fixed '0' in the new map.

Table B.4   Binary Inputs Point Mapping for MAPSEL = B

Numeric Reference	Label Reference	Notes
1616	RLYDIS	
1617	STFAIL	
1618	STWARN	
1619	UNRDEV	
1620	STSET	
1621–1631	0	

Binary Inputs (MAPSEL = E)

Table B.5 lists the mapping for Points 0–15.

Table B.5   Serial DNP3 Extended Map Binary Input Reference Mapping

Numeric Reference	Label Reference	Notes
0	RLYDIS	
1	STFAIL	
2	STWARN	
3	UNRDEV	
4	STSET	
5–15	0	

References 16–265 do not have a good equivalent, because they were dependent on the SER settings.

References 266–271 are reserved so they have no equivalent mapping.

References 272 and above simply map to the SEL-487E-3, -4 Relay Word, starting at Bit 0. To find the label equivalent for these points, subtract 272 from the reference to get the bit number and then find the bit within *Section 11: Relay Word Bits*. You can then use that bit, except as noted in *Table B.1*.

Binary Outputs

Table B.6   Serial DNP3 Binary Output Reference Mapping (Sheet 1 of 4)

Numeric Reference	Label Reference	Notes
0	RB01	
1	RB02	
2	RB03	
3	RB04	

Table B.6 Serial DNP3 Binary Output Reference Mapping (Sheet 2 of 4)

Numeric Reference	Label Reference	Notes
4	RB05	
5	RB06	
6	RB07	
7	RB08	
8	RB09	
9	RB10	
10	RB11	
11	RB12	
12	RB13	
13	RB14	
14	RB15	
15	RB16	
16	RB17	
17	RB18	
18	RB19	
19	RB20	
20	RB21	
21	RB22	
22	RB23	
23	RB24	
24	RB25	
25	RB26	
26	RB27	
27	RB28	
28	RB29	
29	RB30	
30	RB31	
31	RB32	
32	RB01:RB02	
33	RB03:RB04	
34	RB05:RB06	
35	RB07:RB08	
36	RB09:RB10	
37	RB11:RB12	
38	RB13:RB14	
39	RB15:RB16	
40	RB17:RB18	
41	RB19:RB20	
42	RB21:RB22	
43	RB23:RB24	
44	RB25:RB26	

Table B.6   Serial DNP3 Binary Output Reference Mapping (Sheet 3 of 4)

Numeric Reference	Label Reference	Notes
45	RB27:RB28	
46	RB29:RB30	
47	RB31:RB32	
48	OCS	
49	CCS	
50	OCT	
51	CCT	
52	OCU	
53	CCU	
54	OCW	
55	CCW	
56	OCX	
57	CCX	
58–63	unused	
64	OCS:CCS	
65	OCT:CCT	
66	OCU:CCU	
67	OCW:CCW	
68	OCX:CCX	
69–71	unused	
72	RST_DEM	
73	RST_PDM	
74	RST_ENE	
75	RSTTRGT	
76	NXTEVE	
77–79	unused	
80	RST_BKS	
81	RST_BKT	
82	RST_BKU	
83	RST_BKW	
84	RST_BKX	
85–87	unused	
88	89OC1	
89	89CC1	
90	89OC2	
91	89CC2	
92	89OC3	
93	89CC3	
94	89OC4	
95	89CC4	
96	89OC5	

Table B.6 Serial DNP3 Binary Output Reference Mapping (Sheet 4 of 4)

Numeric Reference	Label Reference	Notes
97	89CC5	
98	89OC6	
99	89CC6	
100	89OC7	
101	89CC7	
102	89OC8	
103	89CC8	
104	89OC1:89CC1	
105	89OC2:89CC2	
106	89OC3:89CC3	
107	89OC4:89CC4	
108	89OC5:89CC5	
109	89OC6:89CC6	
110	89OC7:89OC7	
111	89OC8:89CC8	

Counters

Table B.7 Serial DNP3 Counter Reference Mapping

Numeric Reference	Label Reference
0	ACTGRP
4	BKRSOP
5	BKRTOP
6	BKRUOP
7	BKRWOP
8	BKRXOP

Analog Inputs

Table B.8 Serial DNP3 Analog Input Reference Mapping (Sheet 1 of 11)

Numeric Reference	Label Reference
0	IASFMC
1	IASFAC
2	IBSFMC
3	IBSFAC
4	ICSFMC
5	ICSFAC
6	3I0SMC
7	3I0SAC
8	I1SMC
9	I1SAC

Table B.8   Serial DNP3 Analog Input Reference Mapping (Sheet 2 of 11)

Numeric Reference	Label Reference
10	3I2SMC
11	3I2SAC
12	IATFMC
13	IATFAC
14	IBTFMC
15	IBTFAC
16	ICTFMC
17	ICTFAC
18	3I0TMC
19	3I0TAC
20	I1TMC
21	I1TAC
22	3I2TMC
23	3I2TAC
24	IAUFMC
25	IAUFAC
26	IBSUMC
27	IBSUAC
28	ICUFMC
29	ICUFAC
30	3I0UMC
31	3I0UAC
32	I1UMC
33	I1UAC
34	3I2UMC
35	3I2UAC
36	IAWFMC
37	IAWFAC
38	IBWFMC
39	IBWFAC
40	ICWFMC
41	ICWFAC
42	3I0WMC
43	3I0WAC
44	I1WMC
45	I1WAC
46	3I2WMC
47	3I2WAC
48	IAXFMC
49	IAXFAC
50	IBXFMC

Table B.8   Serial DNP3 Analog Input Reference Mapping (Sheet 3 of 11)

Numeric Reference	Label Reference
51	IBXFAC
52	IBXFMC
53	ICXFAC
54	3I0XMC
55	3I0XAC
56	I1XMC
57	I1XAC
58	3I2XMC
59	3I2XAC
60	IAYFMC
61	IAYFAC
62	IBYFMC
63	IBYFAC
64	ICYFMC
65	ICYFAC
66	IASTFMC
67	IASTFAC
68	IBSTFMC
69	IBSTFAC
70	ICSTFMC
71	ICSTFAC
72	3I0STMC
73	3I0STAC
74	I1STMC
75	I1STAC
76	3I2STMC
77	3I2STAC
78	IATUFMC
79	IATUFAC
80	IBTUFMC
81	IBTUFAC
82	ICTUFMC
83	ICTUFAC
84	3I0TUMC
85	3I0TUAC
86	I1TUMC
87	I1TUAC
88	3I2TUMC
89	3I2TUAC
90	IAUWFMC
91	IAUWFAC

Table B.8 Serial DNP3 Analog Input Reference Mapping (Sheet 4 of 11)

Numeric Reference	Label Reference
92	IBUWFMC
93	IBUWFAC
94	ICUWFMC
95	ICUWFAC
96	3I0UWMC
97	3I0UWAC
98	I1UWMC
99	I1UWAC
100	3I2UWMC
101	3I2UWAC
102	IAWXFMC
103	IAWXFAC
104	IBWXFMC
105	IBWXFAC
106	ICWXFMC
107	ICWXFAC
108	3I0WXMC
109	3I0WXAC
110	I1WXMC
111	I1WXAC
112	3I2WXMC
113	3I2WXAC
114	VAVFMC
115	VAVFAC
116	VBVFMC
117	VBVFAC
118	VCVFMC
119	VCVFAC
120	VABVFMC
121	VABVFAC
122	VBCVFMC
123	VBCVFAC
124	VCAVFMC
125	VCAVFAC
126	3V0VFM
127	3V0VFA
128	V1VMC
129	V1VMA
130	3V2VMC
131	3V2VMA
132	VAZFAC

Table B.8 Serial DNP3 Analog Input Reference Mapping (Sheet 5 of 11)

Numeric Reference	Label Reference
133	VAZFAC
134	VBZFMC
135	VBZFAC
136	VCZFMC
137	VCZFAC
138	VABZFMC
139	VABZFAC
140	VBCZFMC
141	VBCZFAC
142	VCAZFMC
143	VCAZFAC
144	3V0ZFM
145	3V0ZFA
146	V1ZMC
147	V1ZMA
148	3V2ZMC
149	3V2ZMA
150	PASFS
151	QASFS
152	SASFS
153	PBSFS
154	QBSFS
155	SBSFS
156	PCSFS
157	QCSFS
158	SCSFS
159	3PSFS
160	3QSFS
161	3SSFS
162	PATFS
163	QATFS
164	SATFS
165	PBTFS
166	QBTFS
167	SBTFS
168	PCTFS
169	QCTFS
170	SCTFS
171	3PTFS
172	3QTFS
173	3STFS

Table B.8 Serial DNP3 Analog Input Reference Mapping (Sheet 6 of 11)

Numeric Reference	Label Reference
174	PAUFS
175	QAUFS
176	SAUFS
177	PBUFS
178	QBUFS
179	SBUFS
180	PCUFS
181	QCUFS
182	SCUFS
183	3PUFS
184	3QUFS
185	3SUFS
186	PAWFS
187	QAWFS
188	SAWFS
189	PBWFS
190	QBWFS
191	SBWFS
192	PCWFS
193	QCWFS
194	SCWFS
195	3PWFS
196	3QWFS
197	3SWFS
198	PAXFS
199	QAXFS
200	SAXFS
201	PBXFS
202	QBXFS
203	SBXFS
204	PCXFS
205	QCXFS
206	SCXFS
207	3PXFS
208	3QXFS
209	3SXFS
210	PASTFS
211	QASTFS
212	SASTFS
213	PBSTFS
214	QBSTFS

Table B.8   Serial DNP3 Analog Input Reference Mapping (Sheet 7 of 11)

Numeric Reference	Label Reference
215	SBSTFS
216	PCSTFS
217	QCSTFS
218	SCSTFS
219	3PSTFS
220	3QSTFS
221	3SSTFS
222	PATUFS
223	QATUFS
224	SATUFS
225	PBTUFS
226	QBTUFS
227	SBTUFS
228	PCTUFS
229	QCTUFS
230	SCTUFS
231	3PTUFS
232	3QTUFS
233	3STUFS
234	PAUWFS
235	QAUWFS
236	SAUWFS
237	PBUWFS
238	QBUWFS
239	SBUWFS
240	PCUWFS
241	QCUWFS
242	SCUWFS
243	3PUWFS
244	3QUWFS
245	3SUWFS
246	PAWXFS
247	QAWXFS
248	SAWXFS
249	PBWXFS
250	QBWXFS
251	SBWXFS
252	PCWXFS
253	QCWXFS
254	SCWXFS
255	3PWXFS

Table B.8   Serial DNP3 Analog Input Reference Mapping (Sheet 8 of 11)

Numeric Reference	Label Reference
256	3QWXFS
257	3SWXFS
258	DPFAS
259	DPFBS
260	DPFCS
261	3DPFS
252	DPFAT
253	DPFBT
264	DPFCT
265	3DPFT
266	DPFAU
267	DPFBU
268	DPFCU
269	3DPFU
270	DPFAW
271	DPFBW
272	DPFCW
273	3DPFW
274	DPFAX
275	DPFBX
276	DPFCX
277	3DPFX
278	DPFAST
279	DPFBST
280	DPFCST
281	3DPFST
282	DPFATU
283	DPFBTU
284	DPFCTU
285	3DPFTU
286	DPFAUW
287	DPFBUW
288	DPFCUW
289	3DPFUW
290	DPFAWX
291	DPFBWX
292	DPFCWX
293	3DPFWX
294	3PSN_MWH
295	3PSP_MWH
296	3PST_MWH

Table B.8 Serial DNP3 Analog Input Reference Mapping (Sheet 9 of 11)

Numeric Reference	Label Reference
297	3QSN_MVARH
298	3QSP_MVARH
299	3QST_MVARH
300	3PTN_MWH
301	3PTP_MWH
302	3PTT_MWH
303	3QTN_MVARH
304	3QTP_MVARH
305	3QTT_MVARH
306	3PUN_MWH
307	3PUP_MWH
308	3PUT_MWH
309	3QUN_MVARH
310	3QUP_MVARH
311	3QUT_MVARH
312	3PWN_MWH
313	3PWP_MWH
314	3PWT_MWH
315	3QWN_MVARH
316	3QWP_MVARH
317	3QWT_MVARH
318	3PXN_MWH
319	3PXP_MWH
320	2PXT_MWH
321	3QXN_MVARH
322	3QXP_MVARH
323	3QXT_MVARH
324	3PSTN_MWH
325	3PSTP_MWH
326	3PSTT_MWH
327	3QSTN_MVARH
328	3QSTP_MVARH
329	3QSTT_MVARH
330	3PTUN_MWH
331	3PTUP_MWH
332	3PTUT_MWH
333	3QTUN_MVARH
334	3QTUP_MVARH
335	3QTUT_MVARH
336	3PUWN_MWH
337	3PUWP_MWH

Table B.8 Serial DNP3 Analog Input Reference Mapping (Sheet 10 of 11)

Numeric Reference	Label Reference
338	3PUWT_MWH
339	3QUWN_MVARH
340	3QUWP_MVARH
341	3QUWT_MVARH
342	3PWXN_MWH
343	3PWXP_MWH
344	3PWXT_MWH
345	3QWXN_MVARH
346	3QWXP_MVARH
347	3QWXT_MVARH
348	87IOPAC
349	87IOPBC
350	87IOPCC
351	87IRTAC
352	87IRTBC
353	87IRTCC
354	DC1
355	FREQ
356	RLYTEMP
357	unused
358–367	DM_01–DM_10
368–377	DMM_01–DMM_10
378	BSBCWPA
379	BSBCWPB
380	BSBCWPC
381	BTBCWPA
382	BTBCWPB
383	BTBCWPC
384	BUBCWPA
385	BUBCWPB
386	BUBCWPC
387	BWBCWPA
388	BWBCWPB
389	BWBCWPC
390	BXBCWPA
391	BXBCWPB
392	BXBCWPC
393–399	unused
400	FTYPE
401	FTAR1
402	FTAR2

Table B.8   Serial DNP3 Analog Input Reference Mapping (Sheet 11 of 11)

Numeric Reference	Label Reference
403	unused
404	FFREQ
405	FGRP
406–407	unused
408	FTIMEH
409	FTIMEM
410	FTIMEL
411–419	unused
420–451	AMV001–AMV032

Analog Outputs

Table B.9   Serial DNP3 Analog Output Reference Mapping

Numeric Reference	Label Reference
0	ACTGRP

Ethernet DNP3 Map Value Changes

The SEL-487E-0, -2 Ethernet DNP3 map was based on database references. The SEL-487E-3, -4 DNP3 mapping uses direct data labels. The following sections describe how to get from this database mapping to the new direct data labels.

Binary Inputs

In the SEL-487E-0, -2 mapping, any bit in the database could be referenced for use by DNP3. In the SEL-487E-3, -4, only Relay Word bits and a few other special bits can be used. The old reference format looked like 1:addr:bit. If addr is 3004h or greater, but not greater than 4000h, then the bits can be associated with the SEL-487E-3, -4 Relay Word. Address 3004h corresponds to Relay Word 0, 3005h to row 1, for example. The bits are simply references in the range 0 to 7 and match the bits within the Relay Word row. Thus the Relay Word bits can be mapped to labels by using the Relay Word table and correcting for any label changes, as noted in *Table B.1*.

Binary Outputs

In the SEL-478E-0, -2, Indexes 0–127 mapped to the CCIN bits. The end-user can remap 32 CCIN bits to the 32 available remote bits. Additional controls are provided. See *Table 10.16* for a complete list of available DNP3 Binary Output control points in the SEL-487E-3, -4 Relay.

Counters

In the SEL-487E-0, -2, counters were referenced as points in the database. There is no direct equivalent in the SEL-487E-3, -4, so this will need to be analyzed to determine the appropriate counter mapping.

Analog Inputs

In the SEL-487E-0, -2, analog inputs were referenced as points in the database with optional "treat as" qualifiers and with per-point class selection. There is no direct equivalent in the SEL-487E-3, -4, so this will need to be analyzed to determine the appropriate analog input mapping.

Analog Outputs

In the SEL-487E-0, -2, analog outputs were referenced by index (0 to 255). These mapped to remote analogs (RA001 to RA256). In the SEL-487E-3, -4, these same remote analogs are available. So if previously Index 0 was referenced, the new reference is RA001. Similarly, Index 1 goes to RA002, etc.

IEC 61850 Object Changes

The SEL-487E-0, -2 implementation of the IEC 61850 protocol suite differs slightly from the SEL-487E-3, -4 implementation. *Table B.10* lists the main functional changes between the two.

Table B.10   IEC 61850 Functional Differences

Topic	SEL-487E-0, -2	SEL-487E-3, -4
ICD File Version	Version 001, 002	Version 003
Incoming GOOSE	Mappable to CCIN001–CCIN128 (binary data)	VB001–VB256 (binary data)
RA001–RA256 (analog data)		
Outgoing GOOSE	Relay Word bits mapped to CCOUT01–CCOUT32 (binary data only)	N/A (Relay Word bits can be sent directly without intermediate mapping; Analog data in RAO01–RAO64 are also available as outputs.)
SER Time stamps	SER-quality time stamps only available for LNs as listed in the SER data set (not editable)	Any points in the SER list (SET R) will have SER-quality time stamps. Otherwise, time-stamp accuracy is within 500 ms of relay time.
Controls	Direct Operate with Normal Security only	Direct Operate with Enhanced Security and Select-Before-Operate (SBO) with Enhanced Security is also available.

Default datasets may be used for MMS Reports or for GOOSE message transmission. *Table B.11* lists the default data set changes in the new ICD file version. Note that the contents of any data set may be modified via ACSELERATOR Architect SEL-5032 Software.

Table B.11   Default Data Set Differences (Sheet 1 of 2)

Default Data Set Description	SEL-487E-0, -2	SEL-487E-3, -4	
	Data Set Names	Data Set Names	Changes
Breaker and Switches	DSet02 and DSet08	DSet02 and DSet10	Added X89CLXSWI9 and 10.
Trips and CCIN	DSet06 and DSet12	DSet06 and DSet13	Replaced CCIN01–CCIN16 with VB001–VB016 mapped LNs.

Table B.11 Default Data Set Differences (Sheet 2 of 2)

Default Data Set Description	SEL-487E-0, -2	SEL-487E-3, -4	
	Data Set Names	Data Set Names	Changes
Counter Values	NA	DSet07 and DSet14	New data set for PCN001–PCN016 and ACN001–ACN016 mapped LNs.
LN points that can provide SER-quality time stamps	Ser1	NA	Removed. Any point in the SER list will have SER-quality time stamps.

Most of the Logical Nodes and Attributes remain the same between the two implementations. *Table B.12* lists the mapping changes in the new ICD file.

Table B.12 Logical Node and Mapping Differences (Sheet 1 of 11)

LD	SEL-487E-0, -2		SEL-487E-3, -4	
	LN	Path	Mapping	Mapping
PRO	SBKRCSWI1	Pos.Oper.ctlVal	BR01?CLEAR:SET	CCS:OCS
PRO	TBKRCSWI2	Pos.Oper.ctlVal	BR02?CLEAR:SET	CCT:OCT
PRO	UBKRCSWI3	Pos.Oper.ctlVal	BR03?CLEAR:SET	CCU:OCU
PRO	WBKRCSWI4	Pos.Oper.ctlVal	BR04?CLEAR:SET	CCW:OCW
PRO	XBKRCSWI5	Pos.Oper.ctlVal	BR05?CLEAR:SET	CCX:OCX
PRO	DC1CSWI6	Pos.Oper.ctlVal	BR06?CLEAR:SET	89CC01:89OC01
PRO	DC2CSWI7	Pos.Oper.ctlVal	BR07?CLEAR:SET	89CC02:89OC02
PRO	DC3CSWI8	Pos.Oper.ctlVal	BR08?CLEAR:SET	89CC03:89OC03
PRO	DC4CSWI9	Pos.Oper.ctlVal	BR09?CLEAR:SET	89CC04:89OC04
PRO	DC5CSWI10	Pos.Oper.ctlVal	BR10?CLEAR:SET	89CC05:89OC05
PRO	DC6CSWI11	Pos.Oper.ctlVal	BR11?CLEAR:SET	89CC06:89OC06
PRO	DC7CSWI12	Pos.Oper.ctlVal	BR12?CLEAR:SET	89CC07:89OC07
PRO	DC8CSWI13	Pos.Oper.ctlVal	BR13?CLEAR:SET	89CC08:89OC08
PRO	DC1CSWI6	OpCls.general	89CLS1	89CL01
PRO	DC1CSWI6	OpOpn.general	89OPEN1	89OPN01
PRO	DC1CSWI6	Pos.stVal	89CL1|89OPN1?0:1:2:3	89CL01|89OPN01?0:1:2:3
PRO	DC2CSWI7	OpCls.general	89CLS2	89CL02
PRO	DC2CSWI7	OpOpn.general	89OPEN2	89OPN02
PRO	DC2CSWI7	Pos.stVal	89CL2|89OPN2?0:1:2:3	89CL02|89OPN02?0:1:2:3
PRO	DC3CSWI8	OpCls.general	89CLS3	89CL03
PRO	DC3CSWI8	OpOpn.general	89OPEN3	89OPN03
PRO	DC3CSWI8	Pos.stVal	89CL3|89OPN3?0:1:2:3	89CL03|89OPN03?0:1:2:3
PRO	DC4CSWI9	OpCls.general	89CLS4	89CL04
PRO	DC4CSWI9	OpOpn.general	89OPEN4	89OPN04
PRO	DC4CSWI9	Pos.stVal	89CL4|89OPN4?0:1:2:3	89CL04|89OPN04?0:1:2:3
PRO	DC5CSWI10	OpCls.general	89CLS5	89CL05
PRO	DC5CSWI10	OpOpn.general	89OPEN5	89OPN05
PRO	DC5CSWI10	Pos.stVal	89CL5|89OPN5?0:1:2:3	89CL05|89OPN05?0:1:2:3
PRO	DC6CSWI11	OpCls.general	89CLS6	89CL06
PRO	DC6CSWI11	OpOpn.general	89OPEN6	89OPN06

Table B.12   Logical Node and Mapping Differences (Sheet 2 of 11)

LD	SEL-487E-0, -2			SEL-487E-3, -4
	LN	Path	Mapping	Mapping
PRO	DC6CSWI11	Pos.stVal	89CL6|89OPN6?0:1:2:3	89CL06|89OPN06?0:1:2:3
PRO	DC7CSWI12	OpCls.general	89CLS7	89CL07
PRO	DC7CSWI12	OpOpn.general	89OPEN7	89OPN07
PRO	DC7CSWI12	Pos.stVal	89CL7|89OPN7?0:1:2:3	89CL07|89OPN07?0:1:2:3
PRO	DC8CSWI13	OpCls.general	89CLS8	89CL08
PRO	DC8CSWI13	OpOpn.general	89OPEN8	89OPN08
PRO	DC8CSWI13	Pos.stVal	89CL8|89OPN8?0:1:2:3	89CL08|89OPN08?0:1:2:3
PRO	X89CLXSWI1	Pos.stVal	89CL1?1:2	89CL01?1:2
PRO	X89CLXSWI2	Pos.stVal	89CL2?1:2	89CL02?1:2
PRO	X89CLXSWI3	Pos.stVal	89CL3?1:2	89CL03?1:2
PRO	X89CLXSWI4	Pos.stVal	89CL4?1:2	89CL04?1:2
PRO	X89CLXSWI5	Pos.stVal	89CL5?1:2	89CL05?1:2
PRO	X89CLXSWI6	Pos.stVal	89CL6?1:2	89CL06?1:2
PRO	X89CLXSWI7	Pos.stVal	89CL7?1:2	89CL07?1:2
PRO	X89CLXSWI8	Pos.stVal	89CL8?1:2	89CL08?1:2
MET	METSMMXU1	A1.phsA.instCVal.mag.f	1:METER:IS[0]	IASFAC
MET	METSMMXU1	A1.phsA.instCVal.ang.f	1:METER:IS[1]	IASFMC
MET	METSMMXU1	A1.phsB.instCVal.mag.f	1:METER:IS[2]	IBSFAC
MET	METSMMXU1	A1.phsB.instCVal.ang.f	1:METER:IS[3]	IBSFMC
MET	METSMMXU1	A1.phsC.instCVal.mag.f	1:METER:IS[4]	ICSFAC
MET	METSMMXU1	A1.phsC.instCVal.ang.f	1:METER:IS[5]	ICSFMC
MET	METSMMXU1	PF.phsA.instMag.f	1:METER:PFS[0]	DPFAS
MET	METSMMXU1	PF.phsB.instMag.f	1:METER:PFS[1]	DPFBS
MET	METSMMXU1	PF.phsC.instMag.f	1:METER:PFS[2]	DPFCS
MET	METSMMXU1	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METSMMXU1	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METSMMXU1	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METSMMXU1	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METSMMXU1	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METSMMXU1	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METSMMXU1	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METSMMXU1	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METSMMXU1	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METSMMXU1	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METSMMXU1	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METSMMXU1	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METSMMXU1	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METSMMXU1	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METSMMXU1	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METSMMXU1	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12   Logical Node and Mapping Differences (Sheet 3 of 11)

LD	SEL-487E-0, -2			SEL-487E-3, -4
	LN	Path	Mapping	Mapping
MET	METSMMXU1	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METSMMXU1	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METSMMXU1	TotPF.instMag.f	1:METER:PFS[3]	3DPFS
MET	METSMMXU1	TotVA.instMag.f	1:METER:SS[3]	3SSFC
MET	METSMMXU1	TotVAr.instMag.f	1:METER:QS[3]	3QSFC
MET	METSMMXU1	TotW.instMag.f	1:METER:PS[3]	3PSFC
MET	METSMMXU1	VA.phsA.instMag.f	1:METER:SS[0]	SASFC
MET	METSMMXU1	VA.phsB.instMag.f	1:METER:SS[1]	SBSFC
MET	METSMMXU1	VA.phsC.instMag.f	1:METER:SS[2]	SCSFC
MET	METSMMXU1	VAr.phsA.instMag.f	1:METER:QS[0]	QASFC
MET	METSMMXU1	VAr.phsB.instMag.f	1:METER:QS[1]	QBSFC
MET	METSMMXU1	VAr.phsC.instMag.f	1:METER:QS[2]	QCSFC
MET	METSMMXU1	W.phsA.instMag.f	1:METER:PS[0]	PASFC
MET	METSMMXU1	W.phsB.instMag.f	1:METER:PS[1]	PBSFC
MET	METSMMXU1	W.phsC.instMag.f	1:METER:PS[2]	PCSFC
MET	METSTMMXU6	A1.phsA.instCVal.mag.f	1:METER:IST[0]	IASTFAC
MET	METSTMMXU6	A1.phsA.instCVal.ang.f	1:METER:IST[1]	IASTFMC
MET	METSTMMXU6	A1.phsB.instCVal.mag.f	1:METER:IST[2]	IBSTFAC
MET	METSTMMXU6	A1.phsB.instCVal.ang.f	1:METER:IST[3]	IBSTFMC
MET	METSTMMXU6	A1.phsC.instCVal.mag.f	1:METER:IST[4]	ICSTFAC
MET	METSTMMXU6	A1.phsC.instCVal.ang.f	1:METER:IST[5]	ICSTFMC
MET	METSTMMXU6	PF.phsA.instMag.f	1:METER:PFST[0]	DPFAST
MET	METSTMMXU6	PF.phsB.instMag.f	1:METER:PFST[1]	DPFBST
MET	METSTMMXU6	PF.phsC.instMag.f	1:METER:PFST[2]	DPFCST
MET	METSTMMXU6	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METSTMMXU6	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METSTMMXU6	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METSTMMXU6	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METSTMMXU6	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METSTMMXU6	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METSTMMXU6	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METSTMMXU6	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METSTMMXU6	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METSTMMXU6	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METSTMMXU6	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METSTMMXU6	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METSTMMXU6	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METSTMMXU6	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METSTMMXU6	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METSTMMXU6	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12   Logical Node and Mapping Differences (Sheet 4 of 11)

LD	SEL-487E-0, -2			SEL-487E-3, -4
	LN	Path	Mapping	Mapping
MET	METSTMMXU6	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METSTMMXU6	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METSTMMXU6	TotPF.instMag.f	1:METER:PFST[3]	3DPFST
MET	METSTMMXU6	TotVA.instMag.f	1:METER:SST[3]	3SSTFC
MET	METSTMMXU6	TotVAr.instMag.f	1:METER:QST[3]	3QSTFC
MET	METSTMMXU6	TotW.instMag.f	1:METER:PST[3]	3PSTFC
MET	METSTMMXU6	VA.phsA.instMag.f	1:METER:SST[0]	SASTFC
MET	METSTMMXU6	VA.phsB.instMag.f	1:METER:SST[1]	SBSTFC
MET	METSTMMXU6	VA.phsC.instMag.f	1:METER:SST[2]	SCSTFC
MET	METSTMMXU6	VAr.phsA.instMag.f	1:METER:QST[0]	QASTFC
MET	METSTMMXU6	VAr.phsB.instMag.f	1:METER:QST[1]	QBSTFC
MET	METSTMMXU6	VAr.phsC.instMag.f	1:METER:QST[2]	QCSTFC
MET	METSTMMXU6	W.phsA.instMag.f	1:METER:PST[0]	PASTFC
MET	METSTMMXU6	W.phsB.instMag.f	1:METER:PST[1]	PBSTFC
MET	METSTMMXU6	W.phsC.instMag.f	1:METER:PST[2]	PCSTFC
MET	METTMMXU2	A1.phsA.instCVal.mag.f	1:METER:IT[0]	IATFAC
MET	METTMMXU2	A1.phsA.instCVal.ang.f	1:METER:IT[1]	IATFMC
MET	METTMMXU2	A1.phsB.instCVal.mag.f	1:METER:IT[2]	IBTFAC
MET	METTMMXU2	A1.phsB.instCVal.ang.f	1:METER:IT[3]	IBTFMC
MET	METTMMXU2	A1.phsC.instCVal.mag.f	1:METER:IT[4]	ICTFAC
MET	METTMMXU2	A1.phsC.instCVal.ang.f	1:METER:IT[5]	ICTFMC
MET	METTMMXU2	PF.phsA.instMag.f	1:METER:PFT[0]	DPFAT
MET	METTMMXU2	PF.phsB.instMag.f	1:METER:PFT[1]	DPFBT
MET	METTMMXU2	PF.phsC.instMag.f	1:METER:PFT[2]	DPFCT
MET	METTMMXU2	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METTMMXU2	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METTMMXU2	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METTMMXU2	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METTMMXU2	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METTMMXU2	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METTMMXU2	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METTMMXU2	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METTMMXU2	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METTMMXU2	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METTMMXU2	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METTMMXU2	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METTMMXU2	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METTMMXU2	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METTMMXU2	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METTMMXU2	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12   Logical Node and Mapping Differences (Sheet 5 of 11)

LD	SEL-487E-0, -2			SEL-487E-3, -4
	LN	Path	Mapping	Mapping
MET	METTMMXU2	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METTMMXU2	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METTMMXU2	TotPF.instMag.f	1:METER:PFT[3]	3DPFT
MET	METTMMXU2	TotVA.instMag.f	1:METER:ST[3]	3STFC
MET	METTMMXU2	TotVAr.instMag.f	1:METER:QT[3]	3QTFC
MET	METTMMXU2	TotW.instMag.f	1:METER:PT[3]	3PTFC
MET	METTMMXU2	VA.phsA.instMag.f	1:METER:ST[0]	SATFC
MET	METTMMXU2	VA.phsB.instMag.f	1:METER:ST[1]	SBTFC
MET	METTMMXU2	VA.phsC.instMag.f	1:METER:ST[2]	SCTFC
MET	METTMMXU2	VAr.phsA.instMag.f	1:METER:QT[0]	QATFC
MET	METTMMXU2	VAr.phsB.instMag.f	1:METER:QT[1]	QBTFC
MET	METTMMXU2	VAr.phsC.instMag.f	1:METER:QT[2]	QCTFC
MET	METTMMXU2	W.phsA.instMag.f	1:METER:PT[0]	PATFC
MET	METTMMXU2	W.phsB.instMag.f	1:METER:PT[1]	PBTFC
MET	METTMMXU2	W.phsC.instMag.f	1:METER:PT[2]	PCTFC
MET	METTUMMXU7	A1.phsA.instCVal.mag.f	1:METER:ITU[0]	IATUFAC
MET	METTUMMXU7	A1.phsA.instCVal.ang.f	1:METER:ITU[1]	IATUFMC
MET	METTUMMXU7	A1.phsB.instCVal.mag.f	1:METER:ITU[2]	IBTUFAC
MET	METTUMMXU7	A1.phsB.instCVal.ang.f	1:METER:ITU[3]	IBTUFMC
MET	METTUMMXU7	A1.phsC.instCVal.mag.f	1:METER:ITU[4]	ICTUFAC
MET	METTUMMXU7	A1.phsC.instCVal.ang.f	1:METER:ITU[5]	ICTUFMC
MET	METTUMMXU7	PF.phsA.instMag.f	1:METER:PFTU[0]	DPFATU
MET	METTUMMXU7	PF.phsB.instMag.f	1:METER:PFTU[1]	DPFBTU
MET	METTUMMXU7	PF.phsC.instMag.f	1:METER:PFTU[2]	DPFCTU
MET	METTUMMXU7	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METTUMMXU7	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METTUMMXU7	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METTUMMXU7	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METTUMMXU7	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METTUMMXU7	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METTUMMXU7	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METTUMMXU7	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METTUMMXU7	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METTUMMXU7	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METTUMMXU7	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METTUMMXU7	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METTUMMXU7	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METTUMMXU7	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METTUMMXU7	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METTUMMXU7	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12   Logical Node and Mapping Differences (Sheet 6 of 11)

LD	SEL-487E-0, -2		SEL-487E-3, -4	
	LN	Path	Mapping	Mapping
MET	METTUMMXU7	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METTUMMXU7	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METTUMMXU7	TotPF.instMag.f	1:METER:PFTU[3]	3DPFTU
MET	METTUMMXU7	TotVA.instMag.f	1:METER:STU[3]	3STUFC
MET	METTUMMXU7	TotVAr.instMag.f	1:METER:QTU[3]	3QTUFC
MET	METTUMMXU7	TotW.instMag.f	1:METER:PTU[3]	3PTUFC
MET	METTUMMXU7	VA.phsA.instMag.f	1:METER:STU[0]	SATUFC
MET	METTUMMXU7	VA.phsB.instMag.f	1:METER:STU[1]	SBTUFC
MET	METTUMMXU7	VA.phsC.instMag.f	1:METER:STU[2]	SCTUFC
MET	METTUMMXU7	VAr.phsA.instMag.f	1:METER:QTU[0]	QATUFC
MET	METTUMMXU7	VAr.phsB.instMag.f	1:METER:QTU[1]	QBTUFC
MET	METTUMMXU7	VAr.phsC.instMag.f	1:METER:QTU[2]	QCTUFC
MET	METTUMMXU7	W.phsA.instMag.f	1:METER:PTU[0]	PATUFC
MET	METTUMMXU7	W.phsB.instMag.f	1:METER:PTU[1]	PBTUFC
MET	METTUMMXU7	W.phsC.instMag.f	1:METER:PTU[2]	PCTUFC
MET	METUMMXU3	A1.phsA.instCVal.mag.f	1:METER:IU[0]	IAUFAC
MET	METUMMXU3	A1.phsA.instCVal.ang.f	1:METER:IU[1]	IAUFMC
MET	METUMMXU3	A1.phsB.instCVal.mag.f	1:METER:IU[2]	IBUFAC
MET	METUMMXU3	A1.phsB.instCVal.ang.f	1:METER:IU[3]	IBUFMC
MET	METUMMXU3	A1.phsC.instCVal.mag.f	1:METER:IU[4]	ICUFAC
MET	METUMMXU3	A1.phsC.instCVal.ang.f	1:METER:IU[5]	ICUFMC
MET	METUMMXU3	PF.phsA.instMag.f	1:METER:PFU[0]	DPFAU
MET	METUMMXU3	PF.phsB.instMag.f	1:METER:PFU[1]	DPFBU
MET	METUMMXU3	PF.phsC.instMag.f	1:METER:PFU[2]	DPFCU
MET	METUMMXU3	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METUMMXU3	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METUMMXU3	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METUMMXU3	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METUMMXU3	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METUMMXU3	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METUMMXU3	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METUMMXU3	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METUMMXU3	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METUMMXU3	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METUMMXU3	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METUMMXU3	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METUMMXU3	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METUMMXU3	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METUMMXU3	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METUMMXU3	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12   Logical Node and Mapping Differences (Sheet 7 of 11)

LD	SEL-487E-0, -2		SEL-487E-3, -4	
	LN	Path	Mapping	Mapping
MET	METUMMXU3	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METUMMXU3	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METUMMXU3	TotPF.instMag.f	1:METER:PFU[3]	3DPFU
MET	METUMMXU3	TotVA.instMag.f	1:METER:SU[3]	3SUFC
MET	METUMMXU3	TotVAr.instMag.f	1:METER:QU[3]	3QUFC
MET	METUMMXU3	TotW.instMag.f	1:METER:PU[3]	3PUFC
MET	METUMMXU3	VA.phsA.instMag.f	1:METER:SU[0]	SAUFC
MET	METUMMXU3	VA.phsB.instMag.f	1:METER:SU[1]	SBUFC
MET	METUMMXU3	VA.phsC.instMag.f	1:METER:SU[2]	SCUFC
MET	METUMMXU3	VAr.phsA.instMag.f	1:METER:QU[0]	QAUFC
MET	METUMMXU3	VAr.phsB.instMag.f	1:METER:QU[1]	QBUFC
MET	METUMMXU3	VAr.phsC.instMag.f	1:METER:QU[2]	QCUFC
MET	METUMMXU3	W.phsA.instMag.f	1:METER:PU[0]	PAUFC
MET	METUMMXU3	W.phsB.instMag.f	1:METER:PU[1]	PBUFC
MET	METUMMXU3	W.phsC.instMag.f	1:METER:PU[2]	PCUFC
MET	METUWMMXU8	A1.phsA.instCVal.mag.f	1:METER:IUW[0]	IAUWFAC
MET	METUWMMXU8	A1.phsA.instCVal.ang.f	1:METER:IUW[1]	IAUWFMC
MET	METUWMMXU8	A1.phsB.instCVal.mag.f	1:METER:IUW[2]	IBUWFAC
MET	METUWMMXU8	A1.phsB.instCVal.ang.f	1:METER:IUW[3]	IBUWFMC
MET	METUWMMXU8	A1.phsC.instCVal.mag.f	1:METER:IUW[4]	ICUWFAC
MET	METUWMMXU8	A1.phsC.instCVal.ang.f	1:METER:IUW[5]	ICUWFMC
MET	METUWMMXU8	PF.phsA.instMag.f	1:METER:PFUW[0]	DPFAUW
MET	METUWMMXU8	PF.phsB.instMag.f	1:METER:PFUW[1]	DPFBUW
MET	METUWMMXU8	PF.phsC.instMag.f	1:METER:PFUW[2]	DPFCUW
MET	METUWMMXU8	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METUWMMXU8	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METUWMMXU8	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METUWMMXU8	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METUWMMXU8	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METUWMMXU8	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METUWMMXU8	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METUWMMXU8	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METUWMMXU8	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METUWMMXU8	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METUWMMXU8	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METUWMMXU8	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METUWMMXU8	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METUWMMXU8	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METUWMMXU8	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METUWMMXU8	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12   Logical Node and Mapping Differences (Sheet 8 of 11)

LD	SEL-487E-0, -2			SEL-487E-3, -4
	LN	Path	Mapping	Mapping
MET	METUWMMXU8	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METUWMMXU8	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METUWMMXU8	TotPF.instMag.f	1:METER:PFUW[3]	3DPFUW
MET	METUWMMXU8	TotVA.instMag.f	1:METER:SUW[3]	3SUWFC
MET	METUWMMXU8	TotVAr.instMag.f	1:METER:QUW[3]	3QUWFC
MET	METUWMMXU8	TotW.instMag.f	1:METER:PUW[3]	3PUWFC
MET	METUWMMXU8	VA.phsA.instMag.f	1:METER:SUW[0]	SAUWFC
MET	METUWMMXU8	VA.phsB.instMag.f	1:METER:SUW[1]	SBUWFC
MET	METUWMMXU8	VA.phsC.instMag.f	1:METER:SUW[2]	SCUWFC
MET	METUWMMXU8	VAr.phsA.instMag.f	1:METER:QUW[0]	QAUWFC
MET	METUWMMXU8	VAr.phsB.instMag.f	1:METER:QUW[1]	QBUWFC
MET	METUWMMXU8	VAr.phsC.instMag.f	1:METER:QUW[2]	QCUWFC
MET	METUWMMXU8	W.phsA.instMag.f	1:METER:PUW[0]	PAUWFC
MET	METUWMMXU8	W.phsB.instMag.f	1:METER:PUW[1]	PBUWFC
MET	METUWMMXU8	W.phsC.instMag.f	1:METER:PUW[2]	PCUWFC
MET	METWMMXU4	A1.phsA.instCVal.mag.f	1:METER:IW[0]	IAWFAC
MET	METWMMXU4	A1.phsA.instCVal.ang.f	1:METER:IW[1]	IAWFMC
MET	METWMMXU4	A1.phsB.instCVal.mag.f	1:METER:IW[2]	IBWFAC
MET	METWMMXU4	A1.phsB.instCVal.ang.f	1:METER:IW[3]	IBWFMC
MET	METWMMXU4	A1.phsC.instCVal.mag.f	1:METER:IW[4]	ICWFAC
MET	METWMMXU4	A1.phsC.instCVal.ang.f	1:METER:IW[5]	ICWFMC
MET	METWMMXU4	PF.phsA.instMag.f	1:METER:PFW[0]	DPFAW
MET	METWMMXU4	PF.phsB.instMag.f	1:METER:PFW[1]	DPFBW
MET	METWMMXU4	PF.phsC.instMag.f	1:METER:PFW[2]	DPFCW
MET	METWMMXU4	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METWMMXU4	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METWMMXU4	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METWMMXU4	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METWMMXU4	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METWMMXU4	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METWMMXU4	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METWMMXU4	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METWMMXU4	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METWMMXU4	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METWMMXU4	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METWMMXU4	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METWMMXU4	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METWMMXU4	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METWMMXU4	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METWMMXU4	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12 Logical Node and Mapping Differences (Sheet 9 of 11)

| LD | SEL-487E-0, -2 | | | SEL-487E-3, -4 |
	LN	Path	Mapping	Mapping
MET	METWMMXU4	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METWMMXU4	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METWMMXU4	TotPF.instMag.f	1:METER:PFW[3]	3DPFW
MET	METWMMXU4	TotVA.instMag.f	1:METER:SW[3]	3SWFC
MET	METWMMXU4	TotVAr.instMag.f	1:METER:QW[3]	3QWFC
MET	METWMMXU4	TotW.instMag.f	1:METER:PW[3]	3PWFC
MET	METWMMXU4	VA.phsA.instMag.f	1:METER:SW[0]	SAWFC
MET	METWMMXU4	VA.phsB.instMag.f	1:METER:SW[1]	SBWFC
MET	METWMMXU4	VA.phsC.instMag.f	1:METER:SW[2]	SCWFC
MET	METWMMXU4	VAr.phsA.instMag.f	1:METER:QW[0]	QAWFC
MET	METWMMXU4	VAr.phsB.instMag.f	1:METER:QW[1]	QBWFC
MET	METWMMXU4	VAr.phsC.instMag.f	1:METER:QW[2]	QCWFC
MET	METWMMXU4	W.phsA.instMag.f	1:METER:PW[0]	PAWFC
MET	METWMMXU4	W.phsB.instMag.f	1:METER:PW[1]	PBWFC
MET	METWMMXU4	W.phsC.instMag.f	1:METER:PW[2]	PCWFC
MET	METWXMMXU9	A1.phsA.instCVal.mag.f	1:METER:IWX[0]	IAWXFAC
MET	METWXMMXU9	A1.phsA.instCVal.ang.f	1:METER:IWX[1]	IAWXFMC
MET	METWXMMXU9	A1.phsB.instCVal.mag.f	1:METER:IWX[2]	IBWXFAC
MET	METWXMMXU9	A1.phsB.instCVal.ang.f	1:METER:IWX[3]	IBWXFMC
MET	METWXMMXU9	A1.phsC.instCVal.mag.f	1:METER:IWX[4]	ICWXFAC
MET	METWXMMXU9	A1.phsC.instCVal.ang.f	1:METER:IWX[5]	ICWXFMC
MET	METWXMMXU9	PF.phsA.instMag.f	1:METER:PFWX[0]	DPFAWX
MET	METWXMMXU9	PF.phsB.instMag.f	1:METER:PFWX[1]	DPFBWX
MET	METWXMMXU9	PF.phsC.instMag.f	1:METER:PFWX[2]	DPFCWX
MET	METWXMMXU9	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METWXMMXU9	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METWXMMXU9	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METWXMMXU9	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METWXMMXU9	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METWXMMXU9	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METWXMMXU9	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METWXMMXU9	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METWXMMXU9	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METWXMMXU9	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METWXMMXU9	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METWXMMXU9	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METWXMMXU9	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METWXMMXU9	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METWXMMXU9	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METWXMMXU9	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12   Logical Node and Mapping Differences (Sheet 10 of 11)

LD	SEL-487E-0, -2			SEL-487E-3, -4
	LN	Path	Mapping	Mapping
MET	METWXMMXU9	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METWXMMXU9	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METWXMMXU9	TotPF.instMag.f	1:METER:PFWX[3]	3DPFWX
MET	METWXMMXU9	TotVA.instMag.f	1:METER:SWX[3]	3SWXFC
MET	METWXMMXU9	TotVAr.instMag.f	1:METER:QWX[3]	3QWXFC
MET	METWXMMXU9	TotW.instMag.f	1:METER:PWX[3]	3PWXFC
MET	METWXMMXU9	VA.phsA.instMag.f	1:METER:SWX[0]	SAWXFC
MET	METWXMMXU9	VA.phsB.instMag.f	1:METER:SWX[1]	SBWXFC
MET	METWXMMXU9	VA.phsC.instMag.f	1:METER:SWX[2]	SCWXFC
MET	METWXMMXU9	VAr.phsA.instMag.f	1:METER:QWX[0]	QAWXFC
MET	METWXMMXU9	VAr.phsB.instMag.f	1:METER:QWX[1]	QBWXFC
MET	METWXMMXU9	VAr.phsC.instMag.f	1:METER:QWX[2]	QCWXFC
MET	METWXMMXU9	W.phsA.instMag.f	1:METER:PWX[0]	PAWXFC
MET	METWXMMXU9	W.phsB.instMag.f	1:METER:PWX[1]	PBWXFC
MET	METWXMMXU9	W.phsC.instMag.f	1:METER:PWX[2]	PCWXFC
MET	METXMMXU5	A1.phsA.instCVal.mag.f	1:METER:IX[0]	IAXFAC
MET	METXMMXU5	A1.phsA.instCVal.ang.f	1:METER:IX[1]	IAXFMC
MET	METXMMXU5	A1.phsB.instCVal.mag.f	1:METER:IX[2]	IBXFAC
MET	METXMMXU5	A1.phsB.instCVal.ang.f	1:METER:IX[3]	IBXFMC
MET	METXMMXU5	A1.phsC.instCVal.mag.f	1:METER:IX[4]	ICXFAC
MET	METXMMXU5	A1.phsC.instCVal.ang.f	1:METER:IX[5]	ICXFMC
MET	METXMMXU5	PF.phsA.instMag.f	1:METER:PFX[0]	DPFAX
MET	METXMMXU5	PF.phsB.instMag.f	1:METER:PFX[1]	DPFBX
MET	METXMMXU5	PF.phsC.instMag.f	1:METER:PFX[2]	DPFCX
MET	METXMMXU5	PhV1.phsA.instCVal.mag.f	1:METER:VV[0]	VAVFAC
MET	METXMMXU5	PhV1.phsA.instCVal.ang.f	1:METER:VV[1]	VAVFMC
MET	METXMMXU5	PhV1.phsB.instCVal.mag.f	1:METER:VV[2]	VBVFAC
MET	METXMMXU5	PhV1.phsB.instCVal.ang.f	1:METER:VV[3]	VBVFMC
MET	METXMMXU5	PhV1.phsC.instCVal.mag.f	1:METER:VV[4]	VCVFAC
MET	METXMMXU5	PhV1.phsC.instCVal.ang.f	1:METER:VV[5]	VCVFMC
MET	METXMMXU5	PhV2.phsA.instCVal.mag.f	1:METER:VZ[0]	VAZFAC
MET	METXMMXU5	PhV2.phsA.instCVal.ang.f	1:METER:VZ[1]	VAZFMC
MET	METXMMXU5	PhV2.phsB.instCVal.mag.f	1:METER:VZ[2]	VBZFAC
MET	METXMMXU5	PhV2.phsB.instCVal.ang.f	1:METER:VZ[3]	VBZFMC
MET	METXMMXU5	PhV2.phsC.instCVal.mag.f	1:METER:VZ[4]	VCZFAC
MET	METXMMXU5	PhV2.phsC.instCVal.ang.f	1:METER:VZ[5]	VCZFMC
MET	METXMMXU5	PPV1.phsAB.instMag.f	1:METER:VV_LL[0]	VABVFMC
MET	METXMMXU5	PPV1.phsBC.instMag.f	1:METER:VV_LL[2]	VBCVFMC
MET	METXMMXU5	PPV1.phsCA.instMag.f	1:METER:VV_LL[4]	VCAVFMC
MET	METXMMXU5	PPV2.phsAB.instMag.f	1:METER:VZ_LL[0]	VABZFMC

Table B.12   Logical Node and Mapping Differences (Sheet 11 of 11)

| LD | SEL-487E-0, -2 | | SEL-487E-3, -4 | |
	LN	Path	Mapping	Mapping
MET	METXMMXU5	PPV2.phsBC.instMag.f	1:METER:VZ_LL[2]	VBCZFMC
MET	METXMMXU5	PPV2.phsCA.instMag.f	1:METER:VZ_LL[4]	VCAZFMC
MET	METXMMXU5	TotPF.instMag.f	1:METER:PFX[3]	3DPFX
MET	METXMMXU5	TotVA.instMag.f	1:METER:SX[3]	3SXFC
MET	METXMMXU5	TotVAr.instMag.f	1:METER:QX[3]	3QXFC
MET	METXMMXU5	TotW.instMag.f	1:METER:PX[3]	3PXFC
MET	METXMMXU5	VA.phsA.instMag.f	1:METER:SX[0]	SAXFC
MET	METXMMXU5	VA.phsB.instMag.f	1:METER:SX[1]	SBXFC
MET	METXMMXU5	VA.phsC.instMag.f	1:METER:SX[2]	SCXFC
MET	METXMMXU5	VAr.phsA.instMag.f	1:METER:QX[0]	QAXFC
MET	METXMMXU5	VAr.phsB.instMag.f	1:METER:QX[1]	QBXFC
MET	METXMMXU5	VAr.phsC.instMag.f	1:METER:QX[2]	QCXFC
MET	METXMMXU5	W.phsA.instMag.f	1:METER:PX[0]	PAXFC
MET	METXMMXU5	W.phsB.instMag.f	1:METER:PX[1]	PBXFC
MET	METXMMXU5	W.phsC.instMag.f	1:METER:PX[2]	PCXFC
MET	METYMMXN1	Amp01.instMag.f	1:METER:IY[0]	IY1FMC
MET	METYMMXN1	Amp02.instMag.f	1:METER:IY[2]	IY2FMC
MET	METYMMXN1	Amp03.instMag.f	1:METER:IY[4]	IY3FMC

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SEL-487E-3, -4 Relay Command Summary

Command[a, b]	Description
2ACCESS	Go to Access Level 2 (full control)
89CLOSE k	Close Disconnect k (Isolator k) ($k = 1–20$)
89OPEN k	Open Disconnect k (Isolator k) ($k = 1–20$)
AACCESS	Go to Access Level A (automation configuration)
ACCESS	Go to Access Level 1 (monitor relay)
BACCESS	Go to Access Level B (monitor and control circuit breakers)
BNAME	ASCII names of Fast Meter status bits
BREAKER n	Display circuit breaker reports; preload/reset monitor data (n = S, T, U, W, X)
CASCII	Generate the Compressed ASCII response configuration message
CBREAKER	Display Compressed ASCII breaker status report
CEVENT	Display Compressed ASCII event report
CFG CTNOM i j	For TiDL relays, configure the nominal CT input value i to 1, 2, 3, or 4 and j to 1, 2, 3, 4, 5, 6, 7, or 8
CFG NFREQ f	For TiDL relays, set the nominal frequency, f (50 or 60)
CHISTORY	Display Compressed ASCII history report
CLOSE n	Close Circuit Breaker n (n = S, T, U, W, X)
COM c	Display Channel c MIRRORED BITS communications data (c = A, B, or M [either enabled single channel])
COM PTP	Display a report on PTP data sets and statistics
COM RTC	Display statistics for synchrophasor client channels
CONTROL nn	Set, clear, or pulse Remote Bit nn ($nn = 01–32$)
COPY m n	Copy settings between instances in the same class (m and n are instance numbers; e.g., $m = 1$ is Group 1, $n = 2$ is Group 2, etc.)
CPR	Display Compressed ASCII signal profiling report
CSER	Display Compressed ASCII sequential events report
CSTATUS	Display Compressed ASCII relay status report
CSUMMARY	Display Compressed ASCII summary event report
DATE	Display and set the relay date
DNAME X	ASCII names of all relay digital points reported via Fast Meter
ETHERNET	Displays Ethernet port (Port 5) configuration and status
EVENT	Display and acknowledge event reports
EXIT	Reduce access level to Access Level 0 (exit relay control)
FILE	Transfer files between the relay and external software
GOOSE	Displays transmit and receive GOOSE messaging information
GROUP	Display the active group number or change the active group
HELP	List and describe available commands at each access level
HISTORY	View event summaries/history; clear event summary data
ID	Display the firmware ID, user ID, device code, part number, and configuration information
LOOPBACK	Connect MIRRORED BITS data from transmit to receive on the same port
MAC	Display MAC Addresses

Command[a, b]	Description
MAP 1	View the relay database organization
METER	Display metering data and internal relay operating variables
OACCESS	Go to Access Level O (output configuration)
OPEN *n*	Open Circuit Breaker *n* (*n* = S, T, U, W, X)
PACCESS	Go to Access Level P (protection configuration)
PASSWORD *n*	Change relay password for Access Level *n*
PING *addr*	Sends an ICMP echo request message to the provided IP address *addr* to confirm connectivity
PORT *p*	Connect to remote devices via Mirrored Bits virtual terminal (for Port *p*; where *p* = 1–3, F)
PROFILE	Display signal profile records
PULSE OUT*nnn*	Pulse a relay control output (OUT*nnn* is a control output)
QUIT	Reduce access level to Access Level 0 (exit relay control)
RTC	Display configuration of received remote synchrophasors
SER	View Sequential Events Recorder (SER) report
SET	Set or modify relay settings
SHOW	Display relay settings
SNS	Display Sequential Events Recorder settings name strings (Fast SER)
STATUS	Display or clear relay status and SELOGIC control equation errors
SUMMARY	Display a summary event report
TARGET	Display relay elements for a row in the Relay Word bit table
TEST DB	Test interfaces to a virtual device database used by Fast Message protocol
TEST DB2	Test all communications protocols except Fast Message
TEST FM	Display or place values in Fast Meter interface
TFE	Display through-fault events
THE	Display transformer thermal information
TIME	Display and set the relay time clock
TRIGGER	Initiate a data capture and record an event report
VERSION	Display the relay hardware and software configuration
VIEW 1	View data from the Fast Message database

[a] See *Section 9: ASCII Command Reference* for more information.

[b] For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.

SEL-487E-3, -4 Relay Command Summary

Command[a, b]	Description
2ACCESS	Go to Access Level 2 (full control)
89CLOSE *k*	Close Disconnect *k* (Isolator *k*) (*k* = 1–20)
89OPEN *k*	Open Disconnect *k* (Isolator *k*) (*k* = 1–20)
AACCESS	Go to Access Level A (automation configuration)
ACCESS	Go to Access Level 1 (monitor relay)
BACCESS	Go to Access Level B (monitor and control circuit breakers)
BNAME	ASCII names of Fast Meter status bits
BREAKER *n*	Display circuit breaker reports; preload/reset monitor data (*n* = S, T, U, W, X)
CASCII	Generate the Compressed ASCII response configuration message
CBREAKER	Display Compressed ASCII breaker status report
CEVENT	Display Compressed ASCII event report
CFG CTNOM *i j*	For TiDL relays, configure the nominal CT input value *i* to 1, 2, 3, or 4 and *j* to 1, 2, 3, 4, 5, 6, 7, or 8
CFG NFREQ *f*	For TiDL relays, set the nominal frequency, *f* (50 or 60)
CHISTORY	Display Compressed ASCII history report
CLOSE *n*	Close Circuit Breaker *n* (*n* = S, T, U, W, X)
COM *c*	Display Channel *c* MIRRORED BITS communications data (*c* = A, B, or M [either enabled single channel])
COM PTP	Display a report on PTP data sets and statistics
COM RTC	Display statistics for synchrophasor client channels
CONTROL *nn*	Set, clear, or pulse Remote Bit *nn* (*nn* = 01–32)
COPY *m n*	Copy settings between instances in the same class (*m* and *n* are instance numbers; e.g., *m* = 1 is Group 1, *n* = 2 is Group 2, etc.)
CPR	Display Compressed ASCII signal profiling report
CSER	Display Compressed ASCII sequential events report
CSTATUS	Display Compressed ASCII relay status report
CSUMMARY	Display Compressed ASCII summary event report
DATE	Display and set the relay date
DNAME X	ASCII names of all relay digital points reported via Fast Meter
ETHERNET	Displays Ethernet port (Port 5) configuration and status
EVENT	Display and acknowledge event reports
EXIT	Reduce access level to Access Level 0 (exit relay control)
FILE	Transfer files between the relay and external software
GOOSE	Displays transmit and receive GOOSE messaging information
GROUP	Display the active group number or change the active group
HELP	List and describe available commands at each access level
HISTORY	View event summaries/history; clear event summary data
ID	Display the firmware ID, user ID, device code, part number, and configuration information
LOOPBACK	Connect MIRRORED BITS data from transmit to receive on the same port
MAC	Display MAC Addresses

Command[a, b]	Description
MAP 1	View the relay database organization
METER	Display metering data and internal relay operating variables
OACCESS	Go to Access Level O (output configuration)
OPEN *n*	Open Circuit Breaker *n* (*n* = S, T, U, W, X)
PACCESS	Go to Access Level P (protection configuration)
PASSWORD *n*	Change relay password for Access Level *n*
PING *addr*	Sends an ICMP echo request message to the provided IP address *addr* to confirm connectivity
PORT *p*	Connect to remote devices via MIRRORED BITS virtual terminal (for Port *p*; where *p* = 1–3, F)
PROFILE	Display signal profile records
PULSE OUT*nnn*	Pulse a relay control output (OUT*nnn* is a control output)
QUIT	Reduce access level to Access Level 0 (exit relay control)
RTC	Display configuration of received remote synchrophasors
SER	View Sequential Events Recorder (SER) report
SET	Set or modify relay settings
SHOW	Display relay settings
SNS	Display Sequential Events Recorder settings name strings (Fast SER)
STATUS	Display or clear relay status and SELOGIC control equation errors
SUMMARY	Display a summary event report
TARGET	Display relay elements for a row in the Relay Word bit table
TEST DB	Test interfaces to a virtual device database used by Fast Message protocol
TEST DB2	Test all communications protocols except Fast Message
TEST FM	Display or place values in Fast Meter interface
TFE	Display through-fault events
THE	Display transformer thermal information
TIME	Display and set the relay time clock
TRIGGER	Initiate a data capture and record an event report
VERSION	Display the relay hardware and software configuration
VIEW 1	View data from the Fast Message database

[a] See *Section 9: ASCII Command Reference* for more information.

[b] For help on a specific command, type **HELP [command] <Enter>** at an ASCII terminal communicating with the relay.