Transformer Event Analysis

Exercise 2: SEL-387 Trips on Energization

Customer Email

We had an issue at one of our stations the other day and had some damage to a transformer's H3 bushing. We replaced the bushing and were closing up the high-side circuit switcher (Winding 1) when the transformer relay operated. The low-side secondary breaker (Winding 2) was open. We are trying to figure out if this was a valid operation and to help direct the testing crew's focus (more than the obvious answer of the H3 bushing). So far, we have tested the CTs and verified that they are correct to each relay. This unit had been energized with these settings before and did not trip.

Available Resources

- Event reports (Exercise 2 Filtered.CEV, Exercise 2 Differential.CEV, and Exercise 2 RAW.CEV)
- SEL-5601-2 SYNCHROWAVE® Event Software
- SEL-387 instruction manual
- "Using SYNCHROWAVE Event to Model Transformer Differential With Harmonic Restraint and Blocking" (AG2020-28) application guide
- "Considerations for Using Harmonic Blocking and Harmonic Restraint Techniques on Transformer Differential Relays" technical paper

Questions and Answers

1. Open Exercise 2 Filtered.CEV. Is this a fault?

It is hard to tell what type of fault this is, or if it is even a fault, based on the filtered event. The relay filters and removes the harmonics and dc offset, so you are only able to see the 60 Hz signal. Therefore, whenever you have an event while energizing a transformer and it is possibly due to inrush, it is important to get both the raw and filtered events.

The currents shown in Figure 1 are in secondary amps. Based on the CTR of 120 for Winding 1, this is in the order of about 300 A primary, which is a fairly low value for typical fault current.

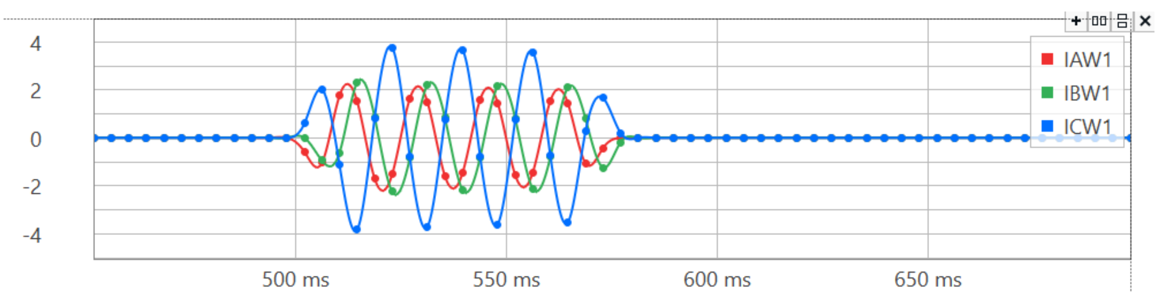

Figure 1 Waveforms from Filtered Event Report

2. Open Exercise 2 RAW.CEV. Is this a fault?

The raw event in Figure 2 shows that this event is not a fault; instead, it is classic inrush. You can see the inrush waveform in the raw event, but not in the filtered event. Whenever you see peaks that are all positive or all negative without zero crossings, we can conclude that it is inrush. If it were a fault, each phase current would be crossing the zero axis.

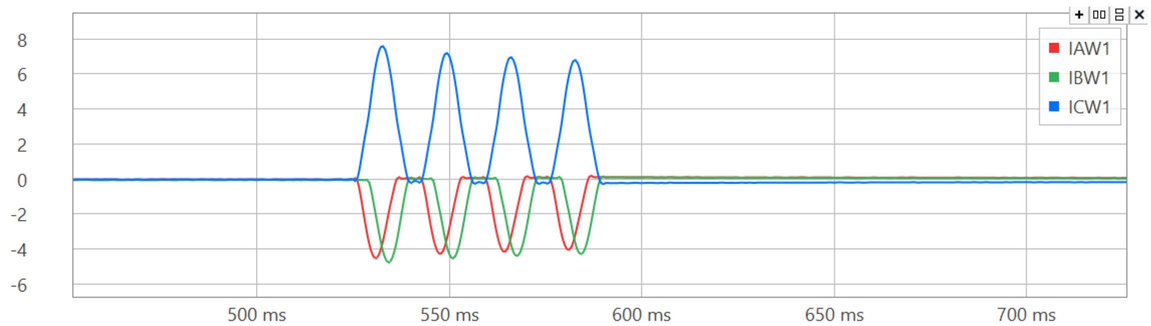

Figure 2 Waveforms from Raw Event Report

3. Should the relay be tripping on this condition, and what features in the relay keep the 87 element secure during inrush?

The relay should not be tripping for inrush. SEL relays use harmonic restraint and harmonic blocking algorithms to prevent tripping on inrush conditions.

4. Refer to Table 2 in AG2020-28. Which algorithm is this relay using to prevent tripping on inrush?

Table 1 (Table 2 in AG2020-28) shows that the algorithm used by the relay can be determined by looking at the HRSTR and IHBL settings in the relay.

Table 1 Determining the Harmonic Restraint/Harmonic Blocking Algorithm Used in the SEL-387

Harmonic Restraint[a] (HRSTR)	Independent Harmonic Blocking (IHBL)	Algorithm Used by Relay
Grayed out/missing or N	N	Common Harmonic Blocking
Grayed out/missing or N	Y	Independent Harmonic Blocking
Y	Grayed out/missing	Harmonic Restraint

[a] Harmonic restraint is unavailable in the SEL-387-0.

The settings in the relay are shown in Figure 3.

TAP1 = 1.39	TAP2 = 4.18		
O87P = 0.40	SLP1 = 30	SLP2 = OFF	
U87P = 8.0	PCT2 = 15	PCT4 = OFF	PCT5 = OFF
TH5P = OFF	DCRB = N	HRSTR = Y	

Figure 3 Relay Settings

Notice that HRSTR = Y, and the IHBL setting is missing. Using the info from Table 1, we can tell that the relay is using the harmonic restraint algorithm.

5. How does the harmonic restraint algorithm work?

See AG2020-28 for an explanation of harmonic restraint and how the operate current is compared to the HR threshold.

6. Extract the contents of the AG2020-28.zip file into the following directory on your computer. Note that the AppData folder is hidden, so you must turn on the Show Hidden Files option in Microsoft Windows to see it.

C:\Users\[username]\AppData\Roaming\SEL\SEL SynchroWAVe Event\Calculations

Open the Exercise 2 Differential.CEV event report. Select the Import Calculations icon at the bottom right of the Custom Calculations window. Select the AG2020-28 SEL-387.txt file and select Open. The first line of the calculations (the import line) will flag red. Why is this, and how can you correct it? Hint: See the note at the bottom of Page 7 of AG2020-28.

The note at the bottom of AG2020-28 Page 7 explains that an error will be flagged if the relay is set to specifically use a single slope (SLP2 = OFF), causing IRS1 to be missing from the settings. You can see that is the case for this event. Solve this by opening the **AG2020-28 SEL-387.txt** file in Notepad and adding a hashtag symbol (#) in front of the first instance of the IRS1 equation to comment it out. Remove the hashtag that exists in front of the second instance of the IRS1 equation and save your changes.

7. Use Table 3 in AG2020-28 to identify which operating quantities and thresholds must be compared to analyze the operation of the harmonic restraint algorithm. Plot these quantities in SYNCHROWAVE Event. Is the assertion of the associated Relay Word bits for the harmonic restraint element as expected?

Table 2 Determining the Harmonic Restraint/Harmonic Blocking Algorithm Used in the SEL-387

Algorithm	Operating Quantities	Compare to Threshold	Result	Relay Word Bits
Harmonic Restraint	IOP1 IOP2 IOP3	HR_thresh_1 HR_thresh_2 HR_thresh_3	Individual 87R*p* bits assert if IOP*p* exceeds HR_thresh_*p*. Any of these will assert 87R.	87R1[a] 87R2[a] 87R3[a]

[a] When comparing signals to thresholds to validate relay operation, note that the SEL-387 has a built-in security delay of 1.25 cycles before the 87R*p* Relay Word bits are allowed to assert.

[b] For any of the harmonic blocking bits to assert, IOP*p* must also be greater than IOP_min. This ensures that the relay does not make decisions on very small current values. In the SEL-387, IOP_min = 0.05 • INOM/2.

Comparing the signals in Table 2 (Table 3 in AG2020-28) for the harmonic restraint algorithm gives us the following plots in Figure 4. You can see that the 87R3 bit asserts 1.25 cycles after IOP3 crosses the HR_THRESH_3 threshold. This behavior is explained in the subnotes of Table 2 (Table 3 in AG2020-28).

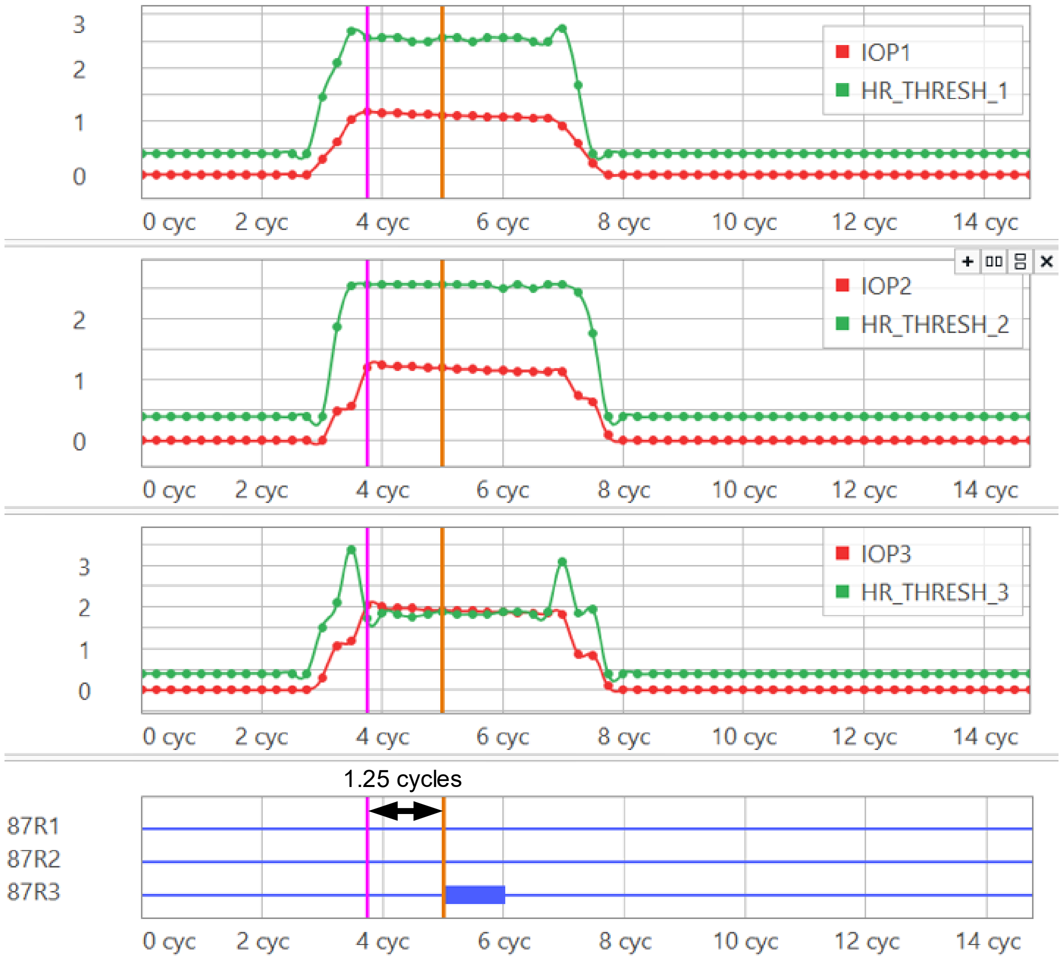

Figure 4 Comparing Operating Quantities to the Harmonic Restraint Thresholds

8. Could lowering the PCT2 setting have helped keep the relay secure? What value would it have to be lowered to in order to prevent misoperation?

It is easy to see what changing a relay setting might do by simply changing the PCT2_USER setting in the custom calculations window from AUTO to the number that you would like. The AUTO setting uses the number in the relay settings (in this case, it is 15). Lowering this setting to 14 would have kept IOP3 from being higher than HR_THRESH_3 for 1.25 cycles, which would have kept the relay secure. Note that changing these settings just changes the analog plots; it does not change the associated digital Relay Word bits.

9. The relay is not set to use the fourth harmonic content for inrush security (PCT4 = OFF). The SEL-387 instruction manual recommends using both second and fourth harmonic content for security. Would turning on the fourth harmonic help keep the relay secure?

Unfortunately, the SEL-387 relay does not include the fourth harmonic content of the operate current as part of its recorded analog values, so we cannot add it to our equations as easily as second harmonic. The SEL-487E, however, can be programmed to include it.

10. Would using common harmonic blocking instead of harmonic restraint help keep the relay secure in this case? Use AG2020-28 to plot the harmonic blocking calculations to prove this one way or the other.

AG2020-28 shows that the signals to compare for the common harmonic blocking algorithm are as described in Table 3 (Table 3 in AG2020-28).

Table 3 Common Harmonic Blocking

Common Harmonic Blocking	IOP1 IOP2 IOP3	S_thresh_1 S_thresh_2 S_thresh_3	Individual 87R*p* bits assert if IOP*p* exceeds S_thresh_*p*. Any of these can assert 87R.	87R1[a] 87R2[a] 87R3[a]
	2H_1 2H_2 2H_3	PCT2 PCT2 PCT2	Individual 87BL*p* bits assert if 2H_*p* exceeds PCT2. If any of these bits assert, they will block 87R from asserting.	87BL1[b] 87BL2[b] 87BL3[b]

[a] When comparing signals to thresholds to validate relay operation, note that the SEL-387 has a built-in security delay of 1.25 cycles before the 87R*p* Relay Word bits are allowed to assert.

[b] For any of the harmonic blocking bits to assert, IOP*p* must also be greater than IOP_min. This ensures that the relay does not make decisions on very small current values. In the SEL-387, IOP_min = 0.05 • INOM/2.

The plots in Figure 5 show that common harmonic blocking would have prevented this operation. All three IOP quantities are above the S_thresh values, meaning that any of the 87R bits may have asserted. However, if any of the 2H_p values rise above the PCT2 threshold, 87R will be blocked from asserting. In this case, 2H_1 and 2H_2 are above the PCT2 threshold and would, therefore, keep all three phases of the relay secure.

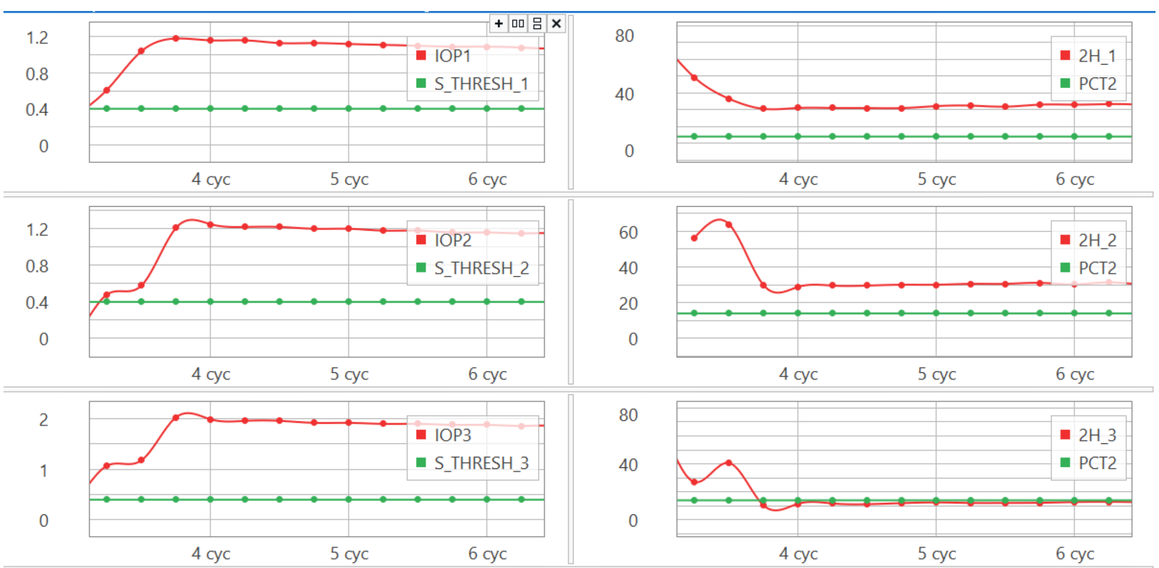

Figure 5 Comparing Operating Quantities to the Harmonic Blocking Thresholds

Harmonic blocking has its downsides. Choosing between harmonic restraint or harmonic blocking is a philosophical decision, and technical papers (such as "Considerations for Using Harmonic Blocking and Harmonic Restraint Techniques on Transformer Differential Relays") describe the pros and cons of each. In newer relays, users do not have to choose between these two algorithms and can enable both harmonic restraint and harmonic blocking to get the best of both methods.

11. Are there any other elements in the relay that could have been turned on to prevent this operation?

Yes, dc ratio blocking is available in this relay, but it is turned off by default. This feature applies to inrush cases when the transformer produces low harmonic content but a high dc offset. This logic detects inrush by looking at the dc offset of the waveform, and it can help block when harmonic content is low (see Figure 6). The customer should consider enabling this feature to add security if this is a reoccurring problem.

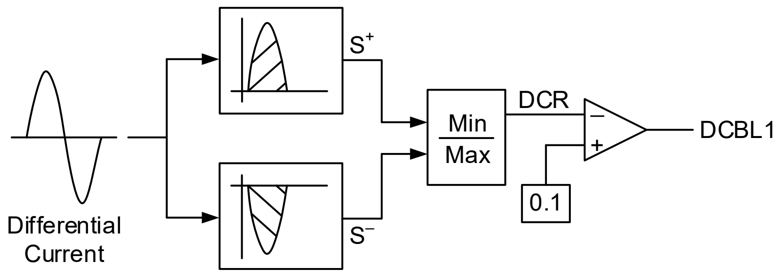

Figure 6 DC Blocking (DCBL1) Logic (All But SEL-387-0)

The new advanced inrush detection algorithms in the SEL-487E are also designed to detect inrush with low second harmonics. These algorithms would have successfully detected and blocked for this inrush condition.

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