A New Digital Distance Element Implementation Using Coincidence Timing

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processing rates now allow implementing and improving principles invented for static relays.

Any comparator in a distance protection element can be shaped by comparing the angle (coincidence) between the operating and polarizing signals. For example, a positive-sequence-polarized mho comparator uses $S_{OP} = I \cdot Z_R - V$ and $S_{POL} = V_1$, where I and V are measured current and voltage, Z_R is reach impedance, and V_1 is positive-sequence voltage. These two signals can be compared in either the frequency domain (phasors) or the time domain (coincidence timing).

This paper presents a new distance element design based on coincidence timing, explains the benefits of using coincidence timing, and shares some key details of digital implementation and improvements that far surpass the dreams of analogue relay designers. Finally, it presents test results for a distance relay implementation that uses the best of both worlds: analogue principles implemented in a microprocessor-based relay.

2 Distance Protection Element Overview

In general, a distance protection element consists of several logical conditions (comparators) joined with an AND gate. For example, a quadrilateral distance element includes a reactance comparator, a right blinder comparator, a left blinder comparator (optional), a directional comparator, and a faulted-loop selection comparator. A mho distance element includes a mho comparator, a faulted-loop selection comparator, and a directional comparator. The mho distance element can be further modified by optionally adding a reactance comparator or a blinder comparator.

The performance of all individual comparators that make up a distance element is important for the overall performance of the element. However, the speed and security of a distance

1 Introduction

When semiconductor components became reliable enough for protective relay applications, relay designers introduced distance relay designs based on filtering and coincidence timing by using analogue circuits with semiconductors. Free of the inherent inertia of electromechanical devices, these distance relays operated very fast. As the industry continued to learn about electromagnetic interference and semiconductor failure modes, microprocessor-based relays disrupted the field with unprecedented flexibility, new functionality, and unparalleled self-monitoring to mitigate failures, increasing both security and dependability. Manufacturers and users moved on to the digital technology, and static relays became a "lost generation."

The early digital relays could apply only very limited sampling and processing rates. Out of necessity, these relays abandoned the time-domain approach of static relays and started a new path for implementing protection functions. This new path focused on "slowing down" the flow of information so that early microprocessors could keep up. These relays applied heavy low-pass filtering in order to be able to sample just several times a cycle. They "compressed samples into phasors" at the front end of the processing chain for the key benefit of processing phasors at low rates. Even today, many microprocessor-based relays process protection logic just a few (four or eight) times a cycle.

Early microprocessor-based relays did not abandon time-domain coincidence timing because of its substandard performance, but rather because their limited processing power did not allow them to use analogue methods. Over the first three decades of microprocessor-based protective relaying, digital protection and phasor-based operation became synonymous. It is time to revisit this notion. New digital relays have enormous processing capabilities. High sampling and

element is mostly affected by what we refer to in this paper as "reach-sensitive comparators." Reach-sensitive comparators are responsible for distinguishing between faults located short of the reach point (element operates) and faults located beyond the reach point (element restrains). All other comparators assert for a fault short of and beyond the reach point, and it is only the reach-sensitive comparator that decides if the element operates or restrains.

These reach-sensitive comparators are the mho comparator in the mho distance element and the reactance comparator in the quadrilateral distance element. To some degree, the blinder comparator (resistive reach comparator) in the quadrilateral distance element is also a reach-sensitive comparator.

Historically, a distance comparator is defined by two signals: an operating signal (S_{OP}) and a polarizing signal (S_{POL}). In a steady state (fault or no-fault state), the two signals are sine waves. A comparator asserts its output if the S_{OP} and S_{POL} signals are approximately in-phase, and it deasserts if the S_{OP} and S_{POL} signals are approximately out-of-phase. Typically, the operating threshold is drawn at 90 degrees. If the angle between the S_{OP} and S_{POL} is between –90 and 90 degrees, then the comparator asserts. If the angle is outside this interval (–90 to 90 degrees), the comparator deasserts. For example, a mho comparator uses the following signals:

$$S_{OP} = I \cdot Z_R - V \qquad (1a)$$

$$S_{POL} = V_{POL} \qquad (1b)$$

where:

I	is the relay current.
V	is the relay voltage.
Z_R	is the reach impedance (setting).
$I \cdot Z_R$	represents a voltage drop across the intended reach impedance Z_R from the relay current I.
V_{POL}	is the polarizing signal, such as the relay voltage (self-polarized mho), healthy phase voltage (cross-phase-polarized mho), positive-sequence voltage (positive-sequence-polarized mho), or a pre-fault voltage (memory-polarized mho).

The V and I terms are adequately selected from the three-phase quantities (V_A, V_B, V_C; and I_A, I_B, I_C) based on the fault type. Typically, six instances of the comparator are implemented to monitor all six protection loops for the AG, BG, CG, AB or ABG, BC or BCG, and CA or CAG faults. For any given fault type, the distance element permits only some loops to operate. A faulted-loop selection comparator is responsible for deciding which loops are permitted to operate.

The S_{OP} and S_{POL} signals can be developed in time domain or frequency domain, as follows:

- *Time-domain* implementation uses the $R \cdot i + L \cdot di/dt$ term to replicate an instantaneous voltage drop across the reach resistance and inductance, subtracts it from the instantaneous voltage, and obtains an instantaneous operating signal (S_{OP_INST}).
- *Frequency-domain* implementation uses the $I \cdot Z$ term to calculate a voltage drop phasor across the reach impedance, subtracts it from the voltage phasor, and

obtains the operating signal phasor ($\overline{S}_{OP}$). Alternatively, a frequency-domain implementation can pass the instantaneous operating signal (S_{OP_INST}) through a phasor estimator to obtain the $\overline{S}_{OP}$ signal.

The reactance comparator uses these signals:

$$S_{OP} = I \cdot Z_R - V \qquad (2a)$$

$$S_{POL} = j \cdot I_{POL} \qquad (2b)$$

where j relates to a phase shift by 90 degrees in the frequency domain or the di/dt operation in the time domain.

We can obtain various reactance comparators by using different polarizing currents. For example, I_{POL} can be the loop current I (self-polarized reactance), the negative-sequence current I_2 (negative-sequence polarized reactance), or the zero-sequence current I_0 (zero-sequence polarized reactance). Note that the mho and reactance comparators only differ by the polarizing signal they use, and the operating signal is identical.

Various relay technologies check the angle between the S_{OP} and S_{POL} signals differently:

- *Electromechanical relays* are designed to develop a torque from the S_{OP_INST} and S_{POL_INST} signals to move the relay rotor in the operating direction if the torque is positive (i.e., the angle between the two signals is between –90 and 90 degrees) and close a contact.
- *Microprocessor-based relays* using phasors can follow one of the following three approaches (see Fig. 1):

  a) Calculate the angle directly and check it against the 90-degree threshold.

  b) Calculate the torque and check if it is positive $Re[S_{OP} \cdot conj(S_{POL})] > 0$.

  c) Calculate the fault distance m-value and check if it is lower than the reach impedance setting.
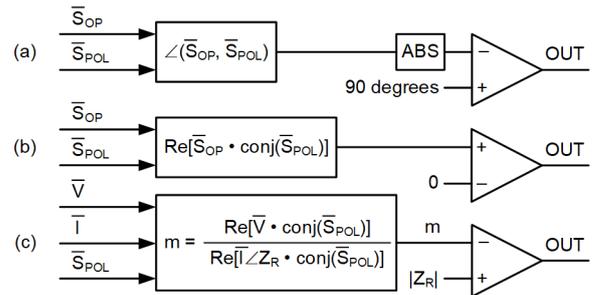
Fig. 1.   Implementations of a distance comparator in phasor-based microprocessor-based relays.

All these phasor-based implementation methods are mathematically identical. They only differ in terms of required operations and computational burden. For example, the m-value method is computationally very efficient when implementing multiple zones with identical settings, except the reach setting.

Static relays use coincidence timers to check how long the S_{OP_INST} and S_{POL_INST} signals are of the same polarity. After low-pass filtering, the S_{OP_INST} and S_{POL_INST} signals are sine

waves. If they are perfectly in-phase, they coincide (have the same polarity) for a half cycle in each half cycle. If they are 90 degrees apart, they coincide for a quarter cycle in each half cycle. If they are perfectly out-of-phase, they do not coincide at all. Static relays use rectifier circuits to detect the instantaneous polarity (sign) of the S_{OP_INST} and S_{POL_INST} signals, a few AND and OR gates to detect if the S_{OP_INST} and S_{POL_INST} signals are the same polarity, and a timer to check if the matching polarity intervals last for longer than a quarter cycle (90-degree coincidence). If so, the static distance comparator asserts (see Fig. 2).
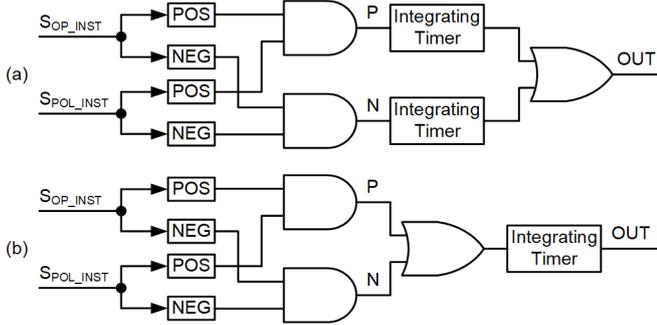
Fig. 2.   Implementations of a distance comparator in static relays: (a) dual-timer method, (b) single-timer method.

The coincidence timing method has several advantages:

- Transients that may be present in the operating and polarizing signals can be used for security. For example, if during the matching polarity period a moment of opposite polarity occurs, the timer can reset or integrate down, providing extra security.
- The comparator operation is fast: it takes only a quarter cycle to detect the 90-degree coincidence.
- An independently designed and optimized filtering scheme can be applied to voltages and currents before passing these signals for coincidence timing.
- Some transients that occur in voltages and currents have a chance to mutually cancel in the $S_{OP} = IZ - V$ signal. The scheme does not need to excessively suppress transients in voltages and currents separately, but it can focus on transients in the operating signal.
- The $S_{OP} = IZ - V$ signal can be inspected for level: large signals indicate faults away from the reach point (internal or external); small signals indicate faults close to the reach point (internal or external). Adaptive levels of security can be applied based on the S_{OP} magnitude.

The coincidence timing method can also bring additional benefits to speed and security. Fig. 3 illustrates operation of three different versions of an integrating timer. The design of Fig. 3a is biased toward security: any momentary dropout of the input restarts the timer. Fig. 3b is biased toward dependability: a momentary dropout results in holding the integrator (for a finite time), and when the input picks up again, the integration starts from where it stopped. Fig. 3c is a hybrid solution: when the input deasserts, the integrator does not reset instantaneously but integrates down, away from the operate threshold and toward a complete reset. A modern digital implementation can use any of these solutions or switch dynamically among them, depending on other conditions.
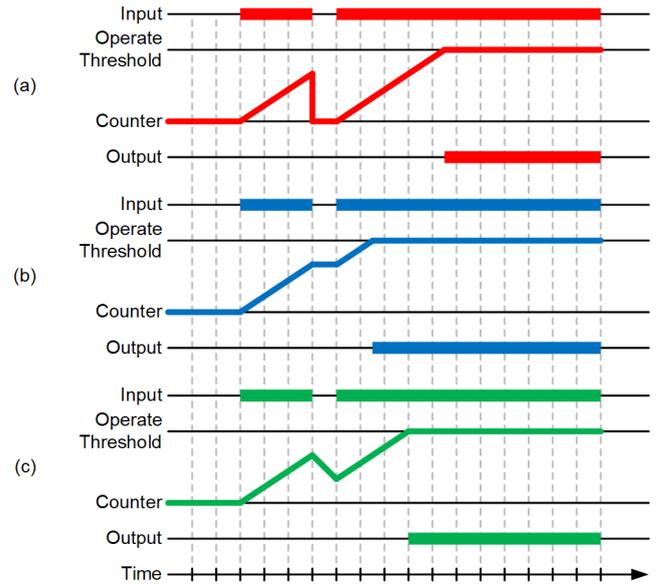
Fig. 3.   Integrating timer: (a) instantaneous reset, (b) hold, and (c) integrate down.

Early microprocessor-based distance relays could not afford fast sampling and processing. They were incapable of emulating the coincidence timing method. Instead, they used phasors. Some relays further distilled phasors into either the angle between the operating and polarizing signals or into the m-value. These methods lose the association with the IZ – V signal and the related benefits listed previously in this section.

3   Signal Processing and Filtering

Our solution derives instantaneous operating and polarizing signals in the time domain. This operation follows the first principle of distance protection for a three-phase power line. The method uses a current derivative to obtain the IZ terms (instantaneous voltage drops across the line replica impedance). This is a classical solution dating back almost a century to the first electromechanical distance relays. References [1] and [2] provide details on the numerical implementation of the line replica circuit.

We low-pass filter the instantaneous operating and polarizing signals with a second-order infinite impulse response (IIR) filter to reject high-frequency signal components that would otherwise violate the RL-line model we used in the numerical line replica circuit. The –20 dB point of this low-pass filter is set at a frequency of several hundred hertz.

Finally, we apply a variable-window finite impulse response (FIR) filter to obtain the direct and quadrature components of the instantaneous operating and polarizing signals. This variable-window filter with dynamic window resizing is a key contributor to the element operating time. Reference [3] describes the filter in detail. To understand this paper, think of this filter as a nonstationary, fast, and accurate phasor estimator, outputting the real (direct component) and imaginary (quadrature component) parts of the input signal.

3

4 Distance Element Design

Our algorithm applies to any comparator comprising a distance element (mho, reactance, blinders, directional, etc.). We describe the algorithm in relation to a general reach-sensitive comparator, such as the mho comparator or the reactance comparator. Fig. 4 shows the overall block diagram of the comparator logic, while the following sections explain the key elements comprising the comparator logic.
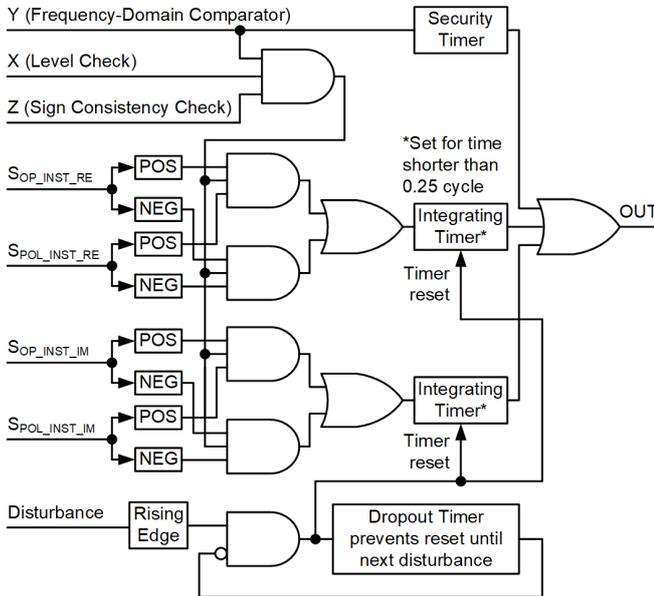
Fig. 4.   New distance comparator logic diagram.

4.1   Using Direct and Quadrature Components for Speed

For speed, our design applies coincidence timing to both the direct (real) and quadrature (imaginary) parts of the operating and polarizing signals. Depending on the point on wave, i.e., the moment of the fault as it relates to the peaks and zero-crossings of the pre-fault voltage, either the real part of a phasor or the imaginary part of a phasor develops faster. Typically, when the real part is slow, the imaginary part is faster, and vice versa. This beneficial relationship is caused by the fact that the real part is related to the signal value and the imaginary part is related to the signal derivative.

An identical coincidence timing logic, depicted in Fig. 2b, is applied separately to the real and imaginary parts of the operating and polarizing signals, with the outputs combined using OR gates, as Fig. 4 shows. Our solution applies the coincidence timer with the integrate-down option (see Fig. 3c).

4.2   Ensuring the Accuracy of Digital Coincidence Timing

Microprocessor-based relays, such as [2], apply high sampling rates and have enough processing power to implement time-domain comparators. However, unless the sampling and processing rates are very high, the time-domain comparator has limited steady-state accuracy. Assume a sampling rate of 2 kHz (a sampling period of 0.5 ms). In a 60 Hz system with a temporal resolution of 0.5 ms, the coincidence timer would have a resolution of $360 \cdot 0.5/16.67 = 10.8$ degrees. This means that instead of the desired 90-degree comparator angle (4.17 ms coincidence timing), the logic performs either an

86.4-degree comparison (4 ms) or a 97.2-degree comparison (4.5 ms). The error can be reduced by higher sampling rates or detecting changes in the polarity of the signals between the samples to accomplish subsample timing. Both these methods require more calculations and increase complexity.

Our design solves the accuracy problem by using a coincidence timer shorter than the accurate value, yielding a comparison angle greater than 90 degrees and supervises the time-domain comparator with a frequency-domain comparator (see Fig. 4). The frequency-domain comparator uses the same voltage and current phasor inputs and simply applies the logic of Fig. 1b. Because of the supervision, the final shape of the operating characteristic is equivalent to having an exact 90-degree comparator limit angle in the time-domain comparator.

4.3   Sign Consistency Check Between the Filtered and Raw Operating Signals

The raw and filtered (real part) operating signals are time-coherent because the filter compensates for the group delay [3]. We can compare them sample by sample. In our design, we check if they have consistent signs, i.e., if both are positive or negative. The disagreement in the sign tells us that the signals may have transients beyond the filtering capabilities of the applied filters, especially when the variable-window filter uses very short data windows just after resizing or a capacitively coupled voltage transformer (CCVT) creates transients that are large compared with the true operating signal. Fig. 5 illustrates the sign consistency logic. We use the output signal (Z) in Fig. 5 to supervise the AND gates in Fig. 4. When signal (Z) deasserts because the raw and filtered operating signals have opposite signs, the timers integrate down.
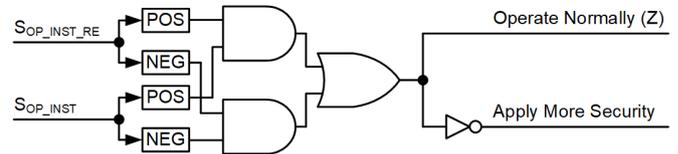
Fig. 5.   Sign consistency logic checking the raw (S_{OP_INST}) and filtered ($S_{OP\_INST\_RE}$) operating signals.

4.4   Checking the Level of the Raw Operating Signal

If the raw operating signal is small, an internal or external fault is very close to the reach point. To add margin for transients for such faults, the element applies more security when operating for very small levels of the raw operating signal. Fig. 6 illustrates the operating signal level logic. We use the output signal (X) in Fig. 6 to supervise the AND gates in Fig. 4. A low signal level, such as below one percent of the nominal voltage, causes the timers to integrate down.
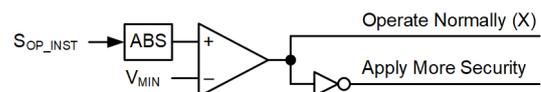
Fig. 6.   Raw operating signal level logic.

4.5 Resetting Coincidence Timers Upon Disturbance

There may be conditions when the comparator is asserted prior to a fault. This is typically the case for the reactance comparator. The load impedance is typically below the reactance set point. If so, the load asserts the output of the reactance comparator. A mho comparator under heavy load conditions may assert as well (the mho element is not operating on load because it is typically blocked by the load-encroachment logic, but the mho comparator itself may be permanently asserted on load).

If the mho or reactance comparator is permanently asserted on load, it has a lower security margin for a subsequent fault external to the zone of distance protection. With reference to Fig. 4, our design uses a disturbance detector to reset the integrating timers. This way, the timers "lose" their memory of the pre-fault load and start "fresh" using only the fault data.

4.6 Dependability for Very Small Operating Signals

By design (see Section 4.4), the fast coincidence timing algorithm restrains if the operating signal is too small. To maintain steady-state accuracy and dependability, our design uses the frequency-domain comparator (Fig. 1b) with a time delay on the order of one to two cycles (see Fig. 4).

4.7 Zone 1 Dynamic Reach

Distance Zone 1 is normally set to underreach the remote line terminal and trip directly without the pilot channel. To improve security, our design dynamically reduces the Zone 1 reach to about 80 percent of the set reach when the filter [3] resizes. Subsequently, the Zone 1 reach grows with the filter window length, and it reaches 100 percent of the set value when the filter window reaches one full cycle.

5 Laboratory Test Results

The presented distance element design has been implemented on a relay platform based on [2] and tested for security, dependability, and operating times under a variety of system conditions using a real-time digital simulator (RTDS). The Zone 1 distance elements are applied to underreach the remote line terminal to trip directly without a pilot channel. The Zone 2 distance elements are applied to overreach the remote line terminal as part of a pilot scheme or for step-distance protection. Therefore, our design applies the solution described in Section 4 to Zone 1, and for Zone 2 it uses a simplified design biased for speed without strict transient reach accuracy requirements. As a result, the operating times and transient accuracy of Zones 1 and 2 differ.

Fig. 7 shows the Zone 1 operating time as a function of fault location, respective to the set reach, for a range of source-to-impedance ratios (SIRs). In strong systems (SIR of 0.1), the element operates in less than a half cycle for locations up to about 80 percent of the set reach. In weaker systems (SIR of 15), the element operates in as fast as 1.2 cycles. The Zone 1 element has excellent transient accuracy with a transient overreach below 5 percent. The operating time curves bend up for locations 20 percent short of the reach point as a result of solutions described in Sections 4.4 and 4.7.
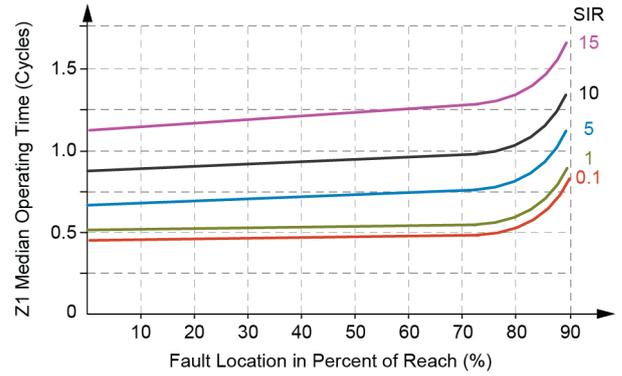
Fig. 7. Underreaching Zone 1 operating times.

Fig. 8 shows the Zone 2 operating time curves. The zone is set to 120 percent of the line, and it provides a near-constant operating time for faults anywhere along the line. Having relaxed transient overshoot requirements, Zone 2 is slightly faster than Zone 1.
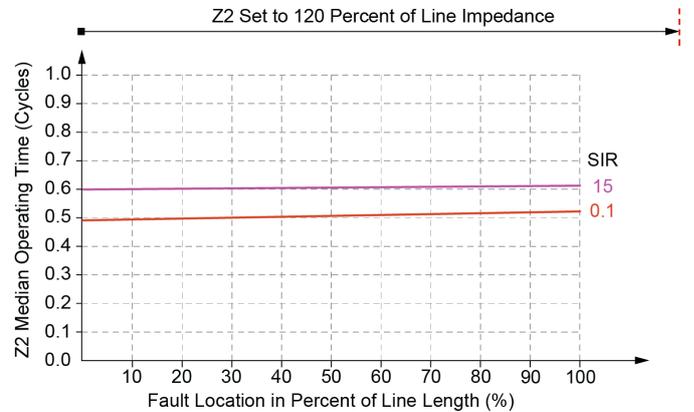
Fig. 8. Overreaching Zone 2 operating times.

Fig. 7 and Fig. 8 apply to both the mho and quadrilateral distance elements (in our design there are very small differences in speed and transient overreach between the two types of distance elements).

6 Illustration With a Field Event

A relay [2] operated for an internal BG fault on a 345 kV, 109 mi line in a 60 Hz network with a high degree of series compensation located in the vicinity of the protected line. The relay recorded the voltages and currents shown in Fig. 9 and operated using a traveling-wave differential scheme, TW87 [1], in less than 2 ms. The relay actuated a two-cycle circuit breaker directly by using a solid-state trip-rated output (10 μs closing time), and the breaker interrupted in 1.5 cycles. As a result, the fault lasted only 25 ms, or 1.75 cycles.

In our tests using this field recording, the variable-window filter [3] resized the window at about 4.5 ms into the fault. The Zone 2 mho and quadrilateral elements, set to 120 percent of the line impedance, responded in about 7.6 ms. The Zone 1 mho and quadrilateral elements, set to 85 percent of the line impedance, responded in about 8 ms. These operating times include the relay processing time and the trip-rated output contact closure time.

Fig. 10 illustrates operation of the Zone 1 mho elements by showing the real and imaginary parts of the polarizing and operating signals. Before the fault, the polarizing and operating signals are out-of-phase. When the fault occurs, the operating signal begins changing, and when the filter window resizes, it jumps to reflect the fault value. About 4.5 ms into the fault, the imaginary parts of the polarizing and operating signals are the same polarity, which engages the coincidence timer and results in Zone 1 operation. The real parts are the same polarity starting at about 7 ms. S_{OP_INST} (IZ – V signal) is large (see Section 4.4) and very clean, despite distortions in the relay voltages and currents. The Zone 1 operation in 8 ms is robust and secure. The polarizing signal in Fig. 10 does not change during the fault because the element is fully memory-polarized.
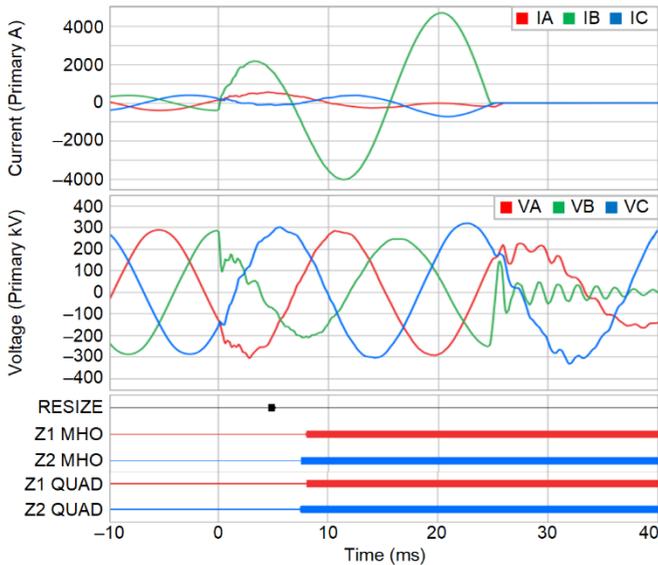
Fig. 9.   Current and voltage signals during a field event.
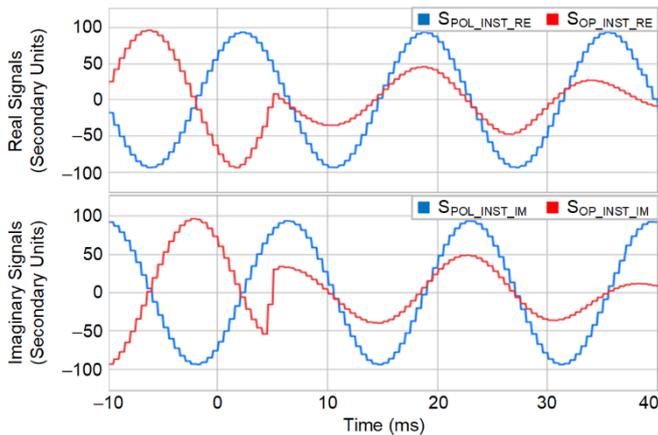
Fig. 10.   Zone 1 mho operating and polarizing signals (real and imaginary parts).

Fig. 11 illustrates the part of the comparator logic that checks if the raw and filtered operating signals have the same polarity. The two signals agree very well, except during the time interval between 0 and 4.5 ms (before the window resizing), which allows the distance element to operate fast (see Section 4.3).

Fig. 12 illustrates the operation of the Zone 1 quadrilateral elements by showing the imaginary parts of the polarizing and operating signals (our quadrilateral elements are polarized with

the loop current). Prior to the fault, the polarizing and operating signals are out-of-phase. When the fault occurs, the operating and polarizing signals begin to change, and when the filter window resizes at about 4.5 ms, both jump to reflect the fault value. About 5 ms into the fault, the imaginary parts of the polarizing and operating signals are the same polarity, which engages the coincidence timer and results in Zone 1 operation.
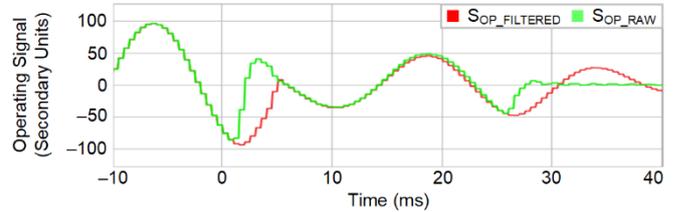
Fig. 11.   Zone 1 mho raw and filtered operating signals.
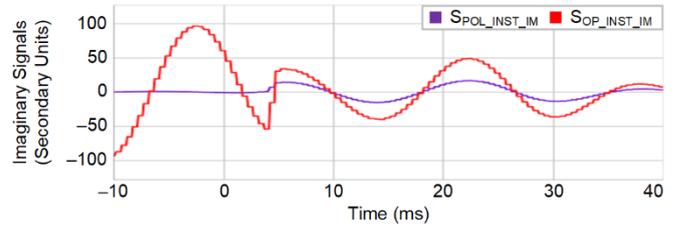
Fig. 12.   Zone 1 quadrilateral operating and polarizing signals (imaginary parts).

7   Conclusion

This paper presents the implementation of a distance protection element in a microprocessor-based relay that uses coincidence timing and window resizing. The paper explains the principles of coincidence timing and its benefits. Taking advantage of digital technology, the paper introduces several enhancements complementing the classic coincidence timing method. The method presented in this paper achieves an excellent balance between speed (half-cycle operating time in strong systems and one-cycle operating time in weak systems) and security (Zone 1 transient overreach below five percent). The distance element logic presented here has been implemented in a relay platform based on [2], and it operates consistently with trip times of a half cycle, including relay processing time and trip-rated output contact closure time.

8   References

[1]   Schweitzer, III, E. O., Kasztenny, B., Mynam, M., et al.: "New Time-Domain Line Protection Principles and Implementation," proceedings of the 13th International Conference on Developments in Power System Protection, Edinburgh, UK, March 2016.

[2]   *SEL-T400L Instruction Manual*. Available: selinc.com.

[3]   Kasztenny, B., Mynam, M. V., Joshi, T., et al.: "A New Digital Filter Using Window Resizing for Protective Relay Applications," proceedings of the 15th International Conference on Developments in Power System Protection, Liverpool, UK, March 2020.