Phase-Shifting Transformer Control and Protection Settings Verification

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***Abstract*—San Diego Gas & Electric® (SDG&E®) initiated a project to add two parallel 400 MVA (+31.3° to −80.1°) phase-shifting transformers (PSTs) at a 230 kV interconnection substation. California ISO (CAISO) proposed the PST project to provide flow control between SDG&E and Comisión Federal de Electricidad (CFE) 230 kV systems during critical N-1 or N-1-1 500 kV line contingencies. With the need to integrate renewable generation, many utilities are using PSTs to manage the grid (e.g., American Electric Power [AEP] has eight PSTs in their system). SDG&E is presently reviewing the need for additional PST projects. The authors collaborated to address the unique challenges of parallel PST protection and control for this wide-ranging PST application, including implementation of CAISO control and automatic contingency-based tap-changer runback.**

This paper discusses SDG&E's process to execute the project, including settings development, simulation, lab and field testing, and in-service testing. The authors discuss oscillography analysis used during lab testing, energization, and loading to verify the overall design and programming.

I. Introduction

The Imperial Valley 500 kV/230 kV substation provides the San Diego Gas & Electric (SDG&E) utility with a 500 kV interconnection to Arizona Public Service (APS) and 230 kV interconnections to Comisión Federal de Electricidad (CFE) and Imperial Irrigation District (IID). The total interconnected generation at Imperial Valley is 1,880 MW, including 1,100 MW of combined cycle and 780 MW of solar generation. In addition, 570 MW of wind generation is connected at the utility's adjacent 500 kV substations. There are two 500 kV lines from Imperial Valley into the San Diego-area load and an underlying 230 kV east-to-west path through the CFE 230 kV system. When a 500 kV line is out of service, the 230 kV path can be loaded to high levels.

A. Analysis and Requirements

California ISO (CAISO) proposed a project in 2014 to install a flow controller on the 230 kV CFE interconnection line at Imperial Valley. The project goal was to provide a means of controlling the flow through the CFE system during N-1 and N-1-1 operating conditions, enabling the 230 kV path to remain in service during stressed conditions. While a back-to-back dc flow controller was considered, two parallel 400 MVA phase-shifting transformers (PSTs) were proposed for installation at Imperial Valley. Based upon power flow studies, these PSTs were specified to have a range of +31.3° to −80.1° over 65 tap positions, with a range from +16 advance tap to −48 retard tap. CAISO targeted an in-service date of May 1, 2017.

Fig. 1 shows a simplified schematic drawing for the project, including the source, load, and bypass circuit breakers.

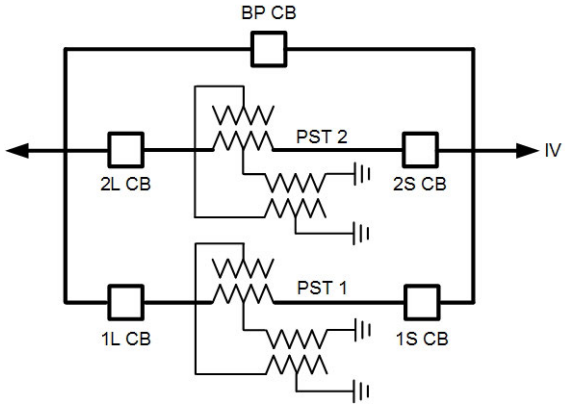


Fig. 1. Two-Core PST – Simplified One-Line Diagram

The utility formed a project team in 2014, including personnel in engineering, project management, environmental management, and supply management. Contract entities included a substation engineering design consultant who provided the substation design package and a protection and control (P&C) engineering services consultant who provided the P&C solutions. The engineering services consultant had provided P&C solutions for more than 20 PST projects throughout North America with a proven design.

CAISO runs a market-based software application to determine generating-unit set points in real time. CAISO decided in late 2015 to set the PST load tap changer (LTC) tap set points as generated by the market-based software, with the possibility of adjusting set points on a 15-minute schedule. It became clear that the PST controllers would need to enable efficient parallel operation in an expeditious manner while interfacing with a signal from CAISO.

The utility and CAISO discussed in early 2016 the proposed operation for when a PST trips. Rather than cross-tripping the remaining unit if overloaded, the utility proposed an automatic scheme to operate the remaining PST LTC in the retard direction, reducing the flow to a value below the 400 MVA continuous rating. This logic was implemented in the controller design.

B. PST Project Features

In summary, the unique features of this PST project were:

- Parallel high-capacity PSTs.
- A very wide phase angle regulating range.
- Nonlinear impedance throughout the operating range.

- 65 LTC tap positions with an advance-retard switch (ARS).
- CAISO tap set points sent remotely.
- Automatic LTC operation to reduce PST loading for loss of one PST.

The transformers were manufactured in Austria, tested in summer 2016, shipped in fall 2016, and arrived at the Imperial Valley substation site in December 2016.

The substation electrical design began in mid-2015 and continued through 2016. The design team included utility engineering and operations personnel, the substation design consultant, and the P&C engineering services consultant. Frequent design review meetings and phone calls ensured that all team members were working in concert. Electrical drawings and test data were shared with the design team as they were made available.

The grid operations team developed standard procedures in 2016 to operate the PSTs, including energizing/loading and unloading/de-energizing. The team decided to provide permissive close signals from the PST controllers to the PST circuit breakers to ensure standard switching practice was followed. Supervisory control and data acquisition (SCADA) points lists were developed to provide analog data, control, and status indication. The P&C engineering services consultant then implemented all custom utility logic, including SCADA control and indication points in the controller logic platforms.

PSTs control power flow on the transmission system. They insert a variable magnitude quadrature voltage into each phase to create a phase shift between the source- and load-side bushings by using a tap changer on the regulating winding. The simplified equation (neglecting losses and shunt admittances) for power flow through a transmission line is demonstrated in (1) [1].

$$P = \frac{E_S \bullet E_R}{X_L} \sin \delta \qquad (1)$$

where:

E_S is the sending-end voltage.

E_R is the receiving-end voltage.

X_L is the series reactance of the transmission line.

δ is the angle between the two voltages.

This equation reveals that power flow is largely a function of the angle between the two voltages. If the angle across the line can be regulated, the power flow through the line can be regulated. By introducing an angle that is additive (advance), the power flow can be increased. By introducing an angle that is subtractive (retard), the power flow can be reduced.

For example, a voltage in phase with V_{BC} or V_{CB} would be combined with V_A to produce a phase shift between the S and L terminals of the transformer. The PST used at the Imperial Valley substation is based on a two-core design and is shown in Fig. 2.

This configuration has two magnetic cores: the series core and the excitation core. The tap-changer mechanism operates on the secondary winding of the excitation core and induces a phase-shifting voltage component through the delta winding on the series core.

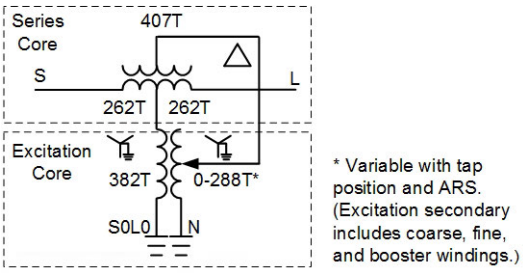


Fig. 2. Two-Core PST

II. General Information and Design Details

This section discusses the unique features of the PST design and some design details. The wide and offset range of regulation of these PSTs made them unusual. To achieve this range of regulation, the PST excitation transformers were constructed with three secondary windings designated as fine, coarse, and booster. Each of these windings has the same number of turns, so they each produce the same voltage.

Fig. 3 shows the configurations of the windings for the range of regulation. The regulation range is broken into four subranges: one in the advance direction and three in the retard direction. The fine winding is the tapped winding that the LTC can insert in 16 steps. The coarse winding is inserted as needed to provide offset from one regulation range to the next. The booster winding is always in the circuit.

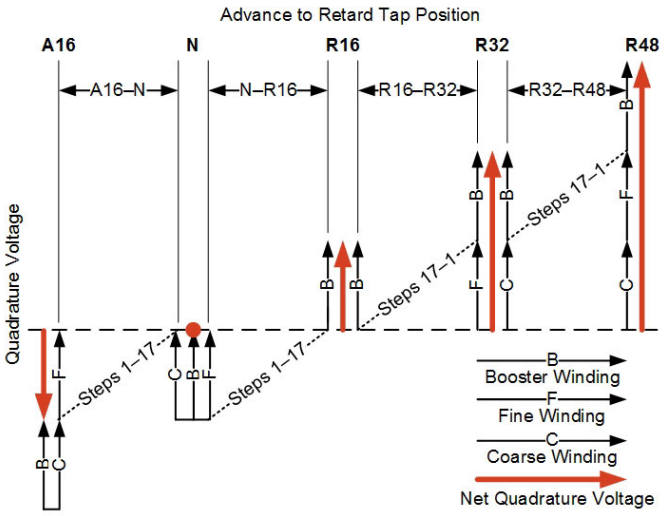


Fig. 3. Three Secondary Windings Provide Wide Range of Regulation

Even though each of the three windings has the same number of turns, the physical arrangement of each winding relative to the others on the core is different, resulting in different leakage reactance depending on which windings are in the circuit. Fig. 4 shows the PST impedance and phase shift during a no-load condition with variation of tap position. The discontinuities are quite evident as different windings are switched in and out and cause complications in the protection and control system design, as discussed in Section IV.

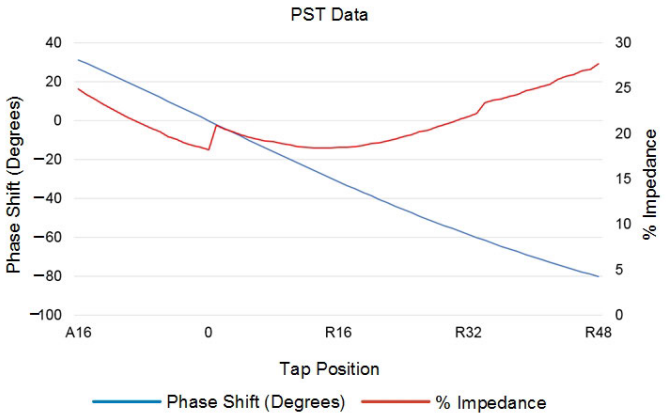


Fig. 4. PST Impedance Variation With Tap Position

III. Protection Scheme Design

This section summarizes the main protection scheme for this PST. Three relays are selected per PST. The detailed protection scheme is beyond the scope of this paper. References [2], [3], [4], [5], [6], and [7] provide various techniques and details involved in PST protection and modeling. Reference [7] provides a good summary of the protection applied for this project.

A. Scheme Design and One-Line Diagram

The two-core PSTs installed at the Imperial Valley substation are protected by three relays per PST. Main 1 consists of two relays, 87-PSTnP and 87-PSTnS, as shown in Fig. 5 It should be understood that in this application, the suffixes P and S do not stand for primary and secondary systems as in a typical redundant protection system. Two relays are required to provide complete coverage of the PST. In the above designations, n = 1 for PST1 and n = 2 for PST 2. Main 2 consists of one relay, 87-PSTnO, as shown in Fig. 6. O stands for the overall differential for this protection system. With the addition of sequence component differential protection to the S and O relays, these relays are responsive to all fault types [7].

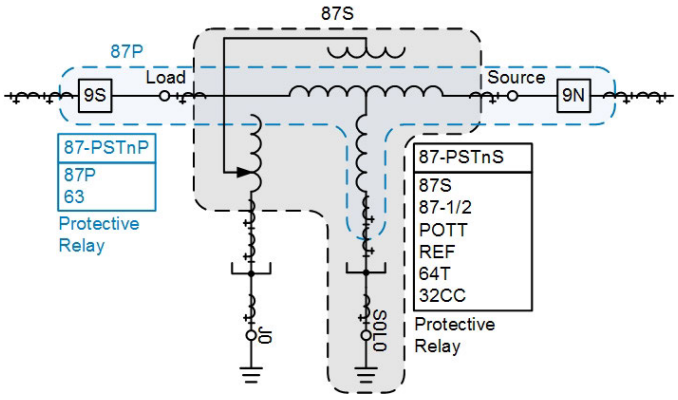


Fig. 5. Main 1 Primary and Secondary Protection

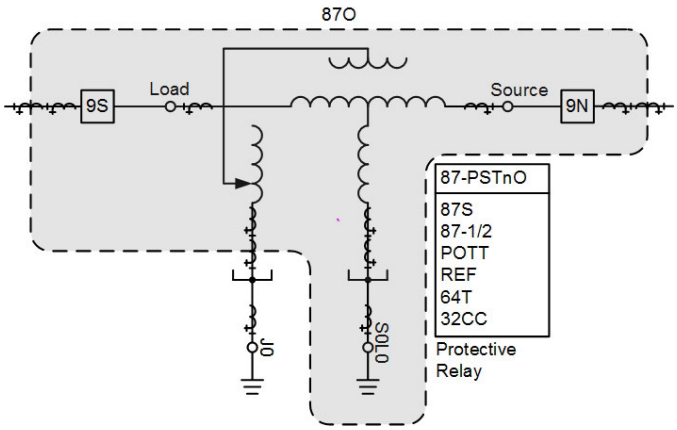


Fig. 6. Main 2 Overall Differential Protection

1) Primary Winding Differential and Sudden-Pressure Protection

The 87-PSTnP relay is designated 87P for primary winding differential, as it only protects against faults in the primary windings of the two transformers that make up a two-core PST. See Fig. 5 for the details of the 87P protection scheme. The 87P relay provides the PST zone with Kirchhoff's current law (KCL) bus-type differential and provides high-speed protection to the primary windings on the series and excitation cores. This relay is also wired to provide PST apparatus trips, i.e., sudden pressure relay (SPR), Buchholz oil temperature protection, etc.

The 87-PST1P and 87-PST2P relays provide KCL differential protection to the primary windings of the two transformers (87P). KCL differentials are immune to transformer magnetic core effects such as inrush and overexcitation because these differential zones do not match ampere-turns (ATs) across the iron core of the PST. Thus, a bus-type differential without harmonic restraint or harmonic blocking is used for this application. The 87P zone is bounded by the current transformers (CTs) on the load breaker, the CTs on the source breaker, and the CTs on the neutral end of the excitation transformer primary windings. The relay trips the source- and load-side breakers and the 86T lockout relay. Because the 87-PST1P and 87-PST2P relays are blind to turn-to-turn faults, the 63 SPRs trip for them to clear these faults.

2) Secondary Winding Differential Protection

The 87-PSTnS relay in Fig. 5 is designated 87S for secondary winding differential. This relay protects against faults in the secondary windings of the two transformers that make up a two-core PST. The zone of protection of the 87S relay is bounded by the PST bushing CTs and the neutral-end phase CTs of the regulating windings. These three sets of CTs provide series transformer ampere-turn-balance (ATB) protection. This scheme is not responsive to faults on the

primary windings of the excitation transformer. In addition, the scheme is not responsive to turn-to-turn faults on the secondary windings of the excitation transformer.

3) Sequence Component Differential Protection

Positive-sequence and negative-sequence differentials are implemented in both the 87S relay and the overall differential relay. This includes the ability to compensate for a PST angle using electrical measurements instead of mechanical indication of tap-changer position. The sequence component differentials require voltage transformer (VT) inputs for angle compensation. The VTs allow directional elements to provide external fault detectors to put the sequence component differentials in a high-security mode. The directional elements are then used in a permissive overreaching transfer trip (POTT) scheme.

4) Overall Differential Protection

The 87-PSTnO relay, shown in Fig. 6, is the overall relay with protection functions similar to the 87-PSTnS relay. The only exception is that different source and load CTs are selected for the 87-PSTnO relay. The use of the breaker CTs instead of the PST bushing CTs allows the 87-PSTnO relay to provide complete fault coverage, because the sequence component differentials only use the two CTs at the boundary of the zone and are therefore responsive to all faults between them. In this way, the 87-PSTnO relay provides coverage for faults between the source and load breakers and the PST.

5) Ground Fault Protection

The 87-PSTnS and 87-PSTnO relay systems provide primary winding (REF) and secondary winding (64T) equipment ground protection. Ground backup protection of the primary winding is disabled for this application because this is a five-legged core transformer. No ground fault contribution is expected for the external faults.

6) Bypass Off Neutral Protection

The 87-PSTnS and 87-PSTnO relays provide circulating current protection (32CC), also known as bypass off neutral logic. The element detects circulating current generated in the loop comprising the PST and the bypass path if the PST is accidentally bypassed when the LTC is off neutral. The differential elements generally do not respond to these potentially damaging currents, so a dedicated protection scheme is provided. If the PST is bypassed off the neutral, the protection system trips the load-side circuit breaker, breaking the circulating path while still leaving the line in service through the PST bypass breaker.

The phase currents are measured on the load side of both PSTs and the bypass circuit breaker. An additive and a subtractive current are calculated from these measurements. The additive current represents the load current down the line. The subtractive current is a measurement of the circulating current in the bypass loop. The ratio of subtractive current to additive current indicates whether circulating current is present. If the bypass is closed, most of the current flows through the bypass breaker. Circulating current can be calculated using (2) through (4).

$$IA_{ADD} = IA_{BYP} + \left(IA_{PST1} + IA_{PST2}\right) \quad (2)$$

$$IA_{SUB} = IA_{BYP} - \left(IA_{PST1} + IA_{PST2}\right) \quad (3)$$

$$IA_{CIRC} = \frac{IA_{SUB}}{IA_{ADD}} \quad (4)$$

The ratios for (2), (3), and (4) are as follows:

- For even distribution of load current between the parallel branches, the ratio is 0.
- For the extreme of no-load current in one of the branches, the ratio is 1.
- The only way the ratio can be greater than 1 is if circulating current is present.

B. Front-Panel Indications

Fig. 7 shows the 87P relay front panel with all protection elements and external trips. Pushbuttons (PBs) and PB light-emitting diodes (LEDs) are not used for this relay. Fig. 8 shows the front panel for the 87S and 87O relays. There are no transformer device trips for the 87S and 87O relays.

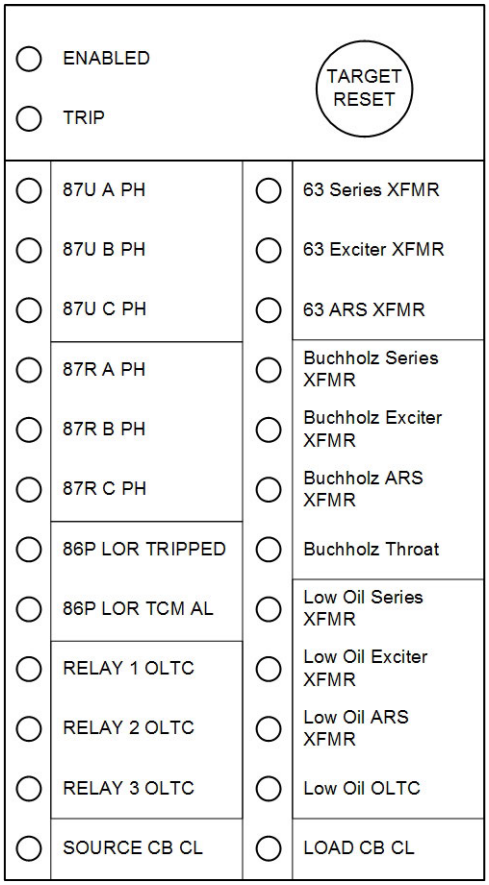


Fig. 7. 87P Relay PST Protection Front Panel

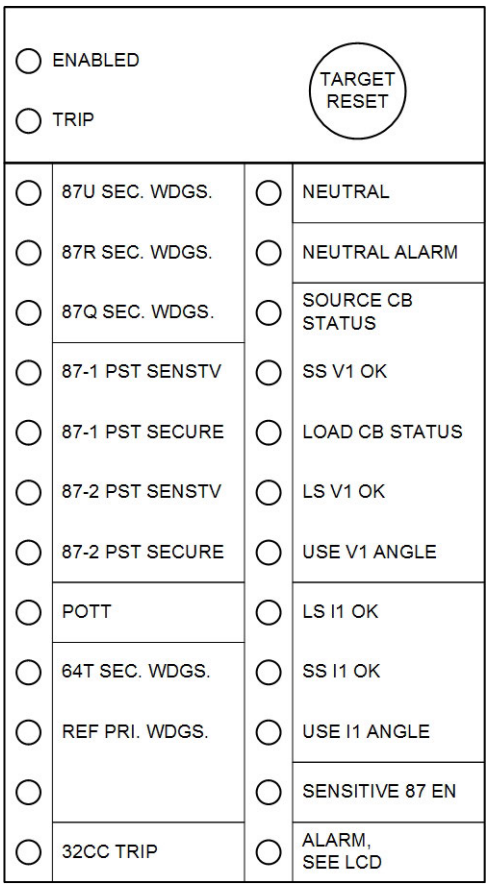


Fig. 8. 87S and 87O Relay PST Protection Front Panel

IV. PST Controller Master/Follower

Custom LTC controller logic was developed for each PST as part of this project [8]. The PSTs operate in Master/Follower mode; either PST controller can be selected as the master controller. The high-speed communication between the two controllers maintains the correct operation modes. High-speed communication also exchanges LTC tap position, real and reactive power, PST breaker status, and motor running contact. This information is used in the PST controller logic.

A. Main Features

PST control includes the following protection monitoring and control features:

- Local and remote manual control to advance and retard tap
- Tap set point per CAISO
- Run-to-neutral control function
- Automatic regulation to keep loading below the PST continuous rating during N-1 conditions
- PST overload (OL) instantaneous and OL delayed alarms
- Automatic operation suspend function
- Master/Follower mode for parallel PSTs and monitoring of:
  - Tap position out-of-synchronism alarm
  - Circulating apparent power alarm
  - Provision to trip motor circuit to prevent runaway out-of-synchronism condition
- Verification of neutral before bypassing
- Local annunciation and remote communication of status and alarm conditions
- Local and remote indication of tap-changer position, power flow conditions, and motor operational parameters
- Custom permissive commands for source, load, and bypass breakers

When Automatic mode is enabled, the controller maintains the tap position as specified by CAISO. CAISO sends the tap position to the energy management system (EMS) via an Inter-Control Center Communications Protocol (ICCP) link, and SCADA sends the set point via DNP3 to the controller. The controller includes features to mitigate overloading. The following overload functions are programmed:

- N-1 overload override
- Low-set overload alarm
- High-set overload alarm

N-1 overload override asserts if the PST load is above a low-set threshold (for example, 400 MVA) for a selected duration when the second PST is out of service. N-1 overrides the CAISO set-point mode and lowers the load on the online PST to maintain the load of a low-set threshold or less, regardless of the CAISO set point.

The PST controller also provides low-set and high-set overload mitigation functions. If loading exceeds a low-set threshold (regardless of being in an N-1 state), the controller alarms after a user-settable delay. If overload exceeds a high-set threshold (for example, 600 MVA), the controller alarms after a user-settable delay.

When in Manual mode, it is possible to enable the run-to-neutral control function. This function initiates tap changes in the appropriate direction upon the rising edge of run to neutral. This command can be initiated either from the front PB or SCADA. Once the first tap change is initiated, the function initiates additional steps after the expiration of the delay between steps timer as long as run to neutral remains asserted. This logic requires input from the Calculate Effective Tap Position function to determine if the tap is in an advance or retard position. The input determines if tap advance operations or tap retard operations are required to get the tap position to neutral. Once Tap Position on Neutral is indicated, Run-to-Neutral in Process deasserts and the process is complete.

B. PST Controller Front Panel

Fig. 9 shows the front panel of the PST controller. There are two parallel PSTs at the Imperial Valley substation. The two LTC controllers can operate in Master/Follower combination or Independent operation modes. When in parallel operation, one of the controllers is assigned as the master and the other becomes the follower. In this mode, the follower simply follows the commands given by the master. Functions (e.g., Advance, Retard, Automatic, and Manual PBs) are disabled for the

follower controller. In the event the PST with the master controller trips, the follower controller mode is changed to Independent mode. The operating state in Independent mode (Off, Automatic, or Manual) will be identical to the master prior to the trip.

The Master/Follower or Independent modes can be chosen locally or via SCADA. When one of the controllers is in Master mode, the other controller automatically becomes the follower. Similarly, if the Follower or Independent command is asserted on either of the controllers, the other automatically becomes the master or switches to Independent mode, respectively. The controllers also switch to Independent mode if the communications channel (serial cable) fails or either PST trips.

C. Tap Position Control Logic

When Automatic mode is enabled, the control operates to maintain the tap position as specified by CAISO. SCADA sends the set point via DNP3 to the controller. Fig. 10 shows the custom logic that reads and processes the CAISO tap for this PST. The control includes features to mitigate overloading. The

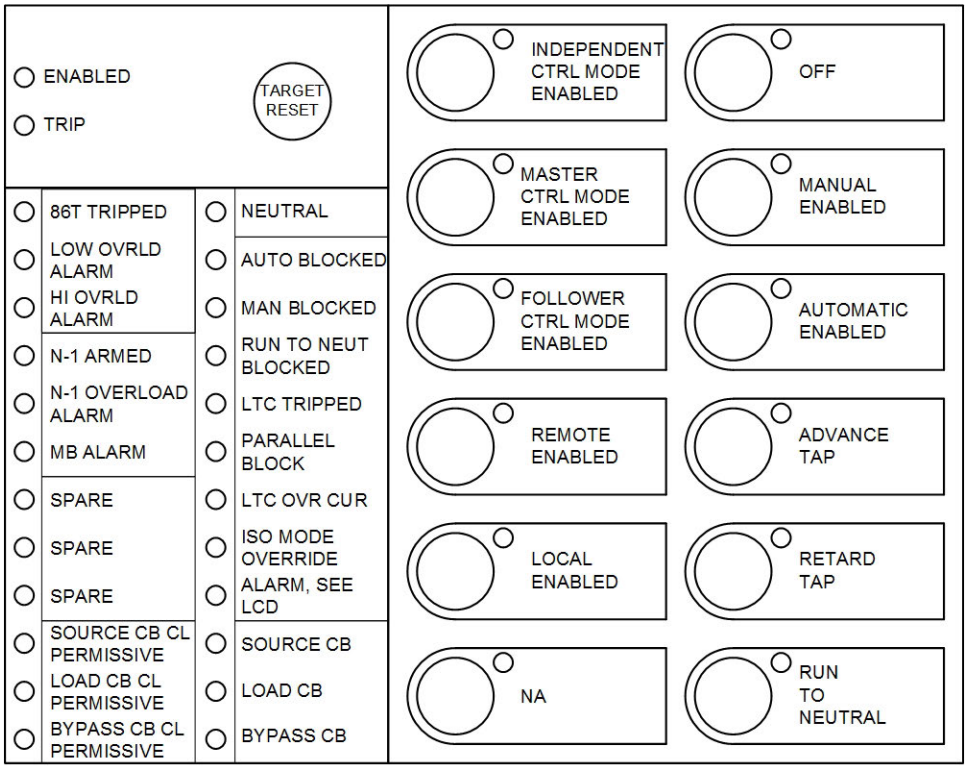


Fig. 9. PST Controller Front Panel

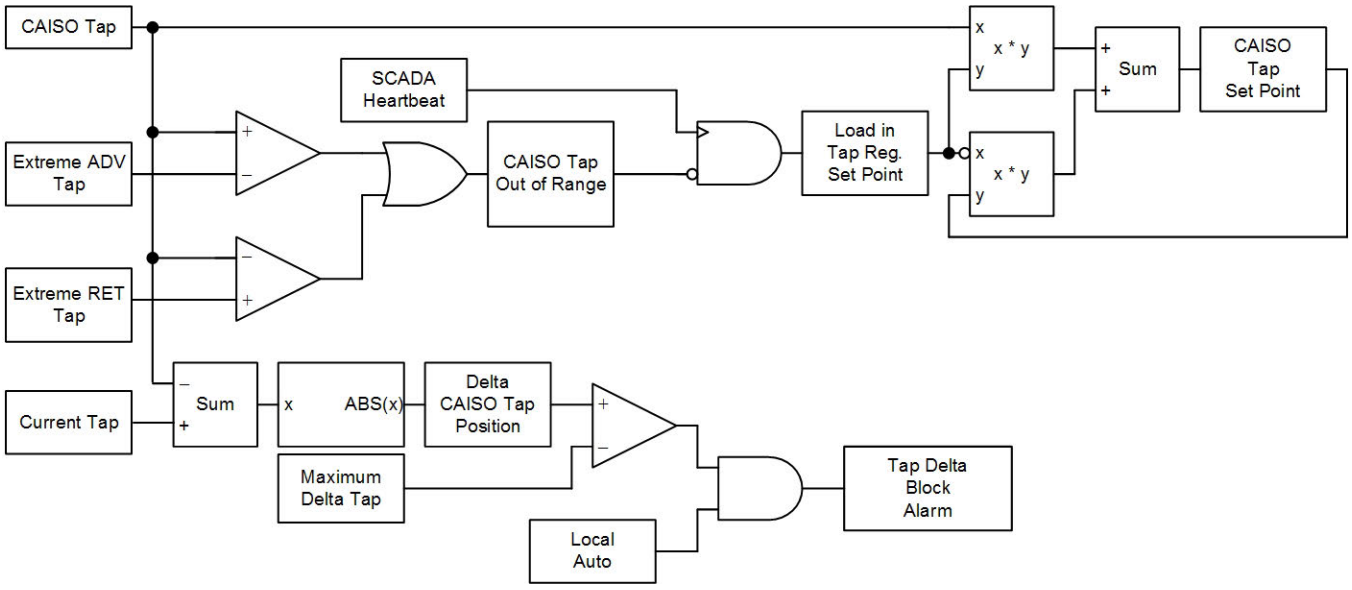


Fig. 10. PST Controller Tap Position Control Logic

regulation set points are stored in volatile memory. If the control logic restarts for any reason, the set points can be lost. The control logic can restart for several reasons. Following are typical examples for restarting control logic:

- The control power is cycled.
- New programming is entered into the control while it is in Automatic mode.
- A self-test restart occurs.

To prevent the control from initiating tap changes to drive the tap position to zero (the default regulation point), the control automatically starts in the Independent and OFF modes. A SCADA heartbeat (HB) system is programmed in the utility SCADA master to ensure that the regulation set point is legitimate as commanded by the CAISO master. The HB script in the SCADA master periodically writes the CAISO set point to remote analog and then asserts the SCADA HB. It then periodically resets the control point HB such that the HB is a square wave with a period set in the SCADA master. The script stops setting and resetting the control point HB if it loses communication with the CAISO master. Similarly, if the SCADA master-to-LTC controller link fails, the control point HB also fails to change state. The LTC controllers monitor this condition and go into alarm if a change of state is not seen for 1.5 times the expected period. This alarm condition blocks automatic control and self-clears as soon as a new HB control point is received.

On the rising edge of the SCADA HB, the control reads remote analog into active memory. This ensures that the active regulation set point is updated soon after a logic restart or after CAISO sends a new set point. It also serves as an integrity poll to refresh the set point periodically to ensure it is always in sync with the CAISO set point. Additionally, the control verifies the validity of the CAISO set point as follows:

- CAISO tap position set point is within the expected range of +16 and –48.
- Maximum tap difference from present tap position and CAISO set point is less than 5 (user-settable), ensuring that a corrupted tap position signal will not result in a tap change that can cause problems with the transmission system.

Tap changer logic reads the tap position sent via CAISO and compares the tap position to the existing tap position. Advance and retard commands are issued based upon the difference between the existing and required taps.

Fig. 11 shows the PST CT/potential transformer (PT) connections. Three-phase currents and voltages are connected on the load side. In addition, single-phase PT connections are on the source side and the load side between the PST and the breaker. The single-phase voltages are used to verify the neutral position. In addition to neutral position contact, the neutral is also verified using the binary-coded decimal (BCD) inputs and the ARS.

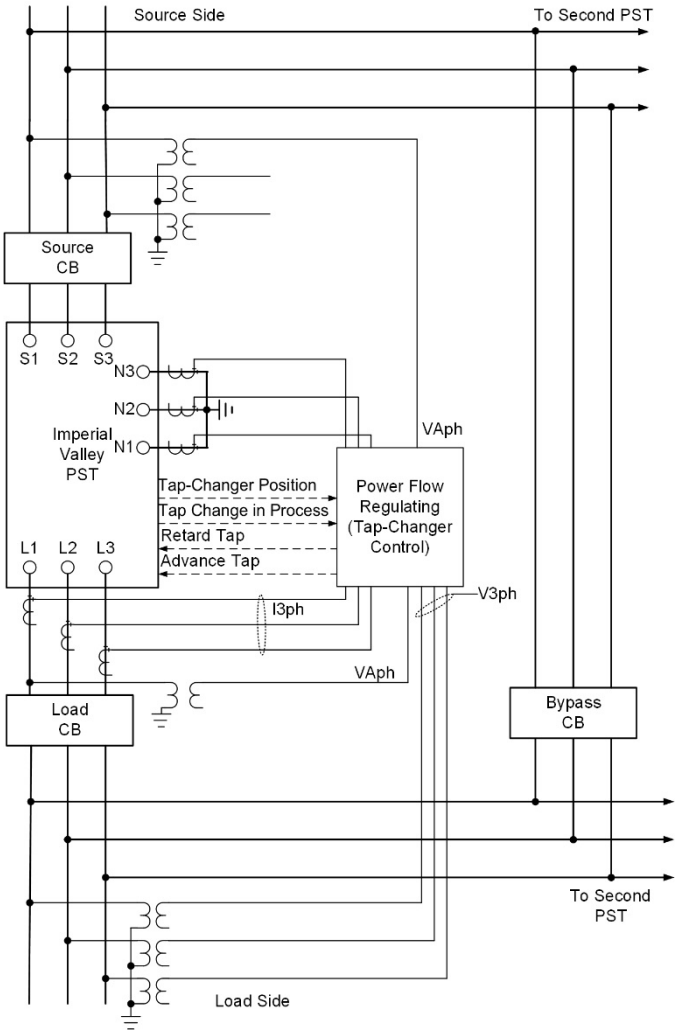


Fig. 11. PST Connection Diagram

Fig. 12 shows the BCD and ARS inputs, which are used for calculating the PST tap position. The logic also indicates the effective tap and provides the following information:

- Tap position on neutral
- Tap position in retard
- Tap position in advance
- Tap position at extreme retard
- Tap position at extreme advance

Additional advance and retard commands are blocked if they come before the delay between tap steps has expired. The appropriate PB LEDs on the front of the control illuminate solidly when a tap change is in process. After a tap step is complete, the two LEDs on the Advance and Retard PBs alternately blink until the delay between tap steps has expired.

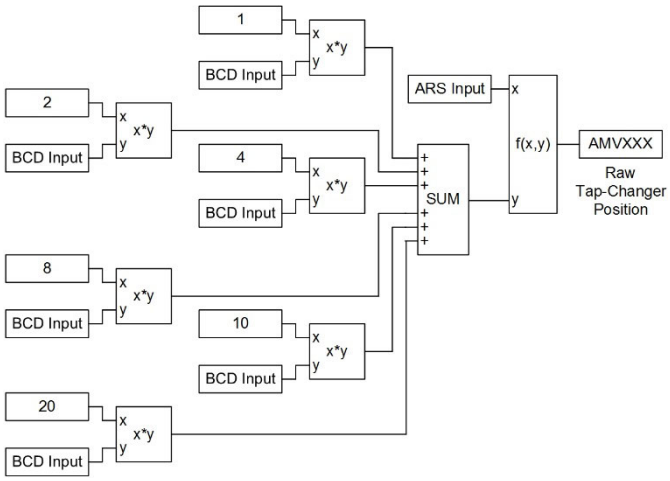


Fig. 12. Tap Position Logic

The tap changer switching contacts can be damaged if the switching current is above a certain level. This can occur during prolonged external faults or overloaded conditions. The Overload Alarm function also includes an overcurrent function that suspends automatic timing and asserts the manual control cutout when any phase current is above this user-settable threshold.

D. Circulating Apparent Power Protection

Large circulating apparent power (S_{CIRC}) may flow if the two PSTs operate at different tap positions. The magnitude of the S_{CIRC} is a function of the impedance of the PSTs and the voltage in the loop, which varies with tap position. Two methods are used to detect an undesired operating condition where both PSTs are at different tap positions:

- Tap position measurement
- S_{CIRC} measurement

Tap position difference logic compares the tap position of the two controllers for alarm and block functions. The present tap position of the two controllers is exchanged over the high-speed communications channels. If the tap position difference is equal to 1, then a parallel alarm is asserted. If the tap position difference is equal to 2, then a parallel block is asserted. Once the parallel block asserts, further tap change is prevented in Automatic mode. In Manual mode, the tap change operation that further increases the tap difference is prevented, while the operation that reduces the tap position difference is allowed.

The circulating apparent power logic uses apparent power measurements for alarm and block. Voltage-regulating LTCs insert an in-phase voltage, which results in the circulating current being almost 100 percent volt-ampere reactives (VARs). Thus, circulating VARs are a good way to monitor and alarm for LTC position mismatch. However, in the case of PSTs, the PST inserts a quadrature voltage but the quadrature voltage is only quadrature to the midpoint between the two terminals. Hence, the circulating current is a combination of the P and Q components in the case of a PST. The team decided to use apparent power S. Because the two PSTs have similar impedance, P and Q divide equally when the PSTs are paralleled and on the same step. S_{CIRC} is defined by subtracting the measured power from half of the total power as shown in (5) and (6). S_{CIRC} is then defined by totaling the quadrature components per (7).

$$P_{CIRC} = \frac{P1 + P2}{2} - P1 \tag{5}$$

$$Q_{CIRC} = \frac{Q1 + Q2}{2} - Q1 \tag{6}$$

where:

P1 and Q1 are the real and reactive power measured by the LTC control.

P2 and Q2 are the real and reactive power measured by the adjacent LTC control.

$$S_{CIRC} = \sqrt{\left(\frac{P1 + P2}{2} - P1\right)^2 + \left(\frac{Q1 + Q2}{2} - Q1\right)^2} \tag{7}$$

The magnitude of S_{CIRC} is a function of the impedance of the PSTs, which varies by tap position (see Section II), and the voltage in the loop, which also varies by tap position. Fig. 13 shows the S_{CIRC} characteristic programmed for this application. The expected S_{CIRC} for a one-step difference (alarm) and a two-step difference (block) varies depending on where in the range the PSTs are operating. The circulating megavolt-ampere alarm curve peak is ~53 MVA and the block peak is ~95 MVA; this is the PST neutral tap position. The Alarm Curve – Circulating MVA function is selected when the PSTs differ by one tap position. The Block Curve – Circulating MVA function is selected when the PSTs differ by two tap positions.

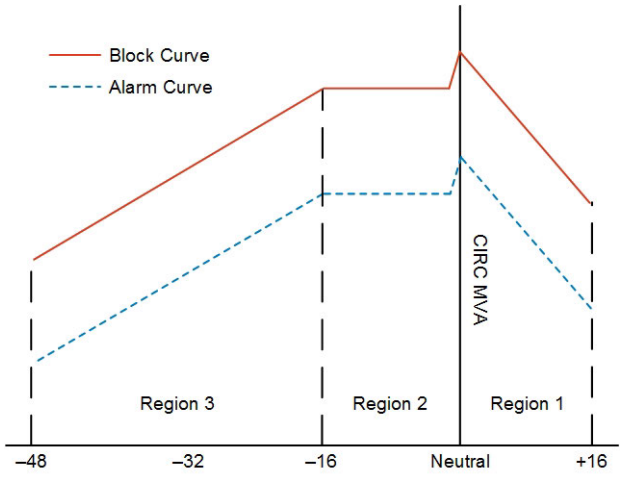


Fig. 13. Circulating MVA Operating Curves

Analysis was performed in ASPEN OneLiner™ to obtain an equation for this characteristic. ASPEN allows a user to model the impedance of the PST for different ranges of angle. To determine the circulating apparent power for one- and two-position differences, the team entered the PST impedance characteristic for the four ranges of regulation from the transformer test report.

PST controllers include the logic for load, source, and bypass breaker permissive closing. Each breaker is installed with the breaker control relay to process the permissive logic from both PST controllers. The sequence of operation for energizing the CFE line is as follows:

1. Energize line from Imperial Valley end only.

2. Close bypass breaker.
3. Close source-side PST breaker.
4. Verify PST in neutral; no trip is asserted.
5. Close PST load breaker.

V. Factory Acceptance Test and Real-Time Digital Simulator Results

The factory acceptance test (FAT), including hardware-in-the-loop testing (HIL) with a real-time digital simulator, was held at the P&C engineering services consultant's lab in July 2016 [9] [10]. Utility attendees included engineers from system protection, substation operations, and grid operations. The purpose of the tests was to observe PST P&C system performance and determine whether any relay setting or control logic changes were required.

A. Lab Test Setup and Results

PST and tap-changer motors were modeled in the real-time digital simulator. Protection and control relays were connected in a closed loop with the real-time digital simulator model to verify the PST operation. A detailed FAT plan was developed to test and verify all protection elements, the front-panel display, and other features for internal and external faults. The detailed test plan also included various operation modes of the PST and controller. For each location and PST tap position, multiple scenarios using scripts were run to verify the operation for various faults and incident angles. Fig. 14 shows the simplified one-line diagram and various fault locations where analysis was performed. Table I summarizes results for various types of faults and relay protection operation. Faults were analyzed for each location (i.e., single-phase, phase-to-phase, and three-phase faults). The faults at fault location (FLOC) 1 through FLOC 7 are internal faults. The faults at FLOC 8 and FLOC 9 are external faults. It can be concluded from Table I that multiple protection elements and relays provide coverage for the internal faults. As discussed in Section III, the 87P relay is based on KCL, and the 87S/87O relay is programmed for POTT, ATB, and custom sequence protection (SEQ) elements [7].

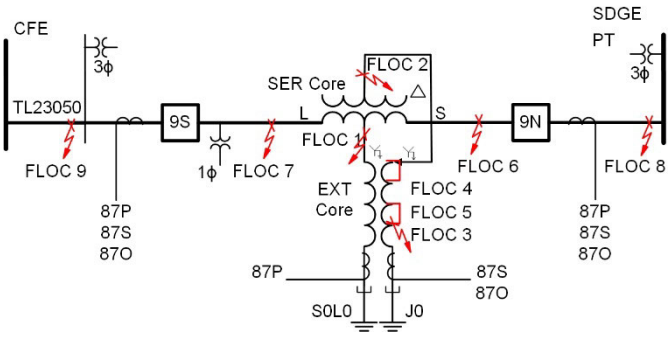


Fig. 14. System One-Line Diagram and Tap Position Control Logic

Fig. 15 and Fig. 16 show the three-phase and single-phase faults at FLOC 1 for the neutral tap position. These results match the results indicated in Table I. Fig. 17 shows a three-phase fault at FLOC 2 with tap −10 retard. POTT and ATB schemes on the 87S and 87O relays will clear this fault.

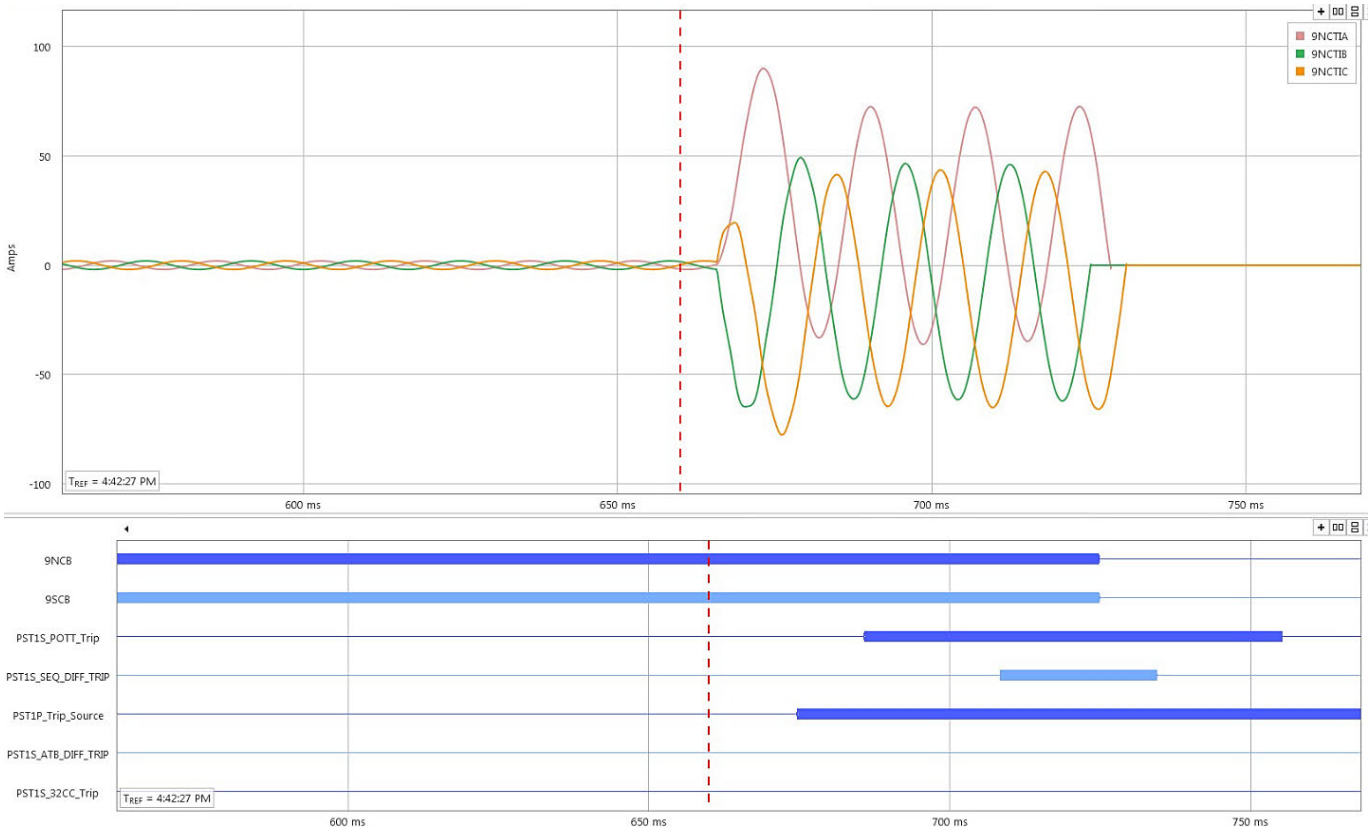


Fig. 15. Three-Phase Internal Fault at FLOC 1 Tap Neutral

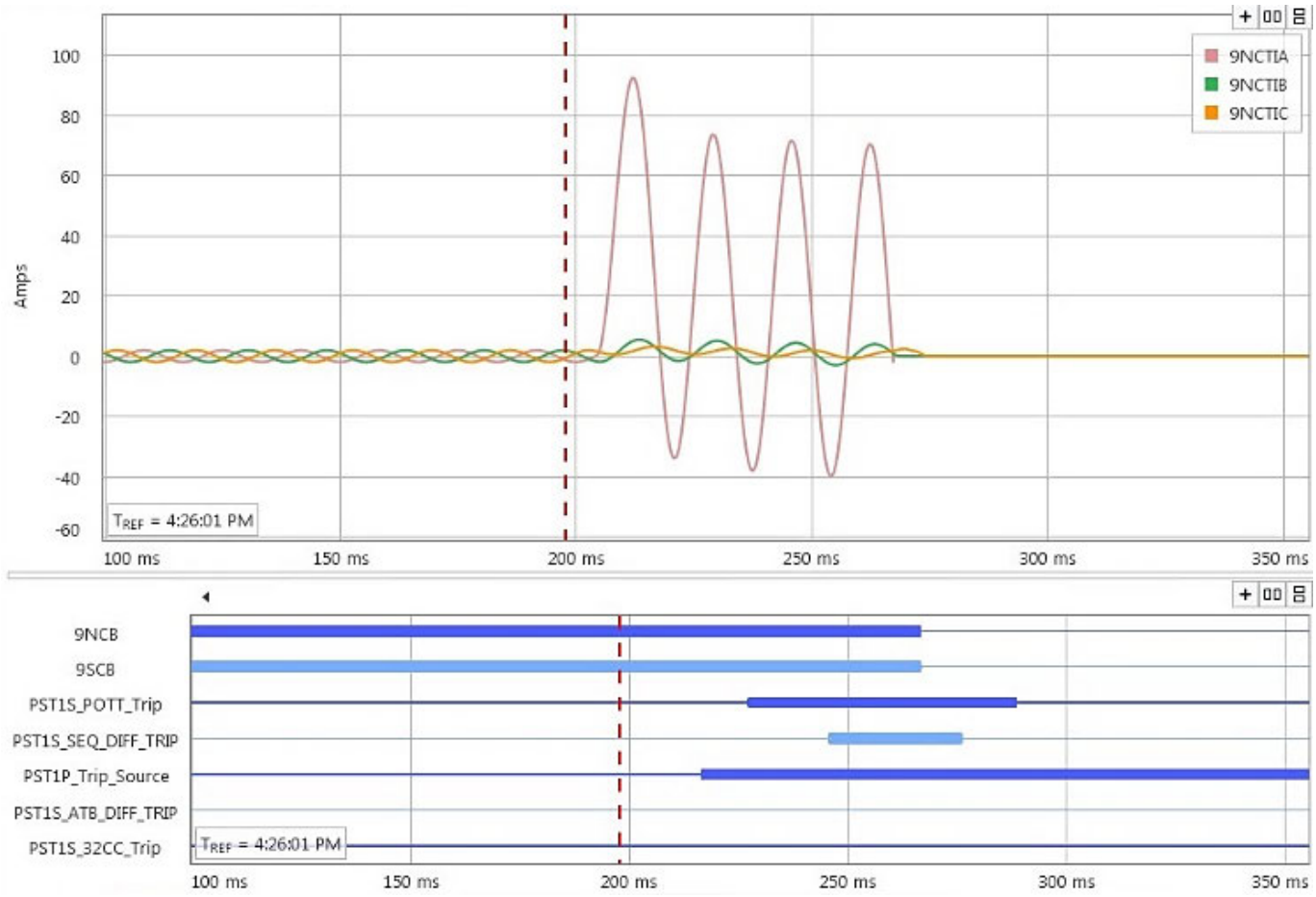


Fig. 16. Single-Phase Internal Fault at FLOC 1 Tap Neutral

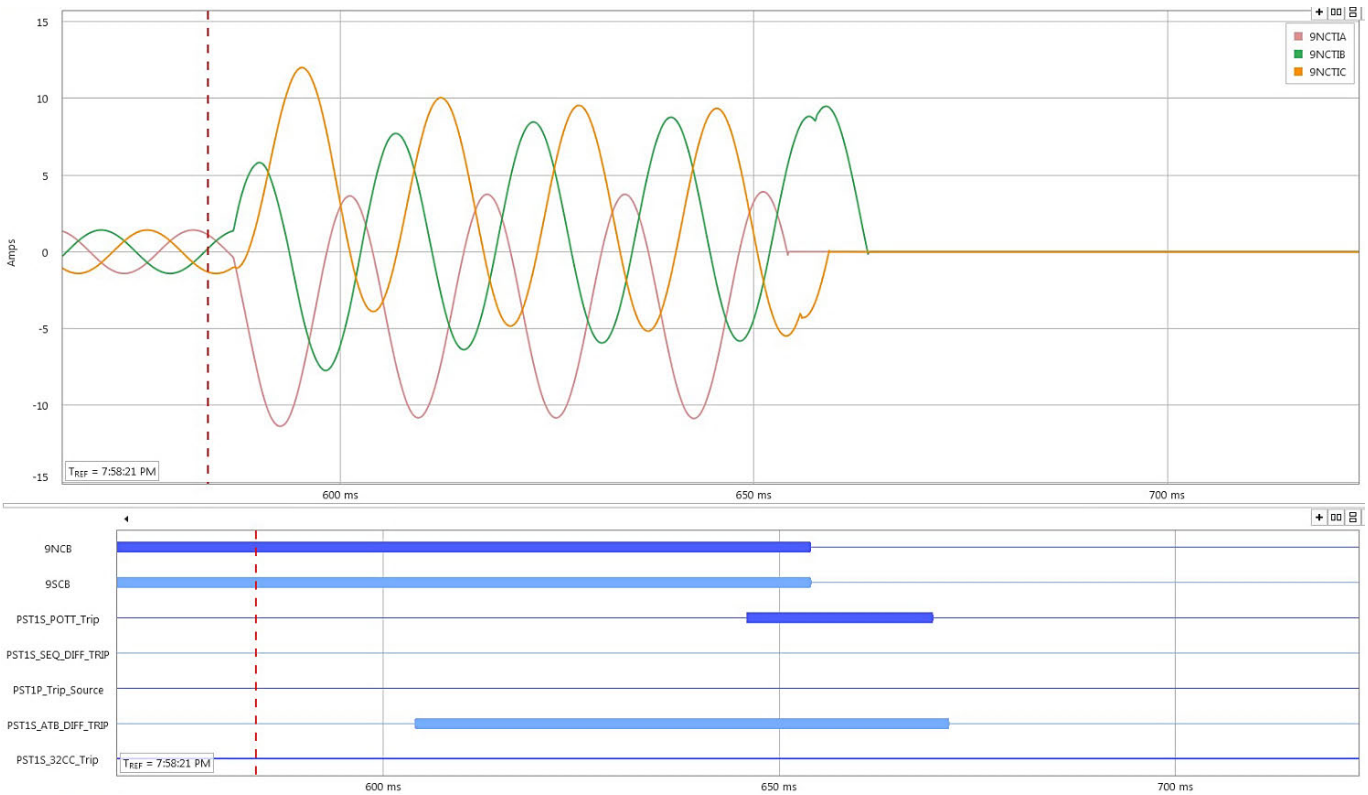


Fig. 17. Three-Phase Internal Fault at FLOC 2 Tap R10

TABLE I
REAL-TIME DIGITAL SIMULATOR TESTING RESULTS

Location	Description	87P	87S and 87O			Fault Type
		KCL	ATB	SEQ	POTT	
FLOC 1	Series Transformer Tap	Y	N	Y	Y	Internal
FLOC 2	Series Transformer Delta	N	Y	M	M	Internal
FLOC 3	Booster Winding Ground	N	M	M	M	Internal
FLOC 4	Turn-to-Turn	N	N	Y	Y	Internal
FLOC 5	Booster Turn-to-Turn	N	N	Y	Y	Internal
FLOC 6	Internal	Y	Y	Y	Y	Internal
FLOC 7	Internal	Y	Y	Y	Y	Internal
FLOC 8	IV Bus	NOP				External
FLOC 9	CFE Line/Bus	NOP				External

Table I shows the results for various faults. The 87P relay provides the PST zone with KCL bus-type differential protection to the primary windings on the series and excitation cores. Hence, the 87P relay can detect faults at FLOC 1, FLOC 6, and FLOC 7, but it cannot detect faults on the secondary windings of the series and excitation cores and turn-to-turn faults.

The 87S/87O relay detects faults in the secondary of the series and excitation windings based on ATB, SEQ, and POTT schemes. For example, the ATB scheme can detect faults at FLOC 2, FLOC 6, and FLOC 7, but it is not sensitive to turn-to-turn faults at FLOC 4 and FLOC 5. The ATB differential scheme is also blind to faults at FLOC 1 at the series transformer primary winding tap point because a fault in the throat between the two transformers is not detected by the ATB balance on the series transformer core. SEQ elements are more sensitive to turn-to-turn faults and booster winding faults. Hence, the PST protection selected for this project can detect all the faults as shown in Table I using multiple detection principles:

- Y – Sure operation
- N – No operation
- M – Maybe in some cases
- NOP – External fault case, no operation

The SCADA master was set up to communicate with both PST controllers to verify controller operation. The system operation was verified for Manual, Automatic, and CAISO modes. Custom applications (i.e., N-1 overloading, Master/Follower, independent, and run to neutral) and other features were verified for this PST. Also verified were the breaker close permissive logic, bypassing the PST when not in neutral, and 32CC circulating current logic. Through detailed testing and verification of all operations of protection and control, a subset of the tests was created for field testing and commissioning.

VI. OPERATIONS TRAINING CLASS

A two-day training class was held in October 2016 at the P&C engineering consultant's lab. In attendance were relay technicians, substation transformer electricians, engineers, and NERC-certified operator trainers. Participants were taught the basics of PST operation and the particulars of the Imperial Valley PST project. The project team shared the real-time digital simulator protection results and demonstrated the protective relay interface including displays and target LEDs. In addition, the team demonstrated the operation of the PST controllers and made the controller displays and target LEDs available for hands-on training.

VII. COMMISSIONING AND FIELD RESULTS

The FAT and real-time digital simulator testing included detailed procedures for the protection scheme and controller in the lab facility. A detailed functional test plan was developed for all control and protection functions prior to energization. The goals of this testing were:

- Verify wiring to and from the PSTs and associated circuit breakers.
- Verify PST LTC control settings with PST LTC motors and contactors.
- Operate the PST LTCs over their full range, from +16 advance to –48 retard tap positions.
- Perform testing using switching sequences from the proposed standard practice.
- Verify local/SCADA and automatic/manual functionality, proving CAISO set-point control.
- Verify Master/Follower control.
- Perform SCADA point-to-point testing, proving all SCADA controls, statuses, and metering.
- Provide field training on local controls, displays, LED targets, and indications.
- Provide system operator training for SCADA controls and indications.
- Develop Sequence of Events (SOE) recording data to document PST operation.

Testing was conducted the week before the May 1, 2017, energization, which took place after all the wiring was completed. A subset of the lab testing during the FAT was used for onsite commissioning. One of the purposes of field testing was to determine the motor running time for each tap-position change and verify operation at each tap position. The motor running time is dependent upon design and cannot be determined only from a lab test.

Using CAISO mode, SCADA commands were issued to verify the PST operation from tap positions +16 advance to –48 retard. A run-to-neutral test was also performed. To verify this operation, a run-to-neutral command was issued from tap positions –5 retard and +5 advance. This testing was helpful in validating the run-to-neutral command and verifying the operation of BCD inputs with actual tap positions on the PST

controller. This testing was performed in both Master/Follower and Independent modes.

A. Field Results – Tap-Change Process

Data from both PST controllers were recorded for analysis and future reference. For each tap-position operation, relay data analysis indicated that BCD inputs used for tap-position calculations disappeared 0.4 seconds after the motor started and reappeared 2.9 seconds after the motor started. The motor completed the run in 3.5 seconds. It was observed during testing that the motor ran for ~3.5 seconds for each tap change. See Fig. 18 for the details of this operation. When passing though the neutral, the motor runs three times with 0.9 seconds between each start and stop. The motor runs ~14–15 seconds. In addition, Fig. 19 shows that the PST is moving from –1 retard to the neutral to +1 advance. For simplicity, only the main Sequential Events Recorder (SER) variables are shown.

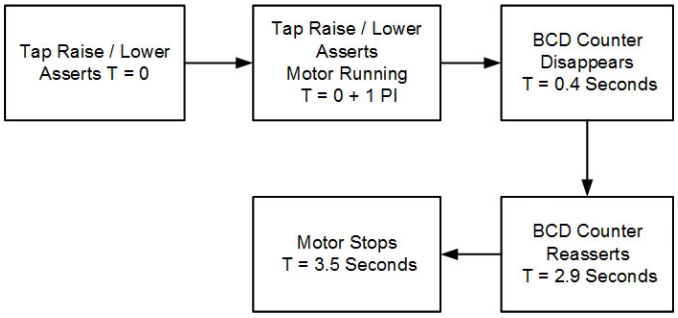
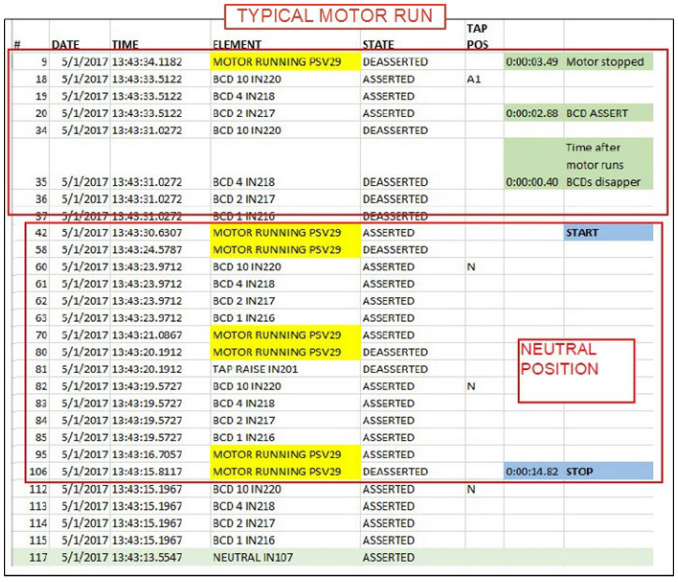


Fig. 18. PST Typical Tap-Change Operation Timing Diagram



#	DATE	TIME	ELEMENT	STATE	TAP POS		
9	5/1/2017	13:43:34.1182	MOTOR RUNNING PSV29	DEASSERTED		0:00:03.49	Motor stopped
18	5/1/2017	13:43:33.5122	BCD 10 IN220	ASSERTED	A1		
19	5/1/2017	13:43:33.5122	BCD 4 IN218	ASSERTED			
20	5/1/2017	13:43:33.5122	BCD 2 IN217	ASSERTED		0:00:02.88	BCD ASSERT
34	5/1/2017	13:43:31.0272	BCD 10 IN220	DEASSERTED			
							Time after motor runs
35	5/1/2017	13:43:31.0272	BCD 4 IN218	DEASSERTED		0:00:00.40	BCDs disapper
36	5/1/2017	13:43:31.0272	BCD 2 IN217	DEASSERTED			
37	5/1/2017	13:43:31.0272	BCD 1 IN216	DEASSERTED			
42	5/1/2017	13:43:30.6307	MOTOR RUNNING PSV29	ASSERTED			START
58	5/1/2017	13:43:24.5787	MOTOR RUNNING PSV29	DEASSERTED			
60	5/1/2017	13:43:23.9712	BCD 10 IN220	ASSERTED	N		
61	5/1/2017	13:43:23.9712	BCD 4 IN218	ASSERTED			
62	5/1/2017	13:43:23.9712	BCD 2 IN217	ASSERTED			
63	5/1/2017	13:43:23.9712	BCD 1 IN216	ASSERTED			
70	5/1/2017	13:43:21.0867	MOTOR RUNNING PSV29	ASSERTED			
80	5/1/2017	13:43:20.1912	MOTOR RUNNING PSV29	DEASSERTED			
81	5/1/2017	13:43:20.1912	TAP RAISE IN201	DEASSERTED			
82	5/1/2017	13:43:19.5727	BCD 10 IN220	ASSERTED	N		
83	5/1/2017	13:43:19.5727	BCD 4 IN218	ASSERTED			
84	5/1/2017	13:43:19.5727	BCD 2 IN217	ASSERTED			
85	5/1/2017	13:43:19.5727	BCD 1 IN216	ASSERTED			
95	5/1/2017	13:43:16.7057	MOTOR RUNNING PSV29	ASSERTED			
106	5/1/2017	13:43:15.8117	MOTOR RUNNING PSV29	DEASSERTED		0:00:14.82	STOP
112	5/1/2017	13:43:15.1967	BCD 10 IN220	ASSERTED	N		
113	5/1/2017	13:43:15.1967	BCD 4 IN218	ASSERTED			
114	5/1/2017	13:43:15.1967	BCD 2 IN217	ASSERTED			
115	5/1/2017	13:43:15.1967	BCD 1 IN216	ASSERTED			
117	5/1/2017	13:43:13.5547	NEUTRAL IN107	ASSERTED			

Fig. 19. SER Data for PST Typical Tap-Change Operation From R1 to A1

B. Commissioning Procedure and In-Service Tests

Grid operations and the P&C engineering consultant collaborated to develop the switching required for in-service testing when the PSTs were energized. For each in-service test, the operate and restraint currents were checked and the events were saved. The team agreed to complete the following tests:

1. Parallel PST 1 and PST 2 and set combined loading at approximately 170 MW. Complete in-service testing on PST 1 and PST 2.
2. Advance tap on PST 1 to +1, and retard PST 2 one tap position to –1. Complete in-service testing, including a circulating apparent power measurement. Check the circulating current against the calculated value.
3. Open PST 2, placing all load on PST 1. Complete in-service testing on PST 1.
4. Move PST 1 to neutral tap, close bypass, open PST 1, move PST 2 to neutral tap, and open bypass. Then, move PST 2 tap to match PST 1 tap from Step 3. Complete in-service testing on PST 2.
5. Move PST 2 to neutral tap, close bypass, close PST 1, and open bypass. Advance tap on PST 1 to +1, and retard PST 2 one tap position to –1. Complete in-service testing, including a circulating current measurement. As done in Step 2, check the circulating current against the calculated value.
6. Verify the compensation using inrush current. During the field testing, validate compensation and magnitudes during first energization and loading conditions.

The team developed calculations for commissioning to determine the 87P and 87S/87O relay currents for operation at +6 advance tap with 160 MW flow. These calculations were based on the loading allowed by CAISO when the PST was loaded for the first time. The I_{SOLO} primary current was calculated for the 87P relay at 84 A; the excitation winding primary current was 896 A. Fig. 20 shows the details and calculations for 160 MW loading and flows in the 87P, 87S, and 87O relays.

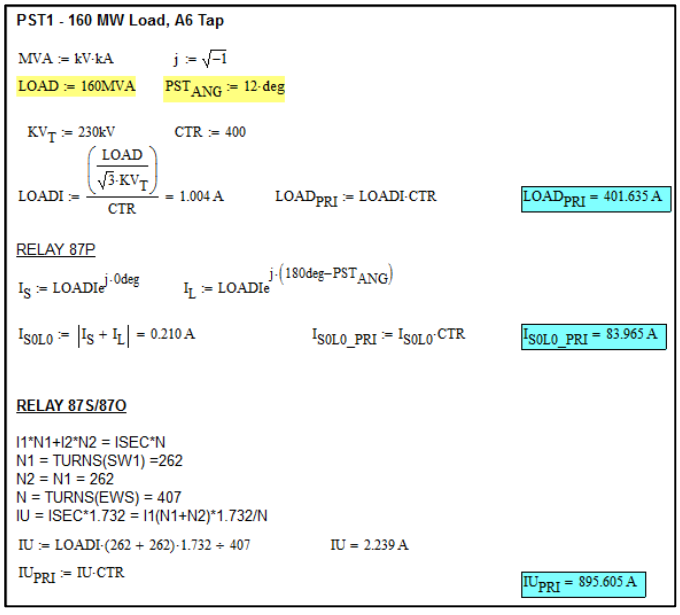


Fig. 20. PST1 160 MW Loading and 87P and 87S Relay Calculations

C. In-Service Compensation Verification

A compensation matrix is critical for the 87S and 87O relay settings. The compensation matrix for the source terminal current (I_S) is defined by $I_A = I_B - I_C$. This is equivalent to compensation Matrix 9 (i.e., counterclockwise [CCW] 30 • 9 = 270 degrees for ABC phase rotation). Load terminal current (I_T) is defined by $I_A = I_C - I_B$. This is equivalent to compensation

Matrix 3 (i.e., CCW 30 • 3 = 90 degrees for ABC phase rotation) [7].

Fig. 21 shows the current magnitudes and angle before compensation for the 87S and 87O relays. Once the compensation matrix is applied for both source and load, the results indicate that AT balance is maintained. In addition, the current magnitudes for 160 MW match the calculations performed as shown in Fig. 20. Fig. 22 shows the current after compensation for source and load currents (exciter transformer primary) and excitation transformer secondary current on the U-winding. The operate current is very low with high-restraint current, hence the compensation is correct.

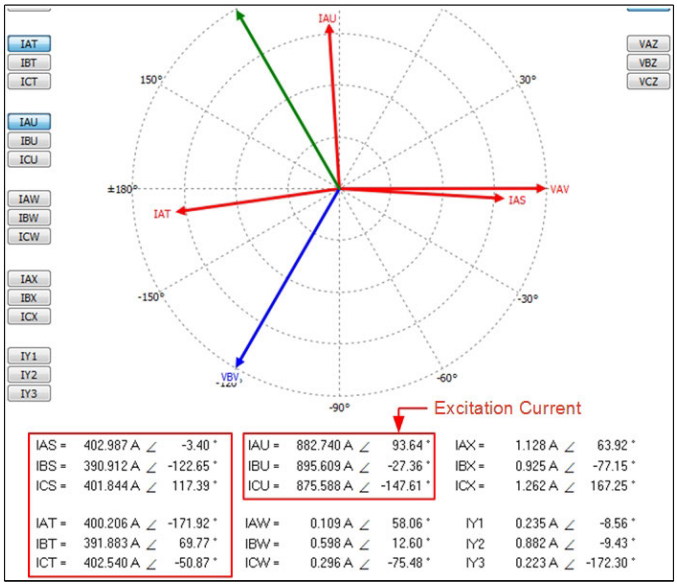


Fig. 21. 160 MW, 87S and 87O Relays Phasors Uncompensated

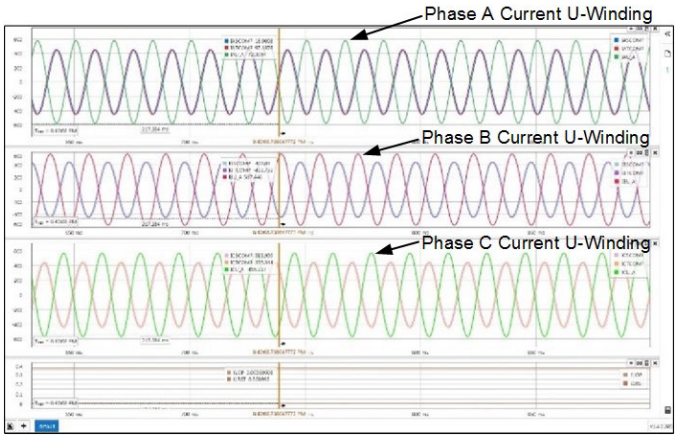


Fig. 22. PST2 87S and 87O Relays Phasors and Compensation

The **met dif** command is shown in Fig. 23. Hence, there is no operate current and high-restraint current. This verification was done during commissioning for the 87P, 87S, and 87O relays during no-load and load conditions.

```
=>met dif

SEC DIFF 87-PST1S                          Date: 05/01/2017  Time: 20:39:29.253
IV Substation-PST1                         Serial Number: 1161930713


Operate Currents (per unit)        Restraint Currents (per unit)
IOPA      IOPB      IOPC           IRTA      IRTB      IRTC
 0.00      0.00      0.00           0.36      0.37      0.35
```

Fig. 23. **met dif** Command for PST

It is clear from Fig. 24 that the Phase A and Phase B CT currents are rolled (not wired correctly). The transformer differential operated and declared this to be an internal fault. Once the CT connections are corrected for Phase A and Phase B, the in-service test determined that the operate current is low with high-restraint current. Because all the logic was already tested and carefully validated during the FAT, the team was confident in the settings and logic. Hence, the commissioning team was able to troubleshoot and determine the root cause of this misoperation very quickly by using the oscillography and event records from the relays.

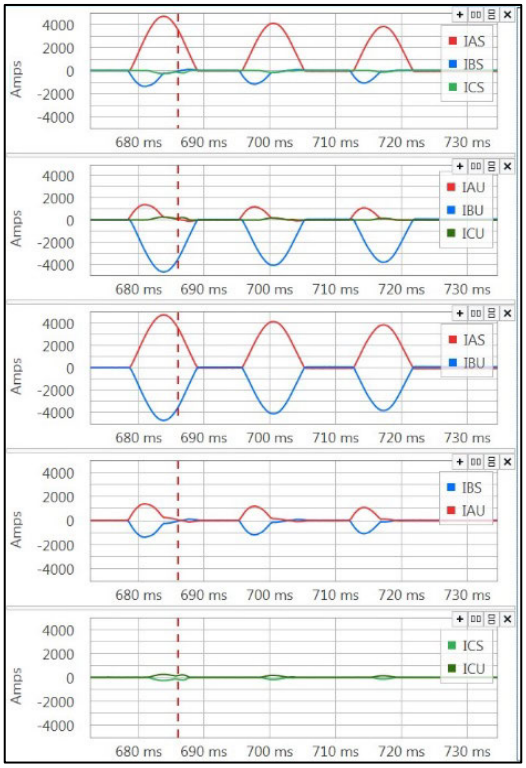


Fig. 24. PST1 87P Relay Incorrect CT Wiring

D. PST Operation and Lessons Learned

Several months after placing the PSTs in service, a PST LTC tap change failed due to a tripped LTC motor breaker on one of the PSTs. The PST controllers operated properly to block additional tap changes and initiated a circulating current alarm because the PST tap positions were one step apart. The SER data were valuable in allowing analysis of the failed tap change compared to normal tap changes from the original data. The team was able to see the motor breaker trip indication, and they knew that the motor breaker did not trip due to controller action. This same event occurred several more times over three months.

Ultimately, the LTC manufacturer made a site visit and provided control circuit additions to provide additional monitoring of the LTC control circuit.

VIII. Conclusion

PST control and protection schemes require a thorough understanding of PST design for successful implementation. Correct design practices and coordination among multiple teams over the design period were critical. During the course of this project, design changes were made to the utility operating standards and requirements of the controller design. Real-time digital simulator testing and a FAT procedure helped utility engineers witness and verify the design and provide feedback. Hence, the design was verified and finalized in a lab environment, which helped in the commissioning. The commissioning was short and limited to only critical tests as needed for the field verification. Any misoperation was troubleshot very quickly, as the team had 100 percent confidence in logic and settings after the detailed FAT.

In summary, the team feels the following actions are key to the verification of PST control and protection systems:

1. Identify control and protection solutions early in project implementation.
2. Assemble a design and verification team to vet and review project design requirements.
3. Review the design from the early stages to ensure the electrical design flows properly.
4. Identify special project design needs to customize the standard design based upon utility operating requirements.
5. Develop detailed control and protection logic.
6. Model PSTs and the transmission system for simulator model development.
7. Incorporate PST factory test data in the simulator model.
8. Conduct a FAT to prove control and protection logic, sharing results with utility engineers.
9. Conduct training for technicians, electricians, engineers, and trainers using a simulator lab setup.
10. Fine-tune the logic and relay settings based on simulator results.
11. Develop detailed functional test plans to verify logic, settings, and field wiring.
12. Develop a startup plan to incorporate in-service testing needs during energizing and loading of the PSTs.
13. Document and save controller and protective relay SER files for future reference.

IX. Acknowledgments

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XI. Biographies

Bill Cook is the Project Manager – Grid Operations at San Diego Gas & Electric (SDG&E). Bill started his career at SDG&E in 1976 as an engineer in the SDG&E Control Center. He moved to the field in 1982, working in the Substation and System Protection groups. He moved to the manager position in System Protection and Control Engineering in 1997. In 2014, he moved to his present position in Grid Operations. Bill earned his B.S.E.E. from California Polytechnic State University in San Luis Obispo. He is a registered professional engineer in California and a member of IEEE. He has been a member of the WECC Remedial Action Scheme Reliability Subcommittee (RASRS) since 1999.

Michael J. Thompson received his B.S., magna cum laude, from Bradley University in 1981 and an M.B.A. from Eastern Illinois University in 1991. Upon graduating, he served nearly 15 years at Central Illinois Public Service (now AMEREN). Prior to joining Schweitzer Engineering Laboratories, Inc. (SEL) in 2001, he was involved in the development of several numerical protective relays while working at Basler Electric. He is presently a Fellow Engineer with SEL Engineering Services, Inc. He is a senior member of the IEEE, member of the IEEE PES Power System Relaying and Control Committee, past chairman of the Substation Protection Subcommittee of the PSRCC, and received the Standards Medallion from the IEEE Standards Association in 2016. Michael is a registered professional engineer in six jurisdictions, was a contributor to the reference book, *Modern Solutions for the Protection Control and Monitoring of Electric Power Systems*, has published numerous technical papers and magazine articles, and holds three patents associated with power system protection and control.

Kamal Garg received his M.S.E.E. from Florida International University and India Institute of Technology, Roorkee, India, and his B.S.E.E. from Kamla Nehru Institute of Technology, Avadh University, India. Kamal worked for POWERGRID India and Black & Veatch for several years at various positions before joining Schweitzer Engineering Laboratories, Inc. (SEL) in 2006. Presently, he is a senior protection engineer at SEL Engineering Services, Inc. Kamal has experience in protection system design, system planning, substation design, operation, remedial action schemes, synchrophasors, testing, and maintenance. Kamal is a licensed professional engineer in the U.S. and Canada and a member of IEEE.

Milind Malichkar received his M.S.E.E. from Michigan Technological University in 2012 and his B.S.E.E. from Sardar Patel College of Engineering, Mumbai University, India, in 2005. Milind worked for Voltas limited (IOBG), India, and Electromechanical Technical Associates (ETA), Abu Dhabi, UAE, as a project engineer for five years before joining Schweitzer Engineering Laboratories, Inc. (SEL) in 2012. Presently he is a protection engineering supervisor at SEL Engineering Services Inc. Milind has experience in power system protection design, short-circuit and coordination studies, and power system modeling and testing using control and power hardware-in-the-loop (HIL) testing with a Real Time Digital Simulator (RTDS). Milind is a licensed professional engineer in the states of Washington and California and a member of IEEE.

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Conference for Protective Relay Engineers.

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