Directional Elements – How Fast Can They Be?

Armando Guzmán, Mangapathirao V. Mynam, Veselin Skendzic, and Jean León Eternod
Schweitzer Engineering Laboratories, Inc.

Rafael Martínez Morales
Comisión Federal de Electricidad

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***Abstract*—Directional comparison schemes provide dependable and secure power line protection. Directional elements are at the heart of directional comparison schemes. Voltage-polarized directional elements require voltages and currents to declare forward or reverse fault conditions. Typically, coupling capacitor voltage transformers (CCVTs) supply voltage signals to directional elements in transmission line protection applications. Recently, traveling wave-based (TW-based) directional elements have been introduced into line protective relays. Because of their construction, CCVTs present challenges to these TW-based directional elements. This paper shows that TW-based directional elements can work with CCVTs by relying on the stray capacitances of the tuning reactor and step-down transformer. In this paper, we use field events captured during forward and reverse faults to analyze the performance of a permissive overreaching transfer trip scheme that combines incremental-quantity and TW-based directional elements for achieving end-to-end scheme operating times on the order of 4 to 6 ms.**

I. Introduction

Directional elements are fundamental building blocks of many protection elements and schemes. Voltage-polarized directional elements require voltages and currents to declare forward or reverse fault conditions. Recently, traveling wave-based (TW-based) directional elements have been introduced and implemented in line relays. Typically, coupling capacitor voltage transformers (CCVTs) supply voltage signals to directional elements in transmission line protection applications. Because of their construction, CCVTs present challenges to TW-based directional elements. Ideal CCVTs do not pass signal components in the TW frequency range (tens to hundreds of kilohertz). However, TW-based directional elements can work with CCVTs by relying on the stray capacitances of the tuning reactor (interturn capacitances) and step-down transformer (interwinding capacitance) for their operation. These capacitances are difficult to quantify when creating power system models to simulate power system transients and analyze directional element performance. New protective relay technologies allow us to record signals from actual system faults at megahertz sampling rates. With this information, we can analyze the performance of protection schemes based on elements that use incremental quantities and TWs.

This paper presents a communications-based protection scheme that uses incremental-quantity and TW-based directional elements to make tripping decisions where CCVTs provide voltage signals to these elements. In this scheme, forward, overreaching, TW-based and incremental-quantity directional elements activate the transmission of a permissive trip signal to the remote end of the line. At the remote end, forward, overreaching, phase incremental quantity directional elements supervise the received permissive trip signal. The proposed scheme takes advantage of the fast TW-based elements, which operate within 150 µs, to speed up the trip decision and takes advantage of the incremental-quantity elements to provide security to the scheme. Additionally, the incremental-quantity elements provide phase selection for single-pole tripping (SPT) applications.

We use field events captured during forward and reverse faults to analyze the performance of the proposed permissive overreaching transfer trip (POTT) scheme, which achieves end-to-end operating times on the order of 4 to 6 ms.

II. Directional Element Principles

Directional elements are key to the reliability and speed of communications-based protection schemes in power line applications. For example, in POTT schemes [1], forward directional elements at the local terminal send a permissive signal to the remote terminal of the line where forward directional elements supervise the received permissive signal before tripping the line breaker. Traditional microprocessor-based relays form directional element characteristics from sequence-component measurements and incremental quantities using phasor information [2] [3] [4].

A. Negative-Sequence Directional Element

Negative-sequence directional elements detect all unbalanced faults and have the advantage of being insensitive to zero-sequence mutual coupling. Reference [2] describes a negative-sequence directional element that explicitly calculates the z_2 scalar value and compares this value with forward and reverse thresholds to make the fault direction declaration. This directional element uses (1) to calculate z_2.

$$z_2 = \frac{\mathrm{Re}[V_2 \bullet (1\angle\theta_{L1} \bullet I_2)^*]}{|I_2|^2} \quad (1)$$

where:

V_2 is the negative-sequence voltage (volts).

I_2 is the negative-sequence current (amperes).

θ_{L1} is the positive-sequence line impedance angle (degrees).

Equation (1) can also be expressed as follows:

$$z_2 = \frac{|V_2|}{|I_2|} \bullet \cos(\theta_{V2} - \theta_{I2} - \theta_{L1}) \quad (2)$$

For a homogeneous network, this equation becomes:

$$z_2 = \frac{|V_2|}{|I_2|} \tag{3}$$

Fig. 1 shows the negative-sequence network for unbalanced faults at two locations in a two-source system. In Fig. 1a, the fault is at the end of the protected line (a forward fault); in Fig. 1b, the fault is behind the relay (a reverse fault). Table I shows the V_2 and I_2 quantities that the relay measures for the two faults and the corresponding results of the z_2 calculation with the assumption that the system is homogeneous.

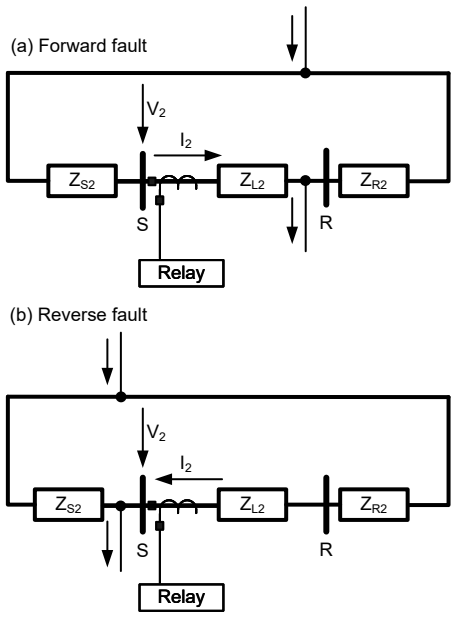

Fig. 1. Negative-sequence voltage and current for (a) forward and (b) reverse unbalanced faults.

TABLE I
MEASURED NEGATIVE-SEQUENCE QUANTITIES AND z_2 CALCULATION RESULTS FOR FORWARD AND REVERSE FAULTS IN A HOMOGENEOUS SYSTEM

Unbalanced Fault	$V_{2\_MEASURED}$	$I_{2\_MEASURED}$	z_2
Forward	$-I_2 \bullet Z_{S2}$	I_2	$-\lvert Z_{S2}\rvert$
Reverse	$-I_2 \bullet (Z_{R2} + Z_{L2})$	$-I_2$	$\lvert Z_{R2} + Z_{L2}\rvert$

In Fig. 1 and Table I, Z_{S2} is the negative-sequence source impedance at local Terminal S (Ω), Z_{R2} is the negative-sequence source impedance at remote Terminal R (Ω), and Z_{L2} is the negative-sequence line impedance (Ω).

The negative-sequence directional element declares a forward fault condition if z_2 is less than a predetermined forward threshold. The element declares a reverse fault condition if z_2 is greater than a predetermined reverse threshold.

B. Zero-Sequence Directional Element

The zero-sequence directional element detects ground faults and complements the negative-sequence directional element in power system operating conditions where there is not enough negative-sequence current for the negative-sequence element to operate [3] [5] [6]. This zero-sequence directional element uses (5) to calculate the z_0 scalar value.

$$z_0 = \frac{\mathrm{Re}[3V_0 \bullet (1\angle\theta_{L0} \bullet 3I_0)^*]}{|3I_0|^2} \tag{4}$$

where:

V_0 is the zero-sequence voltage (volts).

I_0 is the zero-sequence current (amperes).

θ_{L0} is the zero-sequence line impedance angle (degrees).

The calculation results for this directional element are similar to the results shown in Table I but with zero-sequence quantities instead.

C. Phase Directional Element Based on Incremental Phasors

The phasor-based incremental-quantity directional element uses data windows of less than one cycle (e.g., half a cycle) to achieve secure, high-speed tripping. This directional element supervises distance elements and identifies the fault type, which is used to provide phase selection in SPT applications. In one implementation [7] [8], the directional element algorithm calculates three incremental torques to determine the fault direction and the faulted phases, as shown in (6), (7), and (8).

$$\Delta T_{AB} = \mathrm{Re}\left[\Delta V_{AB} \bullet \left(1\angle\theta_{L1} \bullet \Delta I_{AB}\right)^*\right] \tag{5}$$

$$\Delta T_{BC} = \mathrm{Re}\left[\Delta V_{BC} \bullet \left(1\angle\theta_{L1} \bullet \Delta I_{BC}\right)^*\right] \tag{6}$$

$$\Delta T_{CA} = \mathrm{Re}\left[\Delta V_{CA} \bullet \left(1\angle\theta_{L1} \bullet \Delta I_{CA}\right)^*\right] \tag{7}$$

where:

ΔV_{AB}, ΔV_{BC}, and ΔV_{CA} are incremental, phase-to-phase voltages calculated as changes with respect to two-cycle-old values.

ΔI_{AB}, ΔI_{BC}, and ΔI_{CA} are incremental, phase-to-phase currents.

This directional element uses the sign of the torques to establish the fault direction and uses the relative values of these torques to select the fault type. This element operates in less than one cycle for close-in faults and in about one cycle for typical fault conditions.

III. TIME-DOMAIN DIRECTIONAL ELEMENT PRINCIPLES

Advancements in data acquisition and data processing allow for the development of ultra-high-speed (UHS) time-domain directional elements that are faster than the phasor-based directional elements described in Section II. Next, we present the operating principles of these time-domain directional elements, which are part of a fast and secure communications-based protection scheme.

A. Incremental-Quantity Directional Element

UHS time-domain line protective relays include incremental quantity-based directional elements that use instantaneous values of voltages and currents. This type of element is called TD32 in one implementation [9]; this element provides fast, secure, and dependable directional indication [10]. This directional element is part of a POTT scheme, and it supervises

distance elements. It uses signals with frequency content on the order of hundreds of hertz.

1) Operating Principle

Consider the single-phase RL network in Fig. 2 with a fault on the line between Terminal S and Terminal R.

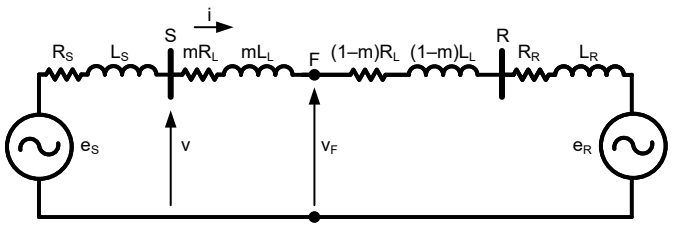

Fig. 2. Two-source single-phase system with a fault at F.

We use Thévenin's theorem together with the principle of superposition to solve the faulted network. We solve it by analyzing the prefault network to obtain the prefault (load) components of the voltages and currents and analyzing the fault network shown in Fig. 3 to obtain the fault-generated components of these voltages and currents. It is important to note that, in the fault network, the driving voltage source Δv_F is at the fault location, and the magnitude of this voltage source is equal and opposite to the prefault voltage at the fault location.

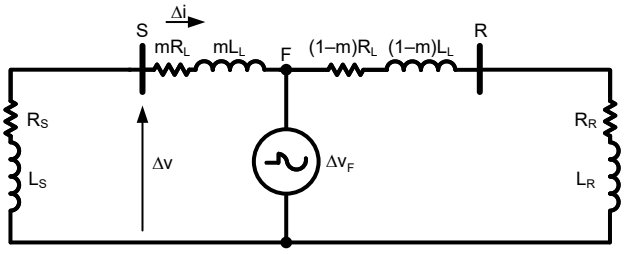

Fig. 3. Fault network of the Fig. 2 system for a fault on the line between Terminal S and Terminal R (a forward fault for a relay at Terminal S).

Because the fault signals are sums of the prefault signals and the fault-generated signals, the fault-generated signals are the differences between the fault signals and the prefault signals. Relays measure the fault signals directly—these are the instantaneous voltages and currents at the relay terminals. Relays also measure the prefault signals and can extrapolate them forward in time. This extrapolation is valid only for a few tens of milliseconds because the power system sources only remain stationary for a short period of time. Therefore, we simply use (8) and (9) to derive voltage and current incremental quantities.

$$\Delta v(t) = v(t) - v(t - T) \tag{8}$$

$$\Delta i(t) = i(t) - i(t - T) \tag{9}$$

where:

Δv is the instantaneous incremental voltage.

Δi is the instantaneous incremental current.

T is the period of the measured quantity.

At the relay location (Terminal S), the incremental voltage and current are related by a voltage drop equation across the Source S resistance and inductance, as is shown in (11).

$$\Delta v = -\left(R_S \bullet \Delta i + L_S \bullet \frac{d}{dt} \Delta i \right) \tag{10}$$

where:

R_S is the resistance of Source S.

L_S is the inductance of Source S.

We scale (10) for ease of further use by multiplying and dividing the right-hand side of the equation by the magnitude of the Source S impedance Z_S [11]:

$$\Delta v = -|Z_S| \left(\frac{R_S}{|Z_S|} \bullet \Delta i + \frac{L_S}{|Z_S|} \bullet \frac{d}{dt} \Delta i \right) \tag{11}$$

We can do this operation without loss of generality because we scale (10) with a scalar to obtain (11). We then simplify (11) using the replica current Δi_Z, which is a combination of the instantaneous incremental current and its derivative. We represent this incremental replica current as follows:

$$\Delta i_Z = D_{0S} \bullet \Delta i + D_{1S} \bullet \frac{d}{dt} \Delta i \tag{12}$$

where:

$$D_{0S} = \frac{R_S}{|Z_S|} \text{ and } D_{1S} = \frac{L_S}{|Z_S|} \tag{13}$$

Now, we can write (15) to determine the incremental voltage measured at Terminal S for a forward event.

$$\Delta v = -|Z_S| \bullet \Delta i_Z \tag{14}$$

Note that (14) is identical to (3), which ties the negative-sequence voltage and current at the relay location for a forward fault.

For reverse faults, we place the Δv_F source behind Terminal S, as Fig. 4 shows. Equation (16) provides the incremental voltage measured at Terminal S for reverse faults.

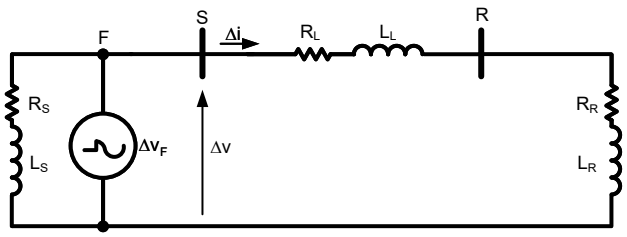

Fig. 4. Fault network of the Fig. 2 system for a fault behind Terminal S (a reverse fault for a relay at Terminal S).

$$\Delta v = |Z_L + Z_R| \bullet \Delta i_Z \tag{15}$$

where:

Z_L is the line impedance.

Z_R is the Source R impedance.

Like (14), (15) is identical to its counterpart equation for the negative-sequence voltage and current. Ideally, the replica current used in (15) is calculated as follows:

$$\Delta i_Z = D_{0R} \bullet \Delta i + D_{1R} \bullet \frac{d}{dt}\Delta i \tag{16}$$

where:

$$D_{0R} = \frac{R_L + R_R}{|Z_L + Z_R|} \text{ and } D_{1R} = \frac{L_L + L_R}{|Z_L + Z_R|} \tag{17}$$

For homogeneous systems where the angles of the local and remote source impedances and the angle of the line impedance are the same, the D_0 and D_1 parameters of the replica current can be represented as follows:

$$D_0 = \frac{R_L}{|Z_L|} = \cos(\theta_L) \text{ and } D_1 = \frac{L_L \bullet \omega}{|Z_L| \bullet \omega} = \frac{\sin(\theta_L)}{\omega} \tag{18}$$

Practical TD32 element implementation uses the line angle θ_L to derive the replica current Δi_Z. This is no different than using the line angle as the maximum torque angle in sequence or phase directional elements.

We conclude that the incremental voltage and the incremental replica current have similar waveforms, their relative polarities indicate the fault direction, and their amplitude relationship depends on the system impedances and the fault direction.

The directional element calculations were implemented for six loops (three phase-to-ground loops and three phase-to-phase loops). Table II shows the incremental loop voltages and currents.

TABLE II
LOOP VOLTAGES AND CURRENTS IN THE TIME DOMAIN

Loop	Voltage	Current
AG	Δv_A	$\Delta i_{AZ} - \Delta i_{0Z}$
BG	Δv_B	$\Delta i_{BZ} - \Delta i_{0Z}$
CG	Δv_C	$\Delta i_{CZ} - \Delta i_{0Z}$
AB	$\Delta v_A - \Delta v_B$	$\Delta i_{AZ} - \Delta i_{BZ}$
BC	$\Delta v_B - \Delta v_C$	$\Delta i_{BZ} - \Delta i_{CZ}$
CA	$\Delta v_C - \Delta v_A$	$\Delta i_{CZ} - \Delta i_{AZ}$

Notice that the loop voltages and currents are similar to those of distance elements. In particular, the ground loop incremental currents are similar to $I_\phi + k_0 \bullet I_0$ in the phasor domain implementation, where ϕ = A, B, and C, and k_0 is the zero-sequence compensation factor [11].

We base the directional element on the product of the instantaneous incremental voltage and the instantaneous incremental replica current, which we call torque as it is referred to for electromechanical relays (see Fig. 5). We apply adaptive restraints for the operating torque using the concept of threshold impedances [2]. The TD32 element calculates the operating torque using a sign-inverted voltage so that the operating torque is positive for forward events. This element uses a positive restraining torque to check the forward direction and a negative restraining torque to check the reverse direction. The two restraining torques are equal to the product of the squared loop replica current and the corresponding threshold impedance magnitudes (TD32ZF for the forward threshold and TD32ZR for the reverse threshold).

The TD32 element integrates the operating and restraining torques. The integrators in this element are controlled by the starting logic as shown in Fig. 5. The restraining torques are integrated as soon as a disturbance is detected and as long as the incremental quantities are valid. To achieve security, the operating torque for any given protection measurement loop is integrated only if that loop was ready to operate prior to the disturbance and if the corresponding phase was involved in the fault.

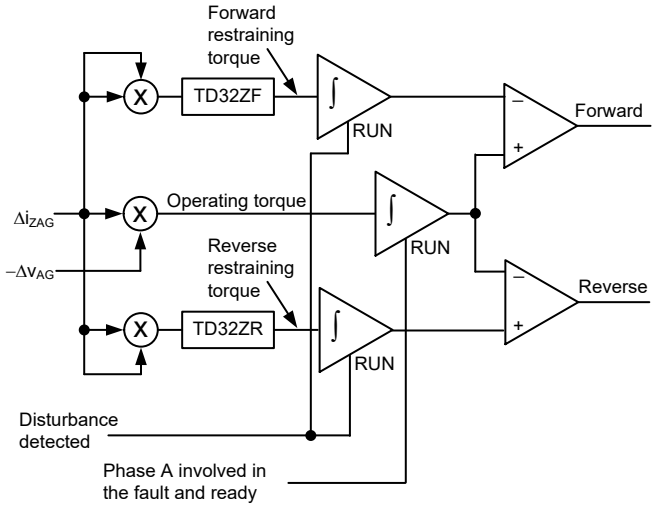

Fig. 5. Simplified logic of the TD32 element for the Phase-A-to-ground (AG) loop.

The TD32 element declares a forward event if the integrated (accumulated) operating torque is positive and greater than the integrated forward restraining torque. The TD32 element declares a reverse event if the integrated operating torque is negative and greater—in terms of an absolute value—than the integrated reverse restraining torque. This operating principle is very similar to that of the negative-sequence directional element. We can therefore rewrite (1) as follows:

$$\text{Re}[V_2 \bullet (1\angle\theta_{L1} \bullet I_2)^*] > z_2 \bullet |I_2|^2 \tag{19}$$

The left-hand side of the equation represents the operating torque, and the right-hand side represents the restraining torque. Substituting z_2 with the forward and reverse thresholds and applying the greater than (>) or less than (<) signs accordingly, we obtain the forward and reverse outputs of the negative-sequence element. Comparing this approach with the TD32 logic shown in Fig. 5 reveals the similarities between the two approaches.

The outputs of the Fig. 5 logic diagram are supervised by sensitive incremental-quantity overcurrent elements and are conditioned according to the fault type for their application in the proposed POTT scheme.

2) *Performance of the TD32 Element for a Forward Fault*

Fig. 6 shows the incremental voltage and incremental replica current for a Phase-C-to-ground (CG) fault in the forward direction recorded in the field on a 400 kV line. As expected, the polarities of the incremental voltage and the incremental replica current are opposite, and the TD32 element declared the event as forward.

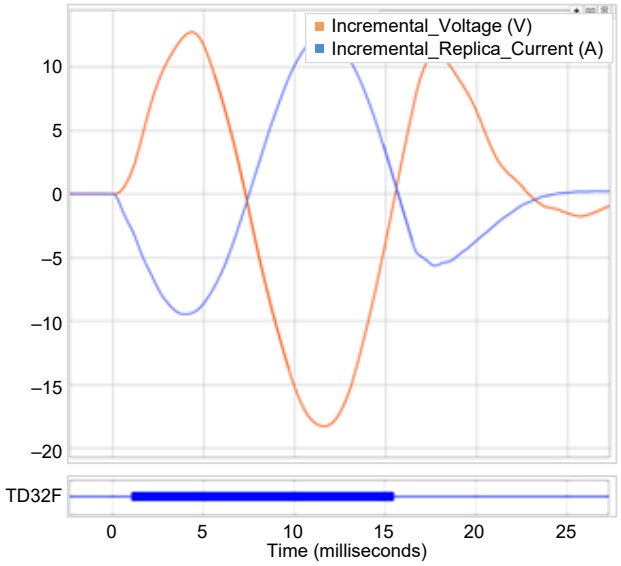

Fig. 6. The incremental voltage and incremental replica current have opposite polarities. Hence, the TD32 element declares the event as forward.

Fig. 7 shows the operating torque, the forward restraining torque, and the reverse restraining torque, as well as the forward directional element output. As expected for this forward event, the accumulated operating torque associated with the faulted phase is greater than the accumulated forward restraining torque.

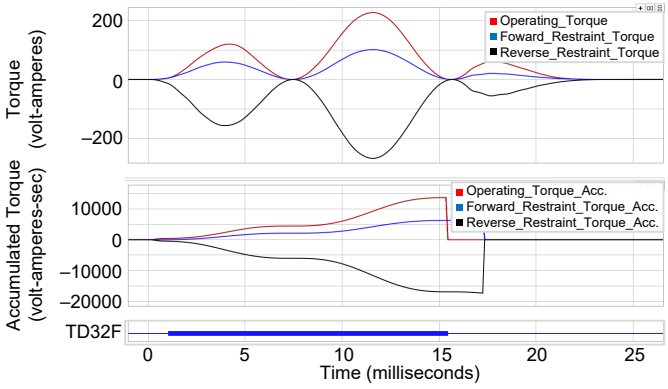

Fig. 7. The TD32 element declares the forward event when the accumulated operating torque is greater than the accumulated forward restraining torque.

B. *TW-Based Directional Element*

TW-based directional elements that acquire voltage and current signals at megahertz rates have greater bandwidth requirements for CTs and CCVTs than phasor-based directional elements. Wide bandwidth allows for considerable improvements in the operating speeds of these elements [11]. Dommel et al. [12] and Johns [13] proposed TW-based directional elements that require high-fidelity voltage measurements that are not available in typical substations. However, in most cases, CCVTs can measure the first voltage TW (because of the interwinding capacitance across the step-down transformer and the interturn capacitances across the tuning reactor of the CCVT). This allows for a new type of TW-based directional element (called TW32) that takes advantage of the information in the first voltage and current TWs; this new element acquires voltage signals from conventional CCVTs. The following are the implementation details of this element [10] [14]. In this implementation, we use a differentiator smoother filter to extract TWs from the raw voltages and currents [15].

1) *Operating Principle*

The TW32 element uses phase voltage and current TWs and calculates the product of the current TW and the sign-inverted voltage TW (so that the product is positive for forward events) for each phase, as shown in Fig. 8. Then, the element integrates this product over time to obtain the energy associated with the first TW. For security, the logic of the TW32 element enables the integrator only if the voltage and current TWs are above their corresponding minimum levels. The logic checks the output of the integrator after the TW32WD timer expires. The integration lasts only for a few tens of microseconds because the TW32 element is designed to respond only to the first TWs. Fig. 9 shows that the energy calculation is positive for a forward fault and negative for a reverse fault.

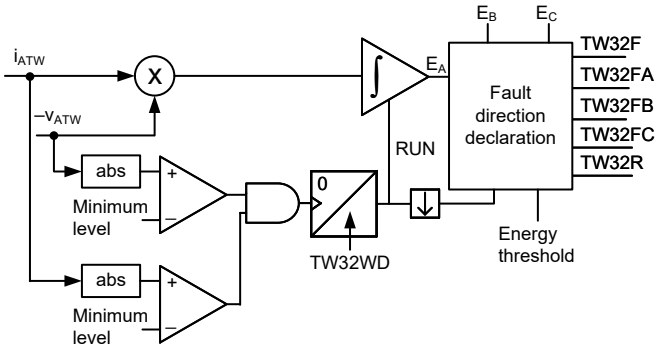

Fig. 8. Simplified logic of the TW32 element.

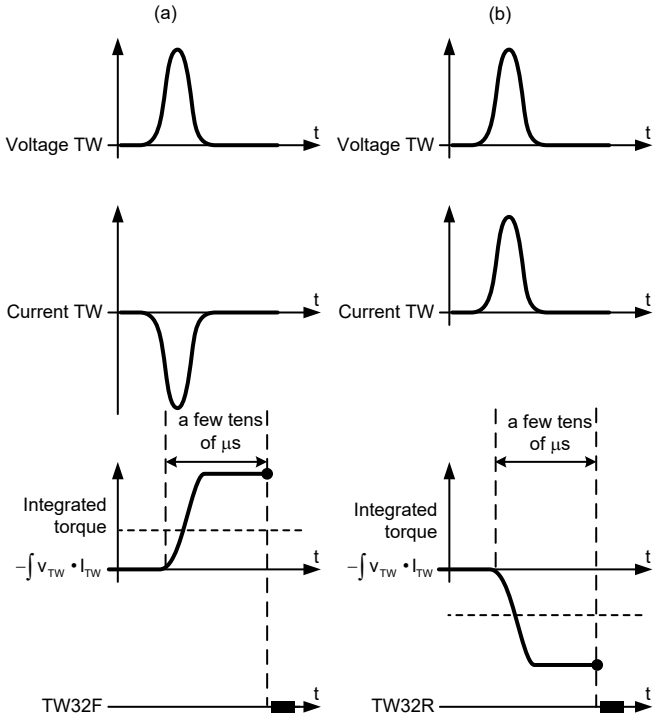

Fig. 9. Voltage and current TWs and the resulting integrated torques for (a) forward and (b) reverse faults.

TWs associated with a line fault can arrive at the relay location from the fault and from the network elements behind the relay. Each TW coming from the line direction integrates up, and each TW coming from behind the relay integrates down. The first TW is higher in magnitude than the subsequent reflections. As a result, we have confidence that the integrated value is a reliable indication of the fault direction even as multiple reflected TWs are integrated over the time period TW32WD, such as is the case when the fault or the discontinuities behind the relay are located very close to the relay.

When the TW32WD timer expires, the integration is complete (see Fig. 8). At the falling edge of the timer, the fault direction declaration logic uses the accumulated values of the per-phase TW energies (E_A, E_B, and E_C) for determining if the event is in the forward or reverse direction. The energy must exceed the security threshold, ENRGYTH, for the logic to assert the forward or reverse bit. The TW32 logic determines which are the maximum and minimum energy values (ENRGYMX and ENRGYMN, respectively) from among the three per-phase energy values (E_A, E_B, and E_C). The element declares a forward event or fault by asserting the TW32F bit if the following conditions are met:

- |ENRGYMX| > |ENRGYMN|
- ENRGYMX > ENRGYTH

The element declares a reverse event or fault by asserting the TW32R bit if the following conditions are met:

- |ENRGYMN| >= |ENRGYMX|
- ENRGYMN < –ENRGYTH

The logic asserts the phase-segregated forward elements (TW32FA, TW32FB, or TW32FC) based on which phase energy value corresponds to the ENRGYMX value. This way, the logic provides sufficient fault phase identification for single-phase-to-ground faults. This logic identifies one of the faulted phases for multiphase faults.

In one implementation of the TW32 element [9], the voltage and current signals that feed the logic in Fig. 8 are acquired at 1 MHz, while the logic runs at 10 kHz. The operating time of this element is on the order of 150 μs or less.

The TW32 element may not assert for faults near the voltage zero-crossing, for high-resistance faults where the change in voltage is small, or with some CCVTs that have limited bandwidth. The TD32 element ensures dependability under these operating conditions.

2) *Performance of the TW32 Element on Double-Circuit Lines*

TWs couple to the unfaulted circuit for faults on double-circuit lines (especially for parallel lines that share the same tower structures) because of the mutual coupling of the two circuits. For this reason, the behavior of TW functions on double-circuit lines is of key interest to protection engineers.

Fig. 10 shows the TW phase currents and voltages for an AG fault on the faulted circuit (right) and on the unfaulted circuit (left) of a double-circuit line. Note that the currents measured at the terminals of the two circuits are superimposed signals of the incident TW, the reflected TW, and the transmitted TW from the other circuit [16]. TW currents recorded on the unfaulted circuit are dominantly ground mode (all the phase currents are of the same polarity; this mode is the zero-sequence mode). Because the two circuits are connected to the same bus, the voltage TWs recorded at the terminals are the same for both circuits. The plots in Fig. 10 illustrate that the TW current and voltage signals of the faulted phase are dominant and provide the necessary information to determine the fault direction in the unfaulted and faulted lines.

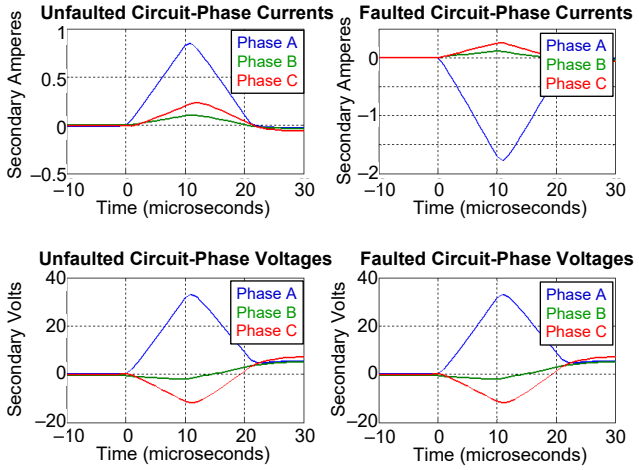

Fig. 10. Voltage and current TWs captured on a double-circuit line for an AG fault.

Next, we focus on the performance of the TW directional elements using the information from the captured TW phase currents and voltages for faults on double-circuit lines. As discussed in Section III, Subsection B.1, a TW directional element responds to the polarity of the voltage and current TW signals. The TW32 element declares a forward event if the

polarities of the voltage and current TWs are opposite, and it declares a reverse event if the polarities of the voltage and current TWs are the same. In this design, the TW32 element determines which directional element output bit to assert based on the phase associated with the maximum energy. For single-phase-to-ground faults, the directional element output follows the decision according to the faulted phase. For multiphase faults, the TW32 element output follows the decision according to one of the faulted phases (the phase associated with the maximum energy), and it relies on the outputs of the TD32 element for selecting the other phases.

To illustrate the performance of time-domain directional elements, we simulated a 500 kV power system with a double-circuit line (two three-phase circuits sharing the same tower structure) using an electromagnetic transients program (EMTP) (see Fig. 11). We played back data from the simulation through the algorithms presented in Section III, Subsections A.1 and B.1. We used scaled primary signals for this analysis.

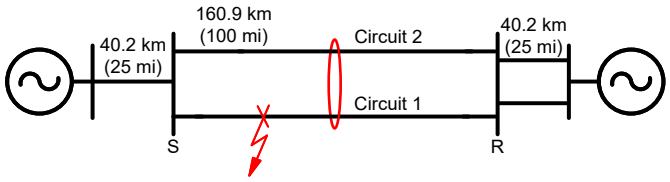

Fig. 11. An AG fault simulated on Circuit 1.

We applied an AG fault 48.28 km (30 mi) from Terminal S on Circuit 1. Fig. 12 shows the phase voltages and currents captured at Terminal S of Circuit 2 along with the directional element response. Fig. 13 shows the TW Phase A voltage and current on Circuit 2. As previously discussed, the TW phase voltage and current have the same polarities. Therefore, the TW32 element declared the event as reverse. Note that the TD32 element also declared the event as reverse at Terminal S.

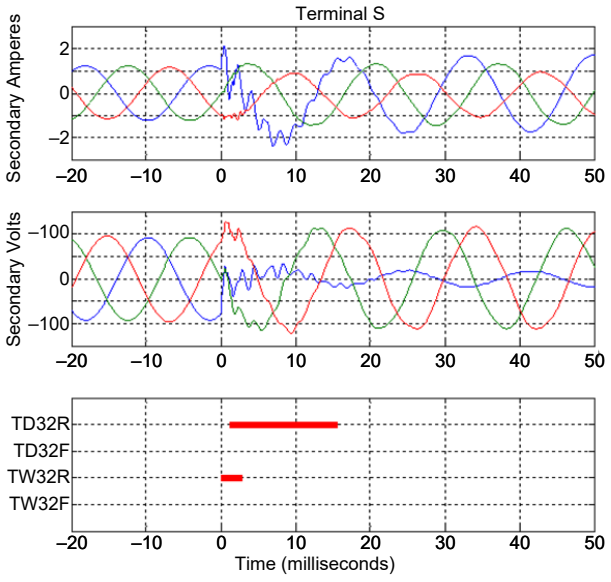

Fig. 12. The time-domain directional elements (TD32 and TW32) on the unfaulted circuit declared the fault shown in Fig. 11 as reverse at Terminal S.

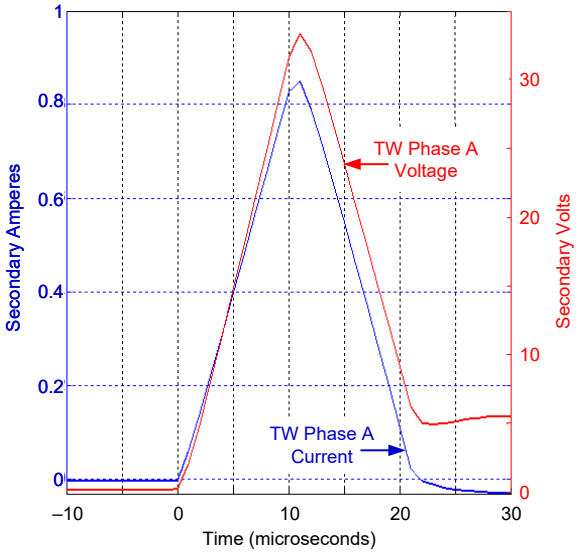

Fig. 13. The TW phase voltage and current of Circuit 2 at Terminal S have the same polarity for the fault shown in Fig. 11.

Fig. 14 shows the phase voltages and currents captured at Terminal R of Circuit 2 along with the directional element response. Fig. 15 shows the TW Phase A voltage and current on Circuit 2. As previously discussed, the TW phase voltage and current have the same polarity. Therefore, the TW32 element declared the event as reverse. However, note that the TD32 element declared the event as forward at Terminal R.

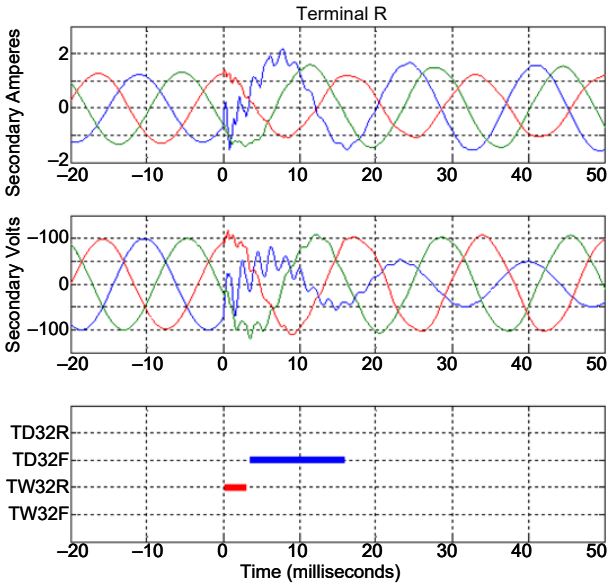

Fig. 14. The TW directional element declared the fault shown in Fig. 11 as reverse at Terminal R.

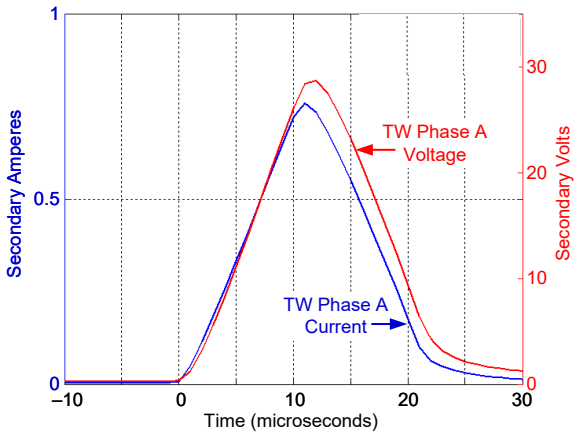

Fig. 15. The TW phase voltage and current of Circuit 2 at Terminal R have the same polarity for the fault shown in Fig. 11.

In our example, the TW32 elements declared the event as reverse on the unfaulted circuit at both terminals; therefore, the TW32 element is secure for this fault condition.

The TD32 elements responded to the current flow during the fault. This is why one terminal declared a reverse fault and the opposite terminal declared a forward fault. This situation is not any different than the behavior of phasor-based directional elements.

IV. Fast and Secure POTT Scheme

In our implementation, the TW32 elements are fast and very sensitive for detecting events [9]. They can detect reactor and capacitor switching, nearby lightning, and other events that might compromise the security of the tripping scheme. The TD32 elements are not as fast as the TW32 elements, but they are very secure and dependable. How can we take advantage of the speed of the TW32 elements without sacrificing scheme security?

In this section, we describe a POTT scheme suitable for single- and three-pole tripping applications that uses the TW-based directional elements for speed, the incremental-quantity directional elements for reliability, and the incremental overcurrent elements for security.

The POTT scheme includes the following logic:

- *Key Transmitter Logic*. This logic sends a phase-segregated permissive signal to the remote line terminal when a forward event occurs.
- *Receiver Logic*. This logic compares the received permissive signal with the local directional element to provide trip permission.
- *Phase Selection and Tripping Logic*. This logic selects the phases to trip and trips the selected phases if there is a trip permission signal.

A. Key Transmitter Logic

The key transmitter logic activates phase-segregated transmission bits (KEYA, KEYB, and KEYC) to send a permissive signal indicating the presence of a forward event to the remote relay (see Fig. 16). The logic uses the phase-segregated forward directional elements TD32F and TW32F to assert the transmission bits. The TW32F element makes the directional declaration faster than the TD32F element, which typically results in speeding up the permissive signals by 1 to 3 ms.

Additionally, the POTT key logic asserts the TDRBA bit when the TD32 element detects the occurrence of a reverse event on Phase A in order to block the permissive signal transmission. If the reverse event indication lasts longer than a very short period of time (e.g., 2 ms), the TDRBA bit remains asserted after the TD32 reverse event indication de-asserts for an extra period of time (e.g., 80 ms). This extra delay is enough for the remote overreaching elements and communications channel to reset after the prior reverse fault clears, in case the reverse event is a fault.

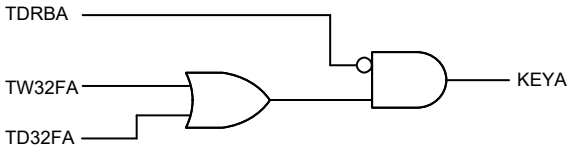

Fig. 16. Key transmitter logic for accelerating the POTT scheme.

B. Receiver Logic

The local relay receives the phase-segregated permissive bits (PTA, PTB, and PTC) through the communications channel. These signals are supervised by the TD32 forward indication but not by the TW32 forward indication. The permissive signals arrive after a channel delay, and at that time the TD32 elements are already asserted and the scheme does not need the TW32 acceleration. By not using the TW32 elements on the receiving end, the scheme is more secure. Phase-segregated directional overcurrent elements, through the use of the OCTPA, OCTPB, and OCTPC bits, supervise the POTT scheme permissive trip signal for security during switching operations, as Fig. 17 illustrates. The current reversal bits (TDRBA, TDRBB, and TDRBC) supervise the POTT scheme permissive trip signal for security during the clearing of a fault on a parallel line. The Phase A-supervised permissive bit PTRXA asserts if there is an overcurrent condition on Phase A and if the corresponding current reversal bit is not asserted.

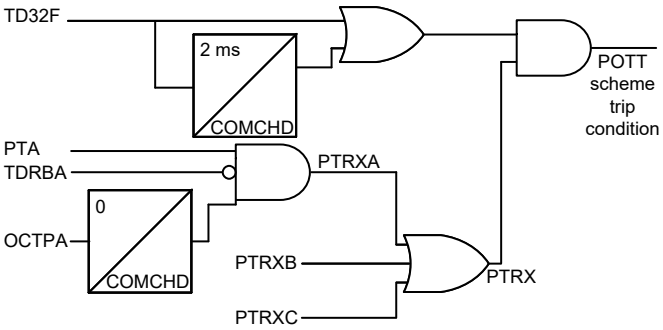

Fig. 17. Receiver logic provides security to the POTT scheme.

The receiver logic extends the assertion of the TD32F bit (the OR combination of TD32FA, TD32FB, and TD32FC) according to the communications channel delay timer COMCHD (e.g., 15 ms) to indicate the presence of a forward event. This extension ensures that the local forward event indication based on incremental quantities is present when the

remote trip permissive signal is received after the channel delay. The logic also extends the OCTPA, OCTPB, and OCTPC bits for the same reason. A POTT scheme trip condition is granted when at least one of the PTRX bits asserts and the local forward event indication TD32F is asserted.

C. Phase Selection and Tripping Logic

Fig. 18 shows the phase selection and tripping logic that executes the trip in Phase A, B, or C for single-phase faults or in all three phases for multiphase faults. The logic selects Phase A for tripping if the POTT scheme operates in Phase A, as signaled by the assertion of the permissive trip signal in Phase A (PTRXA) coinciding with the pickup of the TD32 forward element in Phase A (TD32FA). For multiphase faults, the TD32 element asserts the TD32F bits of all the phases. The logic executes trips in all phases if all the previously mentioned conditions are met. The trip seal-in and unlatch logic asserts the trip outputs TPA, TPB, and TPC while current is flowing through the corresponding pole of the breaker and a predefined time determines the minimum assertion time of the trip outputs (e.g., 200 ms).

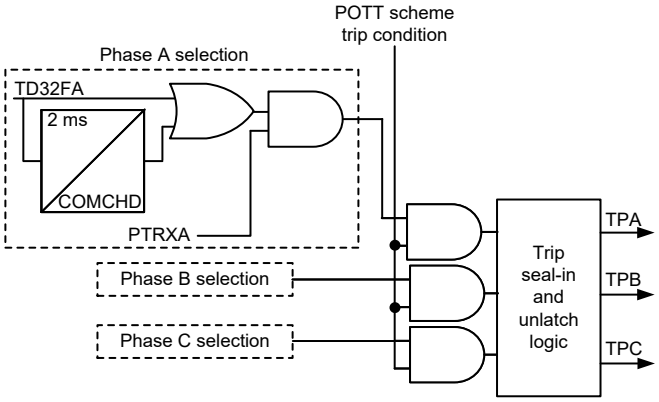

Fig. 18. Phase selection and trip logic for the POTT scheme.

In summary, the TW32 element speeds up keying of the permissive trip signal at the transmitting end if there is no current reversal condition. Note from the parallel line discussion that for external faults, both line ends assert the TW32 elements in the reverse direction and no key from the TW32 element is expected at all. At the receiving end, phase overcurrent elements supervise the permissive signal; a POTT scheme trip condition is granted if the TD32F bit is asserted and there is no current reversal condition. Per-phase tripping occurs when a POTT scheme trip condition exists and the corresponding phase has been selected for tripping. The logic selects a phase for tripping if the per-phase TD32F element and the corresponding PTRX bit coincide. Overall, the receiving end logic provides the necessary scheme security without slowing down the scheme operating time. The POTT scheme takes advantage of the communications channel delay. The very fast overcurrent and incremental-quantity directional elements have enough time to detect the fault condition by the time the permissive signal arrives at the terminal even when using a very fast teleprotection channel.

V. Instrument Transformers

Conventional iron-and-copper instrument transformers are designed to accurately measure the power system fundamental frequency signal components. Higher frequencies, such as fault-induced oscillations, are measured as well but may be attenuated. Attenuation depends on the instrument transformer design and cannot generally be predicted. Manufacturers give virtually no guarantee regarding instrument transformer frequency response above several kilohertz.

From an application point of view, it is desirable for the in-service voltage and current transformers to properly measure high-frequency signals, such as TWs, that occur on power transmission lines. Instrument transformers used to measure these TWs should preferably be used without modification and should take advantage of conventional wiring already installed in the yard. Conventional wiring is also optimized to carry fundamental frequency signals (50 or 60 Hz), further exacerbating the high-frequency measurement problem. Fortunately, as reported in [10], CTs measure signals over a wide frequency range (typically exceeding 100 kHz), while the CCVTs most often used in high-voltage applications rely on stray capacitances to bring the high-frequency signal components to the CCVT output terminals.

Simulation results presented in [10] document the instrument transformer behavior in detail. Regardless of the presented modeling results, engineers are always interested to gain an evidence-based grasp of the amount of high-frequency information provided by instrument transformers in real-life events. To shed some light on the problem, we take a more detailed look at the fault waveforms recorded by a UHS time-domain protective relay installed in the 400 kV series-compensated transmission line described in Section VI. On this line, a CG fault occurred 135 km (83.89 mi) from the measured terminal. The line is equipped with conventional CTs and CCVTs. Fault waveforms were captured using the recording capability (1 MHz/18 bits) of the UHS protective relay. Fig. 19 shows the current and voltage waveforms captured during the fault. Fig. 20 shows the fault initiation detail.

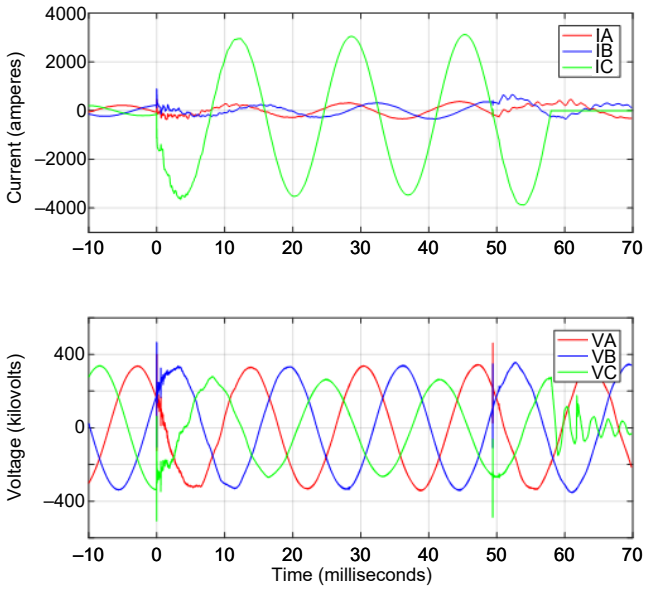

Fig. 19. Waveforms captured during a CG fault on a series-compensated 400 kV line.

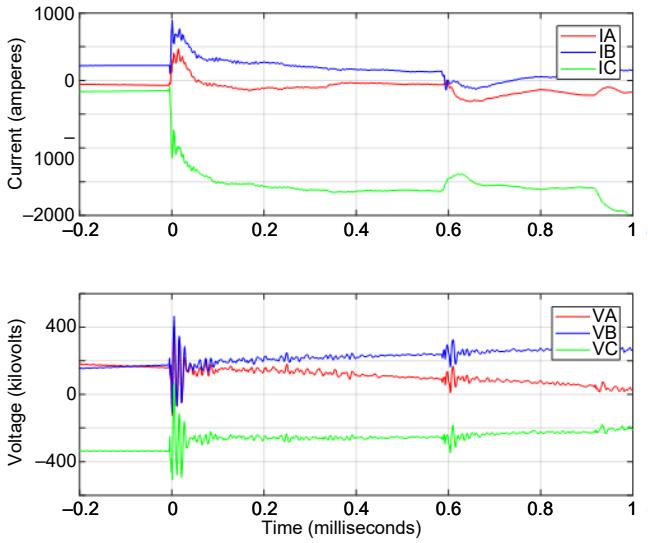

Fig. 20. Fault initiation detail showing the phase currents and the high-frequency voltage information supplied by the CCVTs.

A. Current Transformer (CT) Behavior

Looking at the CT time-domain waveforms shown in Fig. 20, we can see the arrival of the front of the TW (at the 0 ms mark) followed by a number of close-in reflections rippling right after the initial wave arrival. The second reflection from the fault arrives around the 0.6 ms mark; it is attenuated and appears to be clean with high-frequency content attenuated due to the distance traveled (three times 135 km [83.89 mi]). The reflection from the remote end of the line arrives around the 0.95 ms mark and is even more attenuated.

By using a short-window Fourier transform, we can investigate the evolution of the waveform spectral content over time. The analysis is performed by displaying a series of overlapped short-window (256 µs) Fourier transforms on a single graph with time shown on the horizontal axis and signal frequency shown on the vertical axis. Color is used to indicate signal strength.

The CT waveform spectral content is shown in Fig. 21. We can easily identify the fault inception instant marked with the spectral content that reaches up to 500 kHz. These results confirm the Fig. 20 time-domain waveform observations. The signal is clean and well-damped, confirming the CT ability to faithfully reproduce high-frequency signals.

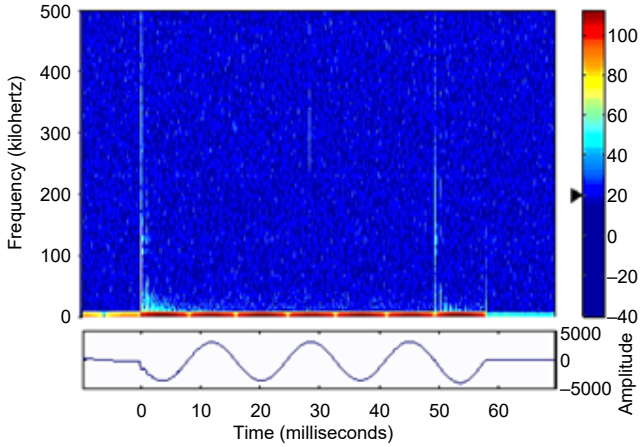

Fig. 21. Phase C (faulted phase) current waveform frequency content evolution over time.

B. Voltage Transformer Behavior

Contrary to the expectations based on the CCVT model, the voltage channel spectrogram shown in Fig. 22 is even richer in detail than the current spectrogram. The high-frequency information associated with the initial wave arrival reaches all the way out to 500 kHz, lasts longer, and is more pronounced than the current information. Correlating the spectral information with the CCVT waveform shown in Fig. 20, we see that the voltage signal delivered to the relay terminals is a much less faithful reproduction of the primary signal than the current signal. TW arrival time information (at the 0 ms mark) is preserved, but the front of the TW is obscured by the secondary cable resonance and cross-coupling between the phases. We can also see multiple power line carrier signals present on the neighboring lines.

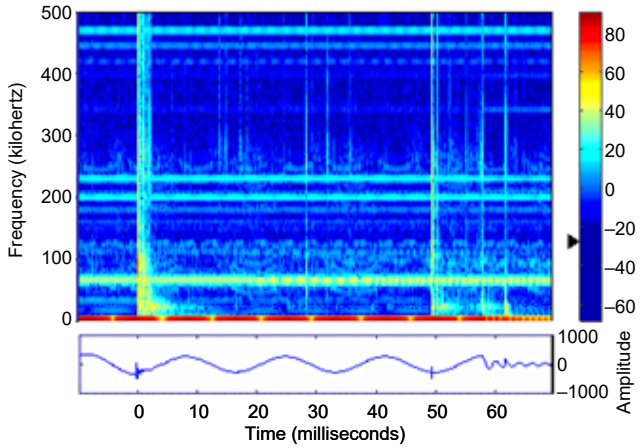

Fig. 22. Phase C (faulted phase) voltage waveform frequency content evolution over time.

There are multiple vertical lines indicating higher levels of cross-coupling from the substation control wires. Cross-

coupling is expected; it confirms the fact that voltage circuits are much easier to disturb than the CT-based current circuits.

As illustrated by the previous fault example, conventional instrument transformers can supply a wealth of high-frequency information to the secondary devices. TW arrival times are clearly identifiable for both current and voltage measurements. CTs provide faithful reproductions of the actual TW shapes, while the CCVT signals require additional processing and supervision when they are used to drive fast directional elements such as the TW32 element.

The extent to which the high-frequency information supplied by the instrument transformers is used varies depending on the relay element using it. For example, the TW32 element uses the current and voltage outputs of the differentiator smoother filter [11], thus eliminating most of the high-frequency (>100 kHz) chatter. Fig. 23 shows the filter frequency response.

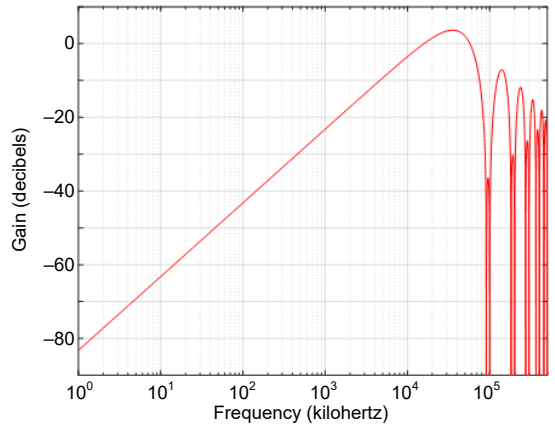

Fig. 23. Differentiator smoother filter frequency response.

Additionally, the TW32 element only responds to data measured in a window of a few tens of microseconds from the start of the event. Fig. 24 shows the TW phase voltage and current (obtained from the faulted phase) and the window of interest for the TW32 element.

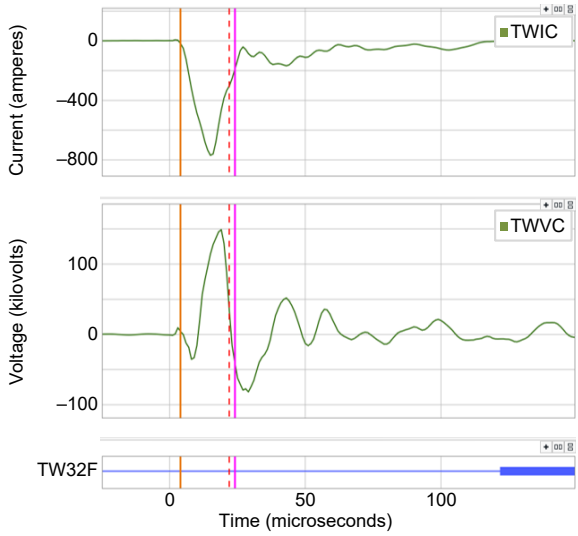

Fig. 24. TW phase current and voltage are of opposite polarities. Therefore, TW32 declared the event as forward.

The TW32 element design considers the behavior of CCVTs and is designed to provide speed to the POTT scheme. The POTT scheme is secured by using an incremental-quantity directional element decision at the receiving end.

VI. Field Experience

Comisión Federal de Electricidad (CFE), the electrical utility company of México, installed two relays that include the directional elements described in Section III, as well as an incremental quantity-based underreaching distance element, a TW-based differential element, and fault location functions. This field installation has the following purposes:

- Evaluate new time-domain protection principles that offer faster tripping times than traditional principles. High-speed tripping minimizes equipment damage, increases stability margins, and increases personnel and public safety.
- Evaluate the settings simplicity of relays that use time-domain principles [14].
- Analyze CCVT response to high-frequency signals.
- Evaluate the accuracy of the TW single-end fault locating method [16].
- Analyze high-resolution oscillography records and evaluate the possibility of using the recorded information for predictive maintenance of lines and other primary equipment.

In the past, CFE installed high-speed relays with time-domain incremental-quantity directional elements in several 400 kV series-compensated lines [17]. These relays provided high-speed performance, but they had some undesired operations and were eventually taken out of service after several years of operation. CFE decided to evaluate this new technology in a 400 kV series-compensated transmission line in a region with a high incidence of lightning events in order to verify the security of the new time-domain protection elements.

Fig. 25 shows the 223.8 km (139.1 mi) line that connects substations Minatitlán Dos (MID) and Temascal Dos (TMD). This line has series capacitors and a line reactor at the TMD terminal. There are two adjacent lines with series capacitors and one 300 MVAR static VAR compensator (SVC) at the TMD substation. The protection scheme should be able to perform single-pole tripping and reclosing. The network and protection requirements make this installation a challenging line protection application. During the first eight months of evaluation, the new time-domain relays have experienced four internal faults, two external faults, and several equipment switching events. The protection elements have been secure and dependable during the evaluation period.

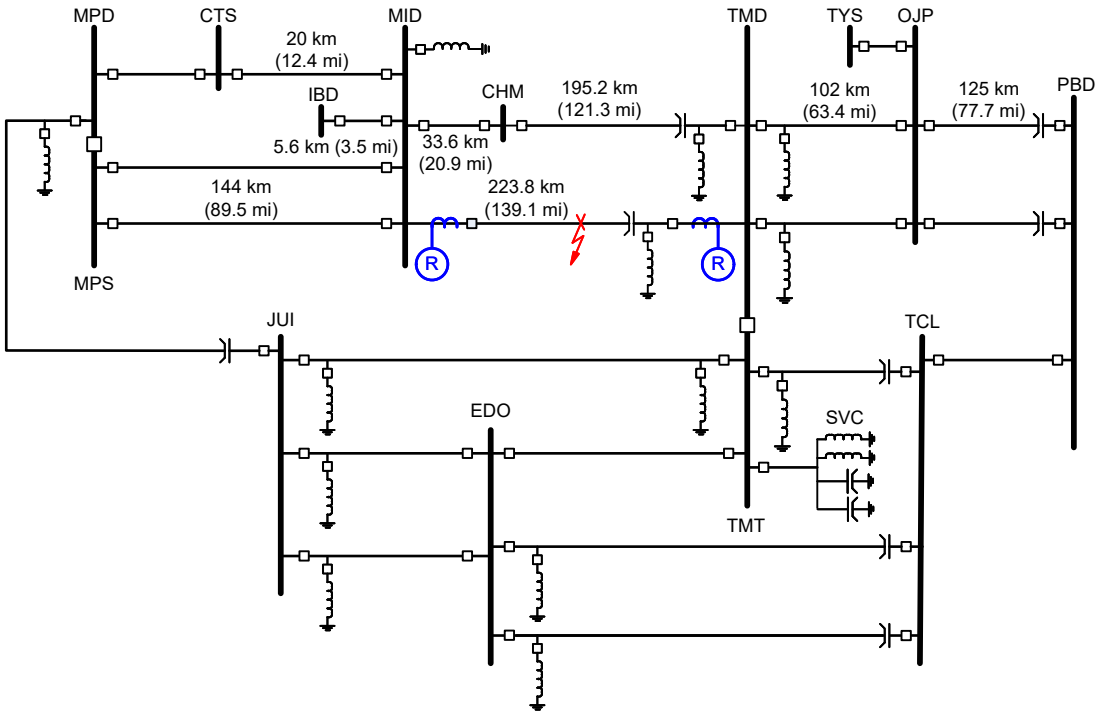

Fig. 25. Time-domain relays installed on the 400 kV line that connects the MID and TMD substations.

Table III in the appendix lists the records that the relays captured for the internal and external faults at the MID and TMD terminals. During the first five months of the evaluation, the relays were configured with very sensitive triggering elements to capture transient events. For this reason, the table does not include recordings from the two terminals because the records were overwritten with new events for some of the faults. The table includes the fault type, TD32 and TW32 operating times, and event observations. The details for each fault are as follows:

- *January 7, 2017 internal AG fault*. The TW32FA and TD32FA bits asserted in 138 µs and 1.2 ms, respectively, and keyed the communications channel at MID. The event at TMD was overwritten with transient events.
- *January 15, 2017 external AG fault*. For the fault behind TMD, the TD32RA bit asserted in 1.7 ms at TMD, and the TD32FA bit asserted in 1.9 ms at MID. The TW32 elements did not operate for this fault. Section VI, Subsection B provides additional information for this event.
- *January 16, 2017 external CG fault*. For the fault behind MID on the 115 kV network, the TD32RC bit asserted in 1.8 ms at MID, and the TW32FC bit did not assert at MID. The event at TMD was overwritten with transient events.
- *March 28, 2017 internal CG fault*. The TW32FC and TD32FC bits asserted in 106 µs and 1.39 ms, respectively, and keyed the communications channel at TMD. The event at MID was overwritten with transient events.
- *May 4, 2017 internal CG fault*. The TW32FC and TD32FC bits asserted in 105 µs and 1.1 ms, respectively, and keyed the communications channel at MID. The TD32FC bit asserted in 1.055 ms and keyed the communications channel at TMD. The TW32FA bit asserted instead of the TW32FC bit at TMD; this assertion did not compromise phase selectivity because the TD32FA bit at MID did not assert. Section VI, Subsection A provides additional information for this event.
- *August 23, 2017 internal AG fault*. The TD32FA bit asserted in 8.75 ms and keyed the communications channel at MID. The TD32FA bit asserted in 7.8 ms and keyed the communications channel at TMD. The TW32 elements did not operate for this fault because of the high fault resistance. The TD32 elements operated 9 ms faster than the conventional directional elements described in Section II.

A. May 4, 2017 Internal CG fault

Fig. 26 and Fig. 27 show the currents and voltages captured at MID and TMD and the time-domain protection element operation for the May 4 internal CG fault. We can observe the assertion of the TW32FC, TD32FC, and KEYC bits at MID and of the TW32FA, TD32FC, KEYA, and KEYC bits at TMD. Notice that the TW32FA bit asserts at TMD but the TD32FA bit does not assert at MID; therefore, the assertion of the TW32FA bit does not compromise the scheme security. The plots also show the assertion of the TD21CG bits at both terminals. The TD21 element is the time-domain underreaching distance element described in [11].

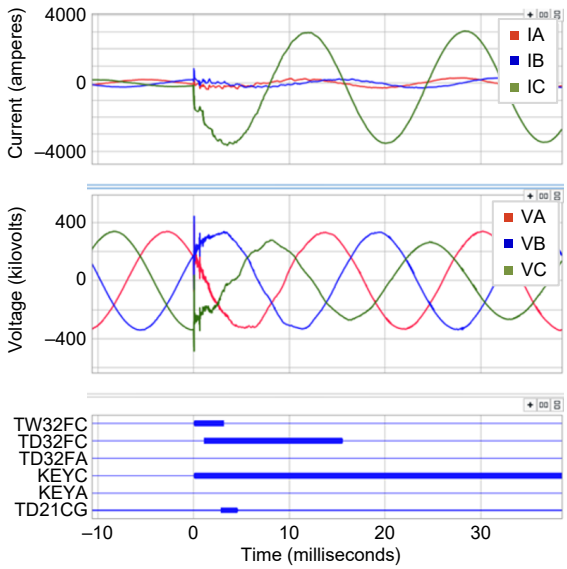

Fig. 26. Currents and voltages captured at MID and the time-domain protection element operation for the internal fault on May 4.

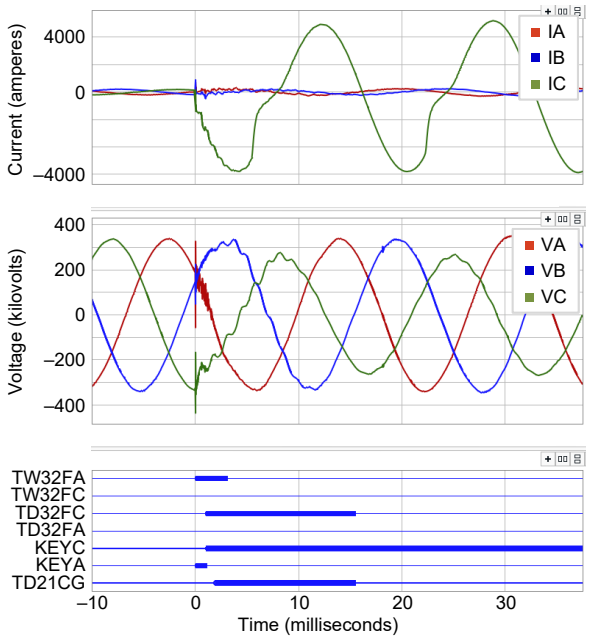

Fig. 27. Currents and voltages captured at TMD and the time-domain protection element operation for the internal fault on May 4.

Fig. 28 and Fig. 29 show the TW current and voltage signals captured at MID and TMD, respectively. The TMD oscillogram shows the TW signals for the three phases. We can observe that the TW voltage signals on Phases B and C have low amplitude. The design of the CCVTs for Phases B and C is different than the design of the Phase A CCVT. Therefore, their frequency responses are different. Because the TW32 element chooses the phase associated with the maximum energy and its reported direction, TW32 selects Phase A for this event and declares the event direction as forward.

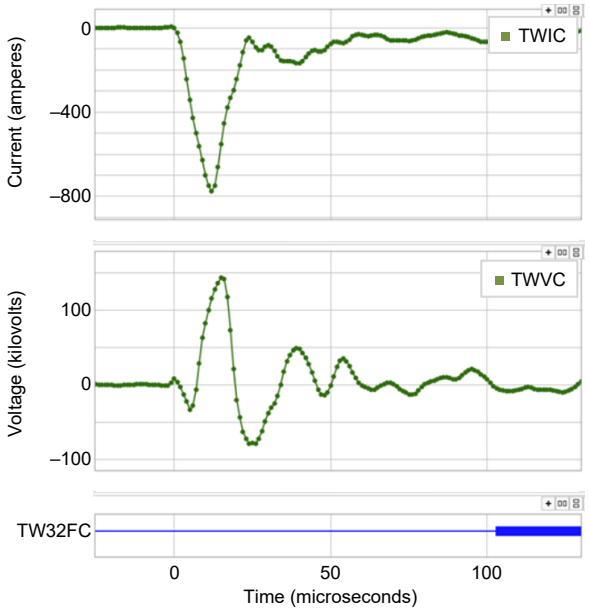

Fig. 28. TW current and voltage captured at MID and the TW32 protection element operation for the internal fault on May 4.

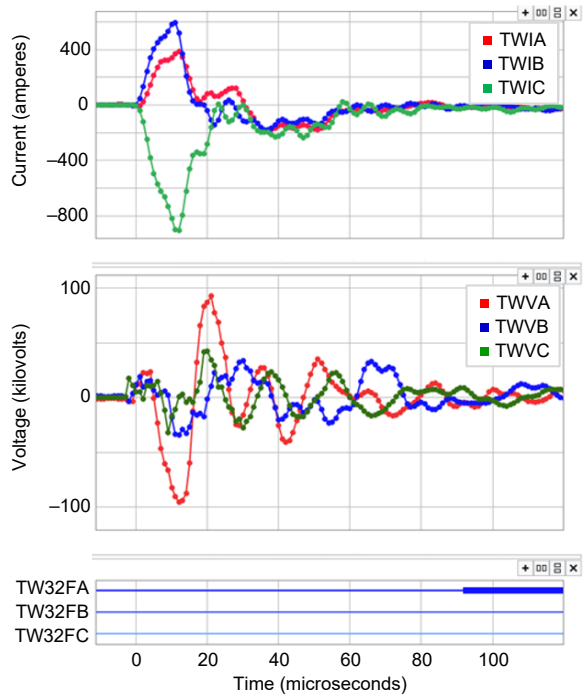

Fig. 29. TW currents and voltages captured at TMD and the TW32 protection element operation for the internal fault on May 4.

Fig. 30 and Fig. 31 show the incremental quantity voltage and current signals captured at MID and TMD, respectively. The plots also show the assertion of the TD32FC bits at both terminals.

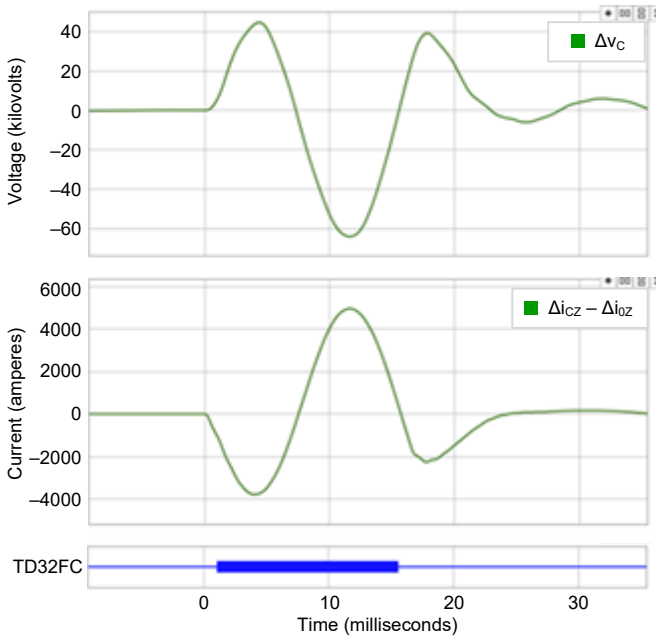

Fig. 30. Incremental voltage and replica current of the CG loop captured at MID and the TD32 protection element operation for the internal fault on May 4.

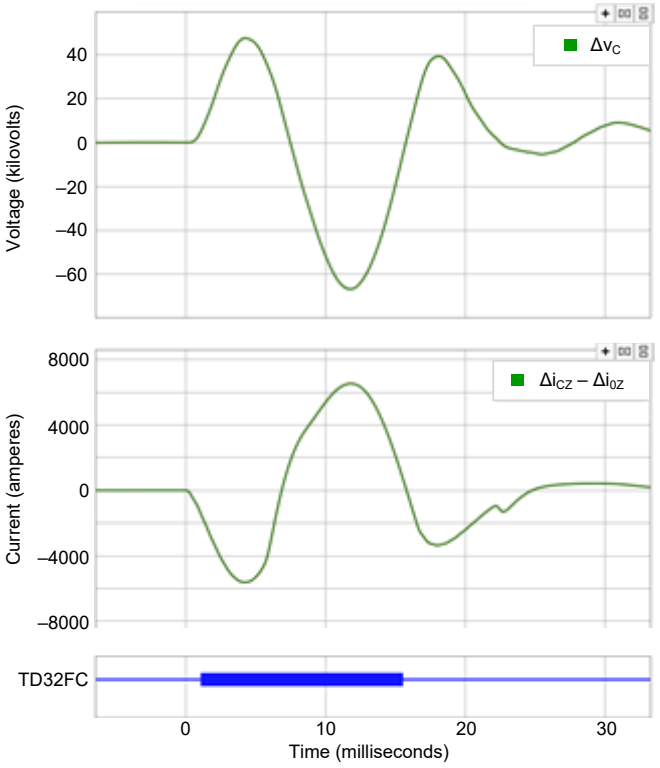

Fig. 31. Incremental voltage and replica current of the CG loop captured at TMD and the TD32 protection element operation for the internal fault on May 4.

B. January 15, 2017 External AG fault

Fig. 32 shows the currents and voltages captured at TMD and the time-domain protection element operation for the January 15 external fault. We can observe the assertion of the TD32RA bit upon detecting the reverse fault condition. Fig. 33 shows the incremental voltage and replica current of the AG loop. For this external fault, the incremental voltage and replica current have the same polarity, as expected.

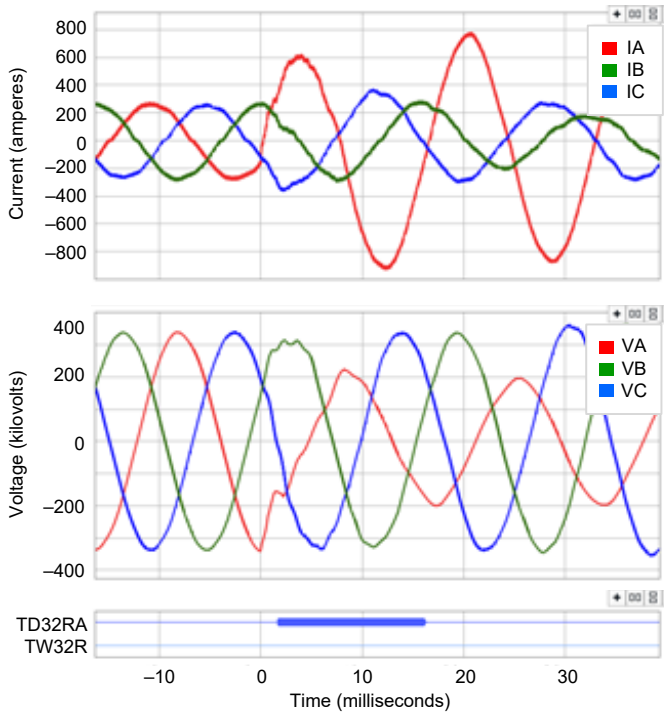

Fig. 32. Currents and voltages captured at TMD and the time domain protection element operation for the external fault on January 15.

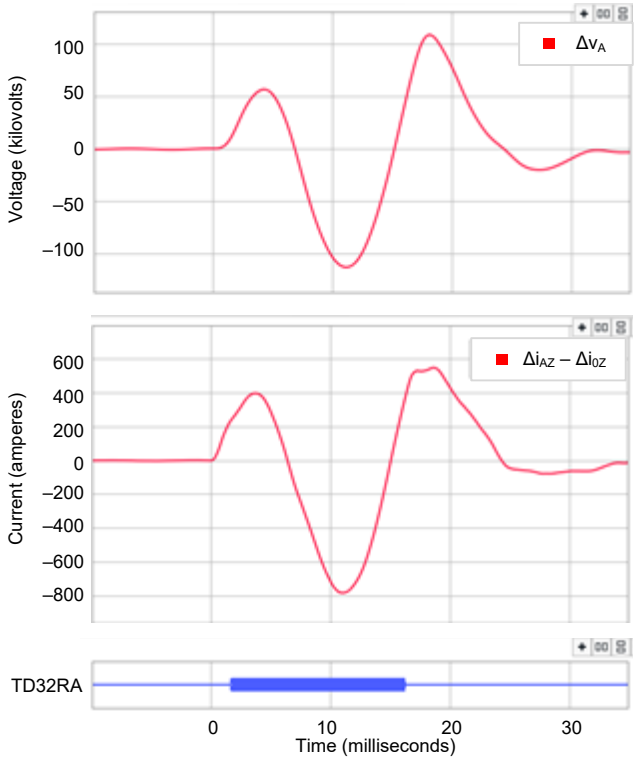

Fig. 33. Incremental voltage and replica current of the AG loop captured at MID and the TD32 protection element operation for the external fault on January 15.

VII. Conclusion

During the evaluation period, the CFE network where the time-domain protective relays are installed experienced four internal and two external faults. The TW32 elements asserted forward in three of the four internal faults and did not assert forward at all for the external faults. The fastest operating time was 105 μs and the slowest was 138 μs, with the average operating time being 116 μs. The TW32 element operations show that for some of the internal faults, the CCVT secondary voltages provide enough signal information for proper element operation, which speeds up the POTT scheme. However, different fault conditions, including factors such as point of wave, fault resistance, distance to external faults, and CCVT response, can lead to weak and distorted voltage TWs that compromise the dependability of this element. As described in the paper, the POTT scheme includes TW32 elements for speed, but it relies on the slightly slower (by 1 to 3 ms) TD32 elements for dependability and security. The TW32 elements were secure for all external faults and transient events.

The TD32 elements operated correctly for all faults, and they did not operate for any voltage or current transient conditions during switching and lightning events. The fastest operating time was 1.055 ms and the slowest was 8.750 ms (for the high-resistance fault on August 23 with very slow current increase), with the average operating time being 2.966 ms for all faults.

The field cases presented in this paper show that the POTT scheme that uses TW32 elements to speed up the transmission of the permissive signal and TD32 elements for phase selection and trip supervision reduces scheme operating times while maintaining security and dependability.

VIII. Appendix

Table III lists the event records that the time-domain relays captured at the MID and TMD substations for six faults. The table shows the details of the time-domain directional element operations.

Table III
Time-Domain Directional Element Operations for Faults on the MID to TID 400 kV Line

Event Date	Terminal	Fault Type	TW32 Operating Time (μs)	TD32 Operating Time (ms)	Observations
Jan 7, 2017	MID	Internal, AG fault	Forward, 138	Forward, 1.2	The TW32FA, TD32FA, and KEYA bits asserted.
Jan 15, 2017	TMD	External reverse, AG fault	No operation	Reverse, 1.7	The TD32RA bit asserted.
Jan 15, 2017	MID	External forward, AG fault	No operation	Forward, 1.9	The TD32FA bit asserted.
Jan 16, 2017	MID	External reverse, CG fault	No operation	Reverse, 1.8	The TD32RC bit asserted. The fault was on the 115 kV network behind the MID 400 kV bus.
Mar 28, 2017	TMD	Internal, CG fault	Forward, 106	Forward, 1.39	The TW32FC, TD32FC, and KEYC bits asserted.
May 4, 2017	MID	Internal, CG fault	Forward, 105	Forward, 1.1	The TW32FC, TD32FC, and KEYC bits asserted. The TD21CG element operated in 2.9 ms.
May 4, 2017	TMD	Internal, CG fault	Forward, 94	Forward, 1.055	The TW32FA, TD32FC, KEYA, and KEYC bits asserted. The TD21CG element operated in 1.855 ms.
August 23, 2017	MID	Internal, AG fault	No operation	Forward, 8.75	The TD32FA bit asserted. This was a very high-resistance fault with slow current increase and no step change. The TD32 element operated 9 ms faster than the conventional directional elements.
August 23, 2017	TMD	Internal, AG fault	No operation	Forward, 7.8	The TD32FA bit asserted. This was a very high-resistance fault with slow current increase and no step change. The TD32 element operated 9 ms faster than the conventional directional elements.

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X. Biographies

Armando Guzmán received his BSEE with honors from Guadalajara Autonomous University (UAG), Mexico. He received a diploma in fiber-optics engineering from Monterrey Institute of Technology and Advanced Studies (ITESM), Mexico, and his masters of science and PhD in electrical engineering and masters in computer engineering from the University of Idaho, USA. He served as regional supervisor of the Protection Department in the Western Transmission Region of the Federal Electricity Commission (the electrical utility company of Mexico) in Guadalajara, Mexico for 13 years. He lectured at UAG and the University of Idaho in power system protection and power system stability. Since 1993 he has been with Schweitzer Engineering Laboratories, Inc. in Pullman, Washington, where he is a fellow research engineer. He holds numerous patents in power system protection and metering. He is a senior member of IEEE.

Mangapathirao (Venkat) Mynam received his MSEE from the University of Idaho in 2003 and his BE in electrical and electronics engineering from Andhra University College of Engineering, India, in 2000. He joined Schweitzer Engineering Laboratories, Inc. (SEL) in 2003 as an associate protection engineer in the engineering services division. He is presently working as a principal research engineer in SEL research and development. He was selected to participate in the U. S. National Academy of Engineering (NAE) 15th Annual U. S. Frontiers of Engineering Symposium. He is a senior member of IEEE and holds patents in the areas of power system protection, control, and fault location.

Veselin Skendzic is a principal research engineer at Schweitzer Engineering Laboratories, Inc. He earned his BS in electrical engineering from FESB, University of Split, Croatia; his Masters of Science from ETF, Zagreb, Croatia; and his PhD from Texas A&M University, College Station, Texas. He has more than 25 years of experience in electronic circuit design and power system protection-related problems. He is an IEEE fellow, has written multiple technical papers, has over 20 patents, and is actively contributing to IEEE and IEC standard development. Veselin is a member of the IEEE Power Engineering Society (PES) and the IEEE Power System Relaying Committee (PSRC) and a past chair of the PSRC Relay Communications Subcommittee (H).

Jean León Eternod is the technology director for Schweitzer Engineering Laboratories, Inc. (SEL) in Mexico. Prior to joining SEL in 1998, he worked for the Comisión Federal de Electricidad (CFE) power systems studies office in protection and control corporate management. While he was at CFE from 1991 to 1998, he worked with wide-area network protection schemes, single-pole trip and reclose studies, and database validation for short circuit, load flow, and dynamic simulation, including generator and control model validation for most CFE generators. He received his BSEE from the National Autonomous University of Mexico (UNAM), where he also completed postgraduate course work in power systems. He received training in power system simulation from Power Technologies, Inc. He has authored numerous technical papers on the topics of power system protection, simulation and wide area protection and control applications.

Rafael Martinez Morales is the head of the power system studies office for Comisión Federal de Electricidad (CFE) Transmission Eastern Region (GRTOR). He graduated as an electromechanical engineer from the Universidad Veracruzana, Coatzacoalcos campus. He has been working with CFE since 1996. He has broad experience in field service at transmission electrical substations from 115 to 400 kV and in working with relays, recorders, and fault locators using different technologies including traveling wave and primary equipment commissioning. He is an instructor for several protective relays and their applications in high-voltage and extra-high-voltage lines. Currently, his main responsibilities are single-pole trip and reclose modeling and implementation, load flow and short-circuit studies for the entire CFE transmission region, and implementation of remedial action schemes.