Utility Implements Communications-Assisted Special Protection and Control Schemes for Distribution Substations

Michael R. Duff
City of College Station

Payal Gupta, Dharmendra Prajapati, and Alex Langseth
Schweitzer Engineering Laboratories, Inc.

This paper was presented at the 70th Annual Conference for Protective Relay Engineers, College Station, Texas, April 3–6, 2017, and can be accessed at: https://doi.org/10.1109/CPRE.2017.8090060.

Utility Implements Communications-Assisted Special Protection and Control Schemes for Distribution Substations

Michael R. Duff, *City of College Station*
Payal Gupta, Dharmendra Prajapati, and Alex Langseth, *Schweitzer Engineering Laboratories, Inc.*

***Abstract*—The City of College Station has implemented high-speed protection at multiple distribution substations using communications-assisted special protection and control schemes (SPCSs). Traditional protection and control schemes negatively impact fault-clearing time, power system restoration time, and equipment lifespan, and they involve significant wiring with associated costs. SPCSs use the state-of-the-art features of microprocessor-based intelligent electronic devices (IEDs) to improve the availability, selectivity, and security of the power system. This paper describes the functionality and benefits of the following SPCSs implemented using multifunction IEDs, rugged logic processors, and protection-speed communications:**

- **Fast bus tripping scheme for significantly reduced bus fault-clearing time.**
- **Breaker failure protection scheme for shorter breaker failure clearing time.**
- **Double-circuit feeder trip scheme for faster clearing of simultaneous faults without causing a substation outage, and stall reclose logic for system availability.**
- **Automatic source transfer scheme for higher power system availability.**

I. Introduction

The City of College Station (COCS) in College Station, TX, provides electric services to residential and commercial customers via their College Station Utilities (CSU) subsidiary. COCS's power system comprises 20 miles of transmission power lines, 458 miles of distribution power lines, and 7 electric substations. The substations have 138 kV ring-bus configurations that are either solely owned by COCS or jointly owned and operated with other Electric Reliability Council of Texas (ERCOT) utilities.

Generally, distribution substations lack bus differential protection, breaker failure backup, and automatic source transfer, and they pose a challenge to coordinating for simultaneous fault conditions. Traditional distribution protection and control schemes require extensive wiring, negatively impact service restoration time, and reduce equipment lifespan [1]. COCS wanted to overcome these limitations and use the full potential of their existing dual, 25 MVA transformer configuration and intelligent electronic devices (IEDs) with emphasis on improved reliability performance. To achieve this, they applied communications-assisted special protection and control schemes (SPCSs) to the distribution system.

A good protection scheme is a combination of reliability, selectivity, resilience, speed, and low cost. A powerful, multifunction, microprocessor-based IED offers robust protection as well as metering, control, and fast communications features. This paper discusses various contingencies that could occur in the power system and the remedial actions that would be taken by SPCSs employed at four of the seven COCS distribution substations presently in service. The communications link status is monitored during normal and trip conditions and is alarmed for failures via a local human-machine interface (HMI) and a remote supervisory control and data acquisition (SCADA) system. The consequences of communications channel unavailability and the backup protection in place for each of the schemes are also examined.

II. Distribution Substation Overview

A typical COCS 13.2 kV distribution substation topology is shown in Fig. 1. There are eight feeders connected to two buses. Each bus is supplied electric power from a 13.2 kV main breaker. The two buses are electrically connected via a normally open tie breaker. The high-voltage sides of the two transformers are connected to a 138 kV ring bus.

A Global Positioning System (GPS) time source with IRIG-B output signals is used to provide system-wide time synchronization with ±100 ns accuracy. The GPS clock distributes IRIG-B time to the logic processors, which in turn distribute the time to individual IEDs using demodulated IRIG-B time source inputs over serial connections. Analysis of time-aligned Sequence of Events (SOE) reports and oscillography event reports generated by system-wide IEDs is highly valuable in determining the root causes of events.

An automation controller is programmed to collect slow-speed data from the IEDs via Distributed Network Protocol (DNP3) over Ethernet. A web-based, local HMI is set up to visualize the power system status and display system alarms. Information is also exchanged with the remote SCADA system for data monitoring, breaker open/close controls, and scheme enable/disable controls.

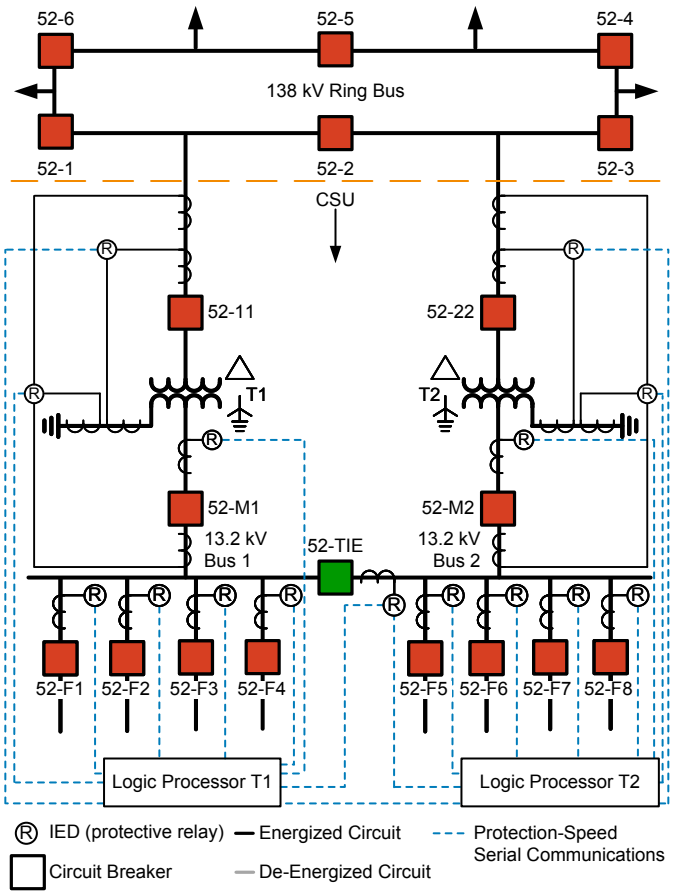

Fig. 1. Simplified One-Line Diagram for a Typical COCS Distribution Substation (the key applies to all one-line diagrams in this paper)

The SCADA communications between the IEDs at the substation and COCS's central control room are secured using a virtual private network (VPN) that provides confidentiality, authentication, and integrity for the transmitted data. Security gateways are installed at each of the distribution substations and at the central control room. The security gateways encrypt data traffic across an untrusted network by establishing an Internet Protocol Security (IPsec) tunnel between the source and the destination, which are at two geographically distant locations. The IPsec tunnel supports very strong encryption and cryptographic authentication, thus protecting traffic privacy [2].

At each distribution substation, the security gateway also performs automated IED password management, which ensures that the passwords are changed regularly and that they conform to complexity rules for strong security. The North American Electric Reliability Corporation (NERC) Critical Infrastructure Protection (CIP) password requirements are satisfied by enforcing strong passwords on IEDs and having the passwords automatically changed on a configurable schedule.

Two rugged logic processors, one for each source side, are used per substation. The IEDs corresponding to the first source side are serially connected to Logic Processor T1, and the IEDs corresponding to the second source side are serially connected to Logic Processor T2 (see Fig. 1). The SPCS algorithms in the logic processors make informed decisions based on the most recent power system information received from the distributed IEDs. The logic for each SPCS was developed using the IEC 61131-3 Programming Languages Standard [3]. The IEDs are also set to locally display the operation of the SPCS using programmable LCDs and LEDs. The local displays help crew members easily identify events and allow them to take appropriate follow-up actions to guarantee faster service restoration.

The IEDs also use point-to-point, protection-speed serial communications over fiber-optic channels to transmit 8 digital bits (transmit bits, or TBs) and receive 8 digital bits (receive bits, or RBs) per message, every 4 ms. Each of the IEDs in the SPCS repeatedly sends and receives a digital logic message while continually monitoring and checking the integrity of the received messages.

In an IED, the digital status bit (ROK) indicates the health of the communications channel. ROK confirms that the digital bit serial communications port of the microprocessor device is receiving valid data from the remote device. ROK de-asserts the instant the IED detects any transmission error or any time the IED detects that it has not received a digital bit message in the time required to transmit three digital bit messages. Typically, the inverse (NOT) of ROK is used to create a digital alarm bit to alert operations of an interdevice communications failure [4].

In the logic processors, an internal monitoring point (represented by IED-COM in Fig. 2) asserts when a good signal is received and de-asserts immediately upon the detection of a bad message. The communications link supervision in the logic processors only allows received data bits of good quality to be considered in the SPCS algorithms.

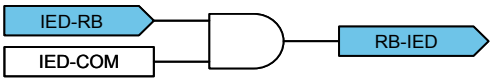

Fig. 2. Communications Link Supervision for Data Bits

The logic processors concentrate all the required fault information from the field IEDs for the operation of the SPCS. The logic processors are also configured for station-wide sequential events recording, which facilitates system-wide fault analysis. The IEDs generate and store oscillographic event reports when an event occurs. A computer in the central control room runs event report collection software that looks for new oscillographic event reports, automatically downloads the event files from the substation IEDs, and stores the files at a centralized location. Fig. 3 illustrates the distribution substation information flow.

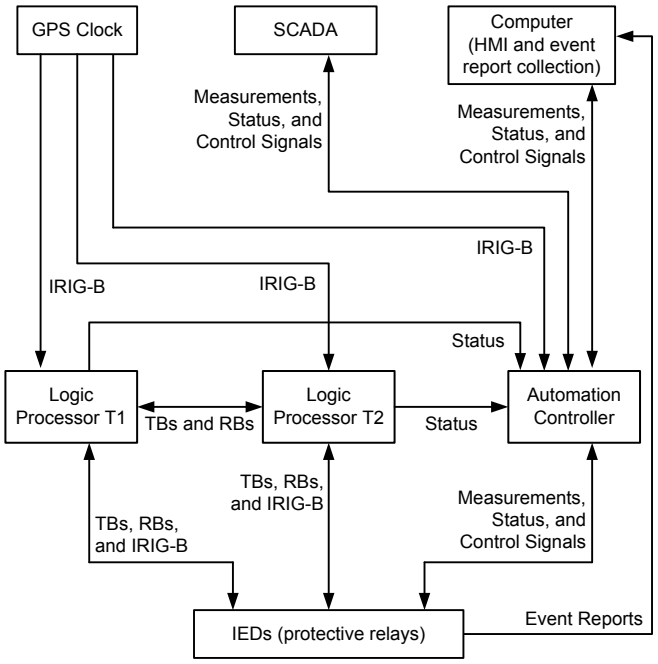

Fig. 3. Information Flow Diagram for a Distribution Substation

III. Fast Bus Tripping Scheme

A bus fault must be cleared fast enough to avoid equipment damage, especially to the most expensive equipment in the substation: the power transformer. COCS's traditional bus protection philosophy for medium-voltage buses is to clear bus faults with transformer backup protection that is time-delayed to coordinate with the feeder protection. Thus, the bus fault-clearing time is not instantaneous but is typically between 0.6 and 1.0 seconds.

Bus differential protection is fast and secure but very costly because of the need for dedicated current transformers (CTs) and their associated wiring, along with the extensive testing required to validate the scheme. COCS instead decided to use the fast bus tripping scheme as a cost-effective solution to protect the buses. A fast bus tripping scheme provides a tripping time close to that of a differential IED and is less costly because the IEDs already in place for other purposes are used to form the scheme. There is less hardware cost, wiring, and testing required for a fast bus tripping scheme relative to a differential scheme.

The fast bus tripping scheme is designed to protect for bus faults. If a close-in feeder fault occurs, the faulted feeder breaker IED and the bus IEDs sense the fault current. The feeder breaker IED trips for the faulted condition and simultaneously tells the bus IEDs that it sees the fault. The bus IEDs' overcurrent elements are prevented from tripping for this condition. When a bus fault occurs, there is no fault current contribution from the feeders. The feeder breaker IEDs do not sense the fault and do not block the bus IEDs' overcurrent elements, so the bus IEDs' overcurrent elements operate to clear the fault.

Referring to Fig. 4, for a fault on Bus 1, none of the feeder breaker IEDs' overcurrent elements pick up to block the torque-controlled overcurrent (67) element in the 52-M1 breaker IED. The 67PT or 67GT element in the 52-M1 breaker IED picks up and trips the 52-M1 breaker. The fast bus tripping signal (referred to as FBT in Fig. 4) is transmitted from the 52-M1 breaker IED to Logic Processor T1. The logic processor then distributes the trip signal to the feeder breaker IEDs for the 52-F1, 52-F2, 52-F3, 52-F4, and 52-TIE breakers to clear the fault. The scheme isolates the faulted bus within 2 to 3 cycles, and it maintains sensitivity and speed even when the CTs approach saturation.

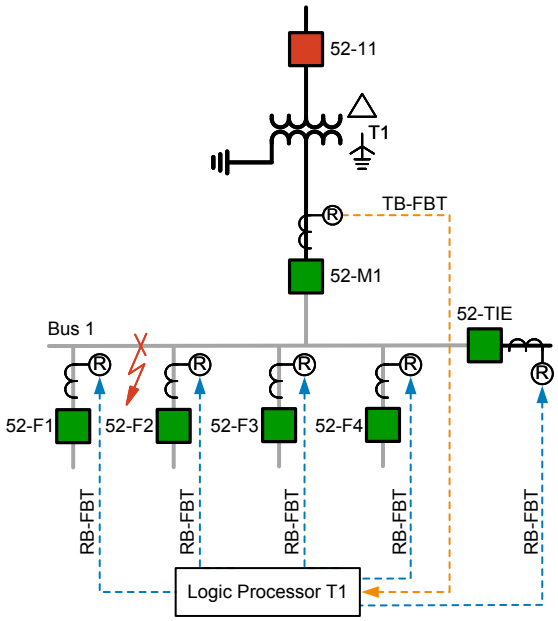

Fig. 4. Fast Bus Tripping Scheme

For a feeder fault, the 67 elements in the 52-M1 and the 52-TIE breaker IEDs receive a signal from the faulted feeder breaker IED to block the fast bus tripping scheme from tripping. Referring to Fig. 5, for a fault on the 52-F1 feeder circuit, the overcurrent element in the 52-F1 breaker IED asserts and sends a signal (referred to as BLK in Fig. 5) to the 52-M1 and 52-TIE breaker IEDs via the logic processor to block the fast bus tripping logic and prevent a bus outage. Proper selectivity is achieved and coordination between the main, tie, and feeder breaker IEDs is maintained.

For a loss of the communications link to the logic processors, the fast bus tripping scheme is disabled. COCS's traditional bus protection consisting of upstream overcurrent IEDs that overreach the protection zone with time coordination is relied upon. Fig. 6 and Fig. 7 show the logic diagrams for the fast bus tripping scheme and fast bus tripping block, respectively.

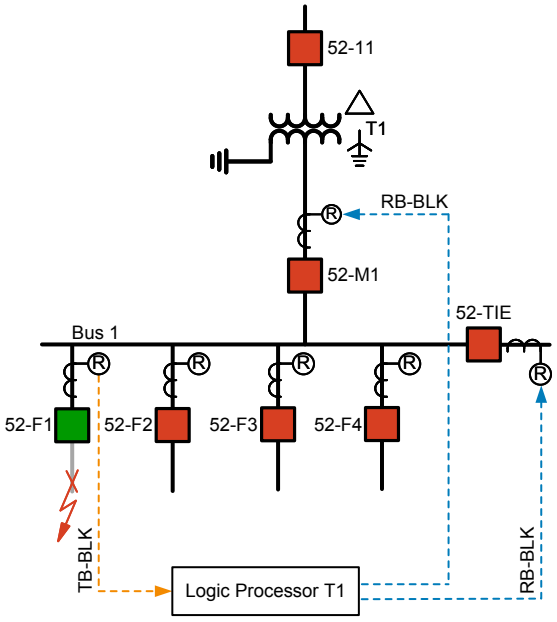

Fig. 5. Fast Bus Tripping Block

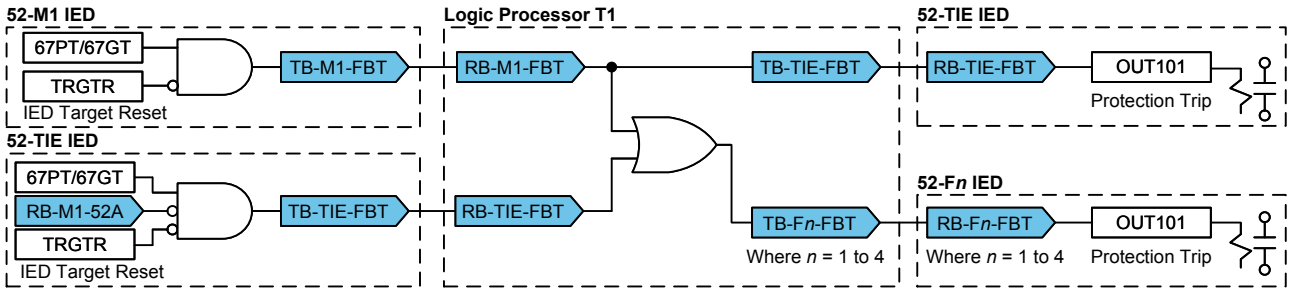

Fig. 6. Fast Bus Tripping Logic Diagram

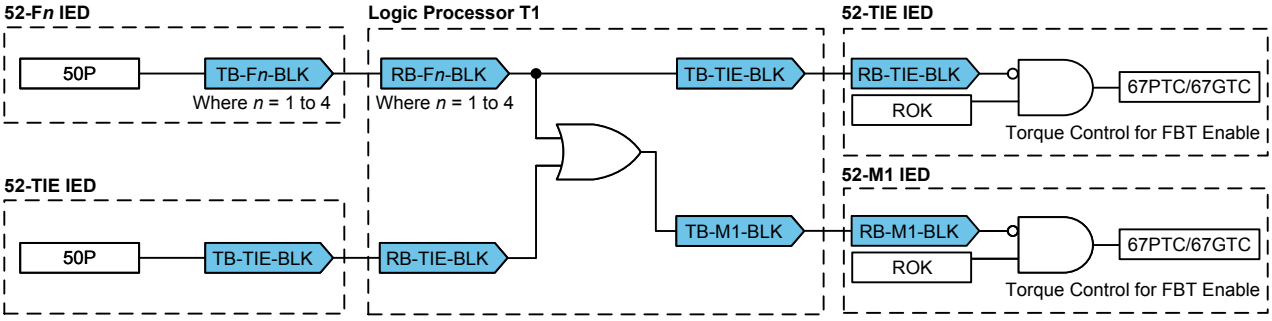

Fig. 7. Fast Bus Tripping Block Logic Diagram

IV. Breaker Failure Protection Scheme

Dedicated breaker failure protection schemes are not part of COCS's traditional distribution substation protection. When a breaker fails to interrupt a system fault, COCS's traditional protection philosophy is to clear the fault with upstream inverse-time overcurrent protection. This method of protection for a breaker failure condition can result in long fault-clearing times that stress the power system and lead to equipment damage or reduced equipment lifespan.

Because dedicated breaker failure protection schemes are simple to implement in the IEDs and because required breaker tripping for the schemes is easily accomplished with the logic processors, COCS decided to include a dedicated breaker failure protection scheme in their new substation protection and control system. With no additional IEDs or communications needed and with minimal additional wiring required, the implementation costs of the scheme are low. Implementing this scheme allows the advantages of faster clearing for breaker failure conditions to be realized.

With the breaker failure protection scheme active in the IED, if a trip signal to the associated breaker remains asserted and current continues to flow through the breaker, the breaker failure trip element asserts after the breaker failure timer expires. The IED issues the breaker failure trip signal to the

logic processors, which then distribute the trip signal to the adjacent breakers to clear the fault and isolate the failed breaker. The breaker failure trip signal also enables the drive-to-lockout (79DTL) control in the IEDs, which blocks the tripped breakers from reclosing. Referring to Fig. 8, the breaker failure protection scheme should operate for a Bus 1 fault and trip the 52-M1, 52-F1, 52-F2, 52-F3, 52-F4, and 52-TIE breakers to isolate the bus. Most substation breakers have interrupting ratings of 5 cycles or less. If the 52-M1 breaker fails to trip and clear the fault, the breaker failure protection logic in the 52-M1 breaker IED times out in 12 cycles and asserts the breaker failure trip signal (represented as BF in Fig. 8), which gets transmitted to Logic Processor T1. The logic processor then sends the trip signal to the 52-11 high-voltage-side breaker IED, which trips the 52-11 breaker to completely isolate the fault. The logic processor also sends the breaker failure trip signal to the 52-TIE, 52-F1, 52-F2, 52-F3, and 52-F4 breaker IEDs, but these breakers are already tripped in the example in Fig. 8.

On the other hand, if the 52-11 breaker fails to interrupt a transformer fault, then the breaker failure element in the 52-11 breaker IED asserts after a time delay and sends a breaker failure trip signal to Logic Processor T1. The logic processor then transmits the breaker failure trip signal to the adjacent breakers 52-M1, 52-1, and 52-2 to isolate the fault. Fig. 9 shows the logic diagram for the breaker failure protection scheme implemented in the IEDs.

Breaker failure protection logic is implemented in high-voltage-side overcurrent IEDs, low-voltage-side overcurrent IEDs, bus tie IEDs, and feeder IEDs. If communications fail between the IEDs and the logic processors, the breaker failure scheme does not operate. In that case, the fault is cleared using out-of-zone, time-coordinated overcurrent backup protection.

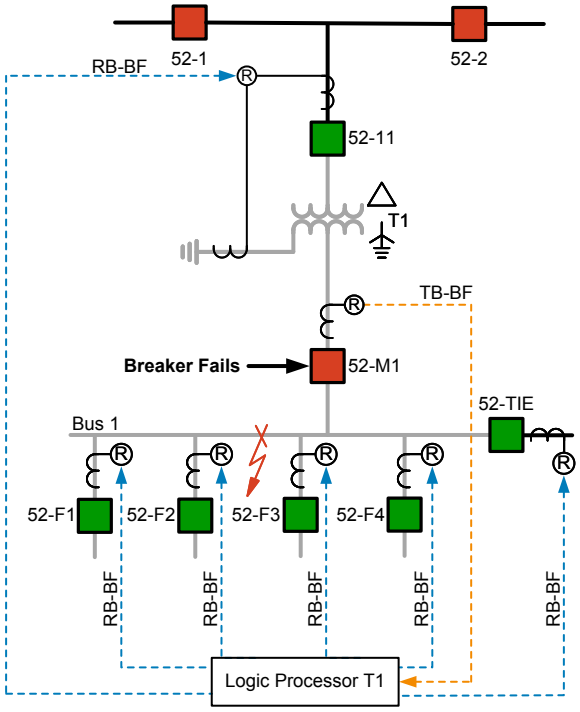

Fig. 8. Breaker Failure Protection Scheme

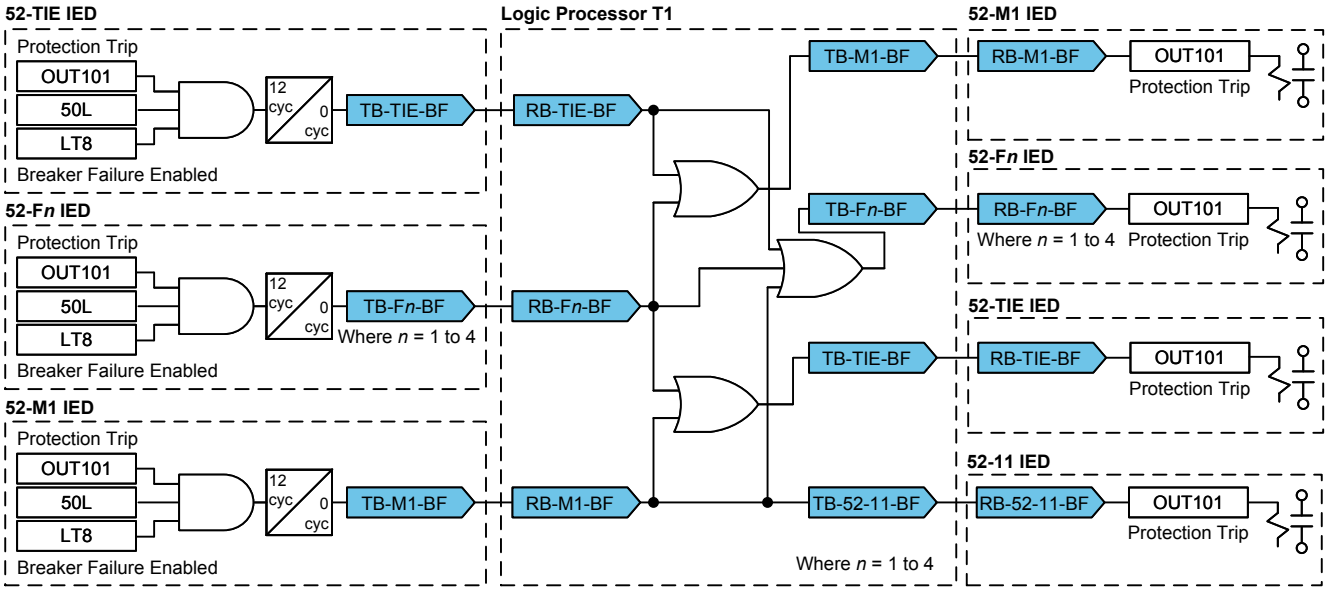

Fig. 9. Breaker Failure Protection Logic Diagram

V. Double-Circuit Feeder Trip Scheme and Stall Reclose Logic

It is common for overhead distribution systems to have double-circuit lines sharing the same electric pole or single-circuit lines running in close vicinity. This distribution network topology increases the frequency of simultaneous electric faults on two circuits. Simultaneous faults may cause problems with coordinating overcurrent protection between the main and feeder breaker IEDs. The main breaker overcurrent protection may misoperate and negatively affect the service availability of the circuits not involved with the fault.

During simultaneous faults in the distribution system, the main breaker IED measures the current that is the sum of the fault currents in all the faulted feeders and the load currents in all the unfaulted feeders. In contrast, a faulted feeder breaker IED measures the fault current respective to its feeder only. This difference in measured currents between the IEDs may cause the main breaker IED inverse-time overcurrent element to operate faster than the inverse-time overcurrent elements of the feeder breaker IEDs. Thus, the main breaker IED backup protection may trip sooner than the feeder breaker IEDs and result in a complete bus outage at the substation.

COCS traditionally had to adjust the IEDs' overcurrent pickup and time-dial settings to deal with simultaneous faults. This resulted in slower tripping by the main breaker overcurrent protection, and sometimes coordination between the main breaker and feeder breaker IEDs could not be achieved. Because the double-circuit feeder trip scheme does not require additional IEDs, it is simple to implement with low cost. It allows the main overcurrent elements to be set faster and thus improves service reliability. For a simultaneous fault on the 52-F1 and 52-F2 feeders (shown in Fig. 10), the inverse-time overcurrent elements (51P) assert in the faulted feeder IEDs, and the IEDs transmit the pickup signals (represented as PU in Fig. 10) to Logic Processor T1. The logic processor then distributes a 51P signal to all the other feeder breaker IEDs on Bus 1. The 51P signal is also transmitted to Logic Processor T2, which in turn distributes the signal to all the feeder breaker IEDs on Bus 2. The scheme algorithm ensures that the 51P signal does not route back to the IED that transmitted it. Fig. 11 shows the logic diagram for the double-circuit feeder trip scheme implemented in the IEDs.

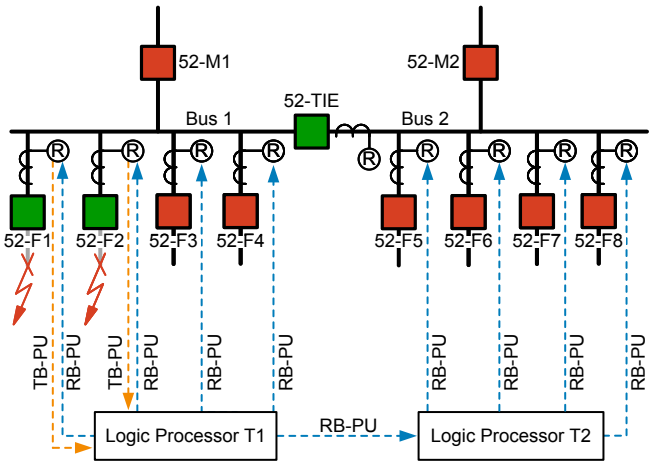

Fig. 10. Double-Circuit Feeder Trip Scheme

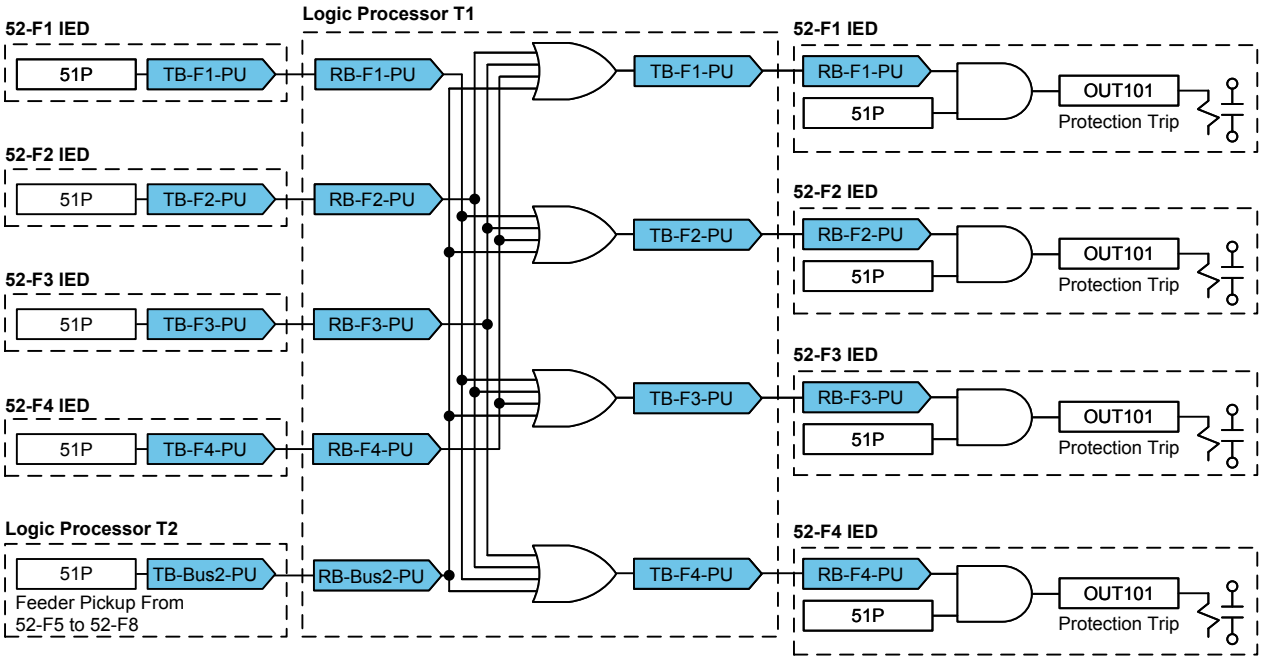

Fig. 11. Double-Circuit Feeder Trip Logic Diagram

Because both the 52-F1 and 52-F2 breaker IEDs have the 51P element picked up and they both received the 51P signal from each other, this confirms the presence of a simultaneous fault in the system. Both of the faulted feeder breaker IEDs instantaneously trip without waiting for their inverse-time overcurrent elements to time out. This protection scheme allows for instantaneous tripping for simultaneous faults on feeder circuits and prevents unnecessary service interruptions to the unfaulted feeders, thus improving service availability.

The reclose function in microprocessor-based feeder breaker IEDs is set for automatic reclosing and is administered by reclose supervision logic in the IEDs. A simultaneous fault on the distribution system trips multiple faulted feeders. Because the type of fault is known, the reclosing logic is started in the feeder breaker IEDs to attempt automatic power restoration. After successful reclose initiation and a corresponding set open-interval time, the feeder breaker IEDs automatically reclose the circuit breaker. This causes the multiple affected feeder circuit breakers to close all at once and, thus, have their combined loads energized all together. The concurrent feeder closing burdens the power transformers because of the inrush currents from starting multiple rotating loads on the power system together.

The stall reclose logic ensures that the feeders do not reclose simultaneously after a double-circuit fault trip. The stall reclose signals are exchanged between the feeder breaker IEDs through the logic processors, which stall the reclosing cycles for the feeder breaker IEDs. The affected feeder breaker IEDs reclose one after another in a sequence predetermined by the stall reclose algorithm and thereby avoid inrush currents on the transformers. Fig. 12 shows the diagram for the stall reclose logic implemented in the IEDs.

The logic diagram shows that the feeder breaker IED transmits a stall reclose signal (represented as SR in Fig. 12) when it trips because of the double-circuit fault or when it receives a stall reclose signal from the preceding feeder breaker IEDs in the lineup. The stall reclose signal from the feeder breaker IEDs stays asserted for 90 cycles. The stall reclose logic in the two logic processors is written such that the sequence of operation starts with the reclosing of the 52-F1 feeder breaker IED first (no stall reclose signal), followed by 52-F2 (stall reclose signal from 52-F1), then 52-F3 (stall reclose signal from 52-F1 or 52-F2), and so on until the last feeder, 52-F8 (stall reclose signal from 52-F1 to 52-F7), is reclosed.

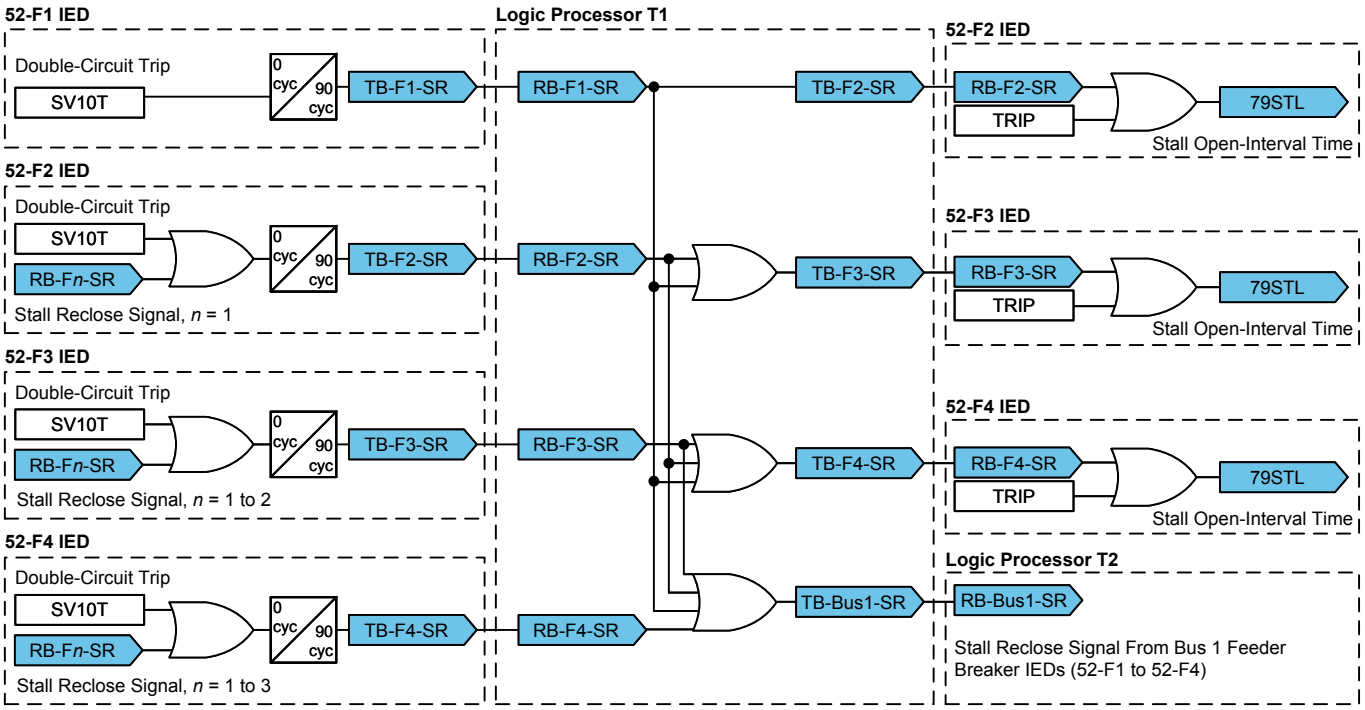

Fig. 12. Stall Reclose Logic Diagram

VI. Automatic Source Transfer Scheme (ASTS)

It is extremely important for utilities to supply electric power to their customers with minimal disruption and short restoration times. To improve power reliability, the distribution system often provides redundant utility sources that can both serve the same load via an ASTS that switches from a primary source to an alternate source in the event of a power interruption in the primary source.

A main-tie-main (MTM) ASTS can be enabled or disabled by an operator via remote control from the SCADA system. The logic for the MTM ASTS resides in the logic processor. The scheme continuously monitors the 52A circuit breaker statuses of the two low-voltage-side main breakers (52-M1 and 52-M2) and the tie breaker (52-TIE). The scheme also monitors for any fault condition on Transformers T1 and T2 received from the transformer differential IEDs that will trip the power source.

The scheme algorithm validates certain conditions (i.e., the ASTS is enabled, both main breakers are closed, the tie breaker is open, and communications are good with the MTM IEDs) to enable the automatic transfer. On detecting an event (transformer fault) that results in an outage of one of the sources, the logic processor sends a close command to the tie breaker IED after a short time delay and restores power to all the affected feeders from the alternate healthy source. Fig. 13 illustrates the action of the ASTS.

If the amount of total load to be picked up from the source with the outage exceeds voltage sag guidelines [5], then the distribution breakers on the faulted transformer bus can be tripped when the main breaker trips. Stall reclose logic is then used to individually restore the distribution circuit breakers in the unenergized bay upon the closing of the tie breaker. This approach is similar to the double-circuit feeder trip and stall reclose logic.

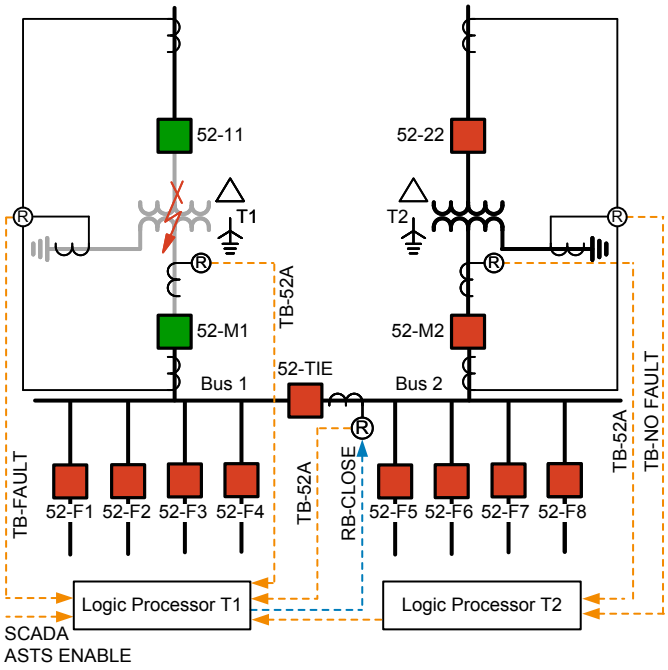

Fig. 13. ASTS

Fig. 14 shows the logic diagram for the MTM ASTS implemented in the logic processor.

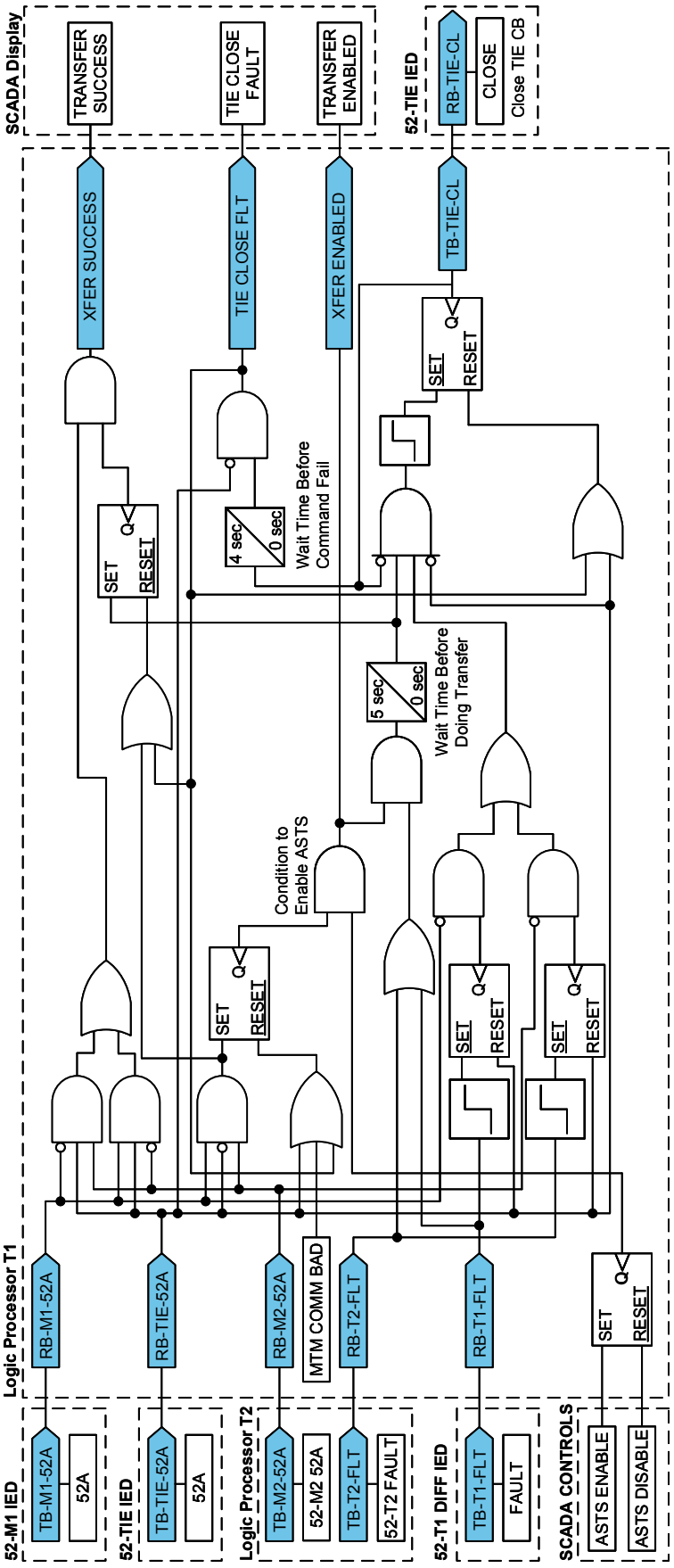

Fig. 14. ASTS Logic Diagram

VII. Other Schemes and Merits

Multiple SPCSs are implemented at COCS using IEDs, protection-speed communications, and specialized algorithms programmed in the logic processors. These schemes are designed to operate in parallel with each other and interact with each other to ensure the reliable operation of the power system. In addition to the schemes discussed in previous sections, there are other schemes that are implemented to further improve the availability and dependability of the distribution system.

During maintenance, the torque-controlled overcurrent elements for the main, tie, or feeder breaker IEDs can be enabled, and the reclose function can be disabled. This is called the hot-line mode, and it can be enabled or disabled by pressing a pushbutton on the front panel of the IED.

Like any lockout/tagout procedure, enabling the hot-line mode is part of COCS's operations and maintenance plans for switchgear or electrical equipment. The IED must be put in hot-line mode to enable instantaneous tripping when personnel are in close proximity to energized equipment. The cost of implementing the hot-line mode is small compared with the benefits of reduced trip times and reduced arc-flash hazards [6].

The health of the IEDs is continuously monitored by the logic processors. In the case of a device hardware alarm (HALARM), software alarm (SALARM), or communications link failure for the tie breaker IED or any of the feeder breaker IEDs, an IED failure initiate signal is triggered by the logic processor. This signal is then transmitted to the low-voltage-side main breaker IED to enable its torque-controlled overcurrent element. The enabled 67 element in the main breaker IED ensures an instantaneous trip on the fault and fast fault-clearing time in case any of the feeder breaker IEDs are unhealthy. The IED failure initiate signal is also sent to the SCADA system to alert the operator to take immediate action. Fig. 15 shows the logic diagram for the IED failure initiate scheme implemented in the logic processor.

VIII. Conclusion

With improvements in communications technology and the use of multifunction IEDs, it is now possible to replace low-density copper signaling with communications-assisted SPCSs. The different schemes run in parallel and coordinate with each other as a complete integrated solution. This paper discusses the functionality and benefits of different SPCSs that are implemented in COCS's substations to suffice six major design criteria:

- Dependability (to ensure that the scheme operates when required to avoid a system collapse).
- Security (to ensure that the scheme does not operate when not required for minimum interruption).
- Selectivity (to ensure that the correct but minimum amount of action is performed for the intended function).
- Resilience (to provide service during a failure and quick recovery over the full range of dynamic and steady-state operating conditions of the distribution system).
- Speed (to ensure fast fault-clearing time).
- Cost (to achieve significant savings in equipment and implementation costs).

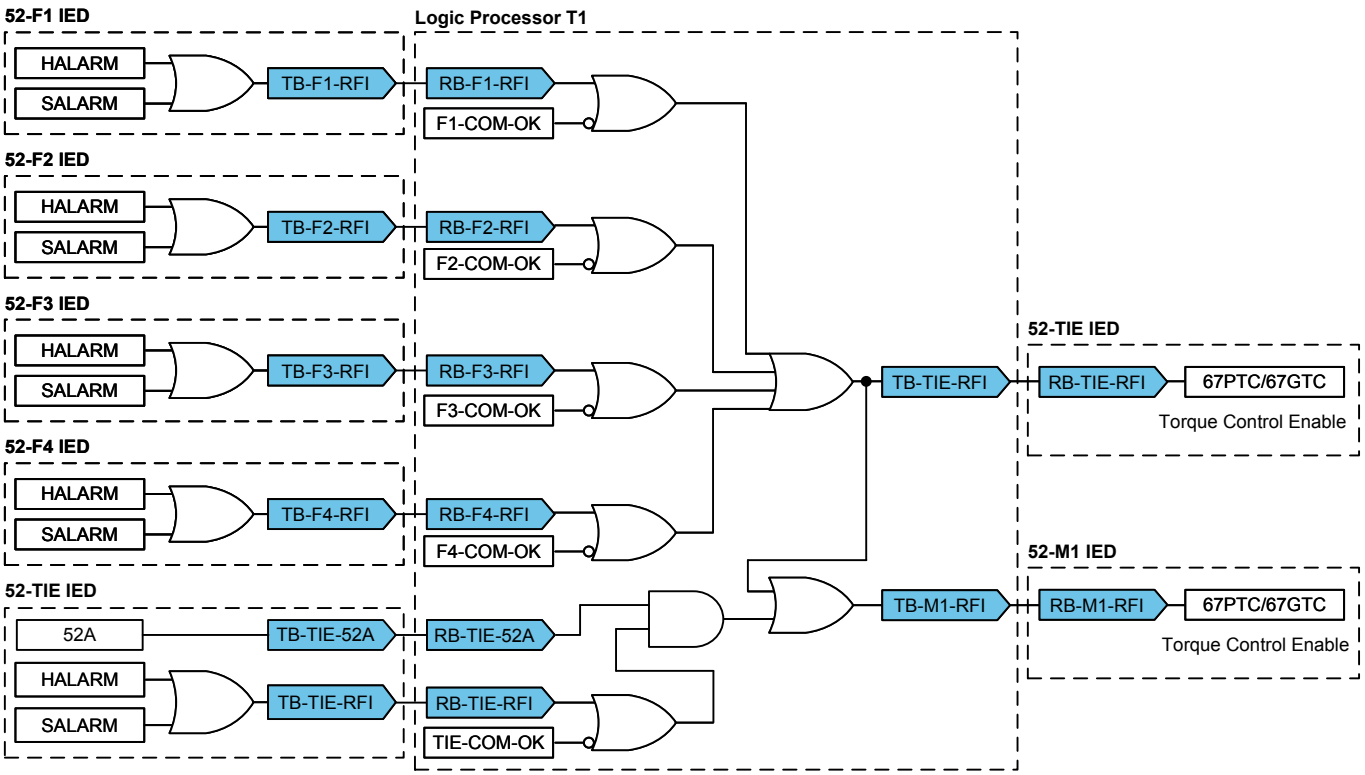

Fig. 15. IED Failure Initiate Scheme Logic Diagram

Implementing a fast bus tripping scheme has reduced bus fault-clearing time from seconds to cycles. The breaker failure protection scheme has reduced the duration of faults for primary breaker failure. Faster fault-clearing time reduces stress on the power system and helps increase equipment lifespan. The double-circuit feeder trip scheme solves low-voltage-side main breaker IED misoperation caused by simultaneous feeder faults. The stall reclose logic helps avoid inrush currents on the power transformer by reclosing the feeder circuits one after the other in a sequence. System reliability is further improved by implementing an ASTS, which detects a loss of source and automatically transfers the affected load to the alternate healthy source, if available.

SPCSs take advantage of existing IED functions and capabilities without the need for extra devices and the associated wiring, engineering, drafting, and construction costs. SPCSs use protection-speed communications channels to pass signals between IEDs without the need for expensive communications equipment and maintenance. Utilities can significantly improve the availability, selectivity, and security of the power system by implementing SPCSs for distribution substations.

IX. References

[1] D. Sánchez Escobedo, E. Alcázar Ramírez, O. A. Márquez Villanueva, H. J. Altuve Ferrer, and A. Martínez del Sol, "Multifunction Relays and Protection Logic Processors in Distribution Substation Applications," November 2005. Available: https://www.selinc.com.

[2] T. J. Hjorth, P. Gupta, and A. Balasubramanian, "University Implements Distribution Automation to Enhance System Reliability and Optimize Operations," proceedings of the 3rd Annual PAC World Americas Conference, Raleigh, NC, August 2016.

[3] IEC 61131-3, Programming Languages, 2013.

[4] J. J. Novak Jr. and R. D. Kirby, "Better, Faster, and More Economical Integrated Protective Relaying and Control Using Digital Bits and Logic," *IEEE Transactions on Industry Applications*, Vol. 46, Issue 4, July/August 2010, pp. 1,281–1,294.

[5] Pacific Gas and Electric Company, "Voltage Tolerance Boundary," January 1999. Available: http://www.pge.com/includes/docs/pdfs/mybusiness/customerservice/energystatus/powerquality/voltage_tolerance.pdf.

[6] J. Buff and K. Zimmerman, "Application of Existing Technologies to Reduce Arc-Flash Hazards," proceedings of the 33rd Annual Western Protective Relay Conference, Spokane, WA, October 2006.

X. Biographies

Michael R. Duff, P.E., received his B.S.E.E. from the University of Kentucky in 1984 and is a registered Professional Engineer in Texas. He has a wide range of experience in utility distribution and transmission protection subjects. He is presently working as the Substation and Metering Superintendent for the City of College Station.

Payal Gupta received her B.S. in electrical engineering from the National Institute of Technology, India, in 2007 and her M.S. in electrical engineering from the University of Houston in 2011. She is presently working as an automation engineer at Schweitzer Engineering Laboratories, Inc. in Houston, Texas. She has been involved in the design, engineering, and implementation of power management systems and distribution automation systems for industrial projects and electric utilities.

Dharmendra Prajapati, P.E., received his B.S. in electrical engineering from the Tribhuvan University Institute of Engineering, Nepal, in 2006 and his M.S.E.E. from Michigan Technological University in 2010. He is presently working as a protection engineer at Schweitzer Engineering Laboratories, Inc.

Alex Langseth, P.E., received his B.S. in electrical engineering from the Georgia Institute of Technology in 2008 and his M.S. in electric power and electromagnetics from the Georgia Institute of Technology in 2009. He has experience in power system protection, system fault analysis, arc-flash assessment, Aurora mitigation assessment, and project management for utility and industrial customers. He also has technical training in substation components and safety, relay programming and testing, and substation commissioning.

Previously presented at the 2017 Texas A&M Conference for Protective Relay Engineers.

20170209 • TP6780-01