New Deterministic, High-Speed, Wide-Area Analog Synchronized Data Acquisition – Creating Opportunities for Previously Unachievable Control Strategies

Javier Martín Herrera, Matias Sanchez Mingarro, and Santiago López Barba
Red Eléctrica de España

David Dolezilek, Fernando Calero, Amandeep Kalra, and Brian Waldron
Schweitzer Engineering Laboratories, Inc.

Presented at the
XIII Simposio Iberoamericano Sobre Proteccion de Sistemas Electricos de Potencia
Monterrey, Mexico
February 19–24, 2017

Previously presented at the
3rd Annual PAC World Americas Conference, August 2016, and
7th Annual Protection, Automation and Control World Conference, June 2016

Previous revised edition released April 2016

Originally presented at the
Power and Energy Automation Conference, March 2016

New Deterministic, High-Speed, Wide-Area Analog Synchronized Data Acquisition – Creating Opportunities for Previously Unachievable Control Strategies

Javier Martín Herrera, Matias Sanchez Mingarro, and Santiago López Barba, *Red Eléctrica de España*
David Dolezilek, Fernando Calero, Amandeep Kalra, and Brian Waldron, *Schweitzer Engineering Laboratories, Inc.*

***Abstract*—This paper describes the new high-speed data acquisition and precise synchronization strategies (in addition to the special considerations and engineering best practices) used to design a communications network for a high-voltage dc (HVDC) link between France and Spain. Because of the mission-critical nature of the system, various contingency scenarios to optimize the availability and dependability of the system are discussed. Additionally, the paper discusses several new hardware and software redundancy methods within the system that improve the overall control system dependability and security.**

I. Introduction

The new high-voltage dc (HVDC) voltage source converter (VSC) interconnection between Spain and France is embedded within an ac network. Operation of the interconnection requires frequent calculation of the power flow across four parallel ac lines and the status of the bus configuration at the associated substations. High-speed analog data acquisition and data redundancy are necessary to satisfy the design requirements of this system. These were previously not available.

Several control modes of operation are implemented in the HVDC VSC link between Spain and France. The power flow mode is based on the knowledge of the total power exchanged and changes in power flow across the existing ac lines. The simulation mode models the dc link as a simulated ac line by monitoring the angular difference between the ac buses.

The power flow mode requires sending the sum of the active power flows through all of the ac interconnection lines to the HVDC controller. Power flow information must be collected from four substations. The distance between the HVDC controller and the four remote substations ranges from 80 to 600 km. Different technologies (including typical, event-driven IEC 61850 Generic Object-Oriented Substation Event [GOOSE] and IEEE and IEC synchrophasor protocols) were investigated and compared. However, none of these protocols could satisfy the stringent design requirement for detection and notification of a change in power flow within 40 ms.

This paper (an expansion of [1]) explains a novel data acquisition method that supports accurate, synchronized, wide-area power flow summation at fixed intervals. This method uses the power calculated within the protective relays at each substation. The calculated power in each relay is published as analog data within IEC 61850 GOOSE messages. The system requires constant supervision of the communications status and the synchronization of the distributed time. A failure alarm for either of these supervised processes causes the data to be sent from the relays to the system's redundant central processing units (CPUs). This is done with standardized IEC 61850 communications protocols and IEC 61131 logic algorithms.

A set of redundant centralized controllers executing algorithms with an IEC 61131 logic engine validates the incoming repetitive IEC 61850 GOOSE messages. Power calculations are triggered and published at the same instant in the protective devices at all four substations. The power in each relay is calculated at a fixed rate, typically 2.5 ms. To preserve bandwidth and reduce computation at the HVDC controller, the calculated power from each of the protective relays is transmitted to the HVDC instead of the individual voltage and current signals. The calculated active power values are uniquely labeled and published as the contents of IEC 61850 GOOSE messages as soon as they are available. The centralized controller validates the communications status, relay time synchronization status, and message delivery latency due to network congestion. This innovative data acquisition method using IEC 61131 logic synchronizes the IEC 61850 GOOSE contents to compensate for the nondeterministic behavior of Ethernet-based message exchange.

Due to the mission-critical nature of the system, various contingency scenarios to improve the availability and dependability of the system were identified. Several new hardware and software redundancy methods within the system improved the dependability and security of the control system.

This paper describes a new high-speed data acquisition system with precise time synchronization. The paper also discusses strategies used in the design of the HVDC controller, as well as special considerations in the design of the communications network.

II. Background

The HVDC link between France and Spain will result in the reliable delivery of electric power and ensure that the increasing distributed generation in the region can be integrated into the power system without compromising the stability of the power system. Additionally, this link will be instrumental in doubling the present energy exchange capacity of 1,400 MW between the two countries.

The two converter stations for the HVDC link are situated in Baixas, France, and Santa Llogaia, Spain. The Modos de Funcionamiento del Enlace (MFE) system is installed in the Santa Llogaia converter station. The MFE system feeds precise analog signals to adjust power flows and to allow correct operation of the converter based on the present real-time condition of the Spanish ac power system. The real-time power measurements are collected using various modern intelligent electronic devices (IEDs) distributed throughout the Spanish-French border. Fig. 1 shows the geographical location of the various substations that have these IEDs installed. The IEDs send both analog and digital information using high-speed IEC 61850 GOOSE messages to two redundant CPUs located in the Santa Llogaia converter station. The station architecture consists of two identical systems operating independently.

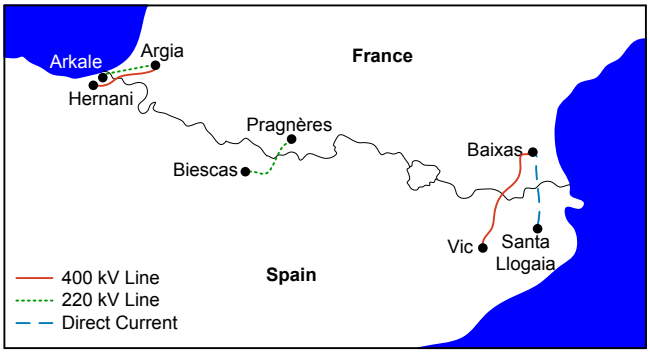

Fig. 1. Geographical locations of the interconnections between Spain and France.

The following signals are sent over the wide-area network (WAN) to the CPUs:

- Locally calculated power flow (active power only) in different Spain-to-France interconnections.
- Statuses of the lines (in or out of service) in the nearest area of influence.
- Frequency.
- Supervision status of system health parameters.

III. System Requirements

A. Hardware Requirements

Because of the mission-critical nature of the application, the devices used in the field have very strict requirements. All of the field devices and CPUs must have a low failure rate, as indicated by their mean time between failures (MTBF) and the ability to withstand a temperature range from –40 to +85°C. Because data validation, computation, and decision-making are performed in redundant CPUs, these devices had the following stringent requirements:

- High-speed communications. The system must support standardized communications to provide high-speed, low-latency, deterministic, and reliable communications links between the CPUs and the I/O modules. EtherCAT® was chosen because it is an Ethernet-based fieldbus protocol designed exclusively for deterministic high-speed data acquisition and to serve control applications on a dedicated Ethernet network. EtherCAT messages combine data from multiple EtherCAT nodes into a single message as large as 4 GB. EtherCAT directly transfers data between modules without encoding or decoding messages, thereby providing a high-speed data exchange. This process is initiated by an EtherCAT master executing an application that starts the EtherCAT messages on a fixed interval and evaluates them on return. EtherCAT messages are designed to optimize the frame size for speed and determinism [2] [3] [4].
- Event recording and retrieval capabilities. The CPUs must be able to record sequential events records for all of the associated I/O modules distributed throughout the field.
- An IEC 61131 logic engine. The CPUs must support IEC 61131-3 programming languages and provide the flexibility to write custom function blocks.
- High-speed processing. The CPUs must have high-speed processing capabilities to synchronously process the time-aligned data acquired via various I/O modules.
- Hardware modularity. The CPUs must have expandability to allow for use at multiple sites with different numbers and variations of combined analog and I/O modules.
- Multiple communications ports. The CPUs must be able to support multiple communications ports to communicate data to multiple centralized servers both in-band on the Ethernet network and out-of-band.
- A built-in human-machine interface (HMI). The CPUs must have a built-in, web-based HMI for viewing the health and status of field devices [4].

B. Software Requirements

The system required very robust software designed to avoid a single point of failure in either the hardware or software. Simultaneous executions of multiple applications with different performance requirements were carried out. The ability to segregate the software into multiple threads with unique processing rates was a requirement. In addition to reducing the probability of error, this modular processing structure also provides future expandability. Various specific function blocks also needed to be built.

C. Performance Requirements

One of the biggest challenges of the MFE system was to create an analog output command signal for the HVDC controller within 40 ms of any change in the power flow at any one of the four monitored substations. A 10 ms budget for the HVDC controller to process the signal as an analog input and react guarantees that the maximum time between the instant that the ac power changes at any one of the substations and the output of the HVDC controller is less than 50 ms.

This 40 ms MFE system time budget includes the unavoidable latency of the Ethernet messages traveling hundreds of kilometers through two local-area networks (LANs) and the WAN multiplexer system. After reviewing the WAN system technology, the worst-case message delivery latency across the network was predicted to be 10 ms. Based on this, the engineering team accepted 30 ms (40 ms overall minus the 10 ms worst-case WAN communications time) as the maximum processing time budget of the devices, LAN communications, and CPU decision-making logic.

IV. Choosing the Appropriate Digital Message for Analog Data

This application requires that the message containing analog ac power system data travel from the substation to the central CPU within 10 ms. Although publishing analog data within Ethernet messages is similar to publishing Boolean data, adding analog values to the payload of Ethernet telegrams makes the messages much larger and requires more processing to publish and receive the data. Therefore, analog data exchange increases the burden on the network as well as the IEDs, which adversely affects the applications if best engineering practices are not followed for correct system design.

Because of stringent application performance requirements, it was essential to select a reliable and high-performance data exchange mechanism. Two high-speed analog protocol technologies were considered and compared for the application. IEEE C37.118 synchrophasor message and IEC 61850 GOOSE message exchange mechanisms were tested to evaluate their ability to satisfy the required system performance. The IEDs used in this project are protective relays with customizable logic that support IEC 61850 GOOSE messages and also perform as phasor measurement units (PMUs) via the publication of IEEE C37.118c synchrophasor messages.

A. Synchrophasor Messages

Synchrophasors are used to solve a variety of power system protection, automation, and control challenges. Synchrophasor information is readily available and straightforward to acquire via IEEE C37.118 protocol. Synchrophasors are often used to operate and manage multiple power system applications such as voltage stability assessment, islanding of distributed generation, control based on the detection of small signal instabilities, and system-wide disturbance monitoring. Synchrophasors solve the time incoherence of distributed data by time-stamping the data and then aligning measurements to a common time reference for processing.

IEEE C37.118.2™-2011 describes a method for the real-time exchange of synchronized phasor measurement data between power system devices [5]. This standard specifies messaging that can be used for real-time communication between PMUs, phasor data concentrators (PDCs), and other applications and synchrophasor clients. The synchrophasor message includes information related to single-phase or three-phase positive-, negative-, or zero-sequence values. Data may be in a rectangular format with real and imaginary values or in a polar format with a magnitude and angle. Messages may also contain information on frequency as well as anonymous digital status information and other sampled analogs, such as control signals or transducer values. These anonymous values are published as generic values not specifically identified within the standard and are decoded and understood by the client. For example, if the relay was programmed to calculate instantaneous ac power values, these could be published as anonymous analogs in addition to the standardized raw data in a rectangular or polar format.

Synchrophasor protocol clients receive messages from PMUs and calculate ac power system values from the mandatory raw phasor values. Phasor representations of sinusoidal waveforms are calculated from the real and imaginary parts of the complex values in rectangular components. The synchrophasor message also includes time-stamp values called seconds of century (SOC) and fraction of second (FRACSEC). SOC is the count of seconds since midnight of January 1, 1970, when the message was created. This SOC value has a range of 136 years, is constantly growing larger, and will roll over in the year 2106. FRACSEC provides fractional second and time quality information when divided by the time base value. The synchrophasor client can use this large SOC + FRACSEC quantity to identify messages from multiple PMUs published at a similar point in time. Then the client can calculate synchronized values, including the instantaneous real-power magnitude for each remote subsite PMU location.

One design consideration was to have the CPU act as a synchrophasor client and calculate ac power flow values. Once calculated, custom logic in the synchrophasor client would have been used to sum the magnitudes of instantaneous power from several PMUs to create the required aggregate power flow for the MFE application. Using this method, the CPU would have been responsible for executing all of the

decision-making logic, acting as a synchrophasor client, calculating instantaneous power magnitudes from the raw values from each PMU, synchronizing values measured at the same SOC, and creating the aggregate power flow. Alternatively, the relays could calculate and publish power information as anonymous values, and the CPU synchrophasor client could decode and use those values. This would free the CPU from performing the individual power calculations in addition to the decision-making logic.

According to IEEE C37.118.2-2011, it is mandatory that PMUs support data reporting at submultiples of the nominal power-line system frequency [5]. Support for other reporting rates is permissible. Higher rates are encouraged but not mandatory and are, therefore, manufacturer-specific. Required publication rates are documented for both 50 Hz and 60 Hz systems as the number of messages, or frames, per second. For 50 Hz systems, the standard requires that the PMU support 10, 25, and 50 messages per second. For 60 Hz systems, the standard requires that the PMU support 10, 12, 15, 20, 30, and 60 messages per second. The actual rate to be used must be user-selectable. The PMU relays used in this project meet the mandatory reporting rates but do not support faster rates. The power system frequency of this system is 50 Hz, so the fastest standardized data interval is every 20 ms. Although this frequency supports all the other applications mentioned previously, it is too infrequent to satisfy the overall system time requirement. The design team chose not to consider faster publication frequencies because they would be specific to a particular PMU. Therefore, the design team looked for a different method to get values from the remote substations more frequently.

B. IEC 61850 GOOSE Messages

IEC 61850 GOOSE messages are flexible and can be configured to contain any values available from the PMU or IED. Rather than publish raw values, custom logic calculates and publishes the instantaneous power magnitude from each IED. Each IED is synchronized to an IRIG-B time source, and the execution of the calculations is synchronized to the IED clock. The IED increments and includes a calculation sequence number with the power value in each GOOSE message publication. The sequence numbers are reset at the top of each second so that they stay small and accurately synchronized. Processing of this small sequence number is much less intensive than the larger SOC + FRACSEC quantity in the synchrophasor payload.

GOOSE messages are published at a fixed rate when no data are changing and also immediately after a change is detected. This change can be the toggle of a binary status or an analog value passing through a reporting dead band. Custom logic was written to toggle the value of an IED logic bit. When this point was added to the GOOSE payload, it provoked a new GOOSE publication each time this logic bit toggled. Using this mechanism, the IED was configured to calculate and publish instantaneous power magnitudes at a fixed frequency regardless of whether or not power values changed. Altering the frequency that the logic toggles the logic bit changes the frequency of the GOOSE publication. This can be done as fast as every IED operating cycle, which is every 2.5 ms on a 50 Hz system. Therefore, GOOSE messages can publish almost 10 times more frequently than synchrophasor messages.

Another advantage of GOOSE messages is that the IEDs publish them with an IEEE 802.1Q virtual LAN (VLAN) tag. This tag is used by the LAN and WAN devices to correctly and precisely deliver the messages to each appropriate device.

C. Distributed Versus Centralized Computation

The design team considered a centralized system where all of the power calculations and logic processing would be performed by the CPU after receiving raw measurement quantities from the remote substations. The team also considered a design where power calculations and decision logic were distributed and performed by relays in the remote substations to simplify the CPU decision-making logic and data processing.

This system takes advantage of both methods. Distributed computation of the power metering values in the various IEDs allows optimization of overall performance. Because of the high-speed data exchange requirements of the application, distributed logic makes it feasible to share the processing burden over multiple processors distributed over a geographical location. Also, system logic installation and testing is simplified when done via repetitive remote installations of identical relay logic as opposed to a larger centralized process.

While power calculation and station performance and health diagnostics are distributed within the remote IEDs, power aggregation, dc control system strategies, and system-wide performance and health diagnostics are centralized in the system controllers.

The provisioning of WAN communications requires a careful allocation of bandwidth for each communications channel. Distributed calculation of power within the relays allows them to publish smaller messages containing information rather than larger messages containing raw voltage and current values. Within GOOSE messages, 7 bytes are required to transfer each additional encoded floating-point analog value, such as power. Messages with both current and voltage values require an additional 14 bytes, while the single power value adds only 7 bytes. The 50 percent reduction in bytes for analog data in the GOOSE message payload translates into a reduced burden on the WAN communications system. Smaller messages also reduce the likelihood of a disruption caused by data loss or corruption. Also, when a message is smaller, it reduces processing burden and improves control signal delivery time.

It is also important to understand that bandwidth allocation for wide-area control messages is very different than allocating bandwidth for data collection. Design for data collection is generally done by understanding the amount of data in bytes that needs to be transferred each second. Then, bandwidth is allocated to satisfy the appropriate number of bytes per second (Bps) or bits per second (bps) as a

throughput calculation. However, control messages are generally small (161 bytes in this system) and need to travel in a fraction of a second.

Traditional bandwidth allocation would design a system to deliver this 161-byte control message within 1 second (i.e., 161 Bps). However, the total control system time is 50 ms, and the message delivery must be a subset of that. Therefore, control message bandwidth allocation must be done differently to satisfy message delivery time. For example, assuming that the message needs to travel across the WAN in 10 ms, a bandwidth to support 161 bytes in 10 ms is needed (i.e., 16.1 KBps or 128,800 bps). This control system bandwidth allocation design to satisfy speed performance is 100 times larger than a typical throughput design. Each additional analog value increases the message size by 7 bytes, which increases the required WAN bandwidth allocation by 700 Bps or 5,600 bps.

V. Feasibility Study

As mentioned previously, it was not feasible to meet the system requirements using the IEEE C37.118 protocol. New technology, and available Ethernet and message parameters, satisfied the speed requirements using IEC 61850 GOOSE messages in a carefully designed system. The relays calculate the power values every operating cycle (every 2.5 ms in a 50 Hz system). The design team assumed worst-case time to create and publish a GOOSE message to be 9.5 ms, CPU processing time to be 8 ms, and generating an analog output to be 8 ms. Then, with a worst-case 1 ms for GOOSE messages to transit both the substation and central LAN, the initial MFE system time budget became 40 ms, as shown in Fig. 2.

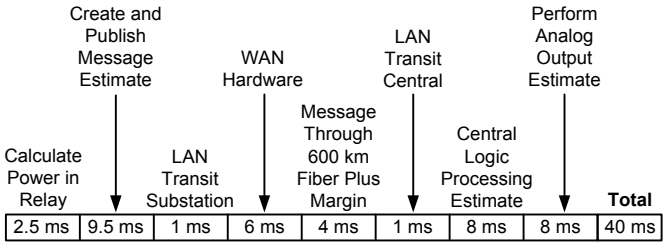

Fig. 2. Initial MFE system time budget.

However, because of the nondeterministic nature of Ethernet and GOOSE messages, as well as the large payload, a feasibility study was required to verify the performance of the technology. Fig. 3 shows a test setup where the synchronized logic IED (SLI1) invokes a test in the CPU and the field device (FD) records the test start and resulting control output from the CPU. For laboratory tests, the MFE system hardware was staged with an HVDC control simulator. The time budget was a combination of the MFE system application and LAN times of 30 ms maximum plus the 10 ms for the HVDC simulator for a total of 40 ms.

This testing revealed that the IEDs were capable of publishing GOOSE messages each operating cycle immediately after calculating power flow values. This meant that the MFE budget could be reduced to 29.5 ms, as shown in Fig. 4.

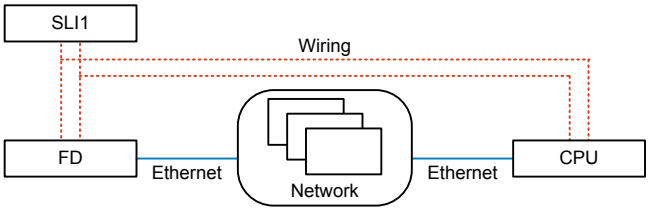

Fig. 3. Setup of test bench.

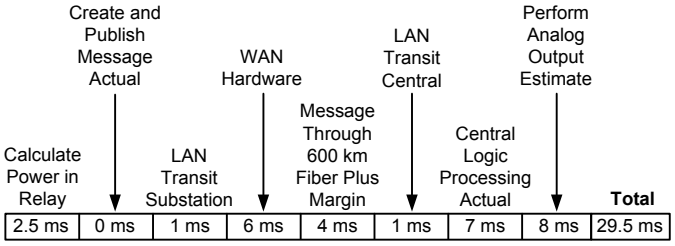

Fig. 4. MFE system time budget adjusted for no message delay.

Even though it is possible to publish a GOOSE message with no delay after the power flow calculation, the design team chose to add a delay for the sole purpose of reducing the WAN system bandwidth use. This delay was predicted and proven to not adversely affect the overall application time. Tests showed that even with a delay of three additional operating cycles, or 7.5 ms, the time budget was still under 40 ms at 37 ms, as shown in Fig. 5.

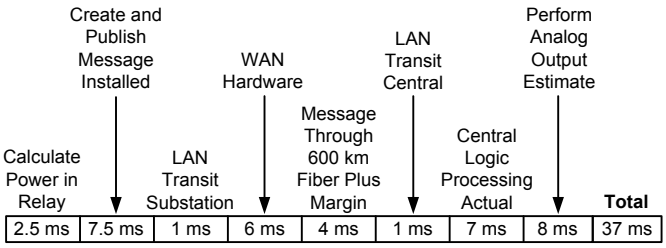

Fig. 5. MFE system time budget adjusted for three-operating-cycle message delay.

Next, the system was staged and tested end-to-end with a device simulating the HVDC controller receiving and acting on the analog output from the MFE system CPU. The results shown in Fig. 6 demonstrate that the system operated even faster than expected. Fig. 6 shows a waveform capture of the typical test results as captured by the field device.

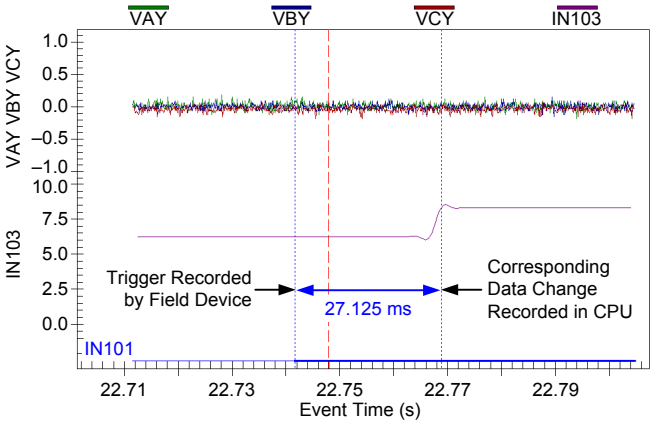

Fig. 6. Waveform showing trigger and response time.

The left vertical dashed line indicates the trigger recorded by IN101 on the field device. The right vertical blue dashed line represents the resulting change of the control output from the CPU recorded by IN103 on the field device. This example shows the time duration between a sudden change of power flow in a field device and the resulting analog output of the CPU to the HVDC controller to be 27 ms. All of the test results were well under the 40 ms design maximum and verified the performance of the design. Further testing with an oscilloscope showed that the device used for the CPU was much faster at producing the analog output than the budgeted 8 ms, as shown in Fig. 7.

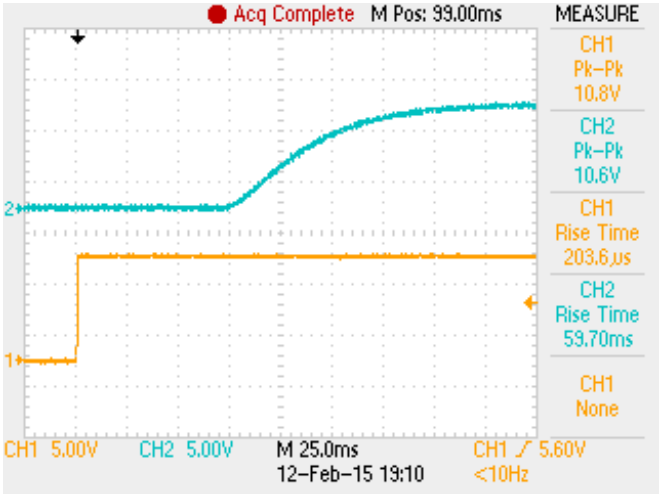

Fig. 7. CPU hardware displayed as CH1.

Channel 2 in Fig. 7 illustrates an analog output reaction time for a typical power system IED. Channel 1 illustrates that the speed of the chosen hardware for the CPU is so fast and efficient that it typically produces an analog output in 0.2 ms.

With this information about the capabilities of the CPU device and the end-to-end test times, the MFE system time budget was amended to 29.2 ms, as shown in Fig. 8.

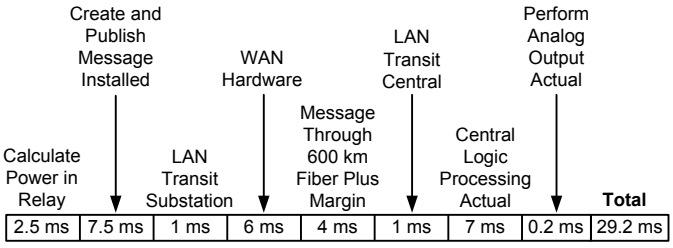

Fig. 8. MFE system time budget adjusted for three-operating-cycle message delay.

These tests also demonstrated that when combined with the actual WAN and HVDC control times, the total system operates well under the 50 ms threshold.

These test results for GOOSE message generation, publication, and transit times verify performance for correctly configured IEDs, controllers, and network devices. Best-known methods for precise GOOSE performance include methods described in multiple international standards. These methods and the associated standards include the following:

- Create message segregation via unique VLAN ID per GOOSE message (IEC 61850 [6] and IEEE 802.1 [7]).
- Create message segregation via unique multicast media access control (MAC) addresses per GOOSE message. (IEC 61850 and IEC 15802 [8]).
- Assign unique application identifier (APP ID) per GOOSE message (IEC 61850).
- Match last octet of MAC Address, VLAN ID, and APP ID.
- Use message priority tags based on mission-critical nature of communications-assisted application (IEC 61850 and IEEE 802.1).
- Assign descriptive rather than generic GOOSE ID (IEC 61850).
- Use descriptive textual name and VLAN ID.
- Carefully design dataset contents and message retransmission properties (IEC 61850 and IEC 60834 [9]).
- Choose IEDs and switches that immediately publish, transmit, and react to GOOSE messages (IEC 61850 and IEC 60834).
- Select root bridge Ethernet switch and IED ports based on actual network performance in primary and reconfigured state (IEC 61850 and IEEE 802.1).
- Ethernet switches must be tested and verified to satisfy reconfiguration times of 15 ms. These methods must be based on standardized spanning tree algorithms (STAs) and Rapid Spanning Tree Protocol (RSTP) rather than proprietary solutions (IEC 61850, IEC 60834, and IEEE 802.1).
- Mission-critical applications must be served by redundant devices as well as redundant communications (IEC 61850).
- All network multicast messages must have a unique VLAN ID and MAC address. All untagged traffic must be tagged with port-based VLAN (PVLAN) 1001 at ingress to the Ethernet network (IEC 61850 and IEC 60834).
- All unused IED and switch communication ports must be disabled. All network engineering ports must have static MAC address filters to prevent all but known engineering laptops (NERC CIP [10] [11] and NERC PRC-005 [12]).
- All IEDs must monitor the multicast message sequence number and state number to supervise data exchange via digital messaging (IEC 61850 and IEC 60834).
- All IEDs must create GOOSE diagnostic reports, including performance and reliability statistics and real-time operational information for each published and subscribed GOOSE message (IEC 61850 and IEC 60834.

- Each IED must supervise all GOOSE attributes to detect and alarm abnormal behavior via the front-panel display, supervisory control and data acquisition (SCADA) alarms, and email to technicians (IEC 61850 and IEC 60834).
- Each IED must time-stamp and create a sequential events record for each GOOSE message failure and then react to the failure by modifying logic as well as local and remote applications to reflect that communications-assisted data acquisition has failed (IEC 61850 and IEC 60834).

VI. System Description

The control system requires that the sum of the active power flows through all of the ac interconnection lines be sent to the HVDC controller. As mentioned previously, the system must satisfy the stringent design requirement for detection and notification of a change in power flow within 40 ms. Fig. 9 shows a simplified diagram of the substations involved in the project. These substations send analog and binary GOOSE messages to Santa Llogaia, the HVDC controller substation.

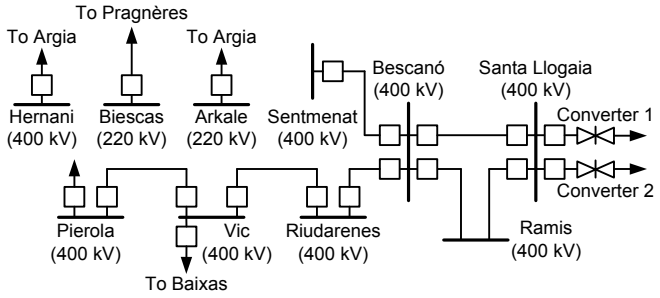

Fig. 9. Simplified substation layout.

A. Communications Architecture

Fig. 10 shows a simplified diagram of the communications architecture of the system.

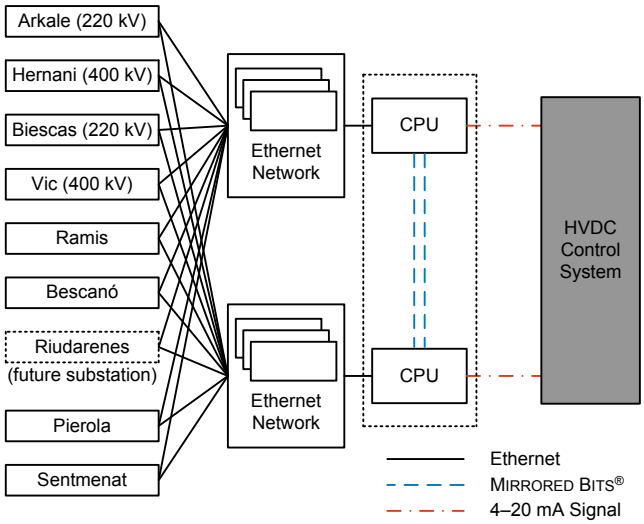

Fig. 10. Communications architecture.

The centralized station receives Ethernet traffic from each of the substations via a WAN. The WAN is built using multiplexers at each substation and is connected to an Ethernet LAN in each substation. Each LAN includes a field IED communicating Ethernet messages (including GOOSE) through the LAN and into the WAN via the multiplexer. The WAN distances for the stations vary from 80 to 600 km. Calculations based on the time to transfer data through fiber plus an appropriate safety margin reveal that direct GOOSE transfer takes approximately 4 ms. The WAN team predicted that the additional latency caused by entering the source multiplexer hardware, passing through interim multiplexers, and exiting the multiplexer at the HVDC station would be approximately 6 ms. Therefore, the WAN team accepted a 10 ms worst-case message delivery time for power flow data transfer from substations to the centralized station.

This leaves a 30 ms margin for the remaining IED power flow calculation, GOOSE publication, GOOSE message transit across both the substation and centralized station LAN, CPU decision logic at the centralized station, and the analog output.

B. Centralized Station

The centralized station consists of redundant CPUs that subscribe to IEC 61850 GOOSE messages from field devices. The CPUs run innovative IEC 61131 logic algorithms to ensure data validity, verify synchronization, and output analog information in the form of 4–20 mA signals. These signals are then fed to the HVDC controller.

VII. CPU Logic Algorithm

IEC 61131 Structured Text (ST) and Continuous Function Chart (CFC) languages were used to write innovative data processing and system redundancy logic. Fig. 11 shows various logic processing steps inside the CPU. Software redundancy provides resilience to the system against multiple hardware and software failure scenarios.

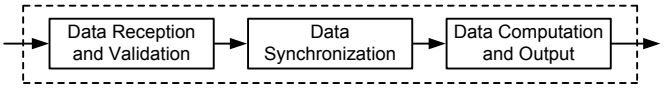

Fig. 11. Stages of data acquisition logic.

VIII. Conclusion

By using modern data acquisition field devices, following proven network engineering best practices, and using rugged and modular centralized controllers, it is possible to achieve high-speed, wide-area control that uses real-time analog measurements and interconnects multiple substations spanning hundreds of kilometers.

IX. References

[1] D. Dolezilek, F. Calero, A. Kalra, B. Waldron, J. M. Herrera, M. S. Mingarro, and S. L. Barba, "Innovative Data Acquisition and Redundancy Methods Enable Previously Impractical High-Speed, Wide-Area Control," proceedings of the 13th International Conference on Developments in Power System Protection, Edinburgh, Scotland, March 2016.

[2] D. Dolezilek, N. Fischer, and R. Schloss, "Improvements in Synchronous Wide-Area Data Acquisition Design and Deployment for Telecontrol and Teleprotection," proceedings of the 14th Annual Western Power Delivery Automation Conference, Spokane, WA, March 2012.

[3] M. Vaughan, R. Schloss, S. Manson, S. Raghupathula, and T. Maier, "Idaho Power RAS: A Dynamic Remedial Action Case Study," proceedings of the 64th Annual Georgia Tech Protective Relaying Conference, Atlanta, GA, May 2010.

[4] D. Kirby, N. Fischer, A. Kalra, and D. Haes, "Case Study: Centralized Ground Fault Detection System for LADWP Ungrounded Distribution System," proceedings of the 41st Annual Western Protective Relay Conference, Spokane, WA, October 2014.

[5] IEEE Standard C37.118.2™-2011, IEEE Standard for Synchrophasor Data Transfer for Power Systems.

[6] IEC 61850, Communication Networks and Systems in Substations.

[7] IEEE 802.1Q-2014, IEEE Standard for Local and Metropolitan Area Networks – Bridges and Bridged Networks.

[8] IEC 15802, Information Technology – Telecommunications and Information Exchange Between Systems – Local and Metropolitan Area Networks – Common Specifications.

[9] IEC 60834, Teleprotection Equipment of Power Systems – Performance and Testing – Part 1: Command Systems.

[10] NERC CIP-003, Cyber Security – Security Management Controls.

[11] NERC CIP-007, Cyber Security – Systems Security Management.

[12] NERC PRC-005-2, Protection System Maintenance.

X. Biographies

Javier Martín Herrera is an electrical engineer with Red Eléctrica de España (REE) in Madrid, Spain. He received a B.S.E.E. degree from the Universidad Carlos III of Madrid in 2002 and joined REE in 2003. He has worked on protection coordination on the Spanish high-voltage power system and is currently involved in protection studies for the Interconnexion èlectrique France Espagne (INELFE) project and the high-voltage dc (HVDC) interconnection between France and Spain.

Matias Sanchez Mingarro is a substation project technical leader at Red Eléctrica de España. He is the engineering manager for control and protection systems and the head of quality and regulation in the substations engineering department. He has an M.Sc. in industrial engineering from Pontificia de Comillas University ICAI in Madrid. He is presently working as a control and protection systems manager for the Interconnexion èlectrique France Espagne (INELFE) project.

Santiago López Barba is the head of the system security department at Red Eléctrica de España (REE) in Madrid, Spain, where he has worked since 2003.

David Dolezilek received his B.S.E.E. from Montana State University and is the international technical director at Schweitzer Engineering Laboratories, Inc. He has experience in electric power protection, integration, automation, communication, control, supervisory control and data acquisition (SCADA), and energy management systems (EMSs). He has authored numerous technical papers and continues to research innovative technology affecting the industry. Mr. Dolezilek is a patented inventor and participates in numerous working groups and technical committees. He is a member of the IEEE, the IEEE Reliability Society, CIGRE working groups, and two IEC technical committees tasked with the global standardization and security of communications networks and systems in substations.

Fernando Calero received his B.S.E.E. in 1986 from the University of Kansas, his M.S.E.E. in 1987 from the University of Illinois (Urbana-Champaign), and his M.S.E.P.E. in 1989 from the Rensselaer Polytechnic Institute, Troy, NY. From 1990 to 1996, Mr. Calero worked in Coral Springs, Florida, for the ABB relay division in the support, training, testing, and design of protective relays. Between 1997 and 2000, Mr. Calero worked for Itec Engineering, Florida Power & Light, and Siemens. Since 2000, Mr. Calero has worked for Schweitzer Engineering Laboratories, Inc. as an application engineer in international sales and marketing, providing training and technical assistance. He is presently a senior automation systems engineer in the international technology group.

Amandeep Kalra is an automation systems engineer with Schweitzer Engineering Laboratories, Inc. (SEL) in Bothell, Washington, with several years of experience in designing automation systems and communications networks. He has authored numerous technical papers focusing on IEC 61131-based automation controllers, Ethernet networks, and Ethernet-based communications protocols as well as IEC 61850 communications standards. He has represented SEL at various international conferences and IEC 61850 interoperability demonstrations organized by Utility Communications Architecture (UCA) and frequently teaches engineering design and application of IEC 61850 solutions. He has a bachelor of technology degree in instrumentation and control engineering from the National Institute of Technology, India, and a master's degree in electrical engineering from California State University, Northridge.

Brian Waldron is an automation engineer with Schweitzer Engineering Laboratories, Inc. (SEL) in Pullman, Washington. He has several years of experience in designing and troubleshooting automation systems and communications networks. He has authored several application guides focusing on integrating automation products. He has represented SEL at IEC 61850 interoperability demonstrations organized by Utility Communications Architecture (UCA) and frequently teaches engineering design and the application of IEC 61850 solutions. Brian graduated from Gonzaga University with a B.S. degree in electrical engineering.