SEL Application Note AN2013-34

Protection Against Simultaneous Faults Using Logic Processors and Digital Relays

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INTRODUCTION

The need to improve service availability has increased the complexity of distribution network topology. During distribution system preventive or corrective maintenance or in abnormal power system network conditions, switching operations frequently leave several circuits fed from a single source. Furthermore, limitations on the rights of way make it necessary to use double-circuit overhead lines or single-circuit lines that run close to each other. All these factors have increased the frequency of distribution system faults that involve more than one circuit. These faults are known as simultaneous faults.

PROBLEM

During simultaneous faults in distribution systems, the backup protection on the transformer low-voltage side can misoperate. This impairs protection selectivity and affects service availability in circuits not involved with the fault. The cause of this possible misoperation is that the transformer overcurrent relay low-voltage side measures the total fault current (sum of the currents on all the faulted circuits) plus the load currents from the unfaulted circuits, while the overcurrent relay of each faulted feeder measures only the feeder fault current. As a result, the transformer inverse-time relay low-voltage side measures a current that is greater than the current measured by the inverse-time feeder relay. Thus, the transformer relay can trip faster than the feeder relay.

It is important to remember that the most critical condition for coordinating these two inverse-time overcurrent relays occurs at the maximum fault current (the same current value for both relays). This is the condition for which both curves have the minimum separation, corresponding to a typical coordination interval between 0.2 and 0.4 seconds.

SEL SOLUTION

The proposed SEL solution depicted in Figure 1 shows the logic diagram for a protection scheme that solves the problem of misoperation due to simultaneous faults.

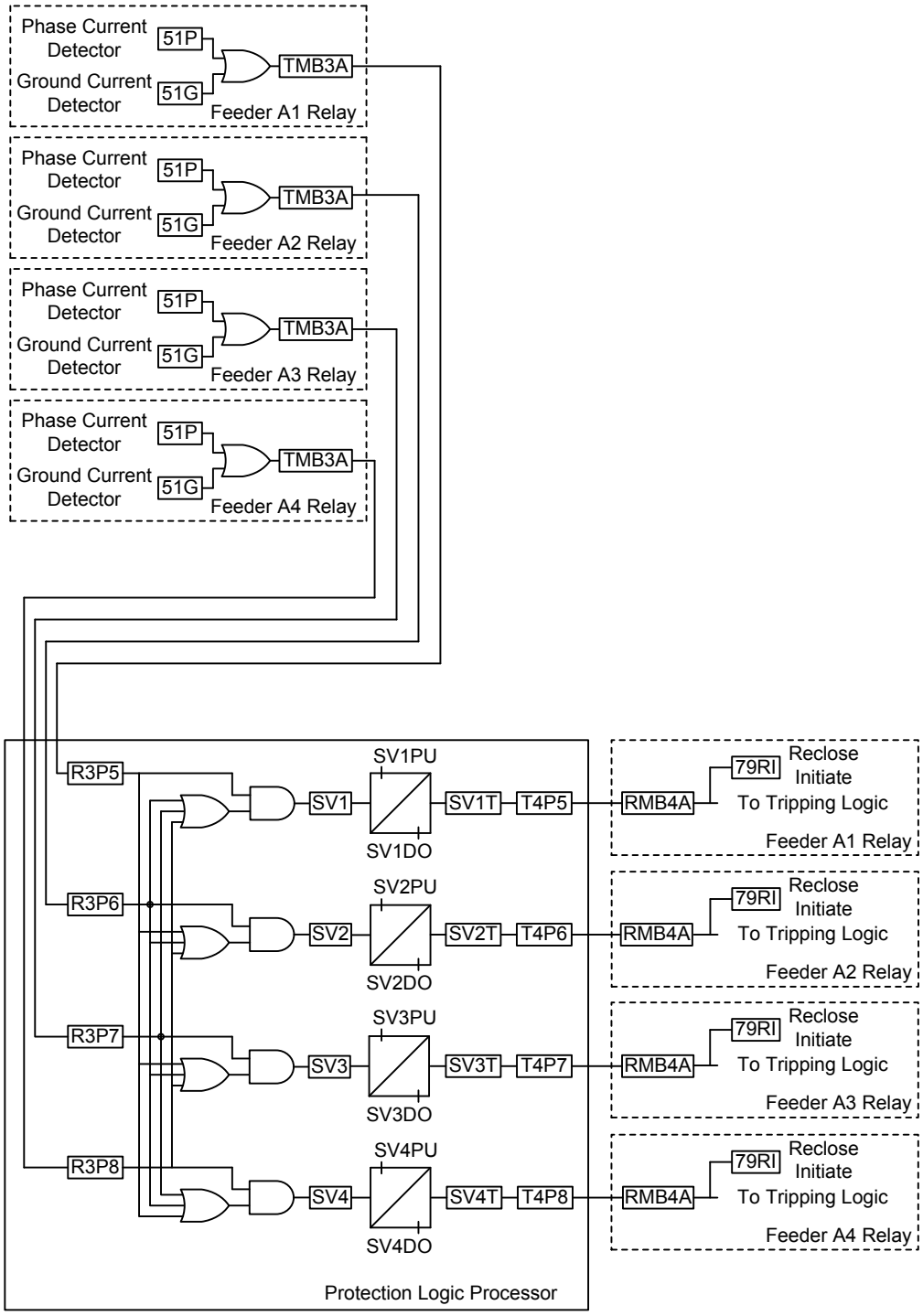

Figure 1 Logic for Protection Against Simultaneous Faults

When a simultaneous fault occurs (i.e., in Feeders A1 and A2), the 51P and/or 51G elements of the relays related to these feeders operate and send information to the protection logic processor. We can use an SEL-2100 Logic Processor or an SEL-3530 Real-Time Automation Controller (RTAC) for this functionality (see Figure 2).

Figure 2 Communications Architecture Using (A) SEL-2100 or (B) SEL-3530 for Simultaneous Fault Clearing

The protection logic processor, after a programmed security delay of 3 cycles, declares that the two feeders have a simultaneous fault by activating the logic variables SV1T and SV2T. Each one of these variables starts the tripping logic of the corresponding feeder relay in order to clear the fault in a secure and dependable fashion. The almost instantaneous breaker operation at the faulted feeders guarantees coordination with the transformer relay low-voltage side. Because the fault type is already known, at the time of tripping the feeder breakers can also start a reclosing logic to attempt automatic power restoration. The operator receives an alarm indicating the fault type. With this information, the operator can take the appropriate actions to guarantee fast power service restoration.

There are several ways to apply this solution. One of the options is to use an SEL-2100 and protective relays that can communicate using MIRRORED BITS® communications. Another possible solution is to use an SEL-3530 and protective relays that can communicate using MIRRORED BITS communications or IEC 61850 Generic Object-Oriented Substation Event (GOOSE) messages.

This solution can be a part of any integrated system for distribution because of its excellent, fast, and dependable performance and advantage in improving the operation of distribution systems.

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