Line Differential Protection Under Unusual System Conditions

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Published in
Line Current Differential Protection: A Collection of Technical Papers Representing Modern Solutions, 2014

Previously presented at the
PAC World Africa Conference, July 2013,
and 67th Annual Georgia Tech Protective Relaying Conference, May 2013

Originally presented at the
39th Annual Western Protective Relay Conference, October 2012

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***Abstract*—It is common knowledge that the line current differential protection principle is not susceptible to unusual system conditions. This is true and straightforward regarding protection security but is not immediately obvious when considering dependability of protection. As a result of dismissing the impact of unusual system conditions, the effect of power swings, weak systems, inverter-based short-circuit current sources, series compensation, or open-pole conditions on line current differential protection is not well understood.**

This paper briefly touches on protection security but focuses on the dependability of line current differential protection under a number of specific system conditions, including series compensation, weak systems, open-pole conditions, power swings and off-nominal frequency, and inverter-based sources. This paper reviews the impact of each of the mentioned conditions and provides illustrations using simulations.

I. Introduction

The current differential principle is a powerful short-circuit protection method. Responding to all currents bounding the zone of protection, the principle has a very high potential for both sensitivity (effectively, it sees the total fault current at the fault location) and security (effectively, it sees an external fault current flowing in and out of the protection zone). Also, differential protection is typically easy to apply because it does not require elaborate short-circuit studies and settings calculations.

In its application to power lines, the line current differential (87L) principle is typically not affected by weak terminals, series compensation, changing short-circuit levels, current inversion, power swings, nonstandard short-circuit current sources, and other issues that may cause problems for single-ended protection techniques (protection based on measurements from a single line terminal) [1]. These advantages, combined with the increasing availability of long-haul, utility-grade digital communications channels, such as direct fiber or synchronous optical network (SONET) networks, accelerate the rate of new 87L installations.

This paper discusses a number of special power system operating conditions and their impact on 87L protection. After discussing line protection security and dependability in general terms (Section II), we focus this paper on the dependability of 87L protection, including sensitivity in series-compensated lines (Section III), under weak system conditions (Section IV), during single-pole tripping and reclosing (Section V), under power swings and frequency excursions (Section VI), and when applied near inverter-based sources (Section VII).

This paper promotes the application of phase, ground, and negative-sequence differential elements [2] in parallel with addressing dependability concerns during these demanding conditions. The inherent security of the differential elements, combined with their diverse responses to internal faults under unusual system conditions, is the primary reason behind our key recommendation.

II. Security and Dependability of 87L Elements

A. Protection Security Versus Dependability Under Stressed System Conditions

The art of protective relaying is a constant balance between the capacity to detect fault conditions in protected assets and the ability to restrain from operation in all other situations. Considered separately, dependability and security of protection are easy targets. It is the necessity to satisfy both requirements simultaneously that makes protective relaying a challenging technical field.

When taken to the level of an individual relay function (such as an impedance element) and considered from the perspective of stressed system conditions (such as a power swing), security is the prevailing concern. Historically, line protection exposed to elevated load levels or power swings has been considered the triggering point for major blackouts. Therefore, securing protection elements under unusual conditions is our primary objective. Blinders or power swing blocking elements are examples of such security measures.

Again, when considered separately from dependability, securing relays under stressed system conditions is not a difficult task. Protective relays, however, are expected to protect assets under all circumstances, including abnormal system events, and must retain a certain level of dependability at all times. A transmission line with increased load or under a swing condition may still experience a fault. Moreover, it is more likely to develop a fault due to the conductor sagging effect of overloads or the overvoltage effect of a power swing. Such faults should be detected and cleared accordingly, regardless of loads encroaching on impedance characteristics or ongoing power swings.

On one level, the issue of dependability is related to the nature of the countermeasures applied for the effects of stressed system conditions. For example, when blocking distance protection using a power swing detection element, we should ensure that an unblocking function is built in and will operate if a fault occurs during the swing.

On a different level, the ability of protection elements to operate correctly may be challenged under severe system events, even if these functions are not purposefully inhibited for security reasons. Consider the concept of memory polarization in an impedance element: it works assuming the prefault and fault voltages do not differ considerably in phase. Therefore, it may fail to operate dependably under unstable power swings.

In general, protection elements face both security and dependability problems when pushed beyond their regular design limits. To provide protection under severe system conditions requires more sophisticated relaying methods. Such methods, in turn, are often more difficult to set and verify. Moreover, they do not provide the same high level of performance, but rather avoid impairing the protection system performance under stressed conditions.

In yet another aspect, protective relays, if made exceptionally secure under stressed and unusual system conditions, can have negative effects on the power system if no adequate system integrity protection is in place. Under the absence of remedial action schemes, loss of security in asset protection provides a crude, random in nature, and not optimal separation mechanism for the system. Protective relays remaining secure under major system events give more time for the remedial action schemes to take an optimal, preplanned, and controlled action. If this remedial action does not take place, the enhanced security of asset protection can inadvertently deteriorate the system as a whole.

B. Differential Protection Versus Single-Ended Protection

Differential elements respond to all the currents measured at all terminals of the protected line. When detecting internal faults and restraining for external faults and other events, they have access to considerably more information compared with any single-ended protection method.

Single-ended methods, such as impedance elements or overcurrent directional elements, including phase, ground, and negative-sequence elements, work on information from one terminal of the line only. Even when used in a directional comparison scheme, the protection elements need to perform correctly at each terminal for the entire scheme to work correctly.

Single-ended protection methods are impacted by unusual system configurations, such as series compensation, power swings, or nonstandard short-circuit sources. Both security and dependability can be affected. With security concerns addressed via element design (manufacturer) or application settings (user), the single-ended methods can face new dependability concerns, in addition to the initial issues arising from the difficult operating conditions in the first place.

One possible solution to the dependability challenge is to use diverse elements in parallel and count on their dependability gaps not overlapping with each other for any particular internal fault. For example, both ground directional and negative-sequence directional elements may be used in a permissive directional comparison scheme. This approach, however, can have a limited positive effect because each element operating in parallel impacts both dependability (favorably, because more elements have a chance to detect an internal fault) and security (unfavorably, because more elements have a chance to misoperate on no internal fault conditions).

Line current differential protection is, of course, a considerably better solution because it is inherently secure. Therefore, using diverse differential elements for dependability does not adversely impact security. The next subsection explains this concept in detail.

C. Security of 87L Elements

The differential principle is inherently secure—the sum of all currents around the protected line with no internal fault equals zero at all times, regardless of series compensation on the protected line or in the vicinity, power swings, open-pole conditions, short circuits fed from nonstandard sources, and so on.

Saturation of current transformers (CTs) can jeopardize the security of 87L elements, but modern line current differential relays incorporate fast and sensitive external fault detectors (EFDs) or similar countermeasures to secure the 87L elements for CT saturation without impacting the speed or sensitivity of protection [2] [3].

Sequence differential elements (zero and negative sequence) are often used in addition to phase differential elements. Typically, the sequence differential elements (87LG and 87LQ) are used for sensitivity [4]. They respond to differential signals created from the zero- and negative-sequence currents, respectively, as shown in Fig. 1. Their superb sensitivity stems from their restraining function being uninfluenced by the load current.

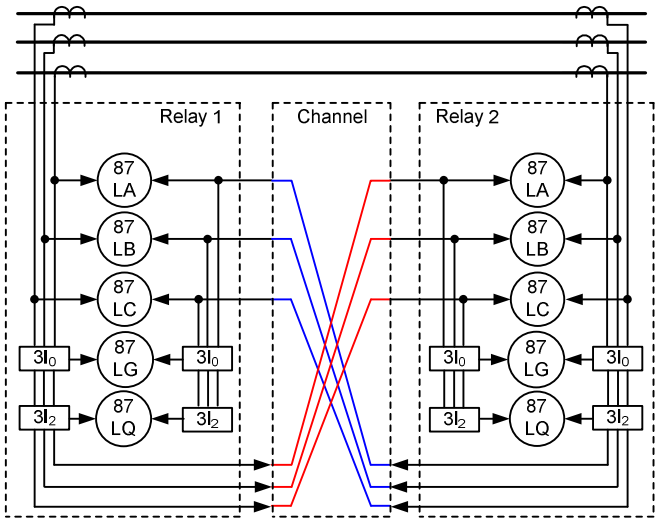


Fig. 1. Line current differential protection scheme with phase, ground, and negative-sequence differential elements.

This advantage of reduced restraint is also a weakness when considering CT saturation. For example, under phase-to-phase external faults, the 87LG element works with zero operating and zero restraining signals. Saturation of any of the CTs that carry the fault current creates a spurious differential

signal in the 87LG element that cannot be restrained with current. These elements, however, are made very secure by incorporating advanced EFD logic and other means in their design [2].

It is intuitively clear that applying phase, negative-, and zero-sequence elements in parallel improves protection dependability under unusual system conditions. Does it adversely impact security? It is our opinion that it does not.

As shown in Fig. 1, all three elements (87LP, 87LG, and 87LQ) operate on the same input currents (phase currents), measured with the same CTs, wiring, relay input circuitry, and communications channel. The sequence currents are derived by calculations from the phase quantities. These calculations are performed in the same microprocessor-based relay for all three elements. As a result, the 87LQ and 87LG elements do not have any additional failure modes compared to the 87LP elements, including possible communications impairments, CT issues, or relay issues [5].

Line charging current is another consideration for security. The charging current demonstrates itself as a spurious differential signal, and therefore, it can jeopardize 87L security. However, there are solutions to this problem, including charging current compensation, as explained in [2] and [6].

The principle of operation for the 87LQ and 87LG elements is as secure as for the 87LP elements (assuming state-of-the-art EFD logic and charging current compensation). User settings for all three elements are straightforward, and the 87LQ and 87LG elements do not bring any additional issues or opportunities for human mistakes.

As a result, applying all three elements in parallel does not erode any security, but it enhances dependability under unusual conditions, as we show in the following sections.

III. Series-Compensated Lines

Series compensation allows higher power transfers, both in steady states and transiently, by reducing the effective impedance between two areas in the system. However, the negative reactance of series capacitors can create challenges for single-ended line protection by causing current or voltage inversions that can affect directional elements, reducing the apparent impedance that can cause impedance elements to overreach, and causing subsynchronous oscillations that can require long, intentional time delays in the protection elements in order to ride through. These issues have been the subject of numerous papers and have been addressed by manufacturers using various concepts [1]. The existing solutions are focused on security and typically require extensive simulations to prove settings for any particular application on, or in the vicinity of, series-compensated lines.

As explained in Section II, line current differential elements are not concerned with security when applied in conjunction with series compensation. In this section, we look at their dependability.

A. Series Capacitors Under Fault Conditions

With reference to Fig. 2, series capacitors are installed in each phase of the transmission line and are protected against overvoltages caused by large through currents, typically with metal oxide varistors (MOVs). The MOVs start to conduct and clamp the voltage across the capacitors when the current reaches two to three times the rated value (typically). The MOVs are further protected against thermal damage by closing a bypass breaker, should the dissipated thermal energy reach unsafe levels for the MOVs. In many installations, controllable spark gaps are installed and triggered upon fault detection in as fast as 1 millisecond in order to bypass the capacitors in all three phases, regardless of the fault type or fault current level.

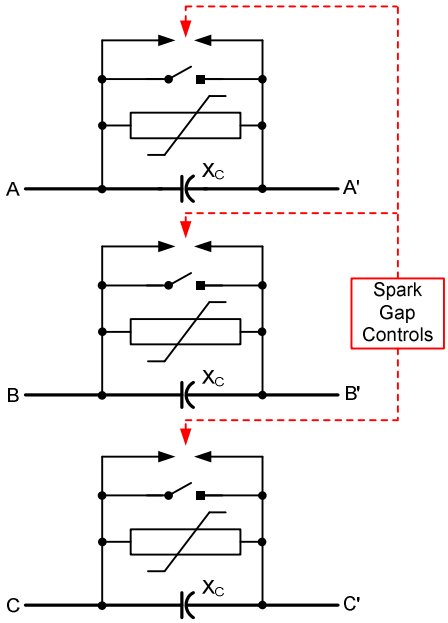


Fig. 2. Series capacitors with MOVs, bypass breakers, and controlled spark gaps.

Assuming the spark gaps are not used or before they are triggered, the MOVs control the behavior of the series capacitor installation. With the MOV voltage practically constant, the effective resistance of the MOV decreases as the current through the series capacitor installation increases. Two basic cases are worth considering: low fault currents with the MOVs not conducting at all and high fault currents with the MOV resistance being much lower than the reactance of the series capacitors (zero current through the series capacitor and all fault current through the parallel MOV).

Consider a single-line-to-ground (SLG) fault in A-phase. The impedance matrix representing the series capacitor installation can be written as (1a) for low-current faults and (1b) for high-current faults.

$$Z_{ABC} = \begin{bmatrix} -jX_C & 0 & 0 \\ 0 & -jX_C & 0 \\ 0 & 0 & -jX_C \end{bmatrix} \quad (1a)$$

$$Z_{ABC} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -jX_C & 0 \\ 0 & 0 & -jX_C \end{bmatrix} \quad (1b)$$

Note that there is no mutual coupling between the phases of the series capacitor installation. Under high-current asymmetrical faults, the impedances are different in different phases.

Converting phase impedances (1) into sequence impedances, we obtain (2a) for low-current faults and (2b) for high-current faults.

$$Z_{012} = -jX_C \bullet \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (2a)$$

$$Z_{012} = -j\frac{X_C}{3} \bullet \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \quad (2b)$$

Equation (2a) signifies that under low-current faults, all three symmetrical networks (positive, negative, and zero sequence) contain the same capacitive reactance that is equal to the physical per-phase reactance of the capacitors. Moreover, the sequence networks remain decoupled at the series capacitor installation, allowing simple fault analysis, similar to uncompensated lines.

Equation (2b) signifies that under high-current SLG faults, each sequence network contains 2/3 of the per-phase reactance of the capacitors but the sequence networks are inductively coupled at the series capacitor installation, complicating fault analysis.

The two cases are illustrated in Fig. 3.

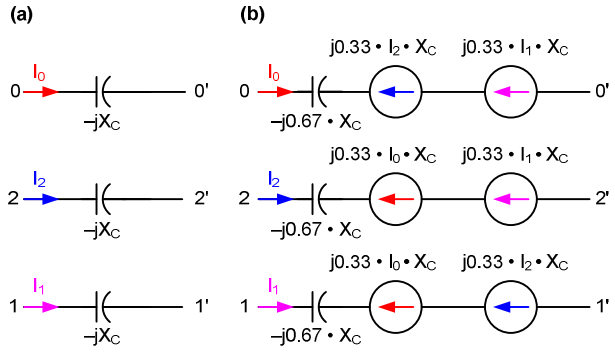


Fig. 3. Sequence networks for series capacitors with MOVs—low-current faults (a) and high-current SLG faults (b).

Note that for the case of Fig. 3b, only 2/3 of the per-phase capacitive reactance is inserted in the sequence networks, suggesting a lesser danger of current or voltage inversion when compared with low-current faults (Fig. 3a). However, mutual coupling between the networks can complicate the situation. The following items are worth pointing out regarding high-current faults that cause the MOV to bypass the series capacitor asymmetrically:

- The positive-sequence current creates a voltage drop in the zero- and negative-sequence networks. This voltage drop affects the sequence current flows and the operating conditions for the 87LG and 87LQ elements. As a result, these elements are no longer independent from the load current.
- Because the mutual coupling is inductive, it helps prevent voltage and current inversion as long as the coupled networks do not experience current inversion themselves.
- Load current can contribute to current and voltage inversion in the sequence networks. Load current in the importing direction creates a voltage drop in the negative- and zero-sequence networks that has the same effect as a voltage drop across a capacitive element.
- Because of the mutual coupling between the sequence networks, the 87LP, 87LG, and 87LQ elements do not respond independently to fault conditions, but their responses are mutually related. The next subsection explains this point further.

We can apply a similar approach to high-current line-to-line faults. The phase and sequence impedance matrices for an AB fault are as follows:

$$Z_{ABC} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -jX_C \end{bmatrix} \quad (3a)$$

$$Z_{012} = -j\frac{X_C}{3} \bullet \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}, \; a = 1\angle 120° \quad (3b)$$

In this case, only 1/3 of the per-phase capacitive reactance appears in the sequence networks. The networks are coupled, as in the case of SLG faults. To complicate things more, induced voltages are shifted 30 degrees and –210 degrees from the coupled currents. We observe the same effects as for SLG faults: impact of the load current on sequence currents, interdependence between the 87LP, 87LQ, and 87LG elements, and so on.

B. Low-Current SLG Internal Faults

First, we consider the case of a low-current SLG fault. The series capacitors are represented by the sequence networks of Fig. 3a, yielding a short-circuit equivalent network, as shown in Fig. 4. Note that the negative-sequence impedances are assumed to be equal to the positive-sequence impedances.

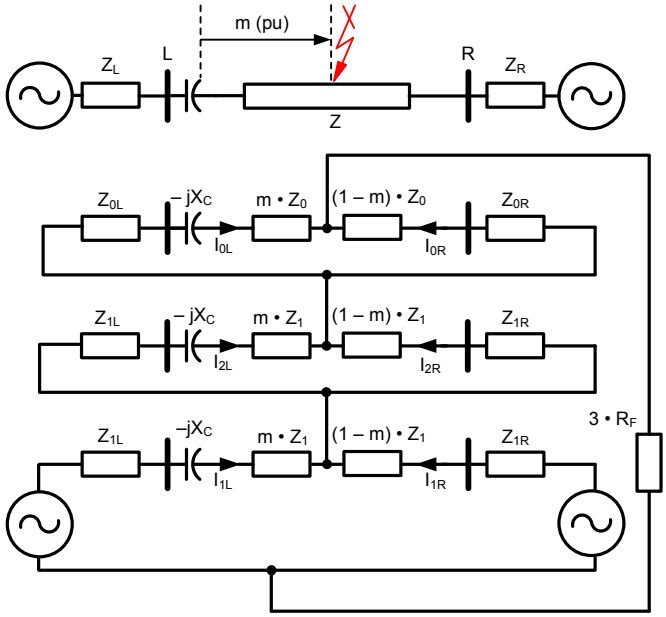


Fig. 4. Equivalent circuit for a low-current SLG fault (where *L* = local, *R* = remote, and *m* = per-unit fault location from Terminal L).

Because the sequence networks are not coupled at the series capacitor installation, we can take full advantage of the sequence components and solve the circuit of Fig. 4 for quantities relevant to the 87L elements. In particular, we are interested in the 87LG and 87LQ elements because these elements are meant to detect low-current faults [4].

For the zero-sequence network, we can write:

$$I_{0L}(Z_{0L} - jX_C + mZ_0) = I_{0R}(Z_{0R} + (1-m)Z_0) \tag{4}$$

We focus this paper on 87L elements based on the Alpha Plane principle [1] [2] and therefore are interested in the ratio of the currents at the line terminals. Equation (4) allows us to calculate this ratio as follows:

$$\frac{I_{0L}}{I_{0R}} = k_0 = \frac{Z_{0R} + (1-m)Z_0}{Z_{0L} - jX_C + mZ_0} \tag{5}$$

The Alpha Plane 87LG element operates for this internal fault if the complex ratio k_0 falls outside of the blocking characteristic depicted in Fig. 5 [1] [2].

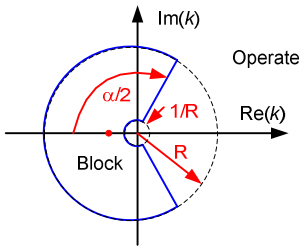


Fig. 5. Typical Alpha Plane blocking characteristic (where α = blocking angle and *R* = blocking radius).

We can perform the following simplified, but conservative, dependability analysis for the 87LG element based on (5) and the settings of Fig. 5.

For simplicity, neglect the resistance part of the system and line impedances. This assumption is justified because of a large margin between the blocking and tripping of the Alpha Plane characteristic (see Fig. 5) in terms of the angle. From (5), the Alpha Plane ratio becomes a real number (the imaginary part is small).

$$k_0 = \frac{X_{0R} + (1-m)X_0}{X_{0L} - X_C + mX_0} \tag{6}$$

The 87LG element will trip reliably as long as the ratio (6) is positive or, in other words, as long as the denominator is positive (i.e., the impedance between the fault and local system is inductive).

$$X_{0L} - X_C + mX_0 > 0 \text{ or } m > \frac{X_C - X_{0L}}{X_0} \tag{7}$$

When (7) is not satisfied, the 87LG element can still reliably operate if the k_0 ratio is larger than the setting *R* or lower than 1/R (see Fig. 5).

Solving for $|k_0| > R$ yields:

$$m > \frac{R(X_C - X_{0L}) - (X_0 + X_{0R})}{X_0(R-1)} \text{ and } m < \frac{X_C - X_{0L}}{X_0} \tag{8a}$$

Solving for $|k_0| < 1/R$ yields:

$$m > \frac{R(X_0 + X_{0R}) - (X_C - X_{0L})}{X_0(R-1)} \text{ and } m < \frac{X_C - X_{0L}}{X_0} \tag{8b}$$

The 87LG element operates reliably for all low-current SLG faults located beyond the value of *m* given by (7) or (8), whichever is lower. Specifically:

- Condition (7) means that the 87LG element will cover the entire line as long as the series capacitance is lower than the local system reactance (no current inversion).
- Condition (8a) means the 87LG element will cover the entire line as long as the local current is considerably higher than the remote current (*R* times), even if there is current inversion at the local terminal.
- Condition (8b) means the 87LG element will cover the entire line as long as the remote current is considerably higher than the local current (*R* times), even if there is current inversion at the local terminal.

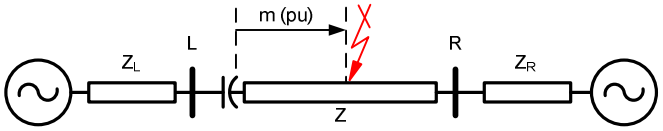
Similar analysis can be performed for the 87LQ element, yielding the following results:

$$m > \frac{X_C - X_{1L}}{X_1} \tag{9a}$$

$$m > \frac{R(X_C - X_{1L}) - (X_1 + X_{1R})}{X_1(R-1)} \text{ and } m < \frac{X_C - X_{1L}}{X_1} \tag{9b}$$

$$m > \frac{R(X_1 + X_{1R}) - (X_C - X_{1L})}{X_1(R-1)} \text{ and } m < \frac{X_C - X_{1L}}{X_1} \tag{9c}$$

Typically, system impedances will have different X_0/X_1 ratios, resulting in different responses of the 87LG and 87LQ elements based on (7) through (9). To illustrate this, we calculated the k_0 and k_2 values for the sample system shown in Fig. 6, as seen in Table I.



E	1 pu			1 pu∠–40°
X_1	0.050 pu	75%	0.25 pu	0.20 pu
X_0	0.075 pu		0.75 pu	0.25 pu

Fig. 6. Sample system to illustrate fault coverage of the 87LG and 87LQ elements.

TABLE I
ILLUSTRATION OF DEPENDENCY OF K_2 AND K_0 ON FAULT LOCATION AND CURRENT LEVEL. SHADED VALUES ALLOW THE 87LQ AND 87LG ELEMENTS TO TRIP WITH SETTINGS OF $R = 4$ AND $\alpha = 200$ DEGREES.

m (pu)	Low-Current SLG Fault		High-Current SLG Fault	
	k_0	k_2	k_0	k_2
0.1	23.6∠162°	3.76∠172°	6.80∠42°	2.76∠106°
0.2	21.5∠17°	4.53∠169°	3.77∠18°	2.82∠73°
0.3	6.84∠5.6°	5.87∠165°	2.31∠8.1°	2.18∠37°
0.4	3.72∠3.1°	8.7∠156°	1.53∠1.8°	1.44∠8.7°
0.5	2.38∠2.0°	16.3∠126°	1.06∠–2.8°	0.98∠–13°
0.6	1.63∠1.3°	14.5∠50°	0.75∠–7.0°	0.71∠–32°
0.7	1.15∠0.9°	6.65∠22°	0.52∠–11°	0.56∠–49°
0.8	0.82∠0.5°	3.84∠14°	0.36∠–16°	0.48∠–64°
0.9	0.58∠0.0°	2.51∠9.7°	0.23∠–24°	0.42∠–74°
1.0	0.40∠–0.4°	1.81∠7.7°	0.14∠–36°	0.38∠–82°

Based on (7), the 87LG element will satisfy the angle check of the Alpha Plane for $m > 0.15$ pu. Table I confirms this by showing angles below 17 degrees for locations 0.2 pu and above. For $m = 0.1$ pu, Table I shows the angle condition will block, but (8a) proves that the current ratio is greater than the setting. Table I confirms this (23.6 > 4). As a result, the 87LG element operates for all low-current faults on the protected line.

Based on (9a), the 87LQ element will satisfy the angle check of the Alpha Plane for $m > 0.55$ pu. Table I confirms this by showing angles below 50 degrees for locations 0.6 pu and above. For $m < 0.6$ pu, Table I shows the angle condition will block, but (9b) proves that the current ratio is greater than the setting. Table I confirms this for locations greater than 0.2 pu. For $m = 0.1$ pu, the current ratio condition will block as well [(9b) gives $m > 0.13$ pu]. As a result, the 87LQ element operates for low-current faults located at $m > 0.13$ pu on the protected line.

Note that the 87LQ element will only respond to faults beyond 0.13 pu in this case, but the dependability gap between 0 and 0.13 pu is covered by the 87LG element.

This analysis is valid for a series capacitor installation at the local terminal of the protected line. Similar analysis can be performed for different series capacitor locations (middle of the line and at both line terminals), as well as for capacitor locations external to the protected line.

C. High-Current SLG Internal Faults

Next, we consider the case of a high-current SLG fault. The series capacitors are represented by the sequence networks of Fig. 3b, giving us the short-circuit equivalent network shown in Fig. 7.

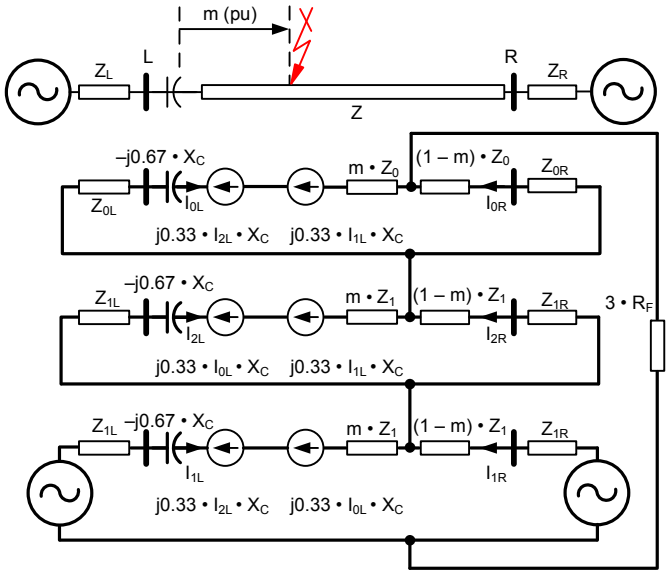


Fig. 7. Equivalent circuit for a high-current SLG fault (where L = local, R = remote, and m = per-unit fault location from Terminal L).

Because the sequence networks are coupled at the series capacitor installation, solving the circuit of Fig. 7 is more complicated. In this paper, we simply show that the Alpha Plane ratios k_0 and k_2 are no longer independent but are related to each other. From Fig. 7, we see:

$$I_{0L}(Z_{0L} - j\frac{2}{3}X_C + mZ_0) + j\frac{1}{3}X_C(I_{2L} + I_{1L}) = I_{0R}(Z_{0R} + (1-m)Z_0) \quad (10)$$

Note that:

$$I_{2L} + I_{1L} = I_{AL} - I_{0L} \quad (11)$$

Inserting (11) into (10) yields:

$$-j\frac{1}{3}X_C I_{AL} = I_{0L}(Z_{0L} - jX_C + mZ_0) - I_{0R}(Z_{0R} + (1-m)Z_0) \quad (12a)$$

Similarly:

$$-j\frac{1}{3}X_C I_{AL} = I_{2L}(Z_{1L} - jX_C + mZ_1) - I_{2R}(Z_{1R} + (1-m)Z_1) \quad (12b)$$

Equating (12a) and (12b) shows how the zero- and negative-sequence currents are interdependent.

$$\begin{aligned} &I_{0L}(Z_{0L} - jX_C + mZ_0) - I_{0R}(Z_{0R} + (1-m)Z_0) = \\ &I_{2L}(Z_{1L} - jX_C + mZ_1) - I_{2R}(Z_{1R} + (1-m)Z_1) \end{aligned} \quad (13)$$

From Fig. 7, we notice further that:

$$I_{0L} + I_{0R} = I_{2L} + I_{2R} \quad (14)$$

Inserting (14) into (13) and rewriting the expression of the current ratios k_0 and k_2 yield:

$$\frac{1+k_2}{1+k_0} = \frac{(Z_{1R} + (1-m)Z_1) - k_2(Z_{1L} - jX_C + mZ_1)}{(Z_{0R} + (1-m)Z_0) - k_0(Z_{0L} - jX_C + mZ_0)} \quad (15)$$

Equation (15) shows that the Alpha Plane operating points for 87LG and 87LQ are correlated and controlled by both the zero- and positive-sequence network impedances.

Table I and Fig. 8 illustrate this finding by using the sample system parameters of Fig. 6 and applying them to the case of Fig. 7.

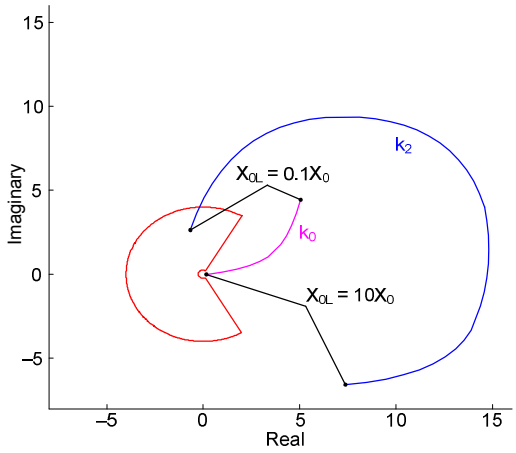


Fig. 8. Illustration of the interdependence between Alpha Plane operating points k_0 and k_2 for m = 0.1 pu, with all parameters constant except for X_{0L} varying between 0.1 and 10 of the line X_0. Changing X_{0L} changes both the k_0 and k_2 ratios.

When examining Table I, we see that for the same system and same fault locations, the values of k_2 and k_0 differ considerably depending on whether the fault is a low-current fault (no MOV conduction) or a high-current fault (full MOV conduction). For example, for m = 0.9, $k_2 = 2.51\angle 9.7°$ for low-current faults and $k_2 = 0.42\angle -74°$ for high-current faults.

Note that the 87LG element covers the entire line, while the 87LQ element has a dependability gap for close-in and remote high-current faults.

When examining Fig. 8, we see that zero-sequence impedances impact the current ratio for both the 87LG and 87LQ elements. The impact of X_{0L} on k_2 is quite dramatic. For low values of X_{0L}, 87LQ will block, and for larger values (weaker local system), 87LQ will operate.

D. Transient Response of 87L Elements

The previous analysis pertains to the steady-state response of the 87L elements. Line terminal currents are, however, subject to subsynchronous oscillations due to series compensation, and the impact on transient errors due to oscillations must be considered as well.

Subsynchronous oscillations do not violate Kirchhoff's current law. Therefore, the differential current remains very low (ideally zero) during any noninternal fault conditions, including transients. The overcurrent pickup condition of the 87L elements guarantees stability of the 87L elements, even if the Alpha Plane trajectories respond to the subsynchronous transients.

Subsynchronous transients can impact the accuracy and speed of 87L elements during internal faults by causing relatively slow changes in the differential current level or the Alpha Plane ratio. However, the high sensitivity of the 87LQ and 87LG elements means that these elements have a large operating margin, and therefore, they will be impacted only minimally by the subsynchronous oscillations.

Often, distance backup elements are used within the 87L relay to account for the loss of channel. The application of distance functions on series-compensated lines can greatly benefit from transient closed-loop scheme testing, such as using the Real Time Digital Simulator (RTDS®). It is a good practice to verify the performance of the 87L elements as well during the transient testing process.

E. Recommendations for 87L Applications

From our analysis, it is clear that the 87L elements (87LP, 87LG, and 87LQ) experience different operating conditions for any given internal fault on series-compensated lines. In order to increase a chance for dependable relay operation and avoid blocking due to current inversion or the impact of load on sensitivity, we recommend using all three elements. This approach does not erode security, as explained in Section II.

IV. Weak System Conditions

A. Challenges With Weak System Applications

Weak system situations occur when there is insufficient short-circuit current for the relay at the line terminal to detect line faults due to a weak source, or no source, behind the terminal. The typical weak system applications are illustrated in Fig. 9. The weak terminal may result from small generators, a weak system behind the terminal, or a load-only terminal. Sources of variable generation, such as wind farms or solar farms, are typically treated as weak sources no matter how large the generation capacity they can provide (see Section VII). A normal line terminal can also become a weak terminal under certain contingencies when adjacent lines or transformers are out of service. Fig. 10 shows special cases of weak system applications in which one line terminal is open or completely isolated from the energized line.

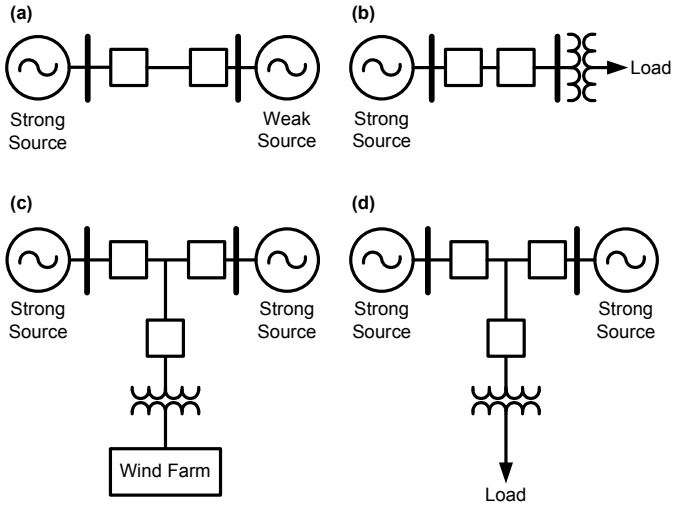


Fig. 9. Weak terminal with weak source (a), load only (b), variable generation (c), or load tapped to transmission line (d).

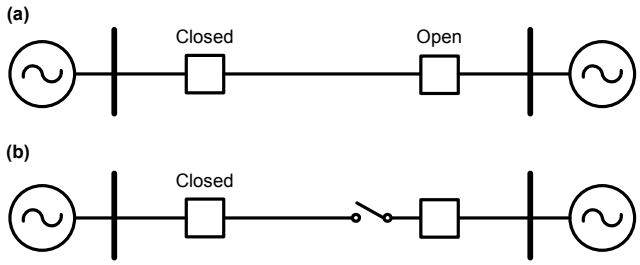


Fig. 10. Special cases of weak terminal: breaker (a) and disconnect switch (b) open at one terminal.

Regardless of whether there is a weak source or pure load behind the terminal, it is expected that a pilot scheme can trip all the terminal breakers with high speed to isolate the fault. However, the weak system applications present challenges to the traditional pilot schemes, such as directional comparison blocking (DCB) or permissive overreaching transfer trip (POTT), of which the distance or directional overcurrent elements may not be able to pick up at the weak terminal. Weak infeed logic, such as permissive echo logic, possibly with undervoltage and/or zero- or negative-sequence overvoltage elements for fault detection, may be needed.

For applications that have only load behind the terminal, as in Fig. 9b and Fig. 9d, it may seem to be an insignificant issue if the breakers at the weak terminal fail to trip for a line fault. However, most loads usually consist of some percentage of motors. Some large motors can backfeed from the weak terminal and sustain the fault arc such that the fault current is not cleared when the breaker at the strong terminal opens and the high-speed reclosing of the strong terminal may fail.

B. Weak Systems and Differential Protection

In comparison with distance and directional protection, the line current differential scheme can handle weak systems by its very nature. No matter how low the fault current contribution is from a weak terminal, the 87L relay at the weak end will be able to see the differential current for an internal fault because of the current contribution from the strong terminal(s) within the 87L zone.

High-resistance faults can be a problem for the phase differential elements. The phase currents may flow out of the faulted line toward the load or a weak system. Application of sequence (87LQ and 87LG) elements along with line charging compensation techniques provides higher fault resistance coverage. In addition, the Alpha Plane 87L elements cater to this outfeed condition with their specially shaped operating characteristics [1].

Microprocessor-based line current differential relays incorporate a number of supervisory conditions for their core 87L elements. One such condition is disturbance detection supervision. Its purpose is to secure the scheme against undetected errors in data received over the communications channel. Therefore, we need to analyze the impact of disturbance detection supervision on the dependability of the 87L scheme with regard to weak system applications.

Disturbance detection logic greatly increases the security of the 87L scheme, which is subjected to communications channel noise, such as interference coupled to the channel medium or electronics, failing components in the electronic devices comprising the network, marginal power budget for fiber transceivers, and so on [5]. Even modern 87L relays that use robust data integrity protection have a finite, non-zero probability of defeating data integrity protection codes, creating the opportunity for corrupted remote current data used in the 87L element resulting in unwarranted operation.

Disturbance detection supervision helps protect against spurious differential operations by qualifying any 87L element assertions with changes in local currents (typically) and voltages (in some implementations).

One possible method of supervising the differential signals is shown in Fig. 11. In this solution, corrupted data that activate the raw 87L function or spuriously assert the received 87 direct transfer trip (87DTT) will typically corrupt only a single packet. Because the disturbance detection supervision does not assert for this event, the element is not allowed to operate. During an actual system fault, the disturbance detector picks up along with the raw differential element and the protection response is instantaneous. If for some reason the disturbance detector fails to assert for an actual system fault, the assertion of the raw differential or 87DTT element is allowed to trip the relay with a slight delay.

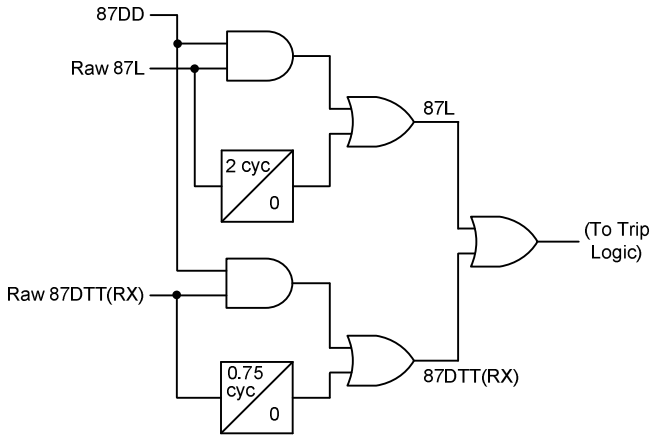


Fig. 11. Application of disturbance detection in an 87L relay.

The basic principle of disturbance detection is simple in nature and greatly improves the security of differential protection. However, the disturbance detector design of the 87L relay needs to be carefully considered to overcome potential dependability problems from various power system situations, especially weak system applications, as discussed next.

C. Disturbance Detector Design and Weak System Considerations

Several disturbance detector implementations depend strictly on local relay currents to supervise the differential element.

One disturbance detector design is illustrated in Fig. 12. In this design, if there is sufficient negative- or zero-sequence current and the difference between the present magnitude of the local sequence current and the magnitude of that sequence current two cycles previous is greater than a specified threshold, a disturbance is declared, allowing operation of the differential elements.

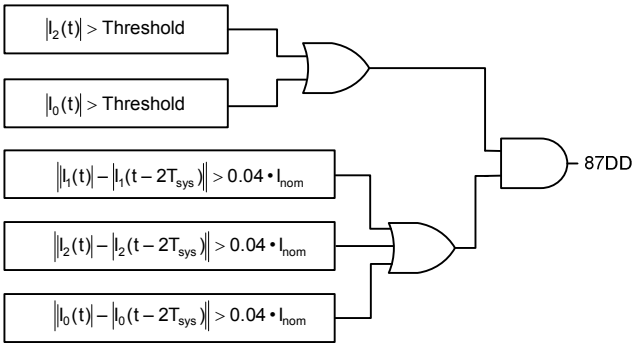


Fig. 12. Single-ended disturbance detector design.

A similar approach to the single-ended disturbance detector design is shown in Fig. 13. This design attempts better sensitivity by monitoring changes in the current angles in addition to monitoring changes in the current magnitudes.

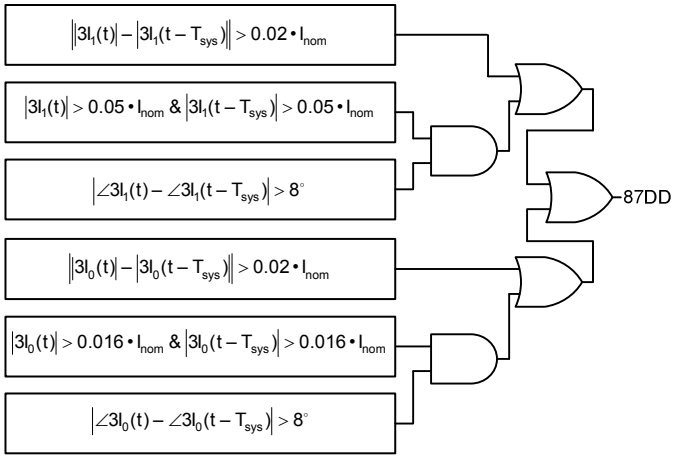


Fig. 13. Alternative single-ended disturbance detector design.

By detecting the sudden change of the sequence currents, these detectors can be sensitive to a disturbance while staying inactive under normal load conditions. However, as is the case with distance and directional protection, weak system scenarios can result in little or no change in the local currents at a weak terminal during a fault condition, resulting in delayed 87L operation, as per the 87DD supervision logic in Fig. 11, or possibly no 87L operation in different relay implementations.

These concerns are often overstated because the weak terminals typically contain grounding sources, such as autotransformers. These sources will supply zero-sequence current. Because the designs of Fig. 12 and Fig. 13 monitor the zero-sequence current in a very sensitive fashion, the 87DD logic at the weak terminal will respond to faults on the line.

An alternative design for the disturbance detector that ensures dependability of the 87DD logic, even if there are absolutely no grounding sources at the weak terminal, is to incorporate the local voltage signals, as shown in Fig. 14. While part of the benefits of line current differential is that, traditionally, it does not require the use of voltages, many modern 87L relays come with complete backup distance protection and will likely have voltage signals available. The benefit of adding voltages for disturbance detection supervision in weak system applications is clear: while weak terminals may not provide sufficient fault current to assert a disturbance detector, the phase voltage depression or the zero- or negative-sequence overvoltage condition will be obvious.

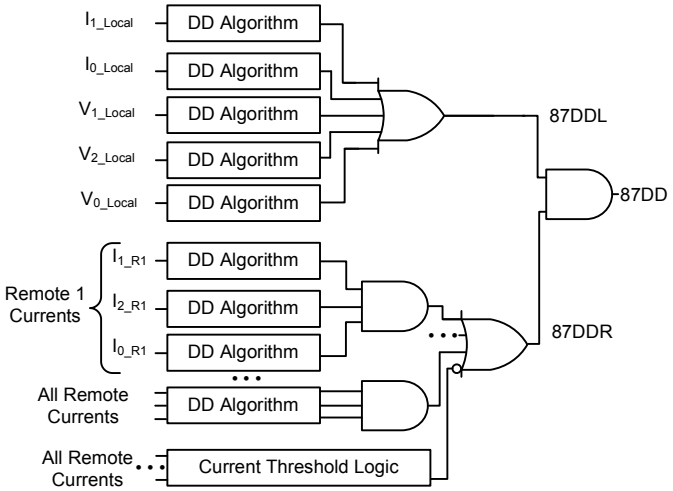


Fig. 14. Multi-ended disturbance detector design.

The security provided by a disturbance detector can be improved by including the received remote currents, as shown in Fig. 14. The benefits of a design that incorporates both local and remote disturbance detection are numerous [5].

Consider the simplified diagram of the 87L scheme shown in Fig. 15. A line current differential scheme consists of two or more independent relays located in different substations and subjected to different environmental conditions, including conducted and radiated electromagnetic transients and static discharge conditions. A disturbance detector design that cross-checks data between individual relays of the scheme, as is the case when incorporating both local and remote signals, provides better security not only against undetected communications errors but also against relay failures.

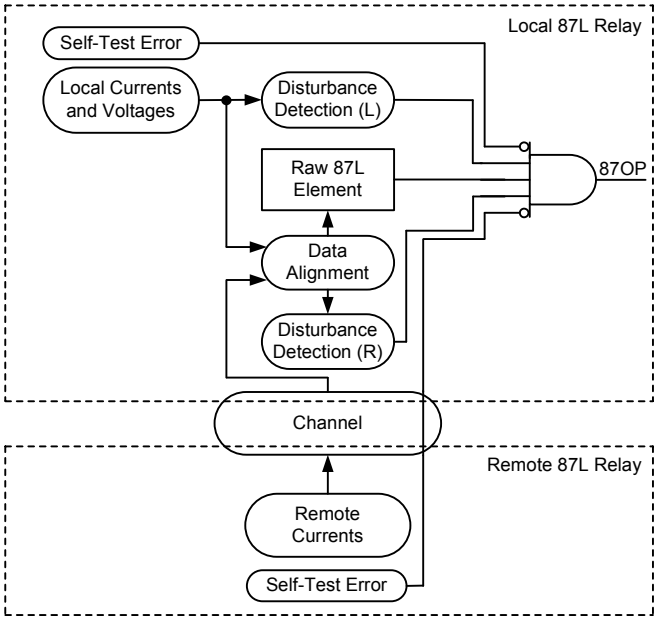


Fig. 15. Multi-ended disturbance detection guards against multiple problems, greatly increasing security.

For example, if the analog-to-digital (A/D) converter component fails in the local relay, the local disturbance detector (87DDL) and the raw 87L function may spuriously pick up because of heavily corrupted local data. However, the portion of the disturbance detection that responds to remote currents (87DDR) will not assert, preventing instantaneous 87L operation. Subsequently, the self-test error will assert in the local relay in response to the problem, taking it out of service. In this way, the disturbance detection logic gives extra time to the self-test logic and, in combination, dramatically improves the security of the 87L scheme.

Similarly, if the remote relay has some problem, the raw 87L and 87DDR functions at the local relay may spuriously assert because of the heavily corrupted remote data. However, the portion of the disturbance detection that responds to local currents and voltages (87DDL) will not assert, preventing instantaneous 87L operation.

With regards to weak sources, care should be taken when adding remote signals to the disturbance detection. A weak terminal may not produce a significant current change (or may produce no change at all, such as when the remote breaker is open), preventing the remote detector logic of the local relay at the strong terminal from asserting for an actual system disturbance. The dependability of the remote disturbance detector is increased by adding current threshold supervision logic, as is shown in Fig. 14. In the case that there is insufficient current from the remote terminals (i.e., weak source or an open breaker), the remote disturbance detector (87DDR) will assert, allowing the local detector logic (87DDL) to identify the disturbance and qualify the differential elements.

The sensitivity of the disturbance detector algorithm is also important to maintain dependability in weak system situations. In one approach [5], both the local and remote parts of the disturbance detection logic shown in Fig. 14 use an adaptive disturbance detector algorithm. Depicted in Fig. 16, the algorithm first calculates a one-cycle difference for the input phasor IN. This operation is executed on a sample-by-sample basis and yields a very fast and sensitive response due to the subtraction of the standing value in the input phasor IN. Subsequently, the magnitude of this incremental signal is calculated. This magnitude, DX, is filtered through an infinite impulse response (IIR) filter in order to get a notion of the standing noise in the DX signal. Normally, this standing noise is very small because even under the presence of harmonics, the phasor errors tend to be periodic and, as such, would cancel as a part of the delta calculation over one power cycle. The input to the IIR filter is clamped at appropriate minimum and maximum values for security and dependability. The standing value of the DX signal, multiplied by a constant, k_{TH}, becomes an adaptive threshold of the comparator. If the DX signal exceeds such threshold, the output OUT asserts. In this way, the disturbance detection algorithm is very sensitive yet will not trigger under load conditions even if the load current or voltages are heavily distorted, as long as they are periodic, making it a good solution for detecting small changes in signals measured at weak terminals.

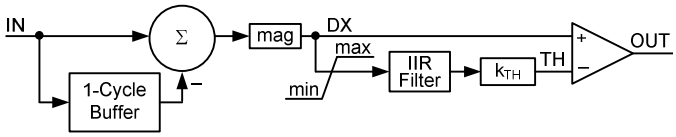


Fig. 16. Adaptive disturbance detector algorithm.

In summary, with careful design considerations, disturbance detector supervision used by 87L schemes can provide both security for 87L schemes and dependability for unusual system conditions, such as weak system applications.

V. Open-Pole Conditions

Single-pole tripping (SPT) and reclosing take advantage of the fact that a vast majority of line faults are transient SLG faults. Opening only the faulted phase while keeping the other two phases energized brings several advantages [7] [8], including the following:

- Enhanced transient power system stability by allowing partial power transfer during the autoreclose period.
- Guaranteed permission from a synchronism-check element when reclosing after the single-pole trip.
- Reduced power oscillations, resulting in lower stress on turbine shafts.
- Reduced switching overvoltages.

Application of SPT requires breakers with independent pole tripping mechanisms, may require line reactors with a neutral reactor to extinguish the secondary arc, and requires slightly more complex protection schemes.

In the context of this paper, we evaluate the 87L elements during the single-pole open (SPO) period of an SPT operation.

A. Sensitivity of the 87LG and 87LQ Elements With All Poles Closed

Consider the power network shown in Fig. 17. For an SLG fault (see Fig. 4 with the series capacitors removed), (16) and

(17) provide the ratio of zero- and negative-sequence currents at the two ends of the line.

$$\frac{I_{0L}}{I_{0R}} = k_0 = \frac{Z_{0R} + (1-m) \bullet Z_0}{Z_{0L} + m \bullet Z_0} \quad (16)$$

$$\frac{I_{2L}}{I_{2R}} = k_2 = \frac{Z_{2R} + (1-m) \bullet Z_2}{Z_{2L} + m \bullet Z_2} \quad (17)$$

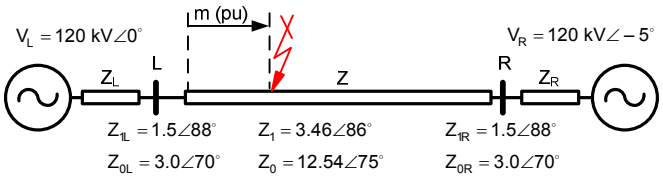


Fig. 17. Power network to study SPO effect on 87L elements.

From these two equations, it is clear that the k_0 and k_2 ratios are independent of load current and fault resistance. They depend only on the system impedances and fault location. Fig. 18 shows the loci of the zero- and negative-sequence current ratios for varying fault locations. In this example, the line and equivalent systems are homogeneous (similar line and system impedance angles) and the ratios are almost purely real numbers located in the first or fourth quadrants, clearly outside of the blocking region of the 87L characteristic. As a result, the 87LQ and 87LG functions are very dependable, with sensitivity limited only by the charging current, CT errors or saturation, or line unbalance [4] [8].

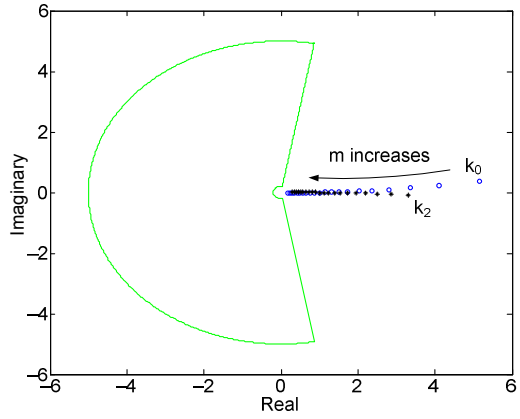


Fig. 18. Loci of the 87LG and 87LQ elements for varying fault locations in the system of Fig. 17.

B. Sensitivity of the 87LG and 87LQ Elements Under SPO Conditions

Fig. 19 shows the equivalent sequence network diagram for an SLG fault (A-phase) under an SPO condition (B-phase) [9].

From Fig. 19, the three sequence networks are connected in series due to the internal SLG fault. In addition, the negative- and zero-sequence networks include sources related to the positive-sequence quantities, which are induced by the SPO condition. These sources drive the negative- and zero-sequence networks in a manner similar to the system electromotive force (EMF) driving the positive-sequence network. Therefore, we observe a through negative- and zero-sequence current during the faulted state due to the open pole, unlike the case of a fault with all three phases closed. These standing currents impact the sensitivity of the 87LG and 87LQ elements in a manner similar to the way load current impacts the sensitivity of the 87LP elements.

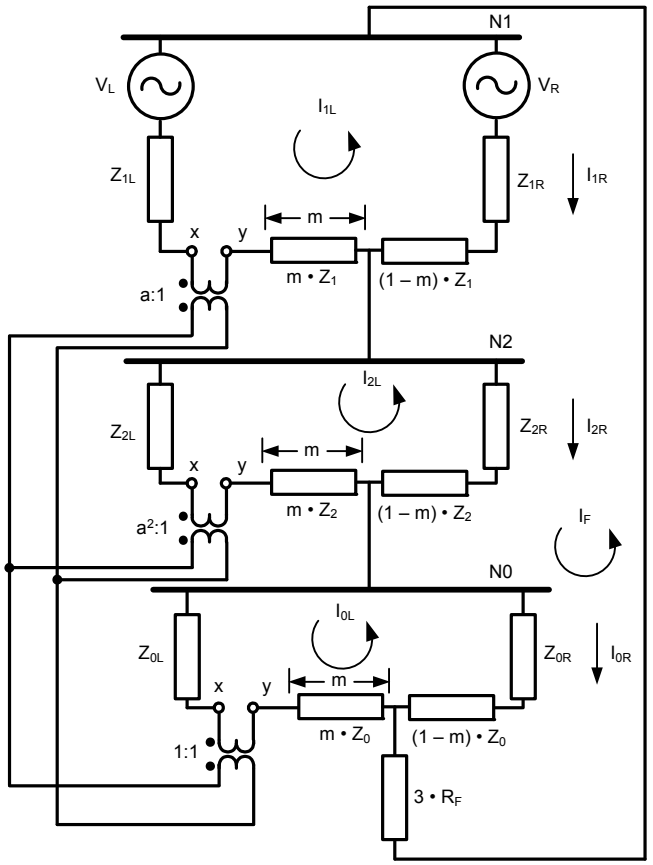


Fig. 19. Equivalent circuit for an SLG fault under an SPO condition.

Fig. 20 illustrates this by plotting the fault currents at Terminal L in the system of Fig. 17 for the SLG fault at $m = 0.33$ pu and fault resistance of 30 Ω during an SPO condition. The fault is cleared without opening the breaker at $t = 0.1$ seconds. Fig. 20 shows the phase currents and plots the negative-sequence current magnitude and angle. Note that the magnitude and angle change only slightly due to this fault.

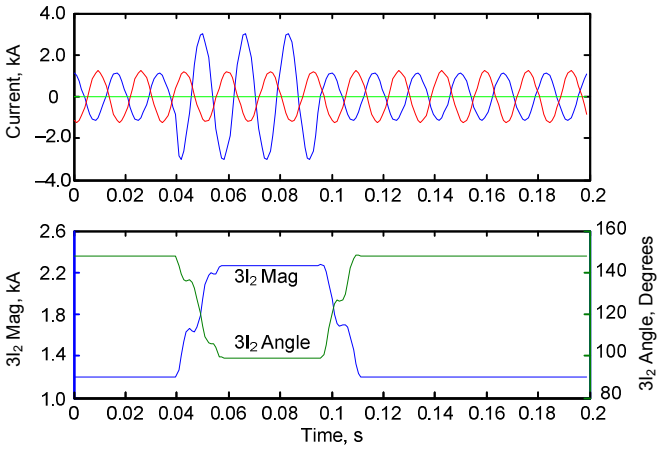


Fig. 20. Terminal L phase current waveforms (top) and the negative-sequence magnitude and angle (bottom) for an SLG fault at $m = 0.33$ pu and $R_F = 30$ Ω during an SPO condition.

Fig. 21 presents the same signals but as measured by the Terminal R relay.

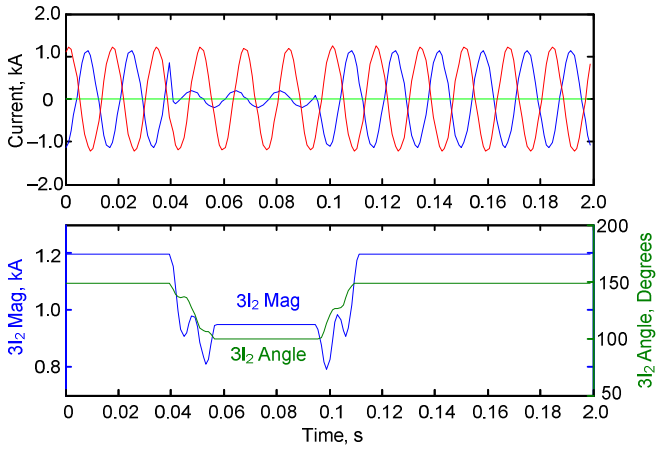


Fig. 21. Terminal R phase current waveforms (top) and the negative-sequence magnitude and angle (bottom) for an SLG fault at m = 0.33 pu and R_F = 30 Ω during an SPO condition.

Prior to the fault, the negative-sequence currents are equal in magnitude and out of phase at Terminals L and R, demonstrating the inherent security of the 87L elements in general. During the fault, the negative-sequence currents at both terminals shift but are not in phase for this high-resistance fault (as they would be for a fault without an SPO condition).

Fig. 22 illustrates this further by plotting the loci of the k_0 and k_2 ratios for an SLG fault at m = 0.33 pu with varying fault resistance. Under SPO with no fault conditions, the k_0 and k_2 loci are located inside the blocking region of the 87L characteristic and move toward the first and fourth quadrants (tripping) only as the fault resistance decreases. In this sample case, the 87LG element operates for a fault resistance lower than 60 Ω and the 87LQ element operates for a fault resistance below 25 Ω.

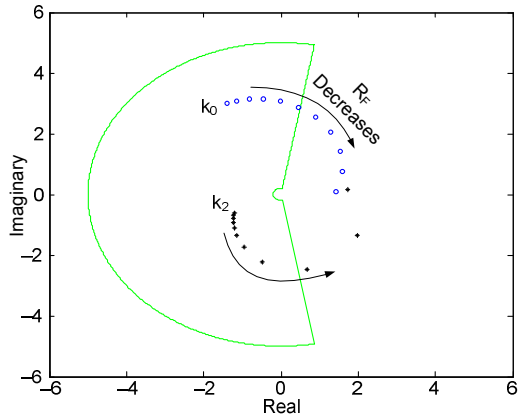


Fig. 22. k_0 and k_2 loci for an SLG fault at m = 0.33 pu under an SPO condition for varying fault resistance.

C. Sensitivity of the 87LP Elements

With all poles closed, the phase current ratio for an AG fault is as follows [8]:

$$k_A = \frac{(2C_1 + C_0) + \dfrac{I_{LD}}{I_{1F}}}{[2(1-C_1) + (1-C_0)] - \dfrac{I_{LD}}{I_{1F}}} \tag{18}$$

where:

$$I_{LD} = \frac{V_{AL} - V_{AR}}{Z_{1L} + Z_{1R} + Z_1} \tag{19}$$

$$I_{1F} = \frac{V_{AL} - I_{LD}(Z_{1L} + m \bullet Z_1)}{2Z_{TH1} + Z_{TH0} + 3R_F} \tag{20}$$

$$Z_{TH1} = \frac{(Z_{1L} + m \bullet Z_0)(Z_{1R} + (1-m) \bullet Z_1)}{Z_{1L} + Z_{1R} + Z_1} \tag{21}$$

$$Z_{TH0} = \frac{(Z_{0L} + m \bullet Z_0)(Z_{0R} + (1-m) \bullet Z_0)}{Z_{0L} + Z_{0R} + Z_0} \tag{22}$$

$$C_1 = \frac{Z_{1L} + (1-m)Z_1}{Z_{1L} + Z_{1R} + Z_1} \tag{23}$$

$$C_0 = \frac{Z_{0L} + (1-m)Z_0}{Z_{0L} + Z_{0R} + Z_0} \tag{24}$$

From these equations, it is clear that the phase current ratio is a function of source angle difference, fault resistance, fault location, and network impedances.

To illustrate this dependence, Fig. 23 shows the locus of the 87LA element for an AG fault at m = 0.33 pu with a source angle difference of 5 degrees as the fault resistance increases. The element operates for a fault resistance below 60 Ω.

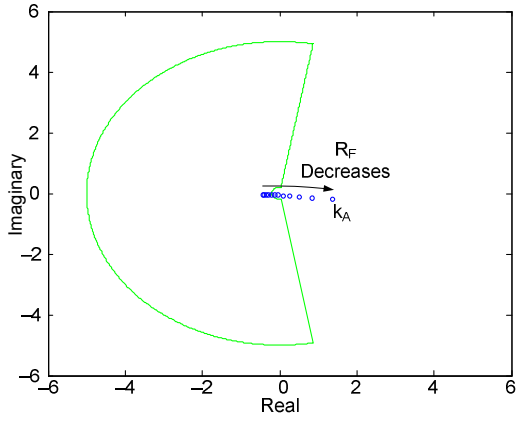


Fig. 23. k_A locus for an SLG fault under an SPO condition at m = 0.33 pu with a 5-degree source angle difference for varying fault resistance.

Fig. 24 shows the locus of the 87LA element for an AG fault at m = 0.33 pu with a 5 Ω fault resistance as the source angle difference increases. The element operates for source angle differences lower than 30 degrees.

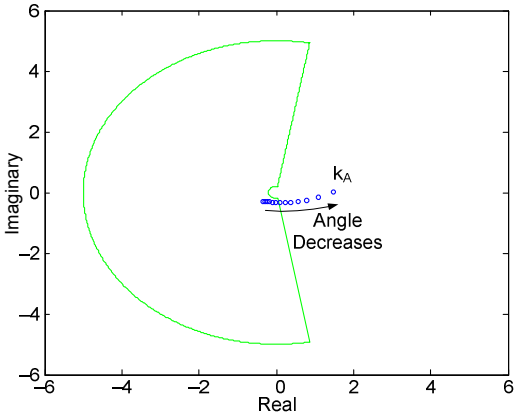


Fig. 24. k_A locus for an SLG fault under an SPO condition at m = 0.33 pu with a 5 Ω fault resistance for varying source angle difference.

Considering open-pole conditions and the sensitivity of the 87LP elements, we conclude that the sensitivity of the 87LP elements is not greatly impacted under SPO conditions and remains similar to the sensitivity with no breaker poles opened.

VI. Power Swings and Off-Nominal Frequency

A. Power Swings

We now explore the dependability of 87L elements during power swings using a sample case of an internal ACG fault during an unstable swing. Fig. 25 and Fig. 26 present the voltages and currents measured at both terminals of the line. The fault occurs at t = 0, where the currents are at the maximum of the swing envelope. The case has been obtained through simulation on a made-to-scale power system model, and the fault is removed after about 0.42 seconds, without opening any circuit breakers.

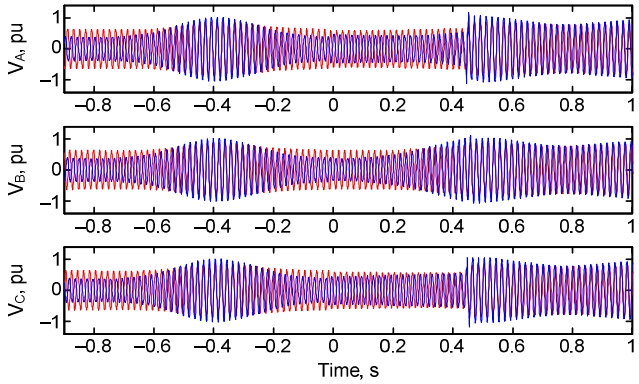


Fig. 25. Line ACG fault during an unstable power swing: phase voltages (fault applied at t = 0 seconds).

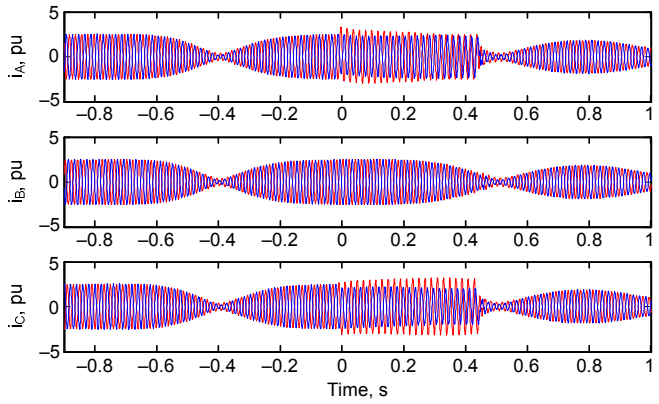


Fig. 26. Line ACG fault during an unstable power swing: phase currents (fault applied at t = 0 seconds).

Fig. 27 shows currents at both ends of the line during the first few tenths of a second of the fault. The fault occurred when the currents were elevated to about two times the CT nominal values. At that time, the two electromotive sources of the equivalent systems were almost out of phase, and the fault had little impact on the values of the phase currents. We can see that the phase currents at both ends of the line remain out of phase and almost equal. A phase differential element (87LP) will restrain for this fault regardless of the operating principle used (percent differential or the Alpha Plane). After about 200 milliseconds, the currents start to displace in phase as the system continues to swing, giving the 87LP element a chance to operate for this fault.

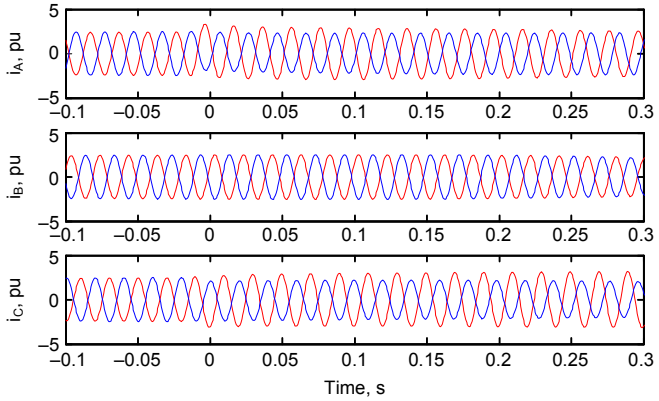


Fig. 27. Line ACG fault during an unstable power swing: phase currents during the internal fault (fault applied at t = 0 seconds).

Now, we examine the performance of the sequence differential elements. Fig. 28 shows the instantaneous $3I_0$ currents at both terminals of the line. Note that this current is zero before the fault and develops to considerable values during the fault. This current swings as the two systems swing against each other during the fault. This can be explained by looking at Fig. 4 (excluding the series capacitors, of course). As the two sources in the Fig. 4 diagram swing, all the currents and voltages follow the swing. However, the zero-sequence currents measured at the two line terminals still

abide by the current divider principle of the zero-sequence network—the fault current swings, but it divides itself between the local and remote line terminals in a constant proportion established by the line and system zero-sequence impedances. This is clearly visible in Fig. 28. The two currents are in phase, and their ratio is constant, regardless of the changing envelope of the two $3I_0$ currents. As a result, the operating point of the 87LG Alpha Plane element k_0 has a positive real part (the currents are in phase) and a constant value (the ratio does not change). Therefore, the 87LG element will operate for this fault very reliably and quickly.

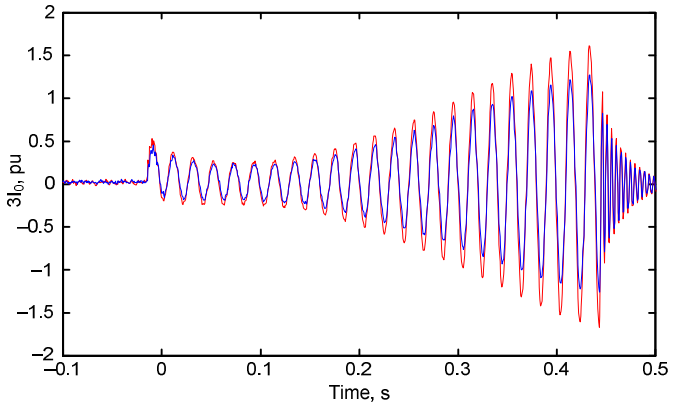


Fig. 28. Line ACG fault during an unstable power swing: zero-sequence currents at both line terminals during the internal fault.

The same is true for a percentage restrained 87LG element. In this case, the ratio between the operating (differential) and restraining currents is constant and significant, placing the operating point deep into the operating region of the percentage restrained 87LG element.

Similar observations can be made for the negative-sequence differential element, 87LQ. Examining Fig. 4, we can see that the negative-sequence currents at both terminals of the line will also swing but will follow the current divider principle and split in a proportion dictated by the impedances in the negative-sequence network. As a result, the $3I_2$ currents at both ends of the line will be in phase, despite the changing envelope of the swing. Therefore, the 87LQ element operates reliably and quickly for faults during power swings.

Will the performance of disturbance detection and external fault detection logic affect 87L dependability during power swings?

First, we examine the disturbance detection logic (87DD). As explained in Section IV, the 87DD logic often monitors the zero- and negative-sequence currents for sudden changes. From Fig. 28, we can see that the 87DD logic will operate reliably in response to the sudden change in the zero-sequence current. The 87DD logic can have trouble with the positive-sequence current as it constantly changes during the swing, but the $3I_0$ and $3I_2$ conditions will reliably assert the 87DD output on fault inception.

Second, we look at the external fault detection logic. Fig. 29 shows one possible implementation of the EFD logic that can use either instantaneous or phasor quantities. The logic uses incremental quantities (derived over a one-cycle time span) to prevent the EFD from picking up on load currents [2]. The EFD asserts when the incremental restraining signal becomes greater than some threshold value *P* and, at the same time, the incremental differential signal remains smaller than a percentage (*q* factor) of the restraining signal during 3/16 of a cycle. Once the EFD picks up, it will remain in that state until the dropout timer (DPO) expires.

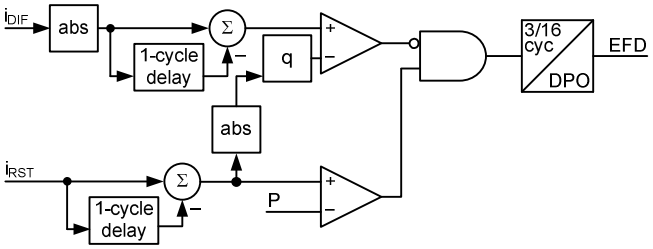


Fig. 29. External fault detection logic.

In order to retain high sensitivity of the 87LQ and 87LG elements, the EFD logic must not assert in response to the power swing or the internal fault that follows. Otherwise, assertion of the EFD logic would trigger extra restraining measures to secure the 87LQ and 87LG elements, typically designed for CT saturation under external faults [2]. Fig. 30 shows the A-phase restraining signal i_{RST} (top of Fig. 30) and the incremental A-phase restraining signal as well as the threshold *P* (blue line in the bottom part of Fig. 30). The incremental restraining signal is not zero because it follows the envelope of the swing. However, the changes due to a power swing are much slower than those due to a fault. Therefore, the incremental restraining signal does not rise above the threshold *P*, and the EFD logic does not assert during a power swing, thus ensuring high sensitivity of the 87LQ and 87LG elements. Note that at $t = 0$ (fault inception), the restraining signal increases, but at this point, the differential signal increases as well. Per the logic of Fig. 29, the EFD will not assert even if the restraining signal crossed the threshold line.

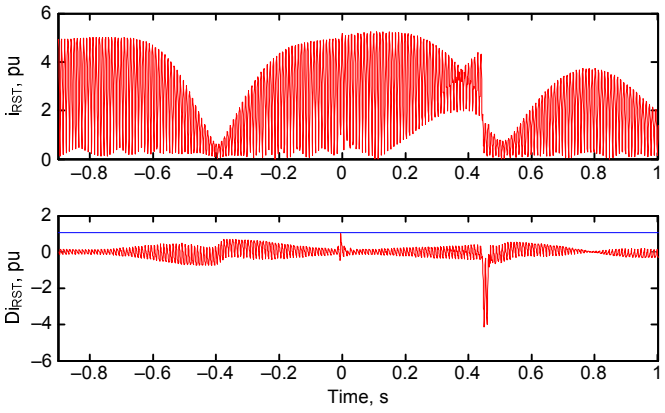


Fig. 30. Line ACG fault during an unstable power swing: the instantaneous A-phase restraining signal (top) and the incremental A-phase restraining signal (bottom).

B. Off-Nominal Frequencies

Off-nominal frequency operation affects single-ended protection methods because it impairs measurement accuracy and creates problems for distance element memory polarization.

Sample-based 87L elements, such as those described in [3], are not concerned with off-nominal frequencies. The sample-based implementations exchange instantaneous values of the currents acquired without frequency tracking. Only after the instantaneous differential signal is formed from the local and remote currents does the relay apply frequency tracking. Without frequency tracking, the measurement errors resulting from the relay tracking to a different frequency than the signal frequency have little impact on the security and dependability of the differential function—a zero differential signal, even if measured assuming an incorrect frequency, is still zero; a significant differential signal, even if measured assuming an incorrect frequency, is still significant. In theory, these errors can impact operation for borderline cases (i.e., when the operating point is located close to the operate/restrain boundary of the 87L characteristic). But for typical cases of internal faults and other conditions (load, external fault), there is a very large margin to accommodate these minor measurement errors.

The situation can be different for phasor-based implementations. If the 87L relays exchange phasors and these relays track to different frequencies, considerable angular errors are introduced in the phasors. These errors may lead to security or dependability problems in a manner similar to issues with memory polarization for distance elements. Therefore, it is imperative that all 87L relays of a given scheme track to the same frequency. If so, even if this frequency is off, the impact is minimal and similar as for sample-based implementations. Typically, in order to track to the same frequency, the phasor-based 87L relays measure the frequency from current phasors (these are available to all relays in the scheme) and not from voltages. This, however, results in lower accuracy of frequency tracking and exposes the tracking algorithm to extra challenges.

VII. Inverter-Based Sources

We use an example of a doubly fed induction generator (DFIG) to illustrate issues when protecting lines connected to wind farms using DFIGs.

A. DFIG Components

The DFIG system shown in Fig. 31 consists of a wind turbine, gearbox, induction generator, and back-to-back voltage source converters with a dc link. The converters are dc/ac rectifiers (grid side) and ac/dc inverters (rotor side), using power electronics, such as insulated gate bipolar transistors (IGBTs). By controlling the timing and sequence of the firing of each IGBT, the frequency and amplitude of rotor currents can be adjusted to optimize the generator outputs per wind speed. The dc chopper circuit and crowbar circuit are included in the DFIG to protect the converters and the dc capacitor. Because of the high efficiency brought by variable speed control, relatively low cost, and low-voltage ride-through capability, the DFIG is the most widely used type of wind generator so far.

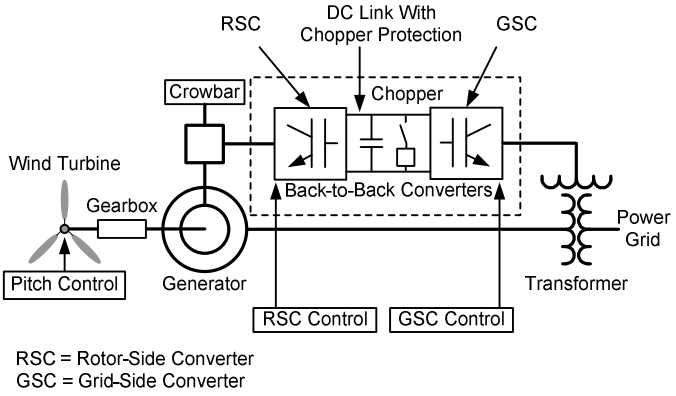


Fig. 31. Simplified block diagram of the doubly fed induction machine wind generator.

B. Fault Studies

Consider the sample system of Fig. 32 from the point of view of line protection, especially regarding the current contribution from the wind generator. In order to obtain the proper transient response associated with the induction machine and its controller, the simulation included a detailed model for a 2 MW DFIG, including the wind turbine control and the induction machine vector control.

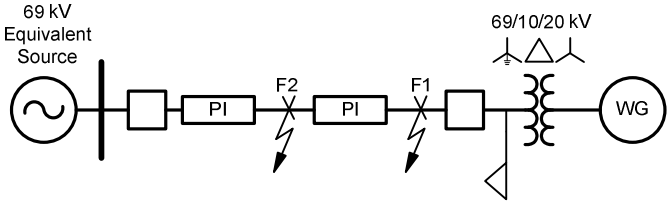


Fig. 32. Simulated system with a wind generator (WG).

Fig. 33 shows the line voltages and currents for a three-phase line fault at F1. Note that the currents shown were contributed from a single DFIG. When a three-phase close-in fault occurs on the 69 kV line, the stator voltage of the DFIG collapses and high rotor currents are induced. To prevent damage to the dc link, the capacitor, and the back-to-back converters, the dc chopper switch (thyristor) is fired to bypass the capacitor, the controller tries to reduce the current and even switch off the IGBTs, and the crowbar circuit may be activated to separate the converters from the rotor circuit. This is the major difference from the synchronous generator or traditional induction generator—the excitation will be significantly modified by the converter controller and the DFIG protection circuits.

As a result, the short-circuit current contributed from the DFIG contains a large dc offset with a limited ac component. Assuming the collector transformer is not immediately saturated, the relays will see both the dc and ac components. However, when considering a three-phase fault, the filtered, fundamental frequency ac currents during the fault are just a fraction of the load current (see Fig. 33). This, in turn, challenges any current-based local protection method (distance, overcurrent) and therefore requires weak infeed logic, such as a blocking scheme or permissive echo logic, to properly protect the line.

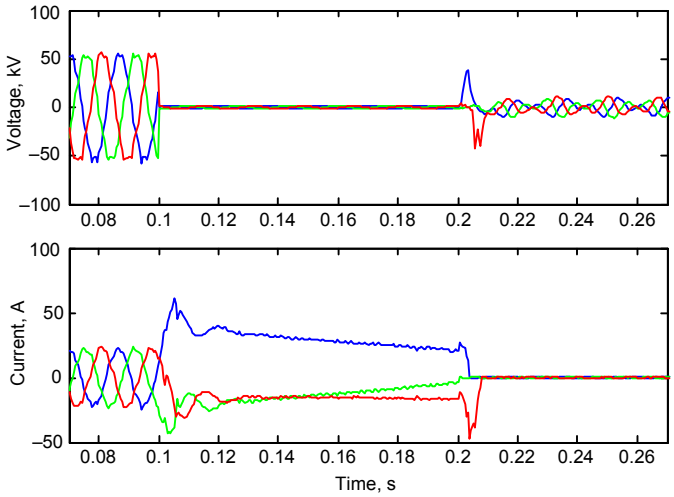


Fig. 33. Line voltages and currents for a three-phase fault at F1.

The 87L schemes work satisfactorily because the grid provides enough fault current contribution to drive the differential signal up, while no restraining is created by the inverter-based sources.

Fig. 34 shows voltages and currents for a phase-to-phase fault at F1 (close-in fault). For this condition, none of the phase-to-ground voltages are considerably reduced, and therefore, the inverter-based source does not trigger its protective control circuits and may provide enough ac current for the distance and overcurrent elements to operate. However, the exact dynamic behavior of the source is not well known because it depends on the proprietary control logic of the DFIG. As a result, distance and overcurrent applications may still face some level of uncertainty not appreciated by most protection engineers.

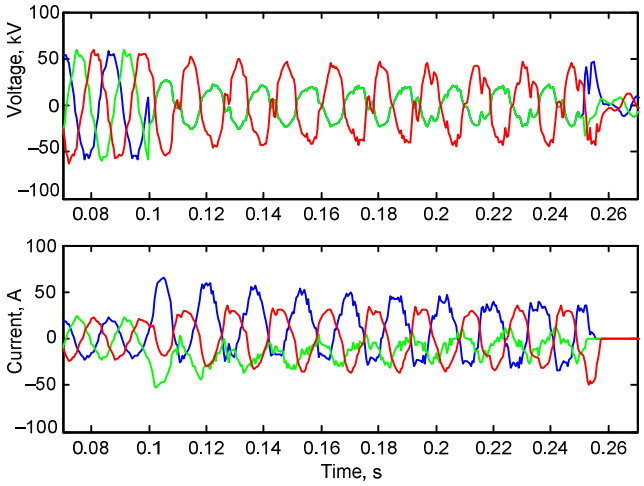


Fig. 34. Line voltages and currents for a phase-to-phase fault at F1.

Again, the 87L schemes work satisfactorily because the grid provides enough current contribution to effectively overshadow the DFIG currents, even if the latter display some unusual characteristics affecting the direction of the DFIG currents symmetrical components.

Fig. 35 illustrates the case of an SLG fault. This case is slightly different because now the wye-connected transformer acts as a source of the zero-sequence current. This is clearly visible with all three currents being of similar magnitude and phase. As a result, ground fault protection can often be provided with the use of ground directional overcurrent elements, or even ground distance elements.

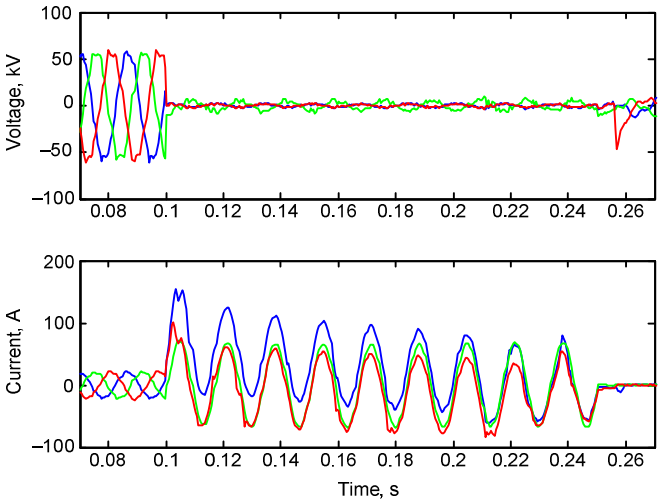


Fig. 35. Line voltages and currents for an SLG fault at F1.

Note that all three voltages collapse for this SLG fault. This is a consequence of the DFIG control system responding in a similar fashion as for the three-phase fault. Fig. 36 illustrates this by plotting the generator currents at the 20 kV winding of the transformer.

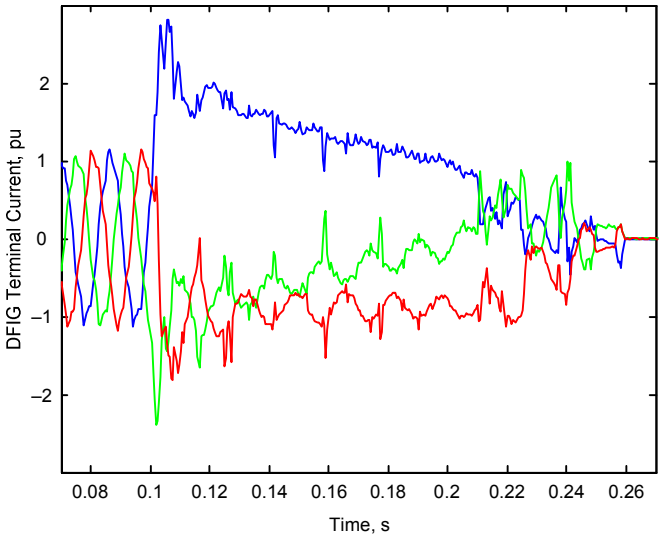


Fig. 36. DFIG currents for an SLG fault at F1.

In general, inverter-based sources act as weak systems, and the interconnected line should be protected using known methods (such as weak infeed logic). The interconnection transformer should be selected with a proper winding configuration, such as wye-grounded-delta-wye or wye-grounded-delta, to provide a ground source allowing better ground fault protection.

The 87L scheme is the preferred choice for primary line protection when connecting the wind farms to the utility grid. The 87L schemes will reliably detect line and ground faults involving inverter-based sources by utilizing the fault current contribution from the grid.

VIII. Conclusion

The line current differential protection principle is inherently secure. The phase (87LP) elements respond to phase currents, are often set above the maximum load currents, and are typically applied to clear heavy faults fast. The sequence (87LG and 87LQ) elements are very sensitive, may be slightly slower by design, and are typically applied to detect high-resistance faults.

All three elements (87LP, 87LQ, and 87LG) use the same measurements, are easy to set, and are inherently secure. Therefore, enabling all three elements does not diminish the security of the application, provided the CTs perform adequately (or the relay incorporates the means to secure these elements under CT saturation, such as EFD logic) and the line charging current is small (or the relay incorporates line charging current compensation).

This paper explains 87L dependability concerns for series-compensated lines, under weak infeed conditions, during single-pole open conditions, during power swings, during off-nominal frequencies, and with inverter-based short-circuit sources. These challenges are considerably less significant for 87L schemes as compared with any single-ended protection method.

Furthermore, any dependability concerns can be reduced or eliminated by applying all three 87L elements—87LP, 87LQ, and 87LG—in parallel.

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X. Biographies

Yiyan Xue received his B.Eng. from Zhejiang University in 1993 and M.Sc. from the University of Guelph in 2007. He is currently a Senior Engineer in the P&C Standards Group of American Electric Power (AEP), working on protection standards, relay settings, fault analysis, and simulation studies. Before joining AEP, he was an Application Engineer with GE Multilin, providing consulting services on relay settings, scheme design, and RTDS studies. Prior to GE, he had ten years with ABB Inc., working on P&C system design, commissioning of relays, and RTU systems. He is a senior member of IEEE and a Professional Engineer registered in Ohio.

Bogdan Kasztenny is the R&D director of technology at Schweitzer Engineering Laboratories, Inc. He has over 23 years of expertise in power system protection and control, including ten years of academic career and ten years of industrial experience, developing, promoting, and supporting many protection and control products.

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